

# Methodology for Mismatch Reduction in Time-Interleaved ADCs

Michael Soudan

Institute of Microelectronics and Wireless Systems, NUIM  
Centre for Telecommunications Value-Chain Research  
Maynooth, Co. Kildare, Ireland  
msoudan@eeng.nuim.ie

Ronan Farrell

Institute of Microelectronics and Wireless Systems, NUIM  
Centre for Telecommunications Value-Chain Research  
Maynooth, Co. Kildare, Ireland  
rfarrell@eeng.nuim.ie

**Abstract**— This paper presents a methodology to minimize mismatch errors in time-interleaved analog-to-digital converters (ADC) by means of averaging multiple channels. A simple algorithm improving both spurious free dynamic range (SFDR) and signal-to-noise and distortion ratio (SINAD) is demonstrated. The presented technique provides robustness against inaccurately identified mismatch errors and does not require computationally expensive post-processing of the signal.

## I. INTRODUCTION

Time-interleaving is an effective possibility to increase the sampling rate of analog-to-digital converters. A time-interleaved ADC (TIADC) utilizes multiple ADCs in parallel to increase the system sampling rate according to the number of used ADCs [1]. The usage of several ADC with a lower sampling rate facilitates the design of high-speed converters with superior power efficiency.

However, gain, offset and timing mismatches between the individual ADCs distort the output spectrum of the TIADC by causing unwanted tones. Various calibration and error correction techniques have been proposed to decrease the impact of gain and offset mismatch [2][3]. Timing mismatch, which is caused by clock skew and different circuit response times, still remains the most significant mismatch type as it is the most difficult to correct. Techniques for compensating timing mismatch are either computationally expensive or require some mechanism for determining the individual timing mismatch, a priori. Another approach to reduce the impact of timing mismatch is controlling the order in which the ADCs are selected. The best known technique is the randomization of the channel selection order, thereby removing the spurious tones at the expense of an increased noise floor [4][5]. Additional ordering techniques have been demonstrated which increase the figures of merit of the TIADC, while requiring an increased oversampling rate due to filtering. Thus, only a part of the Nyquist band can be used and the effective sampling rate of the system is decreased according to the required stop band frequency of the filter. In [6] a technique has been proposed employing randomization within two alternately

selected ADC groups to maximize spurious tones in the out-of-band part of the spectrum. This technique was extended in [7] to an arbitrary number of groups, which results in a decreased in-band noise floor at the expense of additional ADCs, while achieving the same effective sampling rate. A spectral shaping method was presented in [10] to concentrate more mismatch power in the out of band spectrum by a constant selection scheme using no channel randomization. The improved signal-to-noise and distortion performance involves a decreased spurious free dynamic range when compared with other techniques.

In this paper we propose a novel methodology to reduce the mismatch impact on the TIADC spectrum. This technique requires only knowledge about the mismatch magnitude order of the TIADC channels. It will be shown that this new approach provides significant performance improvements over existing techniques.

## II. IMPACT OF MISMATCHES

Gain, offset and timing mismatches between ADC characteristics degrade the signal-to-noise and distortion ratio (SINAD) ratio and the spurious free dynamic range (SFDR) of time-interleaved systems [8]. These non-idealities are static, or slowly changing, differences in either the time of the sample acquisition, the gain or offset of the individual channels. Whereas either signal noise or timing jitter can be assumed to be equally distributed across the bandwidth, channel mismatches result in tonal distortion throughout the spectrum. Shrinking geometries and increasing circuit speed makes timing mismatch the most significant error mechanism in practical devices. The accuracy of a TIADC affected by a relative timing mismatch with a standard deviation of 10<sup>-2</sup> (equals a variance of 10<sup>-4</sup>) will be limited to a maximum resolution of 7 effective bits without correction, irrespective of the resolution of the individual channel ADCs (see Fig. 1).

Randomization of channels facilitates the distribution of mismatch power over the frequency band and increases the SFDR [4].

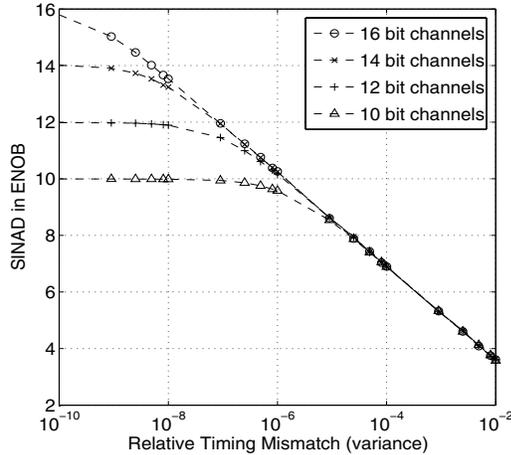


Fig. 1 The impact of timing mismatch error on TIADCs with different channel resolutions [7].

This is diagrammatically shown in Fig. 2. In order to use randomization, a number of redundant ADCs  $R$  have to be dedicated to allow the choice between  $R+1$  available ADCs. With increasing the number of redundant ADCs, the mismatch energy is more evenly spread and the spectrum is flattened [10]. However, the mismatch energy is not reduced by randomization and therefore no SINAD improvement can be achieved. To increase the SINAD performance, we can oversample the randomly sampled input signal and filter out all but the frequency band of interest. With ideal filters and assuming white noise, we can gain 3dB for every doubling of the oversampling ratio.

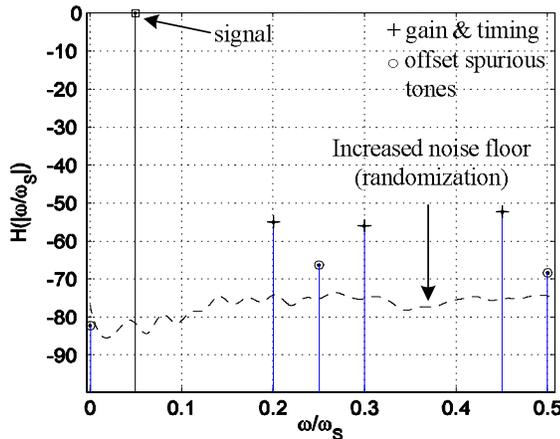


Fig. 2 Output spectrum of a 4 channel TIADC with a constant selection sequence and the superimposed spectrum of the same TIADC with 2 additional ADCs for randomization. This spreads the spurious power over the spectrum (dashed line).

Selection ordering techniques are able to improve the performance of mismatch affected TIADCs when significant oversampling is utilised. Vogel demonstrated a selection ordering scheme where the number of channel ADCs is doubled to improve the figures of merit [6]. The ADCs are assigned to two alternately selected groups according to their mismatch magnitude to maximize the spurious tones in the

out-of-band part of the spectrum. Each group contains redundant ADCs to provide high SFDR performance.

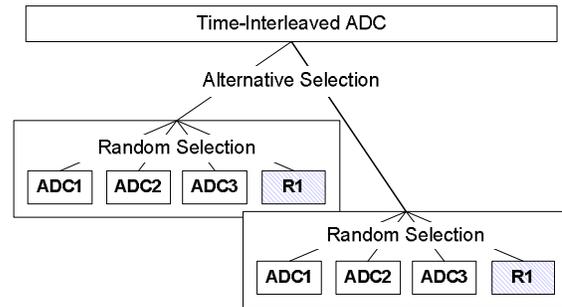


Fig. 3 Randomized selection scheme utilising two additional channel ADCs [7].

This timing and mismatch ordering (TMOG) technique was extended to an arbitrary number of groups  $G$  in [7]. It achieves improved SINAD and SFDR performance at the expense of  $G$  times the ADC number of a system utilizing randomization. The grouping scheme is illustrated in Fig. 4. Spectral shaping has been proposed to maximize out-of-band tonal distortion without providing any guarantee on SFDR performance [10]. The described techniques employ additional converters to minimize the impact of channel mismatch, thereby augmenting the systems power consumption. However, the improved mismatch robustness and the time-interleaved architecture facilitating the usage of highly power efficient converters mitigate this drawback.

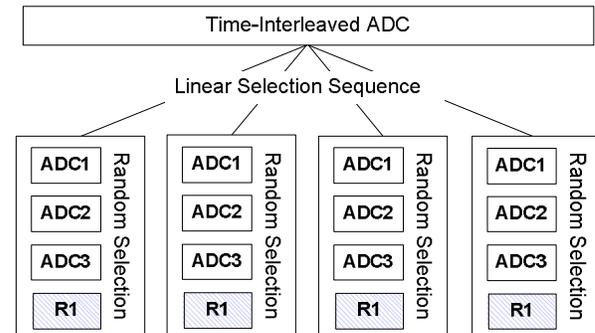


Fig. 4 Selection scheme employing 4 alternately selected groups and a random selection sequence within each group [7].

The proposed methodology reduces the impact of mismatch variances by combining multiple ADCs in a structured manner such that the net variance of each group is substantially smaller. This technique can be combined with randomization to ensure a high spurious-free dynamic range performance. The proposed architecture is illustrated in Fig. 5 where several groups of ADCs are formed and randomly selected. The ADCs assigned to the same group convert the input signal simultaneously and their outputs are averaged. The effective sampling rate of this system, while using the same number of ADCs is the same as that of the selection scheme shown in Fig. 4.

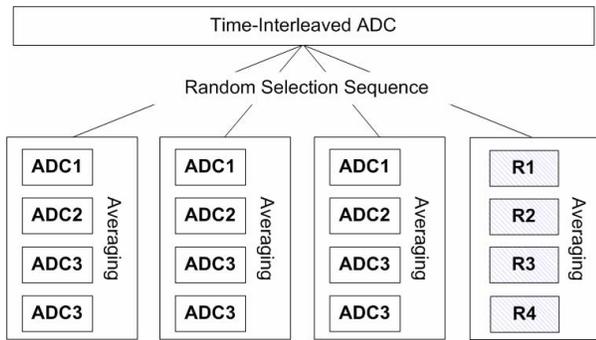


Fig. 5 System with 16 ADCs divided in 4 randomly selected groups. Each groups employs averaging.

The performance of this method is dependent on the selection of the ADCs for each group so as to minimize the effective mismatch. Mismatch in ADCs is typically governed by a Gaussian distribution, as shown in Fig. 6. If the outputs of two ADCs, based on opposite sides of the distribution are averaged, the effective mismatch is reduced, and tends closer to the ideal. This approach can be expanded to multiple ADCs within a group, yielding a more ideal response.

In our proposed method, we have identified an effective selection technique for selecting the ADCs for each group. If we have knowledge of the ranking of the size of mismatch for each ADC, we can then select groups by picking from opposite ends of the list, for example combining the ADCs with the most negative and most positive mismatch error. In Figure 6 this process is illustrated for a system with 16 ADCs with a relative timing mismatch of 0.87% (equals standard deviation of  $8.7e^{-3}$  or a variance of  $74.9e^{-6}$ ). As can be seen in Fig. 6a), by combining ADCs from opposite sides of the distribution, the effective variance of the resulting ADCs has been reduced to  $4.0e^{-6}$ . If this approach is repeated to construct groups of four, then substantial additional improvement can be obtained (see Fig. 6b). As the output mismatch noise in the system is proportional to the variance (Figure 1), these improvements in effective variance will result in improved performance.

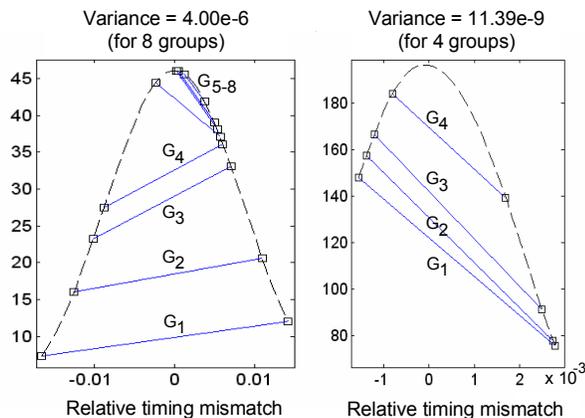


Fig. 6 The assigning of groups illustrated on Gaussian probability density functions of a) 16 relative timing mismatch values (results in 8 groups) and b) 8 averaged timing mismatch magnitudes (results in 4 groups).

This technique can be used to target a specific mismatch error mechanism, for example timing, or may be used to optimize for general mismatch. To achieve this, the algorithm requires only an identification of the relative mismatch levels and not the precise magnitude of the mismatch. This provides robustness against inaccuracy and reduces the complexity of the mismatch identification scheme. For the ranking of the timing mismatch, an offline calibration scheme as proposed in [12] can be used.

The implementation of this technique is similar to other group methods where we identify the mismatch, select the ADCs for each group, and then select the ADCs in the appropriate sequence. In our scheme multiple ADCs sample at the same time and these outputs are averaged digitally (see Fig. 7). All other techniques, other than randomization, require filters with rapid roll-off to remove higher frequency noise and tonal components.

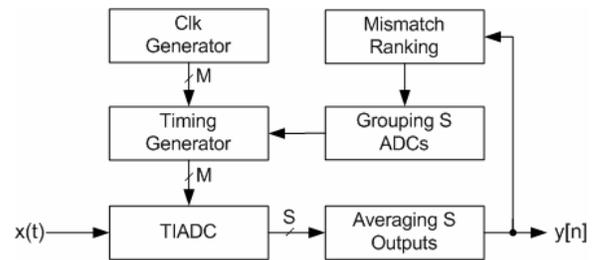


Fig. 7 Principle of a time interleaved system employing mismatch averaging.

### III. SIMULATION RESULTS

This technique has been simulated using a variable number of channel ADCs with 16 bit resolution. Each ADC was given a random value for the relative time mismatch and each simulation was repeated 500 times to provide statistical significance. For each simulation, 4096 coherently sampled points were taken and a sinusoidal input was applied to the TIADC with a frequency of 509 Hertz. The individual channel mismatch was selected using a Gaussian distribution with a standard deviation of 1% for timing mismatch error. The presented figures of merit are the average of all 500 outcomes. In the cases where filtering was needed an ideal brick-wall low-pass filter was used.

In Fig. 8 and Fig. 9 we compare the SINAD in effective number of bits (ENOB) respectively the SFDR in dB of TIADCs employing different selection schemes. To add comparison we have assumed that each system has an equal number of ADCs and an equal signal bandwidth. For the all method which have an excessive bandwidth, we have assumed that an additional 3dB per octave performance that can be achieved through filtering. Four techniques were considered, randomization, Vogel's optimised spectral shaping, and timing-mismatch ordering and a grouping scheme which utilizes 2 groups and randomization. In addition, the SINAD and SFDR performance of the proposed averaging technique for a group size of two is depicted.

As can be seen, the randomization technique (when combined with the 3dB improvement through oversampling)

will provide an SINAD performance of just below 7.7 bits for 12 ADCs. The timing mismatch and ordering technique achieves an SINAD improvement of between  $\frac{1}{2}$  and  $\frac{3}{4}$  effective bits and SFDR increase of about 5 dB over the randomization results. A small SINAD reduction can be observed with increasing ADC numbers as predicted in [11]. Spectral shaping and the proposed technique show similar improved SINAD performance. However, the presented averaging method provides superior SFDR ratio and exceeds the performance of spectral shaping by 8 to 13 dB, while achieving similar SINAD performance.

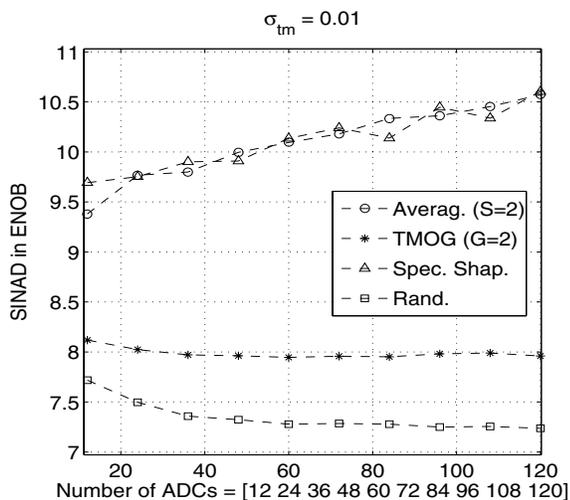


Fig. 8 SINAD in effective number for different selection techniques over the number of ADCs N.

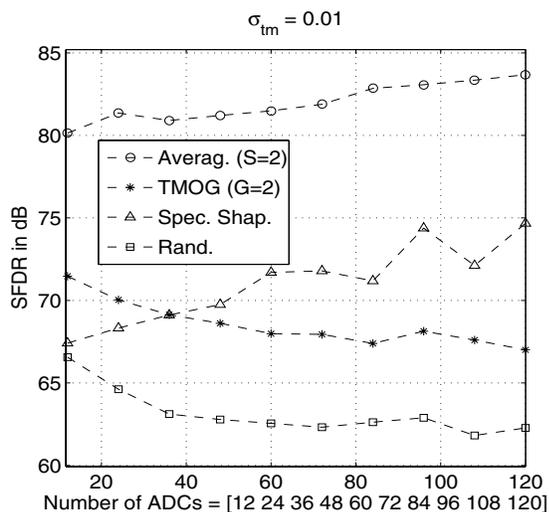


Fig. 9 SFDR in dB for different selection techniques over the number of ADCs N.

#### IV. CONCLUSION

A novel architecture for mitigating mismatch errors by averaging multiple ADCs has been demonstrated. By utilising additional ADCs, the figures of merit can be arbitrarily

increased by reducing the variance of the addressed mismatch errors. Where both signal-to-noise and spurious-free dynamic range performance is required, this technique offers superior performance to existing techniques. It also offers a low-complexity implementation without the complex filtering or complex selection algorithms required by other schemes.

#### V. REFERENCES

- [1] W. Black, and D. Hodges, "Time interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 1022-1029, Dec., 1980.
- [2] Jan-Erik Eklund, Fredrik Gustafsson, "Digital Offset Compensation of Time-Interleaved ADC using Random Chopper Sampling", *IEEE International Symposium on Circuits and Systems, ISCAS 2000*, vol.3, pp. 447-450, 2000.
- [3] Vincenzo Ferragina et al., "Gain and Offset Mismatch Calibration in Time-Interleaved Multipath A/D Sigma-Delta Modulators", *IEEE Transactions on Circuits and Systems*, vol. 51, pp. 2365- 2373, 2004.
- [4] H. Jin, E.K.F. Lee, and M. Hassoun. "Time-interleaved A/D Converter with Channel Randomization", *IEEE Transactions on Instrumentation and Measurement*, vol. 54, Issue 1, pp. 425-428, 1997.
- [5] N. Duignan, R. Farrell, "An architecture for a reconfigurable charge-summation based ADC", *IEEE Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, 2005
- [6] C. Vogel, V. Pammer, and G. Kubin, "A novel channel randomization method for time-interleaved ADCs", *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, vol. 1, pp. 150-155, 2005.
- [7] M. Soudan, F. Zanini, R. Farrell, "Methodology for Minimizing Timing Mismatch in Time-Interleaved ADCs", *submitted to IMEKO 2007*, 2007.
- [8] B. Yu, W. Black, "Error analysis for time-interleaved Analog Channels", *IEEE Int. Sym. on circuits and sys. 2001*, vol. 1, pp. 468-471, 2001
- [9] J. Elbornsson et al., "Analysis of Mismatch Noise in Randomly Interleaved ADC system", *Proc. IEEE ICASSP*, vol. 6, pp. 270-80 vol.6, 2003.
- [10] Christian Vogel et al., "Spectral Shaping of Timing Mismatches in Time-Interleaved Analog-to-Digital Converters", *IEEE Int. Symp. Circuits Sys.*, vol. 2, pp. 1394-1397, 2005.
- [11] Y.C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: Fundamentals and High-Speed Waveform Digitizers", *IEEE Transactions on Instrumentation and Measurement*, vol. 37, pp. 245-251, 1988.
- [12] H. Jin, "A Digital-Background Calibration Technique for Minimizing Timing-Error in Time-Interleaved ADC's", *IEEE Transactions on Circuits and Systems*, vol. 47, pp. 603-613, 2000.