Modular Scan Test for SoC Design

Prakash Srinivasan[1], Ronan Farrell[1], Eamonn M Ward[2]

[1] National University of Ireland, Maynooth
[2] Intel Ireland Ltd

psrinivasan@eeng.nuim.ie, ronan.farrell@nuim.ie

Summary

In this paper we try to reconfigure the existing scan system to a Modular Scan (MS) in order to adapt itself for future complexities of the chip design. One specific application of MS is the Multiprocessor System-on-Chip (MPSoC) design, where each core can have its own scan chain and also have concurrent testing procedure. MS is a process of arranging the scan chains flexibly for multiple usages during scan test. MS can be used in large chip designs to reduce the length of scan chains, and to reduce the testing time. MS based tests allow the test engineer to easily reconstruct the scan chain in an MPSoC design, if any of the existing cores needs to be replaced with a new core in order to meet the new set of specifications. To achieve such a type of testing, generic scan chain architecture needs to be developed in order to ensure an easy plug-n-play scan chain in the system architecture.

1 Introduction

Testing manufactured devices is a critical and expensive part of the silicon industry. One of the most valuable techniques is called "scan" testing due to its excellent ability to detect faults at low cost.. Although scan test fulfils the most of the basic requirements of the chip testing, still it faces considerable challenges as the number of transistors inside the chip increases.

Insertion of scan test circuitry into a design is performed by replacing all the D-type flip-flops in the gate-level architecture with scannable flip-flops known as scan cells. A scan chain is formed by connecting all the scan cells in such a manner as to trigger responses in the combinational logic that would detect faulty elements. As designs become more complex, the chains and the patterns induced become more complex. As the patterns need to be loaded into the scan chains by an external tester, the increasing length of the chains increases the time required to test the chip. Increased test time directly results in increased test costs. There are two approaches used to ameliorate the cost of test: use more chains in parallel to reduce the length of individual chains; and secondly use compression and an on-chip decompression to extract the data. The first of these techniques is widely used but is limited by the number of pins available on a chip. The second technique has proven to be very successful and the cost of dedicated hardware on the chip to do the compression/decompression is far outweighed by the benefits of reduced load times.

Today, scan is a well understood technology that offers excellent test coverage. However scan requires design knowledge of the blocks to be tested. This makes it difficult and expensive to utilise predesigned intellectual property (IP), for example a graphics processor. Ideally one would prefer to take an existing block and without modification utilise the existing in-built scan chains and patterns. This paper will focus on architectures being proposed that would allow for easy and rapid re-use of proven successful designs.

2 Proposed Modular Architectures

There are architectures that could be used for incorporating IP blocks and utilising their pre-designed test function. They will be briefly outlined below:

A. Star Scan Architecture

A centralised decompression unit is connected to each core independently and passes the necessary patterns directly to the core. This results in a large area overhead in terms of wiring and difficulty in maintaining signal integrity. Alternatively each block may have its own compression unit but this again is costly in terms of area and in efficiency as each chain is small.

B. Daisy Chain Scan Architecture

In a daisy-chain architecture, an attempt is made to pass the data through a concatenation of chains. This makes compression more effective. However this approach requires each block to have the same number of chains, which is rarely the case.

C. Hybrid Scan Architecture

Another approach utilises the daisy chain architecture but with limited localised decompression or data manipulation to overcome the mismatch in chain numbers. However this approach is counter to existing compression methodologies and thus is problematic.