Design of signal modulator for RF polar transmitter

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***Abstract*—This paper presents new approach to signal modulation for high efficiency polar transmitter. The new modulator is derived by analyzing complex to polar transforming equations. Once spectral behavior of an envelope and phase signals are known, new architecture offering lower complexity in an analog domain and more flexibility for reconfiguration than a conventional modulator is derived. Concept of the modulator is verified in the course of step-by step simulations with a 5MHz BW input signal at a carrier frequency $f_C = 2.14GHz$. Also, a drain efficiency of a Class E PA driven by the modulator is discussed, and optimal solution for sampling rate is proposed.**

I. Introduction

Switchmode power amplifiers (SMPA) for radio frequencies have become an intensively researched area. The potential of 100% power efficiency makes this group of PA competitive to the existing classes. The switching operation at radio frequencies, however, raises two major implementation issues, namely power dissipation due to high speed of switching power transistors in a PA stage, and a demand for fast digital signal processors capable of converting the RF signal into a binary RF signal.

Fig.1(A) presents a scheme of a Class - S PA. The complex RF signal $x_{RF}(t)$ is encoded by the fast band-pass $\Sigma\Delta$ $(BP\Sigma\Delta)$ modulator. The binary signal then drives the highly efficient switch mode power amplifier. One of the major drawbacks of this method of converting RF signal to a binary pulse stream is the large amount of quantization noise introduced by the $BP\Sigma\Delta$ modulator. Moreover, the power in the output bit stream is constant and independent of input's signal amplitude. As a result, the coding efficiency defined by (1) [1] is very low.

$$\eta = \frac{\Delta_{IN}^2}{\Delta_P^2} \tag{1}$$

where Δ_{IN}^2 denotes the in-band power of a complex signal, i.e. the power recovered after band-pass filtering, and Δ_P^2 is the total power of the output pulse stream. Due to the large amount of quantization noise at the binary output of $BP\Sigma\Delta$, the modulator must operate at high oversampling ratio (OSR) values. For a direct conversion method, the coding efficiency of WCDMA signal is less than 10% [1].

The envelope elimination and restoration (EER) [2] technique can be alternatively used to drive RF SMPA. This

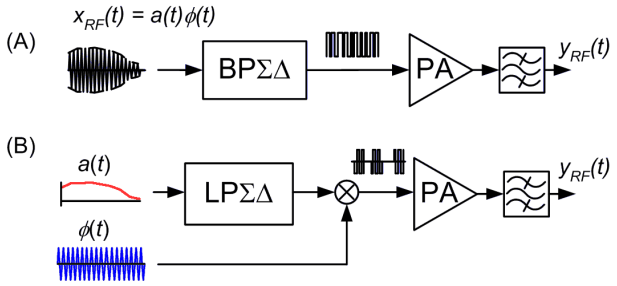

Figure 1. (A) Class S power amplifier (B) Digitized polar power amplifier

method splits the signal into a phase $\phi(t)$ and an envelope $a(t)$ components, with an envelope signal encoded by a low-pass $\Sigma\Delta$ $(LP\Sigma\Delta)$ modulator - Fig.1(B). After mixing the digitized envelope and phase signals, the average power in the output bit stream is proportional to the average amplitude of the envelope. Hence, when the power of the input signal decreases, the magnitude of the output power decreases proportionally. While the power of the encoded signals remain the same, the quantization noise introduced by a polar modulator can be several times lower than in the case of $BP\Sigma\Delta$ modulator of a class S PA. This relaxes the sampling speed requirements for $\Sigma\Delta$, and the task of output band-pass filtering.

The polar modulation technique is more complicated than the direct one used in class S PA. The envelope and phase signals need to be extracted from the complex signal first. Processing these signals is challenging due to the spectral regrowth of phase and envelope signals [3]. In the end, an accurate correction between phase-envelope delay needs to be provided.

In the remainder of this paper an operation of complex to polar conversion is analyzed in Section II, providing basis for the design of a polar modulator. In Section III, a modulator with reduced analog signal processing and extended digital signal processing operations is proposed. Section IV presents the performance of the modulator and the entire power amplifier system with a Class E PA. Concluding remarks are given in Section V.

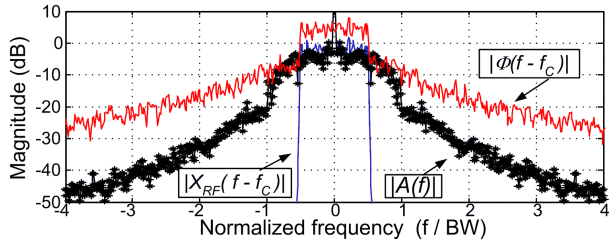

Figure 2. Spectral regrowth of envelope and phase signals

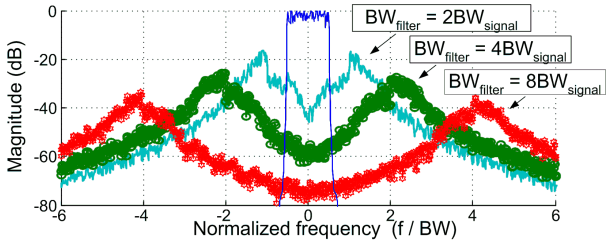

Figure 3. Effect of band limiting of a phase signal

II. COMPLEX TO POLAR CONVERSION

In a polar transmitter, the complex signal can be expressed as a function of envelope and phase signals,

$$x_{RF}(t) = I(t)\cos(\omega t) + Q(t)\sin(\omega t) = a(t)\,\phi(t) \quad where \quad \phi(t) = I'(t)\cos(\omega t) + Q'(t)\sin(\omega t) \tag{2}$$

It is not always clearly pointed out that the conversion of an ideally band limited baseband signals, denoted here as $I(t)$ and $Q(t)$, to envelope $a(t)$ and phase $\phi(t)$ in the course of performing (3) [4] cause spectral regrowth of the latter. This effect can be observed in Fig.2. The $|\phi(f)|$, $|A(f)|$ are plotted with the original complex signal $|X_{RF}(f)|$ for comparison. The frequency has been normalized to the bandwidth of $X_{RF}(f)$ and, in case of $|\phi(f)|$ and $|X_{RF}(f)|$, carrier offset f_C has been added.

$$a(t) = \sqrt{I^2(t) + Q^2(t)},\ I'(t) = \frac{I(t)}{a(t)},\ Q'(t) = \frac{Q(t)}{a(t)} \tag{3}$$

Often the error signal introduced by envelope digitizing by $\Sigma\Delta$ or PWM is highlighted as a major concern. Yet, processing both phase and envelope should be accounted for.

Once (3) applied, the envelope signal $A(f)$, whose spectrum spreads over wider frequency range than that of the $X_{RF}(f)$ is obtained. Usually a $\Sigma\Delta$ modulator with OSR relative to complex signal in a range of 16, 32 [5] to 260 [6] is used for envelope digitization. The sampling speed of $\Sigma\Delta$ in an envelope path often plays dominant role in the final SNR performance of a power amplifier, since this is the element that often introduces the largest amount of noise in the system. A second order $LP\Sigma\Delta$ modulator having a sampling rate of $214MHz\,to\,856MHz$ (OSR=21 to 86) has been considered in this paper for digitizing an envelope signal of $5MHz$ BW complex RF input signal X_{RF}. This sampling rate assumption takes into account the power amplifier's capacity for amplifying a wide-band spectrum of an input signal.

In a practical case, part of I' and Q' (3) spectrum is limited in a polar modulator due to a finite sampling speed of a digital signal processor, digital to analog converters, and limited passband of a quadrature mixer – Fig.4(A). This effect of band limiting can be modelled by a band pass filter (BPF) applied to an ideal phase signal $\Phi(f)$, having its center frequency equal to carrier f_C, and cut off frequencies f_{coff1} and f_{coff2}. The passband of a BPF is defined by $BW_{filter} = f_{coff2} - f_{coff1}$. This band limited phase signal $\Phi'(f)$, can be expressed by a sum of an ideal phase signal $\Phi(f)$ and a phase error $\Phi_e(f)$ representing the removed spectral elements (4)

$$\Phi'(f) = \Phi(f) + \Phi_e(f) \tag{4}$$

Hence the resulting complex signal given by (2), can be now rewritten in a frequency domain as,

$$X'_{RF}(f) = A(f) \star [\Phi(f) + \Phi_e(f)] \tag{5}$$

The phase error $\Phi_e(f)$ has maxima at the BPF cut off frequencies f_{coff1}, f_{coff2}. After convolving $\Phi'(f)$ with the envelope signal $A(f)$ (5), the resulting spectrum of $X'_{RF}(f)$ will consists of an ideal band limited complex signal $A(f) \star \Phi(f)$ plus an error $A(f) \star \Phi_e(f)$, having its peaks at f_{coff1}, f_{coff2} - Fig.3.

III. PROPOSED MODULATOR ARCHITECTURE

In a conventional modulation scheme [4], [5], [7] shown in Fig.4(A), a digital signal processor (DSP) performs the I/Q to polar conversion, using CORDIC algorithm. Next, the obtained envelope signal is fed into a $LP\Sigma\Delta$ modulator, whose output consists of an envelope and quantization noise denoted as $q_A(t)$. The obtained digitized envelope $a(t)+q_A(t)$, $I'(t)$ and $Q'(t)$ signals exit the DSP. Phase signal $\phi(t)$ is obtained by performing an analog quadrature modulation (QM) on $I'(t)$ and $Q'(t)$. After mixing the obtained phase signal $\phi(t)$ with an envelope signal $a(t)+q_A(t)$, the complex envelope output $x_{RF}(t)$ is created.

The new modulator scheme shown in Fig.4(B) reduces the analog signal processing size in a phase path by moving the quadrature modulation to a digital domain, and by replacing digital to analog converters by digital pair of $LP\Sigma\Delta$ modulators followed by a single, analog BPF.

The principle of operation is as follows: the I', Q' signals are fed into pair of fast, $LP\Sigma\Delta$ modulators, where they are converted to binary waveforms. Next outputs from $\Sigma\Delta$ modulators undergo quadrature modulation in the digital domain according to (6)

$$QM[nT] = (I'[nT] + q_1[nT])\cos[2\pi(f_{QM}/4)nT] + (Q'[nT] + q_2[nT])\sin[2\pi(f_{QM}/4)nT] \tag{6}$$

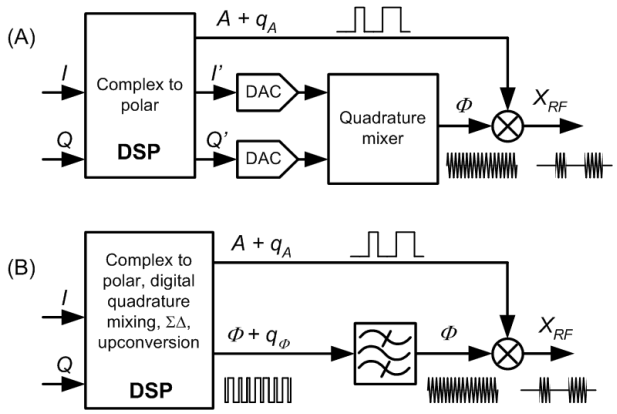

Figure 4. Signal modulator for polar transmitter, (A) Conventional, (B) Proposed

Where q_1, q_2 denote quantization noise introduced by $\Sigma\Delta$ modulators. The output sampling rate of digital quadrature modulator is twice as fast as sampling rate of $LP\Sigma\Delta$, with the phase signal being centered at $f_{QM}/4$. The block diagram of the digital signal processor is presented in Fig.5.

Often in a practical case, $f_{QM}/4 < f_C$, hence the QM signal needs to be upconverted and mixed with high frequency waveform. Two possible cases can be considered for the choice of sampling rates in the modulator. They are associated with the utilization of the lower or upper image created by the mixing stage, as shown in Fig.6. Using the lower image is attractive since the signal has strength higher by approximately 4.4dB than that of the upper image. Hence less gain will be required between the modulator's output and a PA in order to drive the transistor into saturation. Yet, it will also require faster sampling rate from the high speed output buffer (HSOB), denoted here as f_{HSOB}. The output buffer's sampling rate can be determined from (7), depending whether lower - at f_1 or upper, at f_2 image is utilized,

$$\begin{aligned} f_{HSOB_1} &= 2f_C + f_{\Sigma\Delta-\Phi} \\ f_{HSOB_2} &= 2f_C - f_{\Sigma\Delta-\Phi} \end{aligned} \tag{7}$$

where $f_{\Sigma\Delta-\Phi}$ denotes sampling rate of $LP\Sigma\Delta$ modulators in a phase path. E.g. for $f_C = 2.14GHz$ and $f_{\Sigma\Delta-\Phi} =$

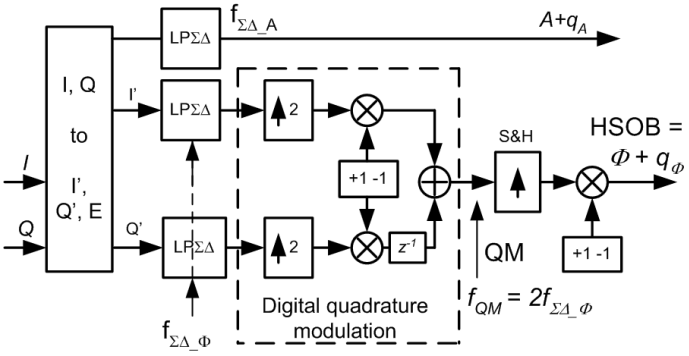

Figure 5. DSP operation in the proposed modulator

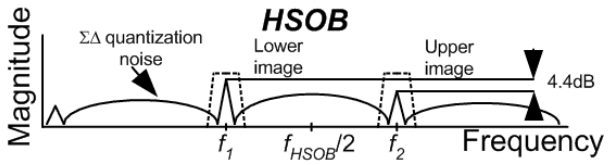

Figure 6. Output spectrum HSOB produced by digital quadrature modulator followed by mixer

$856MHz$, the corresponding sampling rates are $f_{HSOB_1} = 5.136Gb/s$, $f_{HSOB_2} = 3.424Gb/s$. With no additional mixer the bit rate of HSOB would have to reach $f_{HSOB} = 4f_C = 8.56Gb/s$, which can be difficult to achieve.

It can be read from Fig.3, that a phase bandwidth at least greater than the complex's signal $X(f)$ bandwidth needs to be provided. In practice, due to the spectral regrowth, 4 or 8 times wider passband for a phase should be ensured. This can be achieved with a $\Sigma\Delta$ modulator, operating at an appropriate sampling rate. The simulation result in Fig.7 shows that a first-order $\Sigma\Delta$ modulator with $OSR = 21$ ($BW = 5MHz$, $f_{\Sigma\Delta-\Phi} = 214MHz$) can be sufficient to ensure $20MHz$ $(4BW)$ passband for a phase signal. To validate this concept, Fig.8 shows the simulated result of a complete modulator system composed of a second-order $\Sigma\Delta$ modulator at $856MHz$ sampling rate for an envelope signal, and a first order $\Sigma\Delta$ modulator in a phase path sampled at a rates of $214MHz$, $428MHz$ and $856MHz$. The analog BPF in a phase path has a center frequency at $f_C = 2.14GHz$ and a passband of $20MHz$, $35MHz$ and $45MHz$ respectively. The system utilizes upper image, hence the output sampling rate in a phase path of $3.424Gb/s$ is assumed.

IV. System Performance

After providing compensation for the delay of $\phi(t)$ due to band pass filtering in a phase path, the output from the mixer is amplified and fed into a class E PA input shown in Fig.9(A). For the PA simulation, the best performing phase signal with $f_{\Sigma\Delta-\Phi} = 856MHz$ has been chosen. The transistor model in the PA is composed of an input impedance Z_{IN}, drain-to source capacitance C_{DS}, saturation resistance R_{ON}, and R_{OFF} for simulating the current that flows through the device during its off state. The values for the transistor parameters are close to those given for GaN NPTB00004. The purpose

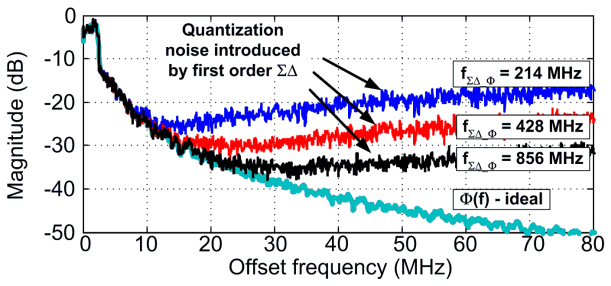

Figure 7. Phase signal encoded by first order $\Sigma\Delta$ with different sampling rates

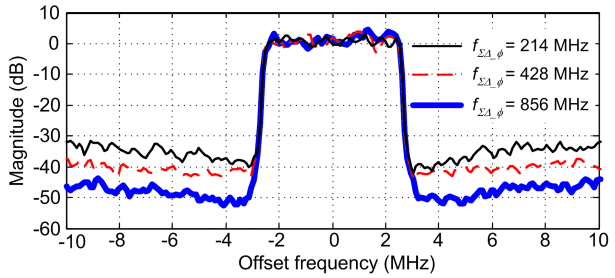

Figure 8. Modulator's frequency response to $f_C = 2.14GHz, 5MHz\ BW$ complex signal. The sampling rate of an envelope $\Sigma\Delta$ is $856MHz$, Three different sampling rates of $\Sigma\Delta$ in phase path has been simulated.

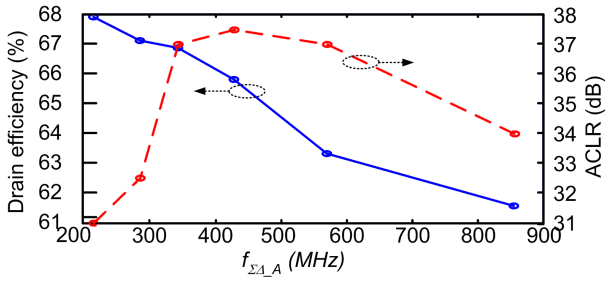

Figure 10. ACLR and PA efficiency vs. sampling rate of an envelope $\Sigma\Delta$

of the PA simulation here is not to find exact figures for the output performance and power efficiency, but rather to establish approximate behavior of a PA driven by the proposed modulator.

Fig.9(B) shows simulated S_{11} parameter for a 50Ω drive source, matched to the input impedance of the transistor. Due to selectivity of the matching network, it is expected that the transistor will be driven most efficiently when a sampling rate of an envelope $\Sigma\Delta$ is rather low, narrowing the input frequency range. In the case of the performance, the faster sampling rate of an envelope $\Sigma\Delta$ is required. However, when a real device is used, at some sampling frequency point the degradation of performance due to frequency selectivity of a matching network arises. Simulated results for ACLR and drain efficiency are given in Fig.10. The best ACLR/efficiency performance has been achieved for an envelope $f_{\Sigma\Delta-A}$ of $342.4MHz$, with 31 (dBm) of a total output power, and 26.3 (dBm) of the inband power. EVM of 3.5% and 2.1% were obtained for $f_{\Sigma\Delta-A} = 214MHz$ and $f_{\Sigma\Delta-A} = 428MHz$ respectively with 4-QAM input. These results were very close for the conventional and proposed modulators cases without PA. Simulation with a two tone input produced third order IMD 40dB below the carrier. No spectrum mask has been applied here due to insufficient sampling rate of the envelope $\Sigma\Delta$ modulator. A 50dB dynamic range is achievable with

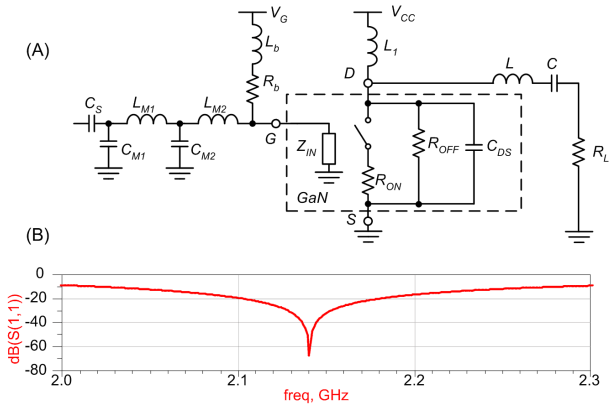

Figure 9. Class E power amplifier, (A) scheme, (B) impedance matching simulation of 50Ω drive source with transistors input impedance (S_{11})

5MHz BW input when $f_{\Sigma\Delta-A} \geqslant 856MHz$-Fig8. In order to use such high sampling rate with the PA, a broadband impedance matching network in Fig.9 is needed.

V. Conclusion

In this paper aspects of spectral regrowth of phase and envelope signals in polar transmitter have been raised and analyzed. A dependency of performance from a sampling speed in a modulator has been derived, which creates a basis for a design of a modulator for polar transmitter. A modulator system with reduced complexity in an analog part has been designed, by replacing digital to analog converters and a quadrature mixer by an equivalent DSP operation followed by single analog BPF. This new architecture offers more flexibility for reconfiguration of the system, since most of a signal processing is being made in by DSP. The proposed modulator has been simulated with a class E PA with various sampling rates, yielding an optimal solution for a modulator for polar transmitter.

Acknowledgment

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References

[1] Johnson, T. And S.P. Stapleton, *RF Class-D Amplification With Bandpass Sigma-Delta Modulator Drive Signals*, IEEE Transactions on Circuits And Systems I, pp. 2507-2520., 2006

[2] .Kahn, L.R.; , "Single-Sideband Transmission by Envelope Elimination and Restoration," Proceedings of the IRE , vol.40, no.7, pp.803-806, July 1952.

[3] Strasser, G.; Lindner, B.; Maurer, L.; Hueber, G.; Springer, A.; , "On the Spectral Regrowth in Polar Transmitters," Microwave Symposium Digest, 2006. IEEE MTT-S International , vol., no., pp.781-784, 11-16 June 2006.

[4] Jau-Horng Chen; Hao-Shun Yang; Chen, Y.-J.E.; , "A Technique for Implementing Wide Dynamic-Range Polar Transmitters," Microwave Theory and Techniques, IEEE Transactions on , vol.58, no.9, pp.2368-2374, Sept. 2010.

[5] Jinsung Choi; Jounghyun Yim; Jinho Yang; Jingook Kim; Jeonghyun Cha; Daehyun Kang; Dongsu Kim; Bumman Kim; , "A ΔΣ-Digitized Polar RF Transmitter," Microwave Theory and Techniques, IEEE Transactions on , vol.55, no.12, pp.2679-2690, Dec. 2007.

[6] Nielsen, M.; Larsen, T.; , "A Transmitter Architecture Based on Delta–Sigma Modulation and Switch-Mode Power Amplification," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.54, no.8, pp.735-739, Aug. 2007.

[7] Yang, H.; Shih, H.; Chen, J.; Chen, Y. E.; , "A pulse modulated polar transmitter for CDMA handsets," Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International , vol., no., pp.1, 23-28 May 2010.