IEICE Electronics Express, Vol.6, No.24, 1745–1751

A 1 V folded common-gate CMOS LNA for full UWB band

Anh Tuan Phan[a)] **and Ronan Farrell**

Institute of Microelectronics and Wireless Systems, National University of Ireland Maynooth

Maynooth, Co. Kildare, Ireland

a) *aphan@eeng.nuim.ie*

Abstract: This paper presents a low voltage 2.8–11.2 GHz CMOS broadband low noise amplifier (LNA) using folded common-gate (CG) topology. The broadband input matching is achieved by adopting CG topology. Bandwidth extension is proposed by inserting an inductor to create a broadband band-pass characteristic with a choke inductor. A folded topology is employed to reduce the supply voltage and thus power consumption. A source follower jointly acts as the buffer stage for broadband output impedance matching and feed-forward path for gain enhancement. Maximum power gain is 11.2 dB and the NF ranges from 2.58 to 4 dB over the full band. The LNA achieves an average IIP3 of −6.5 dBm while consumes only 4.6 mW. The proposed broadband LNA is designed in 0.18-μm CMOS process from 1 V supply.

Keywords: UWB LNA, folded topology, low power, CMOS

Classification: Integrated circuits

References

[1] A. Bevilacqua and A. M. Niknejad, "An Ultrawideband CMOS low noise amplifier for 3.1-10.6 GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[2] H. Zhang, X. Fan, and E. S. Sinencio, "A Low-Power, Linearized, Ultra-Wideband LNA Design Technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.

[3] IEEE 802.15 Task Group 4a. [Online] http://www.ieee802.org/pub/15/TG4a.html

[4] Y.-H. Yu, Y.-J. Emery Chen, and D. Heo, "A 0.6-V low power UWB CMOS LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 229–231, March 2007.

[5] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–10.6-GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, May 2007.

[6] R.-L. Wang, S. C. Chen, H.-C. Kuo, and C.-H. Liu, "A 0.18-μm CMOS UWB Low Noise Amplifier for Full-Band (3.1-10.6 GHz) Application," *IEEE Asia Pacific Conf. Circuits Syst.*, pp. 363–366, Dec. 2006.

[7] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

[8] A. Mirvakili, M. Yavari, and F. Raissi, "A linear current-reused LNA for 3.1-10.6 GHz UWB receivers," *IEICE Electron. Express*, vol. 5, no. 21, pp. 908–914, 2008.
[9] D. J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS Low-Noise Ampliifers," *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, pp. 97–100, June 2004.

1 Introduction

Ultra-wideband technology using the unlicensed frequency band from 3.1 to 10.6 GHz has become much interested in broadband wireless communication recently [1, 2]. UWB technology can be found in many applications nowadays such as sensor networks, vehicular and ground penetrating radars, radio-frequency identification (RFID) and short range wireless communication systems like wireless personal area network (WPAN), wireless body area network (WBAN) [3].

Full UWB-band LNAs designed using several topologies have recently been published, such as distributed amplifiers [4], feedback amplifiers [5, 6], common gate [7, 2, 8], or LC ladder filters LNA [1]. With technology scaling, short channel devices suffer from poor linearity as the low supply voltage is mandated and due to high field mobility effect. New architecture and solution for low supply voltage is preferred. Also, the signal to noise ratio (SNR) is more stringent as it reduced with low supply voltage. It poses more challenge on NF performance of the preceding stage like LNA. Folded topology is among few candidates for low supply voltage design.

In LNA design, at frequencies well below the f_{T} of transistors, cascode or CS topologies provide a low noise figure, good input matching, and a high reverse isolation. At higher frequencies, on the other hand, the pole at the cascode node (typically on the order of $f_{\mathrm{T}}/2$) shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by the cascode device. With technology scaling, the CG topology is starting to be recognized as an alternative to the common-source or cascode for the LNA, especially at frequencies near 10 GHz or higher [9]. Moreover, CG shows a constant NF with respect to $\omega_0/\omega_{\mathrm{T}}$ which is not feasible with cascode or CS topology. Also, it provides better isolation as the missing of C_{gd} path from input to output like in CS LNA.

In this paper, we propose a low voltage broadband LNA operating in the full UWB band from 3.1 to 10.6 GHz. The folded common-gate LNA is adopted for the first time with the proposed bandwidth extension technique and forward path for gain enhancement.

2 Proposed folded broadband LNA

2.1 Circuit topology

To take advantage of CG topology and folded structure as abovementioned, the proposed folded CG broadband LNA is presented in Fig. 1. The LNA

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

consists of NMOS M1 at input common-gate stage and PMOS M2 at the folded branch. A RF chock inductor L_c is inserted to steer the RF signal current toward the output branch. In conventional folded topology with RF choke inductor, L_c only ensures to deliver the RF signal current to the output just within the narrow bandwidth of operation frequency. It is because the high impedance seen from choke LC tank is achieved around the resonant frequency of L_c and parasitic capacitances at the source of M1 and drain of M2.

Not to spoil the wideband input wideband characteristic of CG M1, the proposed series inductor L_e is inserted at node X to broaden the bandwidth (BW) at this bottle neck of the folded topology.

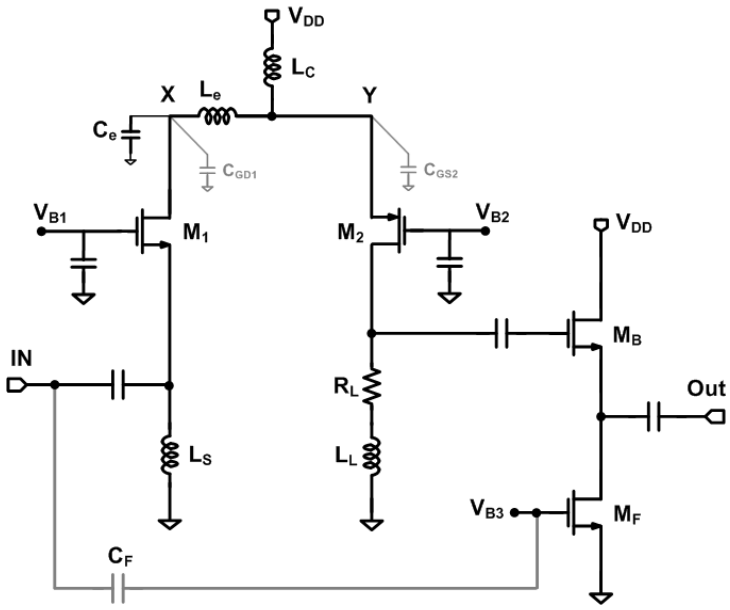


Fig. 1. Schematic of the proposed broadband folded CG LNA.

In order to control the gain flatness, a small capacitance C_e is also inserted at node X. C_e will give a room for tuning the Q-factor as well as BW of gain transfer function, which will be analyzed in the section 3.

The source follower buffer is used to ensure the wideband matching and measurement purpose at the output. The gain is enhanced by feed-forwarding the input to the buffer, through C_F, a DC blocking capacitor.

2.2 Gain enhancement

By exploiting the current source of the buffer, the gain is enhanced by feed-forward connecting the input to the buffer through AC coupling capacitor C_F. At the same time, the input signal flows to the output through both folded branch and C_F with the same sign. Hence, a summation occurs to reinforce the signal level and thus the gain at the output. Fig. 3 (a) shows the S21 performance with and without extra forward path. More than 2 dB of gain improvement is achieved.

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

3 Bandwidth extension technique

Fig. 2 (a) describes the small signal model of the folded CG LNA proposed in Fig. 1. C_X is the total capacitance at node X, $C_X = C_{GD1} + C_e$. Without L_e, near resonant choke frequencies of L_c //$(C_X + C_{gs2})$, most of the current flows to node Y as the choke impedance is high. However, the effect works only within a narrow frequency range around the peaking. To increase the effect over wide frequency range, inductor L_e is inserted in series between nodes X and Y. The LC network between X and Y can be now created and decomposed into a LC π-network around L_e which acts like a LPF with a high cut-off frequency (ω_2) and a resonant choke around L_c at lower peaking frequency (ω_1) as a narrow BPF. The resultant transfer function is a broadband BPF characteristic as illustrated in Fig. 2 (b).

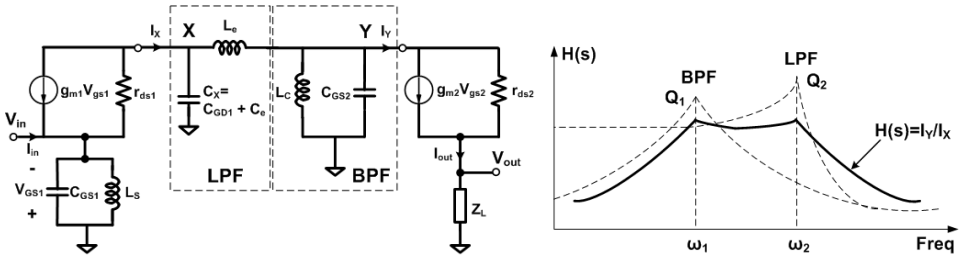


Fig. 2. Small signal model of the folded CG LNA (a), and the transfer function of LC network between node X and Y (b).

Qualitatively, at low frequency near ω_1 (around 3 GHz), Z_{Lc} presents negligibly small impedance, thus the LC network effectively acts like only a tank of L_c //$(C_X + C_{gs2})$. Since the tank presents high impedance around the resonant frequency $\omega_1 \approx 1/\sqrt{L_c(C_X + C_{gs2})}$, a large portion of input current I_X is delivered to node Y as I_Y. As the frequency goes up to ω_2 (near 10 GHz), the large choke inductor L_c can be considered open. Effectively, the LC network acts like a LPF LC π-network of C_X-L_e-C_{gs2}. The cut-off frequency is put further away at $\omega_2 \approx 1/\sqrt{L_e(C_X + C_{gs2})}$. Input current signal below this cut-off frequency will be delivered to the output at node Y. The ratio of ω_2/ω_1 can be approximately estimated as

$$\omega_2/\omega_1 \approx \sqrt{L_c/L_e} \tag{1}$$

Quantitatively, the transfer function from node X to Y ($H(s)=I_Y/I_X$ is derived as follows

$$H(s)=\frac{sL_c g_{m2}}{s^4 L_e C_X L_c C_{gs2}+s^3 L_e C_X L_c g_{m2}+s^2(L_e C_X+L_c C_{gs2}+L_c C_X)+sL_c g_{m2}+1} \tag{2}$$

$$H(s) = \frac{a_1 s}{s^2 + s\frac{\omega_1}{Q_1} + \omega_1^2} \times \frac{a_2}{s^2 + s\frac{\omega_2}{Q_2} + \omega_2^2} \tag{3}$$

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

where $s = j\omega$, Q_1 and Q_2 are the Q-factor of BPF and LPF, respectively. From (2), H (s) can be represented by the standard transfer function of high order BPF and LPF as shown in (3). From (2) and (3), the relation of LPF's cut-off frequency and HPF's peaking frequency are extracted from (2) as

$$\omega_1 \times \omega_2 = 1/\sqrt{L_e C_X L_c C_{gs2}} \tag{4}$$

From (3) as well as from the qualitative analysis above (1), the frequency characteristic of the LNA can be controlled with and by selecting proper values of L_e, L_c and C_X. A small C_e of 40 fF is added to C_X to control the BW as well the Q-factors as in (2) for the optimal gain flatness. In this design, L_e and L_c are selected as 3.6 nH and 11 nH, respectively.

4 Simulation results and discussion

Fig. 3 (b) presents the S21 performance of the designed LNA without L_e and with various values of L_e to examine its effect on the bandwidth of the LNA. The bandwidth is enhanced significantly, more than 2.2 times. S21 achieves its best performance with L_e value of 3.6 nH.

The LNA is simulated and designed in 0.18-μm CMOS process from 1 V supply. Fig. 3 (c) shows the gain and matching performance over -1 dB bandwidth from 2.8 to 11.2 GHz band. The average power gain is around 10.5 dB and almost constant within the full bandwidth. Good input/output matching with S11/S22 of below $-10/-13$ dB is observed in the whole band, respectively.

The simulated NF of the proposed LNA is also presented in Fig. 3 (d), which is improving with frequency. It is because the effect of L_s on input matching and NF increases at high frequencies. This is also the advantage of CG topology over other architectures like CS or cascode amplifiers, whose NF is increasing with frequency. In this LNA design, the NF values range from 2.58 to 4 dB, which is good at GHz range of operation frequency.

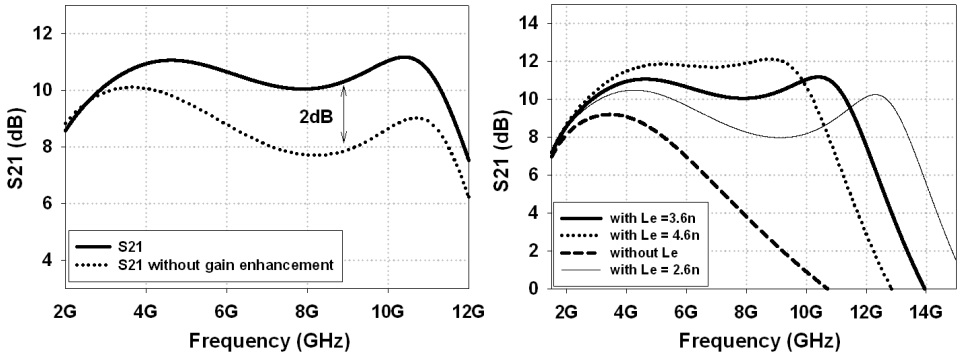
Two-tone test with 1 MHz spacing is applied at various frequencies to examine the IIP3 linearity performance of the proposed LNA. In the frequency range of 3–10 GHz, the IIP3 varies from -5 to -8.1 dBm. The linearity is acceptable given moderate power consumption.

Table I summarizes the designed LNA performances and compare with other state-of-the-art published works in wideband LNA designs, shown in Fig. 3 (e). The proposed LNA consumes only 4.6 mW from 1 V supply with good performance for broadband applications. This is the first reported common gate folded LNA intended for 3.1–10.6 GHz full UWB band and broadband applications using standard 0.18-μm CMOS technology.

5 Conclusion

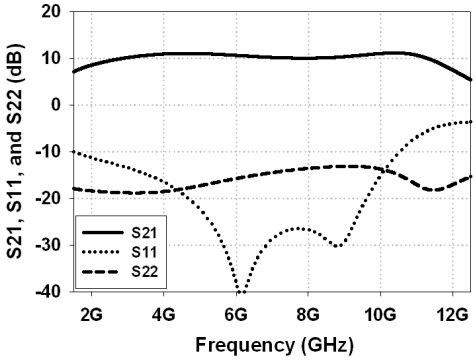
A low power broadband LNA working in the UWB full band of 3.1–10.6 GHz was proposed and designed in 0.18-μm CMOS technology. Wideband performance is achieved by adopting bandwidth extension technique for folded common-gate (CG) topology using an extra inductor. The large headroom

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

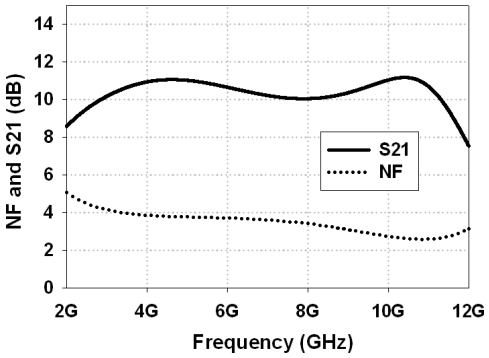


(a)

(b)



(c)



(d)

	BW (GHz)	Power (mW)	S21 (dB)	S11/S22 (dB)	NF (dB)	V_D (V)	Tech. μm	Topology
[1]	3.1-10.6	9	9.3	<-10	~5.3	1.8	0.18	LC Ladder
[4]	2.7-9.1	10	7	<-10	3.8-6.9	0.6	0.18	Distributed
[5]	3.1-10.6	9	15.1	<-10	2.1-2.8	1.2	0.13	Feedback
[6]	3.1-10.6	27	14.9	<-10	2.9-3.6	0.9	0.18	Folded-CS
[7]	3.1-10.6	20	9.7	<-11	4.5-5.1	1.8	0.18	CG
[2]	1.5-8.1	2.62	8.6-11.7	<-9	3.6-6	1.3	0.13	CG
[8]	3-10	13.5	13.5	<-10	2.7-4.2	1.2	0.13	Reuse-CG
This work	2.8-11.2	4.6	10.2-11.2	-10/-13	2.58-4	1	0.18	Folded-CG

(e)

Fig. 3. Simulated S21 with and without extra forward path for gain enhancement (a), S21 without Le and the effect of Le on BW extension at 2.6 n, 3.6 n, and 4.6 nH (b), simulated S11 and S22 of the proposed LNA (c), S21 and NF (d), and performance comparison table of the proposed LNA with previously published works (e).

of single stack LNA ensure good linearity performance at low supply voltage for low power consumption. The proposed LNA has an average gain of 10.5 dB and NF of around 3 dB over the full UWB band. The folded CG LNA consumes only 4.6 mW from 1 V of supply voltage. With technology scale down, the proposed LNA will achieve even better performance. It is suitable for cost-effective low-power trends of CMOS hardware integration in the next generation wireless and UWB radios.

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009

Acknowledgments

The authors would like to thank Centre for Telecommunication Value-Chain Research (03/CE3/I405) supported by Science Foundation Ireland under the National Development Plan.

DOI: 10.1587/elex.6.1745
Received October 30, 2009
Accepted November 19, 2009
Published December 25, 2009