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Benchmarking CMOS Adder Structures

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Abstract – **Adders are key components in digital signal processing, performing not only addition operations, but also many other functions such as subtraction, multiplication and division. The difficulty with comparing adder structures from different sources is that quite often different implementation techniques and technologies have been used in the design. A second problem that arises when comparing structures is that several different measurement techniques may have been used, the target technology can differ and key features may not been measured. Therefore, this paper will investigate the seven most commonly used adder structures in a way which makes them directly comparable. This is achieved by implementing all adder structures with the same technology, the same level of abstraction and then using the same set of tools to determine the features of each of the designs.**

Keywords – **Adder Structures, High-Level CMOS Design, Ripple Adder, Transmission Gate Adder, Carry-Skip Adder, Carry Look Ahead Adder, Carry Select Adder, Conditional Carry Adder, Conditional Sum Adder, Carry Save Adder, Tree Adder, Chain Adder.**

I INTRODUCTION

In this paper the implementation of seven adder structures is presented. The Ripple Adder (ADD) [1] used was implemented using AND, OR and XOR gates and inverters. For the Transmission Gate Adder (TG), both Carry Select Adders and the Conditional Sum Adder were implemented as shown in [1]. Version 1 of the Carry Select Adder (CS) has the original carry select logic as found in standard texts. In Version 2 of the Carry Select Adder (CS_2) the carry select logic part is replaced by a 2 to 1 multiplexer as suggested in [1]. The Carry-Skip Adder (CSK) was implemented as shown in [2]. In this case only the transistors in the output of the ripple shells were replaced by multiplexers. The reason behind this is that all designs can be described at the same level of abstraction, thus making them directly comparable. Version 1 of the Conditional Carry Adder (CCA) was implemented as shown in [3]. Version 2 of the Conditional Carry Adder (CCA_2) differs from the original design in [3] by having a serial jumping carry (JC) section. The Carry Look Ahead (CLA) adder was implemented as suggested in [4].

All adder structures were implemented using the VHDL hardware description language. The designs were synthesised into the ES2 ECDP 0.7µm CMOS technology without any design constraints using the Synopsys Design Compiler. All results were obtained using the typical industrial simulation setting.

a) Area Requirements

From Figure 1 the relationship between area and bit size for the different adder structures can be seen. Adders which have hierarchical selection used in a parallel or expanding tree such as the carry or sum computation blocks of the CLA have the fastest growing area requirements, with respect to the bit size. There are four structures with this feature presented in

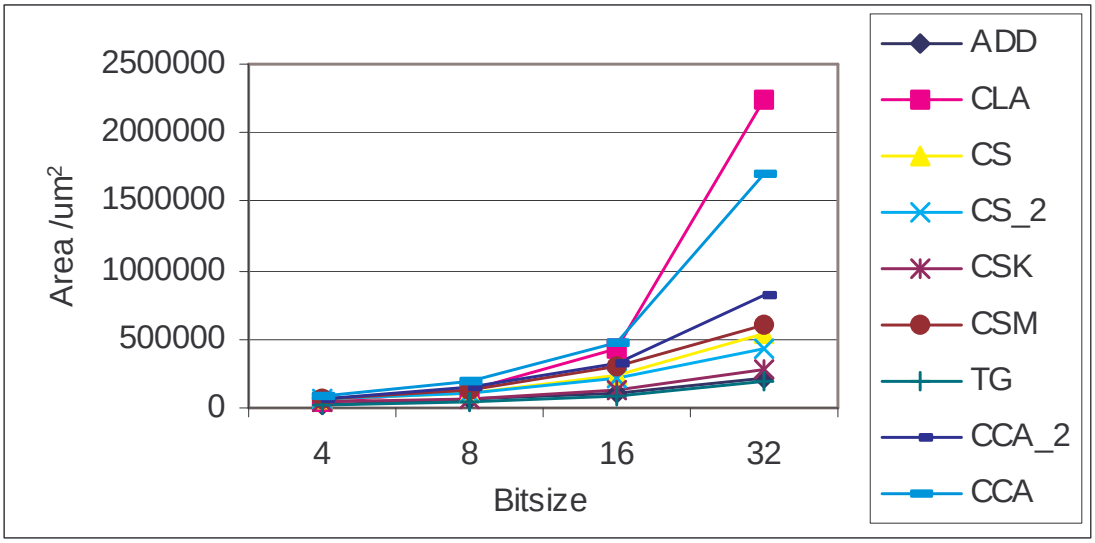

Figure 1: Area Requirements

this paper. The Carry Look Ahead Adder, which has an expanding tree carry computation structure has an exponential growth rate which causes the fastest growing area requirements of all structures in this project. Version 2 of the Conditional Carry Adder also has a hierarchical carry selection, which is used in parallel and has the second fastest growing area requirements. Version 2 of the Conditional Carry Adder has also a hierarchical carry selection part, but it is used serially. Therefore, this structure gives Version 2 a slower growth rate in area requirement. The Conditional Sum Adder has the fifth highest area requirement, due to a structure which has hierarchical multiplexer parts where both sum and carry bit are selected. The area requirement growth rate for Carry Select Adders is less than the large adders growth rate. However, it is larger than the growth rate of small adders such as the Ripple Adder, the Transmission Gate Adder and the Carry-Skip Adder. The low area and the linear growth in area requirements for these three small adders are both due to the parallel structure where all bit stages are similar.

b) Active Capacitance

Figure 2 shows the active capacitance, which is proportional to the power consumption [5], of the adder structures implemented in this project. The active capacitance was determined using PowerCount [6] for a uniform white noise input to provide a measure for the maximum power consumption of each adder structure.

The active capacitance of all adder structures grows approximately at the same rate as the area requirements, which were shown in Figure 1. The active capacitance of a circuit depends of two variables, the physical node capacitance and the switching activity. The increase in area requirement is caused by the increased number of the transistors in the circuit. This increases the physical node capacitance, but the increase in the area does not mean a direct increase in switching activity in most digital circuits. The direct relationship between the area requirements and active capacitance is caused by the fact that the basic structure remains the same when the adder size is increased, so in theory the switching activity should increase at the same rate as the area requirements increases. As seen from Figure 2 and Table 2 the Carry Look Ahead Adder has the largest active capacitance growth rate when the bit size is increased in addition to the fastest growing area requirements. The smallest adder structure, the Transmission Gate Adder has the smallest active capacitance values.

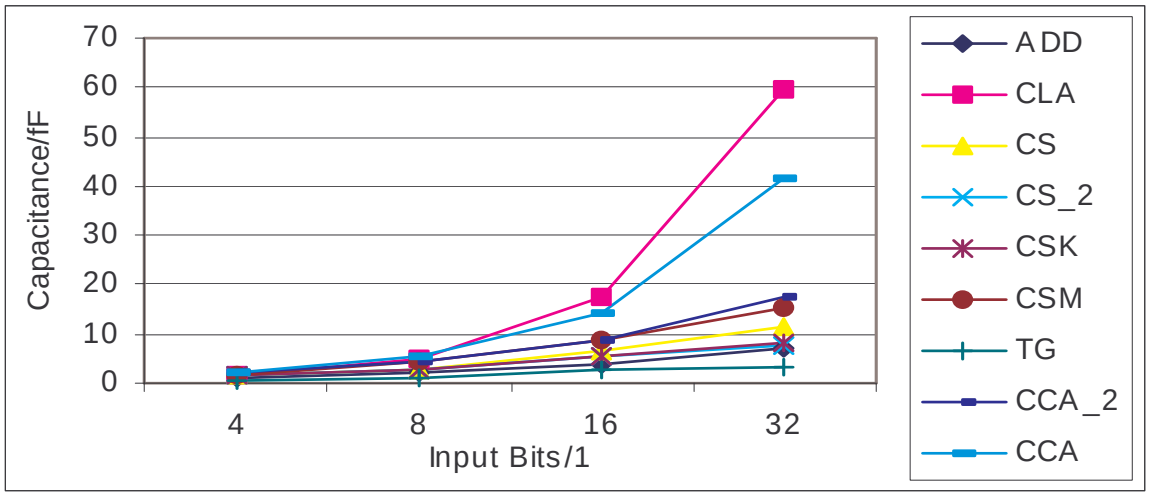

Figure 2: Active Capacitance

c) Maximum Operation Frequency

As can be seen in Figure 3 ,the fastest 4-bit adder is the Version 2 of the Conditional Carry Adder. The second fastest adder is the Conditional Sum Adder, which has 0.7% smaller maximum operation frequency than the Version 1 Conditional Sum Adder. Third fastest is the Version 1 Conditional Carry Adder. With this adder the difference is 0.9%. Since these values are within a range of 1%, the difference may be caused by error in the delay measurements. For larger bit sizes the Conditional Sum Adder is clearly the fastest adder structure in this project. Surprisingly, for 4-bit adders the Transmission Gate Adder and the Ripple adder are both faster than the Carry Look Ahead Adder. For the 8-bit adders the effect of parallel or tree selection structure can be seen more clearly than with the 4-bit adders. The Ripple Adder, Transmission Gate Adder and the Carry-skip adders are clearly slower than the adders with these parallel or tree-like selection blocks. When increasing the bit size from 8 to 16 more changes can be seen between Carry Select Adders and Conditional Carry Adders. Here the increase in maximum operation speed between the Carry Select Adders is caused by the sequential carry signal of Version 2. Between the Conditional Carry Adders the growth in maximum operation frequency difference is caused by the delay characteristics of the last multiplexer in the JC components. The difference between 4-bit adders is 0.9%, between 8-bit adders it is 9.6%, between 16 adders the difference is 16.3%, but between 32-bit adders it is only 8%. The reason why the maximum operation frequency values for the Conditional Sum Adder starts to decrease more for larger bit sizes is the fan out limitation of the multiplexers, as for Version 2 of the Conditional Carry Adder.

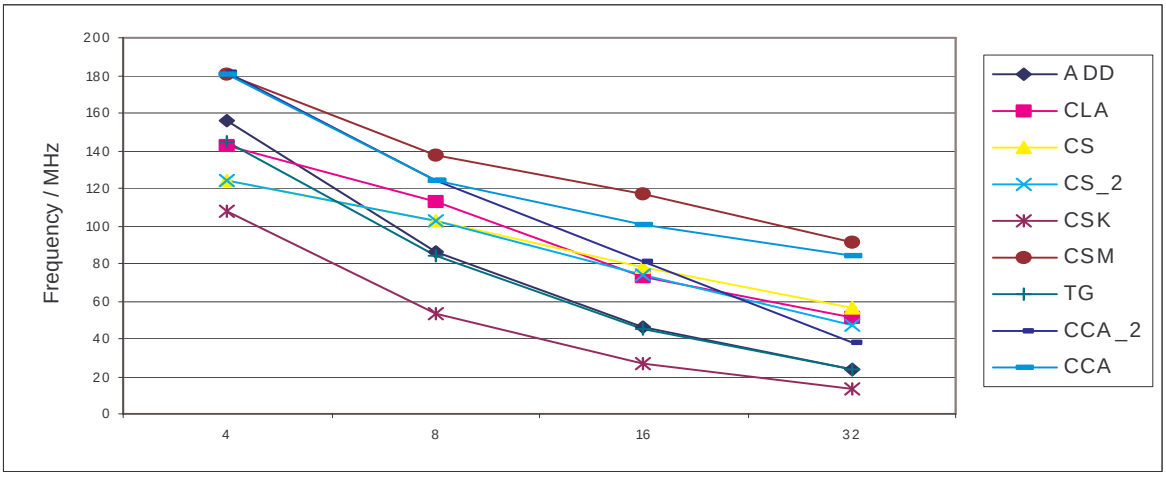

Figure 3: Maximum Frequency of Operation

II CONCLUSIONS

Most of the adder structures discussed in this paper are applicable to general purpose designs, with a few exceptions. The first exception is the Carry-Skip Adder, which is the slowest adder for all bit sizes. It has also larger area requirements and higher active capacitance than the Ripple Adder or the Transmission Gate Adder for all bit sizes. It may always be replaced with either one of these adder structures. The second adder structure which can be always replaced is the Carry Look Ahead Adder. For 8 to 32 bit circuits the Conditional Sum Adder has better results across all three features than the Carry Look Ahead Adder. For the 4-bit adder this adder structure can be replaced with the Transmission Gate Adder or with the Ripple Adder, because both of these structures have better results in all measured features. Either of the Conditional Carry Adders also should be avoided in deigns. The Conditional Sum Adder has better results across all measured features with one exception. The 16-bit Version 2 of the Conditional Carry Adder has 4.3% smaller active capacitance compared to the 16-bit Conditional Sum Adder. The Ripple Adder can be usually replaced with the Transmission Gate Adder to achieve better power consumption and smaller area requirements. The only reason why it might not be replaced is the frequency limitation of the Transmission Gate Adder. For a 4-bit adder the Ripple Adder has 7.3% higher maximum frequency of operation. For bit sizes 8 to 32 the difference in maximum operation frequency between these two structures is less than 3%.

This paper has presented a comprehensive comparison of the seven most commonly used adder structures. A detailed analysis of the area requirement, the maximum operational speed and the power consumption has provided a convenient way to compare the advantages and trade-offs of each design. Thus, the adder best suited to any given design may be easily selected using the data presented.

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