An Embedded Rectifier-Based Built-In-Test Circuit for CMOS RF Circuits

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***Abstract*—Built-In-Test (BIT) for Radio Frequency Integrated Circuits (RFIC) is an effective method to reduce the testing cost, especially with the increase of integration level and operating frequency. In this work, a fully integrated CMOS BIT methodology is proposed. The BIT circuit used is rectifier-based and gate-source connected MOS transistor with Substrate Positively-Biased (SPB) scheme is used to further improve the detecting sensitivity. With little current consumption, high input impedance and high frequency scalability this circuit can predict complex high frequency performances of RF circuits such as gain, operating frequency, bandwidth and linearity. Besides, the influence of Process, supply Voltage, and Temperature (PVT) variations on the performance of RF circuits can also be monitored by using this BIT circuit.**

I. INTRODUCTION

Recently, the testing of Radio Frequency Integrated Circuit (RFIC) has faced great challenges especially for multi-gigahertz RF components. Two main problems exist regarding to the testing of RFIC: relaying the multi-gigahertz RF signal to the external tester without affecting the performance of tested RF circuits and use of prohibitively expensive RF production tester. These problems are mainly due to the RF design has been driven far into the future by the advanced technology and market requirement, while testing practice has not followed the trend of high frequency and high integration level. As a result, reliable high frequency testing has become a significant restrictive and influencing factor for the time-to-market of novel wireless products [1]. Built-In-Test (BIT) provides a flexible way to test the High Frequency (HF) circuits by including BIT circuits on-chip and allowing HF circuits tested by using lower frequency or DC external testers [2]. Since the last two decades, BIT or BIST (Built-In-Self-Test) strategy has been a common practice for the testing of digital and mixed-signal systems [3,4], in which the most commonly used method is to employ Digital-to-Analog Converter (DAC) to generate analog stimuli and Analog-to-Digital Converter (ADC) to quantize the output in digital form. However, when considering RFIC testing, some issues need to be taken into account such as powerful ADC & DAC, area overhead issue for embedding, power consumption, etc. Presently, some advanced works to develop efficient testing techniques for the RF systems and individually building blocks have been carried out [5-9]. Recent efforts for RF circuit testing have focused on the design of on-chip embedded detectors, or sensors, where the output signals can be tested easily [5, 7-8], and on the methodologies and algorithms for automated test design [6, 9]. Instead of testing the devices specifically for performance metrics, the outputs of the detectors were used to estimate the target test specs when the Circuit-Under-Test (CUT) was stimulated.

Fig.1 shows the schematic with embedded BIT circuit included in RF system, and there are several monitoring points can be accessed for the critical signal paths to evaluate the performance of RFIC. In this figure, the stimulus is provided by external signal source, but the response of different circuit blocks can be obtained through the output of BIT circuit.

Based on the testing architecture in Fig.1, an embedded CMOS BIT circuit for the testing of RFIC is proposed in this work. For verification, a 2.4GHz Low Noise Amplifier (LNA) has been designed and its high frequency performances have been verified by using this BIT circuit. The BIT circuit is rectifier-based and uses Substrate Positively-Biased (SPB) Gate-Source (GS) connected MOS transistors to realize the rectifying of input HF signal, and the detecting sensitivity has been improved. Because of the high input impedance of this BIT circuit, the performance of RF circuits such as gain, linearity, operating frequency and bandwidth can be obtained without influencing the

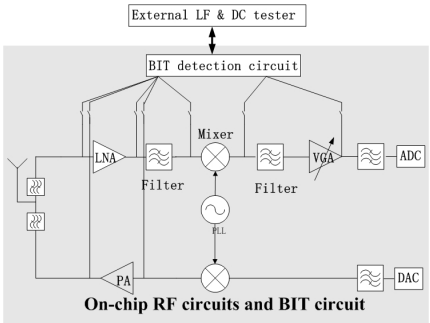

Figure 1. Schematic with on-chip BIT circuit for RF systems

performance of the attached RF circuit. Besides, the influence of Process, supply Voltage and Temperature (PVT) variations on the performance of RFIC is also investigated by using this circuit. With this BIT methodology, the high frequency output signal of RF circuits can be transformed into DC signal and can be tested easily by using low frequency or DC external tester.

II. BIT CIRCUIT

The BIT circuit is illustrated in Fig.2, which is a charge pump configuration proposed for high voltage generation [10]. In the design, SPB scheme with +0.6V is introduced to reduce the turn-on voltage of the GS connected MOS transistors and to improve the detecting sensitivity. Capacitor C_1 and transistor M_1 shift the voltage $\upsilon_{in}(t)$ up at A and C_2 and M_2 rectify the voltage at A. When equilibrium is reached the circuit enters its steady state mode and delivers a constant output current and a constant output voltage. Since there is no biasing voltage needed, this detection circuit is actually a passive circuit, and would not consume additional power when applying in the testing of power hungry RF circuits. In this design, Agilent ADS simulator is used for verification and UMC 0.18um mixed signal design kit is adopted.

The parameters of the components in this circuits are C_1=100fF, C_2 =700fF, while the channel length and width are 0.3um and 0.35um respectively. Fig.3 is the dependence of transient output voltage of this BIT circuit on the input signal amplitude. The voltage amplitude a1 of input signal sweeps from 0.1V to 0.3V in 0.1V steps, and the operating

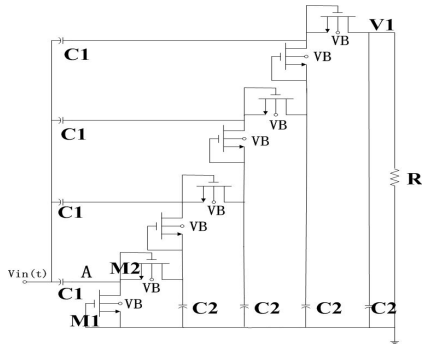

Figure 2. BIT circuit schematic with SPB GS connected MOS devices

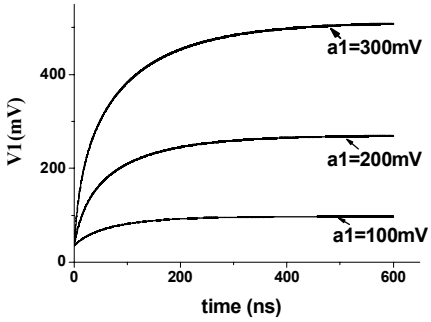

Figure 3. Transient output of BIT circuit at different input amplitude

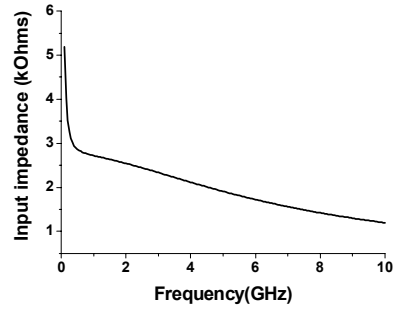

Figure 4. Input impedance of the BIT circuit in Fig.2

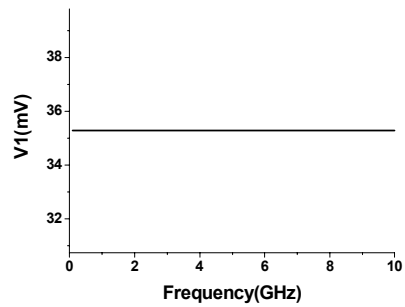

Figure 5. Output of the BIT circuit at different input signal frequency

frequency is 2.4GHz. It can be seen that the input HF signal can be transformed into DC value and the output voltage varies with the change of the input signal amplitude. From Fig.3 it can be found that this BIT circuit requires 0.4us settling time.

The equivalent input impedance of this BIT circuit is analyzed and this impedance should be large enough to avoid any loading effect when attached to the tested RFIC. From Fig.4 it can be seen that this impedance is larger than 1Kohms under 10GHz operating frequency, and would have little influence to the attached RFIC.

Fig.5 investigates the frequency scalability of this BIT circuit and shows the dependence of the DC output voltage on the input signal frequency in which the input frequency changes from 100MHz to 10GHz. The result illustrates that there is no significant change of the DC voltage output under this frequency range. This figure shows the high frequency scalability of this circuit when using it to test RFIC with even higher operating frequency.

III. SIMULATION RESULTS

In order to investigate the validity of this BIT methodology for the testing of RF circuits, a two-stage 2.4GHz LNA with fully on-chip input matching network is designed. The gain of LNA is 18.6dB, noise figure=2.16dB, S11=-9dB, IP1dB=-10dBm, bandwidth=950MHz and the current consumption is 7.5mA. By attaching the BIT circuit

to the tested LNA circuit, the validity for RFIC testing of this BIT circuit is verified.

A. Sensitivity analysis

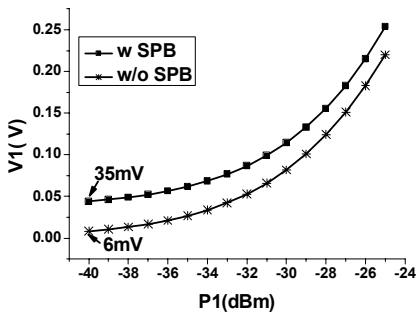

Figure 6. Sensitivity comparison with and without SPB scheme

The high sensitivity performance of BIT circuit is important for RF circuits with weak input signal. During detecting sensitivity analysis, the input signal amplitude of LNA sweeps from -40dBm to 0dBm in steps of 5dB, and DC output of BIT circuit is investigated. Fig.6 evaluates the effectiveness of SPB scheme used in this BIT circuit for the improvement of detecting sensitivity. With SPB MOS transistors in the BIT circuit, at -40dBm input power, the DC voltage output of the BIT circuit is 35mV compared to 6mV when without SPB. Hence it can be seen that the detecting sensitivity can be improved to a large extent by adopting the SPB scheme.

B. Gain performance

Fig.7 gives the extracted gain of LNA which is measured by using the BIT circuit attached to the input and output of the tested LNA circuit respectively. The outputs of BIT circuit when attached to the output and input of LNA are each designated by the curve with marker M1 and M2 respectively. The gain of LNA can be measured as the distance in dB between marker M1 and M2 at the start of linear region in both curves. It can be found that the extracted gain is 18.4dB, and has no significant difference when compared with the high frequency gain 18.6dB of stand-alone LNA.

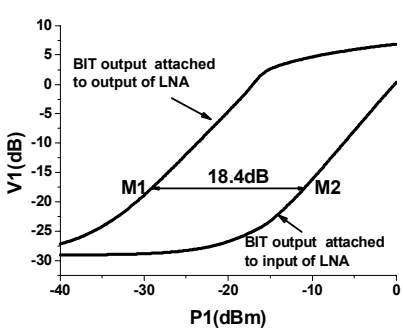

Figure 7. Extracted gain from the output of the BIT circuit

C. Operating frequency & Bandwidth

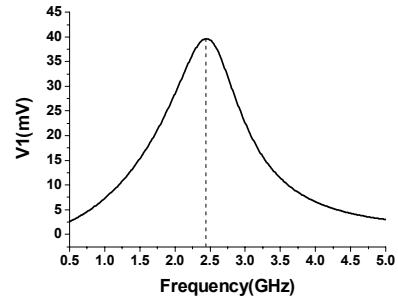

Figure 8. Operating frequency and bandwidth extracted from the DC output of the BIT circuit

For narrow-band and wide-band RF ICs, it is important to know the operating frequency and the bandwidth of the circuits. By investigating the dependence of DC output voltage V1 of the BIT circuit on the input frequency at fixed input signal amplitude, the operating frequency and bandwidth of the tested LNA can be obtained which is shown in Fig.8. The extracted operating frequency and bandwidth for this 2.4GHz LNA are 2.45GHz and 890MHz respectively.

D. Linearity performance

Fig.9 shows the comparison of the output of the LNA and the output of the BIT circuit, and the input 1dB compression point can be extracted from these curves, which is -12.5dBm. From the results we can see that the extracted linearity has a certain error because of the rectifying behavior of this BIT circuit.

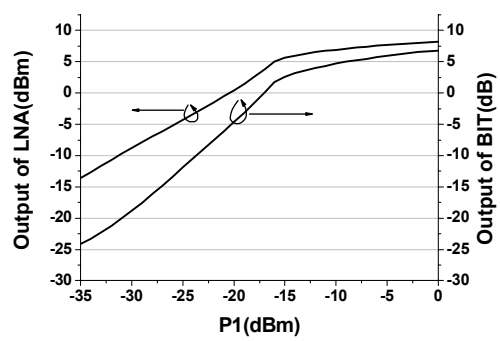

Figure 9. Extracted linearity performance

E. PVT variation monitoring

During production evaluation, the influence of PVT variations on the performance of RFIC needs to be fully investigated. Because this BIT circuit is rectifier-based, most of circuit components work at a lower frequency than the input signal frequency. So, this BIT circuit can be used to

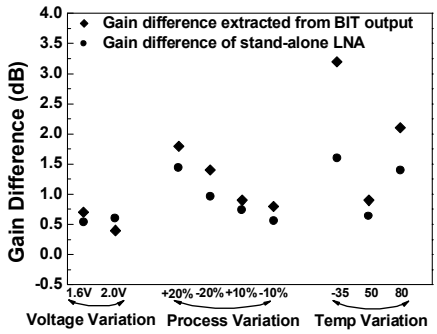

Figure 10. Comparison of gain difference due to PVT variations

evaluate the influence of PVT variations on the performance of RF circuit. During the analysis, ±20% and ±10% percentage variations are used for all the parameters in the circuit, which includes LNA and BIT circuit. The supply voltage changes from 1.6V to 2.0V and operating temperature varies from -35℃ to +80℃. For process variation, two extreme process variations are included, namely all parameters in the circuit vary from unchanged to the plus or minus specified percentage variation.

Fig.10 shows the gain difference due to PVT variations. Shown in the figure are the gain differences extracted from the output of the BIT circuit, and that obtained from the stand-alone LNA. From the results obtained, this BIT scheme is able to accurately measure the gain variations, to within 0.5 dB of the LNA for significant variations in process and voltage. For obvious temperature variations, the BIT circuit is not as accurate as each transistor in the BIT circuit will experience small variations in threshold voltage due to temperature changes. However even for over a 50℃ variation, the error is only 1.5 dB. Thus it can be said that PVT variations can be detected and monitored through this on-chip BIT circuit.

Table I also shows the performance of this stand-alone LNA compared with the same LNA with BIT circuitry attached, also the results extracted from BIT circuit. It can be found there is nearly no loading effect when attaching this BIT circuit to do RF testing.

TABLE I. PERFORMANCE COMPARISON OF STAND-ALONE LNA, LNA WITH BIT ATTACHED AND PERFORMANCES EXTRACTED FROM BIT OUTPUT

	Gain (dB)	f_0 (GHz)	bandwidth (MHz)	NF (dB)	S11 (dB)	S22 (dB)	IP1dB (dBm)
1*	18.6	2.4	950	2.16	-9	-1.84	-10
2*	18.6	2.4	950	2.16	-9	-1.96	-10
3*	18.4	2.45	890	-	-	-	-12.5

1 performance of stand-alone LNA

2 performance of LNA attached with BIT circuit

3 performance extracted from BIT DC output

IV. CONCLUSIONS

An embedded CMOS Built-In-Test (BIT) circuit is proposed for the testing of RFIC. The Validity of this BIT circuit for functional verification of RFIC has been tested by using LNA. The BIT circuit used is rectifier-based and SPB scheme is used to further improve the detecting sensitivity. This BIT circuit has high input impedance, little power consumption and high frequency scalability. By using this circuit, the high frequency performance metrics such as gain, operating frequency, bandwidth and linearity can be extracted from the DC output voltage of this BIT circuit. Also, the influence of PVT variations on the performance of RFIC can be investigated. The achieved results show that this BIT methodology can be applied to carry out functional verification of RFIC and also used to monitor the PVT variations without affecting the HF performance of the tested RFIC.

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