Computationally efficient fixed-parameter digital control of power converters

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***Abstract*—This paper studies the effect of variable sampling frequency on the dynamic of the fixed-parameter digital compensator in switched-mode power supplies. Based on the resulting analysis, we propose a simple technique to design a computationally efficient adaptive predictive functional controller (PFC) which can be implemented in a low-cost micro-controller. While the approach should have general applicability to systems where the sampling/switching frequency is varied, in this paper we use the example of a flyback power converter operating in discontinuous conduction mode (DCM). The performance of the proposed controller is verified with both simulation and experimental results.**

I. Introduction

In recent years, digital computing power has become a viable alternative to its analog counterpart thanks to the rapid development of IC computing resources, paralleled by vast reduction in their production cost and multi-feature integration capability. Digital control of power converters not only lends itself to expensive and large systems, such as solar power inverters, 3-phase AC/AC converters, etc., but also to low-cost AC/DC applications, e.g. laptop chargers, LED lighting and many others.

In the field of off-line AC/DC external power supplies, a single stage flyback converter, as illustrated in Fig. 1, is a primary candidate for low-power devices due to its inherently simple structure and cost-effective nature. Traditionally, the flyback converter is controlled by an analog compensator through an opto-isolation mechanism. Although this approach has been successfully applied in the past decades, it can not keep up with the stringent requirements on the converter efficiency, performance, size and cost which are recently imposed to cope with the rapid growth in both the number and processing power of personal gadgets.

Digital control has been intensively exploited to improve the energy conversion efficiency of flyback converters [1]–[3]. Due to the nature of these approaches, the controller has to use a variable switching frequency in order to minimize the total losses occurring inside the system. As the properties of the converter loss is strongly nonlinear, it is impossible to analytically express the optimal switching frequency as a simple function of the flyback converter parameters and external excitations [2], [3]. The wide variation of the input voltage and output load, in addition to the variable switching frequency, pose a serious challenge to designing a stable and efficient compensator for such a system.

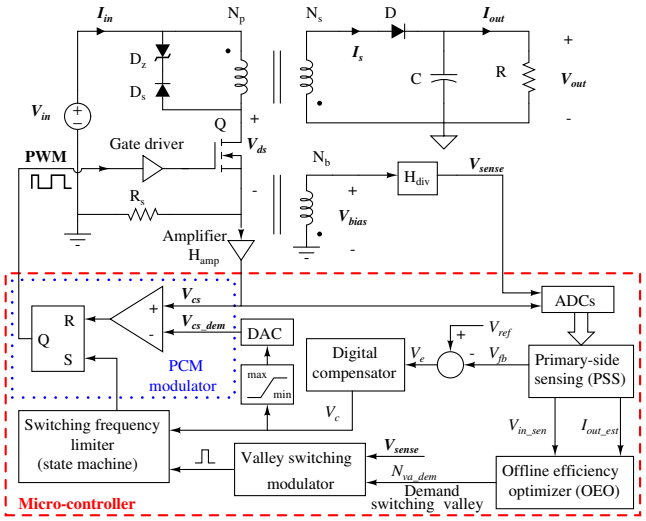


Fig. 1. Block diagram of digital peak current mode (PCM) controller with primary-side sensing (PSS) and off-line efficiency optimization for a flyback converter application

This paper is motivated by the fact that:

i) There is wide variation in the system model, resulting in an impossible task for a 'traditional' robust H_∞ control approach [4].
ii) We have specific knowledge of the origin of the parametric variation. Therefore, we need to exploit this knowledge.
iii) Since the proposed solution will be implemented in a low-cost micro-controller, we have very limited computational power at a sampling frequency in the region of 100kHz.

We want to use (ii) to come up with a controller that satisfies (iii), i.e. is implementable. This paper firstly studies the effect of a variable sampling frequency on the dynamic of a fixed-parameter digital compensator in switched-mode power supplies. Based on the resulting analysis, we propose a simple technique to obtain an efficient adaptive predictive functional compensator for a flyback power converter, as sketched in Fig. 1.

The remainder of this paper is organized as follows. Firstly, the operation of the proposed control architecture and the effect of variable switching frequency on the dynamic of the digital

compensator are addressed in Section II. Section III describes how to derive a simplified converter model, which is then used for compensator design. Section IV presents the application of the proposed controller to a Flyback converter and verifies its performance through both simulation and experimental tests. Finally, the conclusion is drawn in Section V.

II. Microcontroller-based digitally controlled flyback converter

A. Control architecture

The operation of the proposed control structure in Fig. 1 can be outlined as follows. The primary-side sensing (PSS) block is based on the magnetizing sensing principle [5], [6] to estimate the output voltage from the bias winding. The use of PSS helps to not only eliminate the opto-coupler and its auxiliary circuit, but also to improve the output voltage regulation and converter performance. In addition to the feedback signal estimation, the input voltage and load current could be also obtained from this block.

Peak current mode (PCM) control is employed to regulate the output voltage. Unlike traditional PCM control, where the switching frequency is fixed and decided by an internal oscillator, the proposed controller implements valley switching, also known as quasi-resonant control [7], to improve the system efficiency at the expense of a variable switching frequency.

In order to maximize the converter efficiency, an off-line optimization procedure, as described in [2], [3], is applied to pre-calculate the switching frequency as a function of input voltage and output load. The optimal switching frequencies for different input voltages is illustrated in Fig. 2. Due to some implementation difficulties [2], [3], the optimum switching frequencies are transformed into equivalent switching valleys and saved into a look-up table (LUT), which is essentially the efficiency optimizer block in Fig. 1.

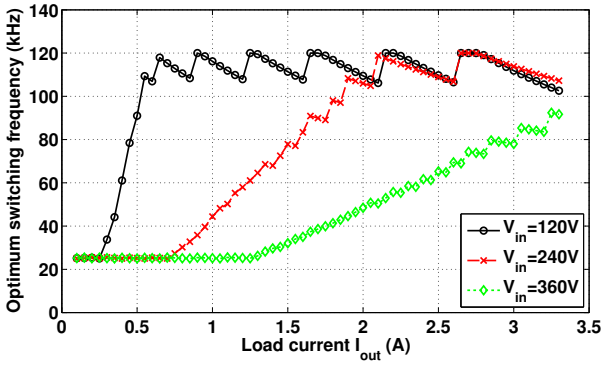


Fig. 2. Optimum switching frequency at different working loads for a 65W flyback converter with $V_{in} = 120V, 240V$ and $360V$. The searching range is limited to $25kHz - 120kHz$ which is required to minimize EMI and audible noise

The main function of the valley switching modulator is based on the waveform of the bias winding voltage and sets the SR latch to turn the MOSFET on at the demand valley, which is output by the efficiency optimizer block. To minimize the audible noise and EMI, the switching frequency should

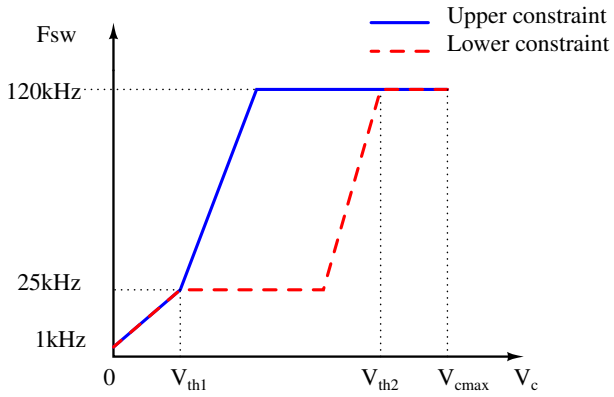


Fig. 3. Typical curves of upper and lower switching frequency threshold levels

be restricted to a pre-defined range during the operation. This restriction is implemented in the switching frequency limiter block of Fig. 1. In particular, this block stores a set of upper and lower frequency constraints, as a function of the compensator output, V_c. A typical choice of these constraints is sketched in Fig. 3. The valley switching operation is achieved only if the PWM frequency lies between the upper and lower threshold levels, otherwise it will be clamped by either one of these two limits, whichever is violated. When the upper and lower constraints coincide, as in the case of Fig. 3 with $V_c \leq V_{th1}$ (light load) or $V_c \geq V_{th2}$ (over load), the PWM frequency will be equal to the lower one and there is no valley switching operation any more. Though the efficiency optimizer function suggests the frequency at which the converter should operate, the real working frequency is always decided by the frequency limiter block.

B. Effect of variable sampling frequency on digital compensator

From a practical perspective, it is much easier and more stable to sample the feedback signal and calculate the compensator output once per switching cycle rather than via fixed sampling period from the theoretical calculation. This hardware-favored design, however, leads to a huge mismatch between the theoretical and experimental performance of the compensator, when the update rate is not the same order as the designed sampling frequency. The discrepancy is mostly due to the variation of the equivalent continuous-time poles and zeros in response to the changing sampling period, subject to fixed parameters of the digital compensator.

For simplicity, we will demonstrate the idea through an example. Without loss of generality, it is assumed that the discrete-time compensator has 2 poles and 2 zeros, with an effective sampling frequency of T_{pwm}, and is formulated by,

$$G_c(z) = G_{c0z}\frac{(1 - z_1 z^{-1})(1 - z_2 z^{-1})}{(1 - p_1 z^{-1})(1 - p_2 z^{-1})}, \qquad (1)$$

where G_{c0z} denotes the controller gain while z_1, z_2, p_1 and p_2 are compensator zeros and poles, respectively. The continuous-time equivalent of $G_c(z)$ can be found via Tustin's transformation, which substitutes $z^{-1} = \frac{1-sT_{pwm}/2}{1+sT_{pwm}/2}$ into Eq. (1) and

collects terms to

$$G_c(s) = G_{c0}\frac{(1-\frac{s}{w_{z1}})(1-\frac{s}{w_{z2}})}{(1-\frac{s}{w_{p1}})(1-\frac{s}{w_{p2}})}, \tag{2}$$

where

$$G_{c0} = \frac{G_{c0z}(1-z_1)(1-z_2)}{(1-p_1)(1-p_2)},$$
$$w_{z1} = \frac{z_1-1}{z_1+1}\frac{2}{T_{pwm}}, \qquad w_{z2} = \frac{z_2-1}{z_2+1}\frac{2}{T_{pwm}},$$
$$w_{p1} = \frac{p_1-1}{p_1+1}\frac{2}{T_{pwm}}, \qquad w_{p2} = \frac{p_2-1}{p_2+1}\frac{2}{T_{pwm}}.$$

From Eq. (2), one can work out that the poles and zeros of the continuous-time compensator $G_c(s)$ *are directly proportional* to the sampling frequency while the compensator gain does not change, and is equal to that of $G_c(z)$. This effect can be explained in the sense that the value of a pole/zero of any discrete-time transfer function shows the relative position of their continuous-time equivalent counterparts as a function of the sampling frequency. If we retain the same values for the discrete-time pole/zero, and change the sampling frequency, this will vary the continuous-time poles/zero correspondingly. In general, a fixed discrete-time transfer function with a variable sampling frequency is equivalent to variable continuous-time transfer function and vice versa.

III. Digital controller design

A. Converter small signal model

Due to constraints on the switching frequency, as well as the size of the transformer, the converter is designed to stay in discontinuous conduction mode (DCM) at all operating conditions. Hence, only a DCM small signal model of the flyback converter is needed for the controller design phase.

Since the system in Fig. 1 uses a peak current modulation to generate the PWM signal and regulate the output voltage, its small signal model can be derived based on the same principle as described in [8]–[10]. Figure 4 shows a complete block diagram of the small signal model of the DCM flyback converter, taking into account the effect of the magnetizing sensing mechanism, and voltage divider circuitry, as well as the A/D and D/A converters. In order to design the digital compensator $G_c(z)$, it is necessary to know the transfer function of all blocks within the control loop.

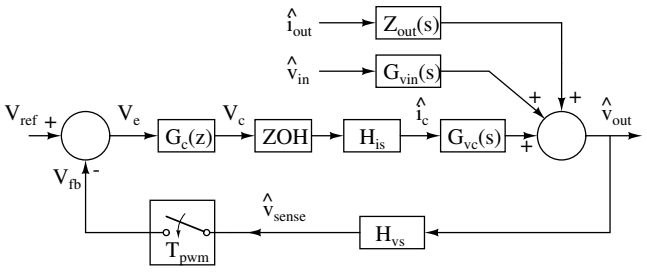


Fig. 4. Block diagram of the small signal model of the digitally controlled Flyback converter operating in DCM. H_{vs} and H_{is} represent the output voltage and inductor current sensing gains respectively. ADC and DAC are described by the sampler and zero-oder-hold block respectively. $G_c(z)$ is the digital compensator which we want to design.

It is presumed that the primary-side sensing function performs correctly and consistently, irrespective of converter operating point variations. Therefore, the transfer function from the output voltage V_{out} to the sense voltage V_{sense} in Fig. 1 can be simply modelled by

$$H_{vs} = \frac{\hat{v}_{sense}}{\hat{v}_{out}} = \frac{N_b}{N_s}H_{div} \tag{3}$$

where N_s and N_b are the number turns in the secondary and bias windings respectively. H_{div} represents the voltage divider gain. The current sensing gain can be simply derived from the sense resistor R_s and amplifier gain H_{amp} via

$$H_{is} = \frac{1}{H_{amp}R_s}. \tag{4}$$

A/D and D/A conversion gains can be modelled by

$$H_{adc} = \frac{2^{M_{adc}}-1}{\Delta V_{adc}}, \qquad H_{dac} = \frac{\Delta V_{dac}}{2^{M_{dac}}-1}, \tag{5}$$

where M_{adc} and M_{dac} are the number of ADC and DAC resolution bits respectively, while ΔV_{adc} and ΔV_{dac} denote the dynamic range of ADC input and DAC output respectively.

Using the state averaging method outlined in [8]–[10], with an assumption that $R_s = 0$ and all components are ideal, one can work out the transfer function from the control signal $\hat{i}_c$ to the output voltage $\hat{v}_{out}$ in DCM as

$$G_{vc}(s) = \frac{\hat{v}_{out}}{\hat{i}_c} = F_m G_{vd}(s), \tag{6}$$

where

$$G_{vd}(s) = \frac{V_{in}DT_{pwm}R}{2nL_mM}\frac{\left(1-\frac{DT_{pwm}}{2}s\right)}{\frac{DT_{pwm}RC}{4M}s^2+\left(\frac{RC}{2}+\frac{DT_{pwm}}{4M}\right)s+1}, \tag{7}$$

$$M = \frac{V_{out}}{nV_{in}}, \qquad D = \frac{1}{\sqrt{\frac{T_{pwm}R}{2L_m}}}\frac{V_{out}}{V_{in}},$$
$$F_m = \frac{1}{\left(M_a+\frac{V_{in}}{L_m}\right)T_{pwm}}, \qquad n = \frac{N_s}{N_p}.$$

Recall that M_a is the slope of the compensation ramp $i_a(t)$, while D and T_{pwm} indicate the duty ratio and period of the PWM signal respectively. Focusing on the coefficient of s in the denominator of $G_{vd}(s)$ in Eq. (7). For small L_m design, one can point out that

$$\frac{RC}{2} \gg \frac{DT_{pwm}}{4M}. \tag{8}$$

Therefore, we can replace $\left(\frac{RC}{2}+\frac{DT_{pwm}}{4M}\right)$ with $\left(\frac{RC}{2}+\frac{DT_{pwm}}{2M}\right)$ in Eq. (7) and factorize to

$$G_{vd}(s) = \frac{V_{in}DT_{pwm}R}{2nL_mM}\frac{\left(1-\frac{DT_{pwm}}{2}s\right)}{\left(1+\frac{RC}{2}s\right)\left(1+\frac{DT_{pwm}}{2M}\right)}, \tag{9}$$

Equation (9) shows that the plant has two poles and one right-half plane zero, but only one of them, i.e. the dominant pole $w_p = \frac{2}{RC}$, is located at a frequency less than half of the switching frequency. While the high frequency pole and zero is critical to predict the intra-cycle phenomena in PCM, their information is not very useful for controller design which focuses on the inter-cycle behaviour. Therefore, the converter transfer function in Eq. (6) can be simplified to

$$G_{vc}(s) = \frac{V_{in}DR}{2nL_mM\left(M_a + \frac{V_{in}}{L_m}\right)} \frac{1}{\left(1 + \frac{RC}{2}s\right)} \tag{10}$$

The model in Eq. (10) does show the variation of the converter gain and pole as a function of external excitations, i.e. input voltage and output load. However, we want to express these parametric changes in a way which is tractable and intuitive for the control design step. For a DCM flyback converter with a resistive load, one can find the following relations

$$D = \frac{I_{pk}L_m}{V_{in}T_{pwm}}, \tag{11}$$

$$R = \frac{2V_{out}^2T_{pwm}}{L_mI_{pk}^2} \tag{12}$$

where I_{pk} is the steady state peak current of the magnetizing inductor. For DCM, let us assume that $M_a \ll \frac{V_{in}}{L_m}$ and substituting Eq. (11) and (12) into Eq. (10), we can arrive to

$$G_{vc}(s) = \frac{V_{out}}{I_{pk}} \frac{1}{1 + \frac{V_{out}^2CT_{pwm}}{L_mI_{pk}^2}s} \tag{13}$$

As implied in Eq. (13), the approximated gain of the converter is dependent on both the output voltage V_{out} and inductor peak current I_{pk}. Interestingly, V_{out} is a regulated variable and should be kept constant during the operation, so the gain of $G_{vc}(s)$ is essentially inversely proportional to I_{pk}.

The representation of the pole in Eq. (13) is somehow complicated compared to that of Eq. (10); however, this can help to explain the benefit of a fixed-parameter digital control compared to the continuous-time technique. For example, if we use a continuous zero to compensate for the plant pole in Eq. (13), this compensator zero will remain fixed irrespective of the movement of the converter pole due to the change of I_{pk} and/or T_{pwm}, in response to a load variation. Unlike the continuous-time approach, a fixed discrete-time zero essentially behaves like a continuous-time counterpart, but varies linearly with the switching frequency. This effect can be exploited to compensate for the dependency of the flyback converter pole (see Eq. (13)) on T_{pwm}.

B. Fixed parameter digital compensator

Since the converter model in Eq. (13) is rather simple and implementable, a model-based control method would be a best fit for our application. Many techniques, such as Q-parameterization [11], predictive functional control (PFC) [12], etc., have been proposed to design a controller based on an internal model. In this work, PFC has been chosen because it allows us to formulate the control law directly in the z-domain.

PFC belongs to the family of model predictive control; however, it makes use of an independent internal model (i.e the model output depends on the control variable only) and the measured process output to calculate the control action. In general, we can customize the reference trajectory, i.e. desired closed-loop time response, in PFC and correspondingly derive the control law. However, for simplicity, the following settings are performed in this paper:

- The reference trajectory is an exponential decay function $y(t) = e^{-\frac{t}{T_r}}$, where T_r is the time constant of the exponential decay.
- The coincidence point, i.e. the point where the future plant response should coincide with the reference trajectory, is set to 1 sample, i.e. $h = 1$.
- The internal model is based on the converter transfer function in Eq. (13).

According to the block diagram in Fig. 4, the internal model should be formed based on the transfer function from the compensator output V_c to the feedback signal V_{fb}, which is,

$$V_{mdl} = \frac{K_{mdl}}{1 + \tau_{mdl}s}V_c, \tag{14}$$

where

$$K_{mdl} = \frac{H_{adc}H_{dac}H_{vs}H_{is}V_{out}}{I_{pk}}, \tag{15}$$

$$\tau_{mdl} = \frac{V_{out}^2CT_{pwm}}{L_mI_{pk}^2}. \tag{16}$$

The zero-order-hold equivalent of Eq. (14) is given by,

$$V_{mdl}(k) = \alpha V_{mdl}(k-1) + K_{mdl}(1-\alpha)V_c(k-1), \tag{17}$$

where $\alpha = e^{-(T_{pwm}/\tau_{mdl})}$. Using the expression of τ_{mdl} in Eq. (16), one can confirm that α does not depend on the switching frequency. This result is consistent with our discussion in Section III-A. Given the reference trajectory and the internal model, one can obtain the control law [12], via

$$V_c(k) = \frac{(V_{ref} - V_{fb}(k))(1-\lambda^h)}{K_{mdl}(1-\alpha^h)} + \frac{V_{mdk}(k)}{K_{mdl}}, \tag{18}$$

where $\lambda = e^{-\frac{3T_{pwm}}{T_r}}$. Since the desired response of the closed-loop system is specified through the reference trajectory, we can tune the controller by varying the value of T_r and h. As a rule of thumb, the desired settling time of the closed-loop system is typically approximated by $3T_r$. Note that if the parameter λ is kept fixed during the operation, the ratio T_{pwm}/T_r is constant. This implies that the closed-loop response will be forced to follow the switching period. This feature would be desirable because the nature of the response characteristic will be invariant with the switching frequency.

C. Internal model update and implementation

When the converter moves away from the designed operating point, the internal model is less accurate. Fortunately, the model can be updated to cope with the new working condition. Let's revisit the model equations in Eq. (17), (15) and (16).

Since both the model gain and pole are dependent only on the steady state peak current, it is possible to update both of them. However, it will take much less effort to recalculate K_{mdl} rather than τ_{mdl}. Hence, only gain adaptation will be exploited in this study.

If the condition $M_a \ll \frac{V_{in}}{L_m}$ is satisfied, the peak current I_{pk} can be accurately approximated by $H_{dac}V_c$. Therefore, instead of measuring the peak current, the compensator output V_c is used in this paper to adapt the model gain. Since a steady state value of the peak current is needed, a low-pass filtered version will be required.

It can be seen that K_{mdl} appears in both the internal model Eq. (17) and the control law Eq. (18), and will require a lot of computation effort to update K_{mdl}. To handle this issue, we divide the two sides of Eq. (17) by K_{mdl} and replace V_{mdl}/K_{mdl} with V_{mds}. The new model and control law are given by

$$V_{mds}(k) = \alpha V_{mds}(k-1) + (1-\alpha)V_c(k-1) \qquad (19)$$

$$V_c(k) = \frac{(V_{ref} - V_{fb}(k))(1-\lambda)}{K_{mdl}(1-\alpha)} + V_{mds}(k). \qquad (20)$$

For high-frequency noise rejection and gain-adaptive purpose, two first-order unity DC-gain low-pass filters, named $G_{lp1}(z)$ and $G_{lp2}(z)$, are added to the compensator. The complete structure of the PFC, with an adaptive gain, is illustrated in Fig. 5. Since the main function of $G_{lp1}(s)$ is to eliminate the high-frequency noise, its cut-off frequency should be chosen to be close to the half sampling frequency and away from the system loop-gain cross-over point. The cut-off frequency of $G_{lp2}(s)$ should be smaller then $T_{pwm}/20$.

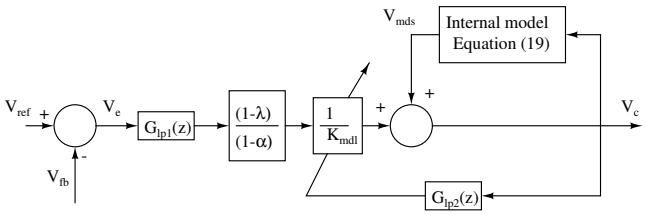


Fig. 5. Block diagram of the adaptive predictive functional control, where both $G_{lp1}(z)$ and $G_{lp2}(z)$ are digital low-pass filter. The use of $G_{lp1}(z)$ is to filter out all the high frequency noise invading to the feedback signal through the sampling process, while $G_{lp2}(z)$ is required for the gain adapting function.

IV. Simulation and Experimental Results

The proposed control algorithm of Section III is evaluated and implemented in this section. A 65W flyback converter, whose parameters are listed in Table I, is chosen as a typical example. The converter will operate in DCM, and vary its operating point whenever it sees a fluctuation in either input voltage or load current. Since the proposed controller can adapt itself to handle such variation, we need to design for one operating point only.

Let's consider the case where the input voltage $V_{in} = 150V$, the load current $I_{out} = 3A$, the switching frequency $F_{pwm} = 110kHz$, the compensation slope $M_a = 10^4 A/s$. The converter is expected to have a critically damped response and settle after 90 switching cycles, i.e. $T_r = 30T_{pwm}$. The parameters of the PFC are listed in Table II.

TABLE I. Power stage parameters for a 65W Flyback converter application

Input voltage, V_{in}	$120V$ - $373V$
Output voltage, V_{out}	$19.5V$
Load current, I_{out}	$0.01A - 3.3A$
Switching frequency, F_{pwm}	$1kHz - 120kHz$
Magnetizing inductance, L_m	$172\mu H$
Primary winding turns, N_p	26
Secondary winding turns, N_s	6
Bias winding turns, N_b	4
Output capacitor, C	$1390\mu F$
Current sense resistor, R_s	$200m\Omega$
Voltage divider gain, H_{div}	0.165
Current amplifier gain, H_{amp}	4

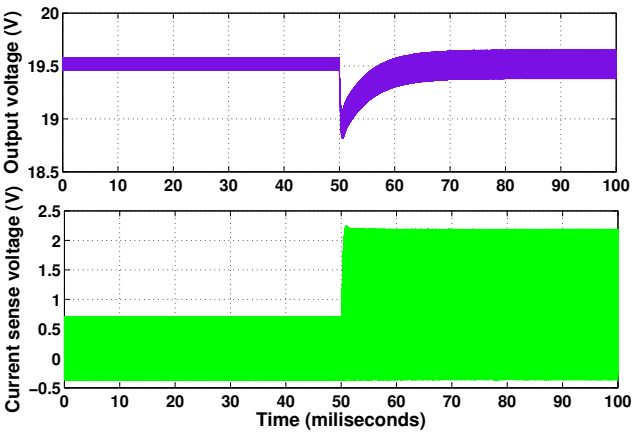
TABLE II. Adaptive PFC parameters

K_{mdl}	4.316
α	0.998
λ	0.9048
Low-pass digital filter, $G_{lp1}(z)$	$0.1515\frac{1+0.98z^{-1}}{1-0.7z^{-1}}$
Low-pass digital filter, $G_{lp2}(z)$	$0.125\frac{z^{-1}}{1-0.875z^{-1}}$

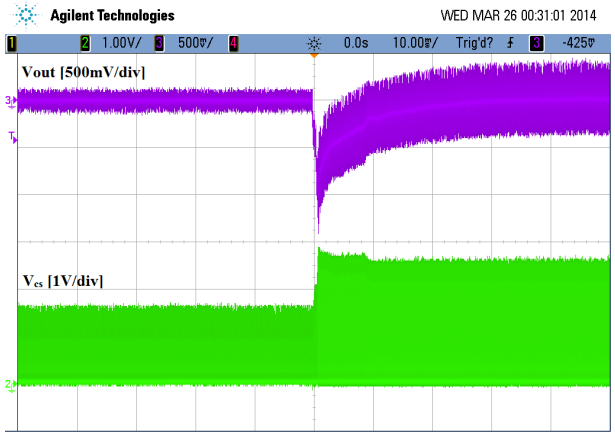
In order to evaluate the stability and performance of the obtained controller, both simulation and experiment are conducted. For simulation purposes, the switched signal model of the flyback converter and the designed controller are implemented in the MATLAB/SIMULINK environment, while the experiment is set up using a flyback power stage interfaced with a TI C2000 micro-controller (F28069 Piccolo ControlSTICK) and an external gate drive circuit. The proposed control structure in Fig.1 is implemented entirely in C2000, and minimizes the external auxiliary hardware.

A standard step-load test from 5% to 95% of the maximum load is applied in the tests. The converter transient response over different working conditions from both simulation and experiment are captured and plotted in Fig. 6 where the load is stepped from $0.165A$ to $3.15A$, and in Fig. 7, where the load is stepped from $3.15A$ to $0.165A$. As can be seen from Fig. 6 and 7, the simulation results are consistent with the experimental ones and can accurately predict the behaviour of the closed-loop system under different loading conditions. The only inconsistency can be found is between the amplitude of the simulation and experiment current sense voltage. This discrepancy is due to the presence of the spike in the experiment inductor current waveform which is typically ignored in the modelling process. Figure 6 and 7 shows that the proposed controller offers a fast recovery time and specifically a critically-damped closed-loop response as expected.

Future work will focus on designing a simple but robust control for a flyback converter in both continuous and discontinuous conduction mode as well as improving the performance of the control structure to maximize the efficiency at very light load or no load.

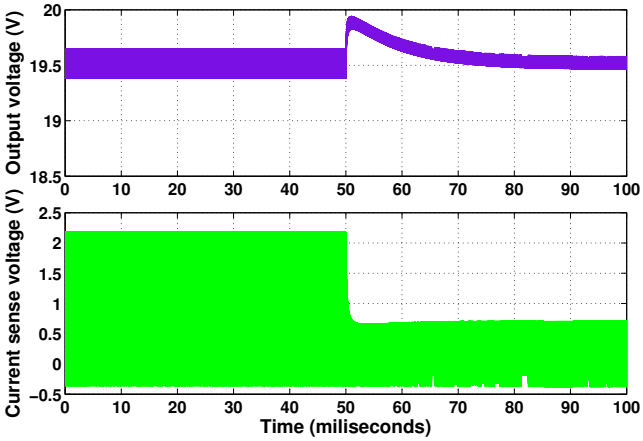


(a) Simulation results: V_{out} = upper curve, V_{cs} = lower curve

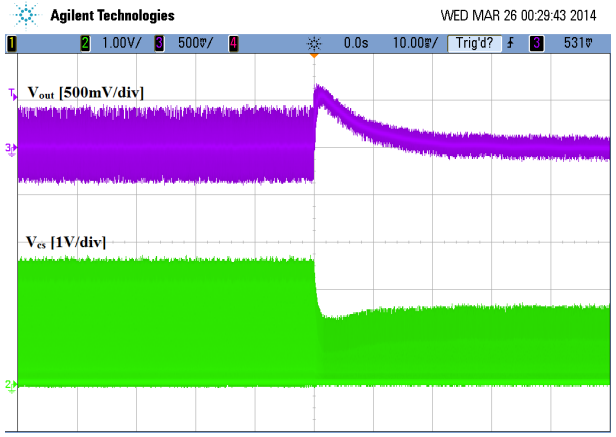


(b) Experimental results: V_{out} = Ch3 [500mV/div], V_{cs} = Ch2 [1V/div]

Fig. 6. Simulation and experimental results of the converter output voltage and inductor current (through current sense voltage) in response to a $0.165A$ to $3.15A$ step load with $V_{in} = 150V$



(a) Simulation results: V_{out} = upper curve, V_{cs} = lower curve



(b) Experimental results: V_{out} = Ch3 [500mV/div], V_{cs} = Ch2 [1V/div]

Fig. 7. Simulation and experimental results of the converter output voltage and inductor current (through current sense voltage) in response to a $3.15A$ to $0.165A$ step load with $V_{in} = 150V$

V. Conclusion

In this paper, we investigate the impact of a variable sampling frequency on the dynamic of a fixed-parameter digital compensator. A new simple representation of the converter model, which is suitable for controller design, is also derived. Based on this, we proposed an adaptive predictive functional controller for a wide operating range flyback converter. Compared to other techniques, the approach is simpler and can be implemented with a low-performance micro-controller.

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