

# N-way Digitally Driven Doherty Power Amplifier Design and Analysis for Ku band Applications

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**Abstract**—With an increasing interest in backwards compatibility for existing satellites and the emerging satellite markets, wireless transceivers at Ku band are increasing in popularity. This paper presents the design of a four-way digitally driven Doherty amplifier, aimed at applications in Ku-band. Single tone measurements indicate a maximum drain efficiency of 53.4% at a maximum of 19.2 dBm output power. The final output power can readily be adjusted by changing the biasing in each stage accordingly. The N-way Doherty power amplifier was tested with an 800 MHz bandwidth, 64 QAM test signal aimed for future communication signal standards. An analysis of this configuration has also been performed for 2-way, 3-way and 4-way architectures.

**Keywords**—N-way Doherty, Ku band, Digitally driven Doherty

## I. INTRODUCTION

5G and high throughput satellite applications demand more efficient linear operation from the wireless system hardware well into the microwave frequency range. Ku-band frequency range plays an integral role in the provision of direct broadcast satellite and fixed satellite services. As viewer habits shift to on-demand streaming and the emergence of Low-Earth Orbit (LEO) satellite constellations for low-latency satellite internet provision, interest in Ku band hardware is set to increase. Providers of equipment will require reliable and efficient designs to minimize signal interference and power consumption. Central to any new wireless transceiver design with these requirements, is the power amplifier.

Modern communication systems require high input data rates and the capacity to handle wide bandwidth complex envelope modulated signals. The evolution through symmetrical, asymmetrical, and mostly to Digital Doherty has yielded steady improvements to power amplifier efficiency. These improvements are linked to changes in the input signal characteristics to realize better power amplifiers for specific applications in Ku band are a potential next target for this trend to provide a power amplifier architecture with high efficiency for wideband complex input signal.

Reference [8] has performed an extensive research on a variety of Doherty power amplifiers (DPA) architectures that were introduced since the original idea of a Doherty amplifier was invented by William H Doherty in 1936. [10] This analysis includes Multistage, N-way and dual Doherty power amplifiers digitally driven dual input Doherty architecture, etc. Reference [2] discuss the use of 3-way digitally driven amplifiers and its advantage in achieving greater performance over a wide bandwidth. Reference [21] describes 3-way Doherty as an integrated structure in a die assembly. Reference [22] describes the use of a multi-way Doherty power amplifier as a combination of a two-way amplifier individual paths integrated in a semiconductor device. Based on conventional methods and on recent developments described above that contributes to the state-of-the art in Doherty PA's, a derivation of a novel digitally assisted four-way Doherty design is presented for the use in wideband applications in Ku-band.[2],[3],[4],[6],[8],[9],[10],[11],[13],[14],[15],[18],[19],[21],[22],[23].

The remainder of the paper is arranged as follows: In section II the device used for this work is introduced. Section III highlights the design and analysis of the DPA structure. Section IV presents results and discussions, proving the concept with the addition of possible improvements that can be performed in the future. Proceeded by conclusions in section V.

## II. DEVICE SELECTION

In designing a suitable DPA, the first and foremost challenge lies in selecting a suitable device and a device model for simulation if they are available. Specifications for required output power, the level of acceptable efficiency to mechanical size of a possible test fixture, and thermal handling capabilities etc must be considered. A suitable device for the chosen Ku band application chosen has a spice model based on pseudomorphic Hetero-Junction FET and is the NE3210S01 from NEC. Although this device is aimed at receiver applications considering operating conditions such as frequency-band of operation, etc, availability of suitable models for other devices it was deemed sufficient to perform a first stage power

amplification. Therefore, in-terms of traditional power amplifier classified terms such as efficiency figures and output power capability, the measured test results are observed to achieve near maximum intended levels of the device itself.

### III. DESIGN AND TEST OF POWER AMPLIFIER

#### A. Symmetrical Doherty Power amplifier

As the first step to an N-way Doherty design a simple symmetrical Doherty power amplifier was built and tested under single-tone test conditions. The main steps involved in this procedure of the design include, validating the spice model with NEC HEMT device data-sheet values, determining the correct biasing level for the device, investigation of stability (K and Mu) [16], [17] and choosing a suitable summing node impedance value. Secondly, load and source pull simulations are performed to design input and output matching networks and then obtain offset lines for proper Doherty operation. Finally, an impedance inverter, on the output of the DPA carrier path is set such that the output impedance seen by the carrier amplifier node is transformed to the desired load impedance in a low power region. The complete architecture of the dual input DPA is shown in Fig. 1.

$$Z_0 = \sqrt{Z_{in} \cdot Z_L} \quad (1)$$

$$Z_{in} = \frac{(Z_0)^2}{Z_L} \quad (2)$$

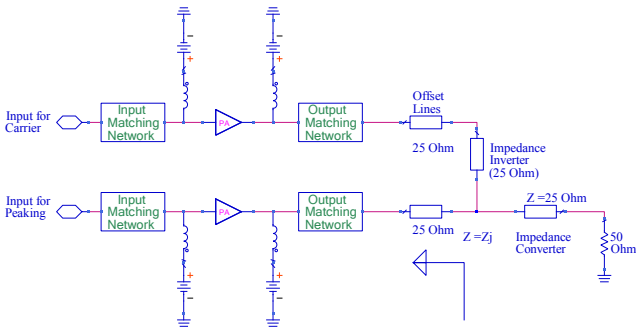


Fig. 1. Organization of a dual input Doherty PA

The summing junction impedance is set by (2) above, as it is a quarterwave transmission line. Following equation (2) if a characteristic impedance of 25 Ohms has been chosen, since,  $Z_L = 50 \text{ Ohm}$ , then  $Z_{in} = 12.5 \text{ Ohm}$ . According to load modulation principles two parallel paths carrying the same amount of current will yield  $Z_j = 25 \text{ Ohm}$ , thus allowing an ideally perfect match at the summing junction. [5], [7], [8],[12], [19]

#### B. Derivation of multi-level parameters for the specified architecture

For simplicity the same network of the peaking amplifier is then advanced into providing three and four parallel paths as additional peaking amplifiers. Considering the current characteristic impedance used (25 Ohm), based on load modulation for all three paths the summing junction is expected

to be at an impedance of 8.33 Ohms. Using equation (1)  $Z_0 = 20.412 \text{ Ohm}$ . Accordingly, four-way summing node junction impedance would be 6.25 Ohms. Again, by equation (1) it can be deduced that the characteristic impedance of the impedance converter should be  $Z_0 = 17.678 \text{ Ohm}$ . These calculations can be further verified by performing a ‘‘Harmonic Balance’’ analysis of an impedance sweep. In this work this task was carried out using Keysights Advanced Design System software, and a plot of this is shown in Fig. 2. Appropriate calculations, then need to be made in-order to find the peak performance in comparison to the swept impedance of the impedance converter.

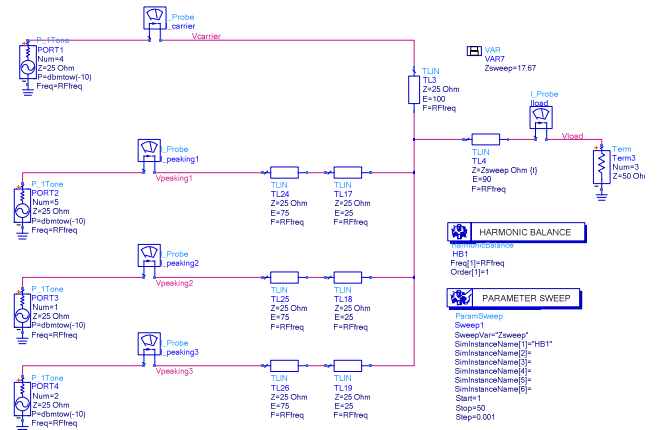


Fig. 2. Test setup used to test and compare the derived characteristic impedance value of the impedance converter.

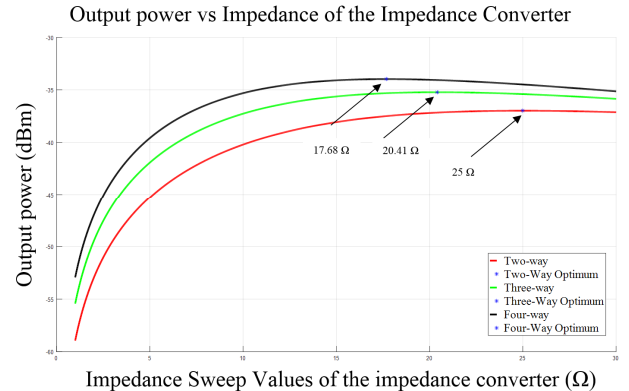


Fig. 3. Impedance sweep performed to check the calculated impedances of the impedance converter at maximum output power that was delivered.

Plotting the swept impedance values against the resulting output power, as shown in Fig. 3, allows confirmation of the optimum impedance converter value that will yield the maximum output power. This value can then be checked for agreement with the values derived for the multi-way Doherty impedance converter. Furthermore, by observing the nodes before and after the summing junction and impedance inverter, it is possible to deduce the quality of the design of the Doherty combiner as the waveforms should add constructively and present a higher value in Voltage or in Current after the impedance inverter.

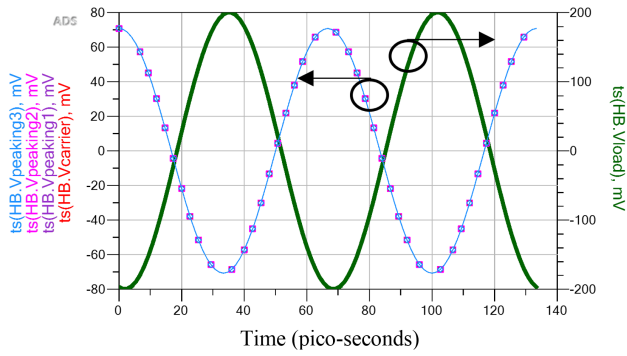


Fig. 4. Voltage levels of nodes of DPA carrier and peaking sections separately (left-hand side scale) and resulting constructive summation at the load after the impedance converter (right-hand side scale).

The resulting waveforms for the current design are presented in Fig. 4. It is possible to observe from Fig. 4 where,  $V_{load}$  plotted on the right Y-axis is the result of the constructive summation of all signals that appears after the impedance converter. All input signals to the impedance converter are in-phase before the summing node ( $Z_j$ ) and are plotted on the left Y-axis. Input and output waveforms to the impedance converter are also 90 degrees phase offset since the impedance converter is also a quarter-wave transmission line.

### C. Single tone dual input test-setup

Under Class AB and Class C normal operating conditions for the chosen device achievable DC to RF conversion efficiency lies in-between 30 to 42% (based on bias point simulations). Therefore, the maximum achievable power added efficiency level is below 42% for the device alone. Therefore, for the fully designed power amplifier expected to have a power added efficiency (PAE) level of 30 to 50% for a single tone depending on the drive level. Next, the symmetrical analogue DPA is modified to operate at separate input conditions, thus allowing two input signals feeds, for testing the dual input DPA as a system for its output power, efficiency, and input drive conditions.

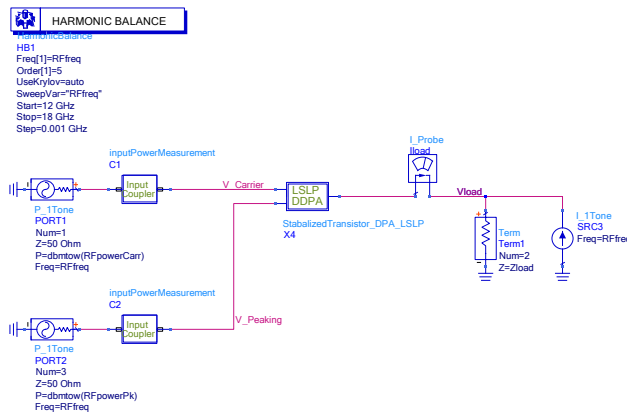


Fig. 5. Single tone test setup for dual input Doherty power amplifier

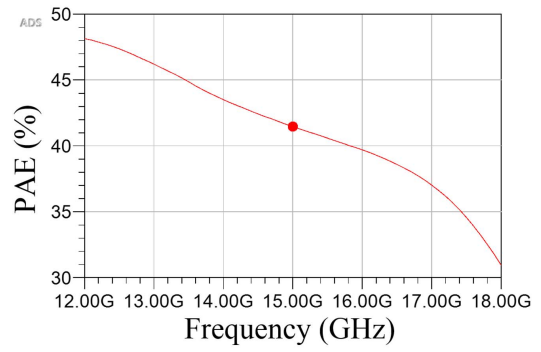


Fig. 6. PAE vs Frequency sweep plot for the single tone dual input DPA test-setup

Equations for PAE and output power for the dual input DPA were derived from the fundamentals of circuit theory. The DPA is also tested for its frequency sweep performance in Fig. 6, demonstrating an acceptable performance over the entire Ku band. The test setup Fig. 5 yielded an output power level of 15.0 dBm at a maximum drain efficiency of 52 % for peaking amplifier with gate bias level of -1.45 V. At a different bias level of -0.95 V output power can be elevated to 16.10 dBm which indicated a maximum drain efficiency of 53.4 % and PAE of 41 % at 15 GHz (Fig. 7). The cost of the increase in efficiency results in a reduction in transducer power gain since the linearity of the two devices is compromised as the PAs are driven into their saturation levels. Based on the requirements the designer can adjust the biasing levels of the peaking amplifier to meet the specifications. If the test setup is a hardware testbench, then the relevant drain current value can be observed to tune, the performance meet the criteria.

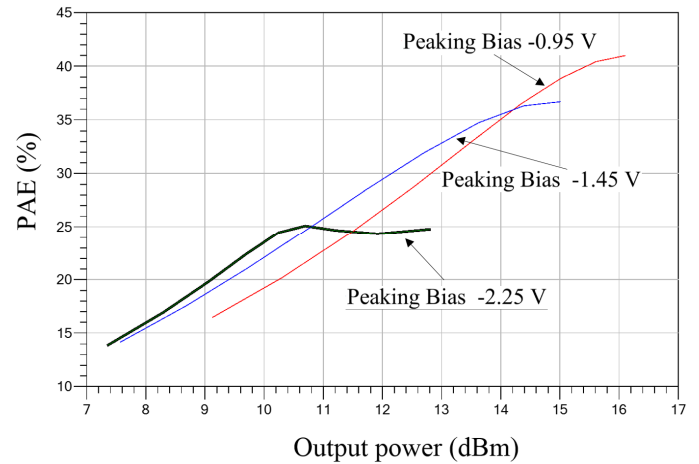


Fig. 7. Plot of Power Added Efficiency vs delivered output power of the DPA in dBm at different class C biasing levels of gate terminal of the peaking amplifier 2-way Doherty configuration under single tone test conditions.

To understand the maximum input power that corresponds to better performance the same setup was used. As seen from Fig. 5 the carrier and peaking power amplifiers were assigned specific input power levels in dBm. These were swept in a "Harmonic Balance" simulation and the results were tabulated to calculate the best input power level on both-paths that yields the best efficiency and output power at the output. As observed

by Fig. 8 and Fig. 9 maximum PAE is achieved at an input power level for single tone simulations are at 5 dBm for both branches.

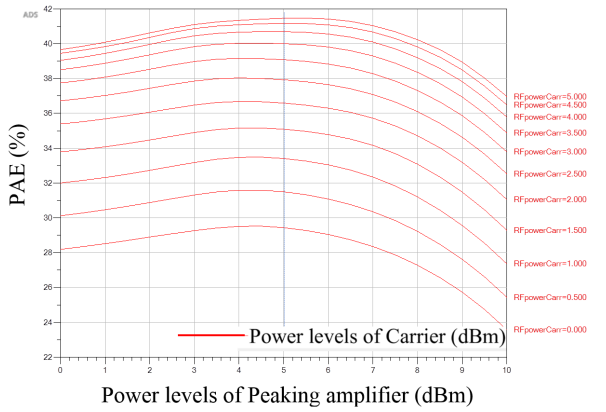


Fig. 8. PAE calculated according to the swept input power levels of carrier and peaking amplifiers under single tone operating conditions.

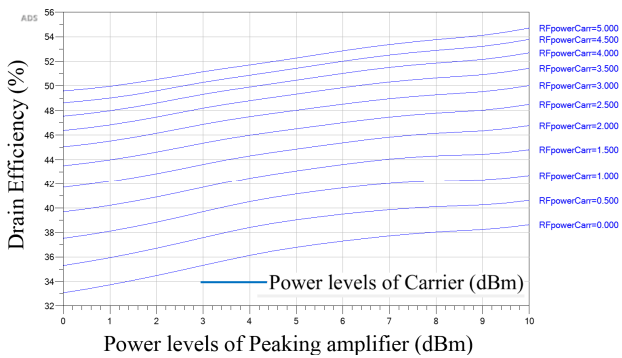


Fig. 9. Drain efficiency calculated according to the swept input power levels of carrier and peaking amplifiers under single tone operating conditions.

#### D. Modulated signal input simulations

As highlighted above the concept is then extended to a four-way design using the calculated impedance converter characteristic value and the corresponding summing junction impedance value. The values for signal tone input power levels offers a starting point for the input power level that needs to be set for the driver amplifier gain for modulated signal input simulations. However, these values can later be adjusted according to the needs of the application, e.g. maximum output power, linearity requirements etc.

Modulated tests include a 64 QAM input signal sampled at 2 GHz with a symbol rate of 800 MHz at a raised cosine roll-off factor of 0.25, with a total number of 8192 points and with 6144 of number of bits. Above settings were chosen to test the performance of the device accurately and to have a reduced simulation time with lesser number of data points. This signal is chosen to observe the response of the four-way DPA to the multiple level of amplitudes at a wide-bandwidth.

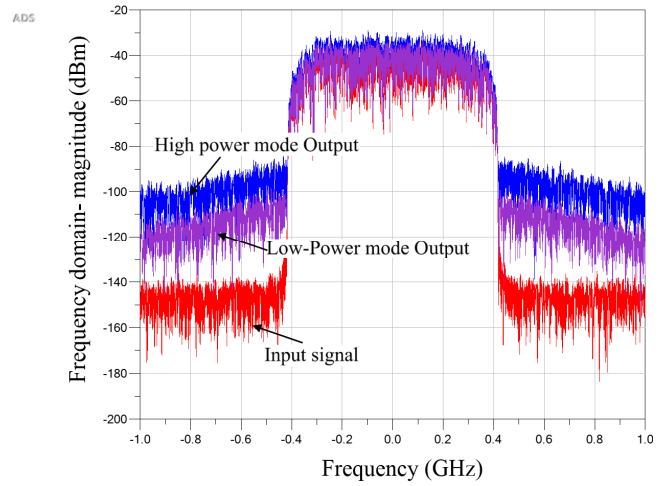


Fig. 10. Magnitude spectrum at the output of the 4-way digitally driven PA for a 64 QAM input.

According to results indicated by Fig. 10 the initial capture at lower input power level of the output signal in its frequency domain magnitude spectrum indicates a level of  $\sim 70$  dB in dynamic range. Confirming the validity of the linear performance of the class AB carrier amplifier. At the high power mode, both carrier and peaking power amplifiers are expected to be in operation together. As anticipated a rise in noise floor can be observed for higher power level input, as nonlinear class C operation C stages will be in-effect. Approximately 60 dB of dynamic range was obtained in high power operation mode. According to [20] the current design meets the spectral mask requirement of a -35dBc dynamic range for the Digital Video Broadcasting (DVB - S2) standard.

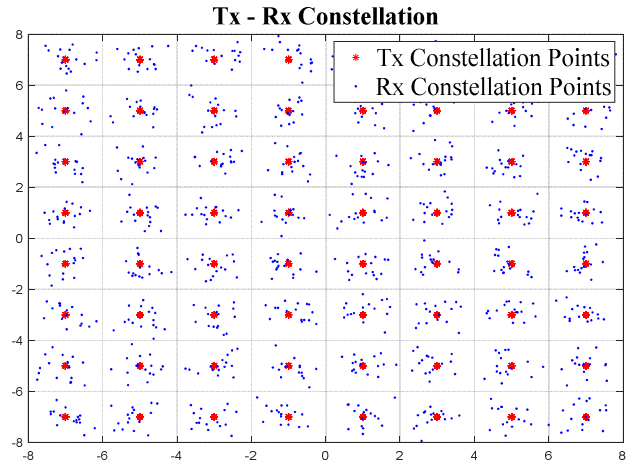


Fig. 11. Transmitted (Tx) and Received (Rx) constellation data points for 64 QAM input signal captured at the PA output.

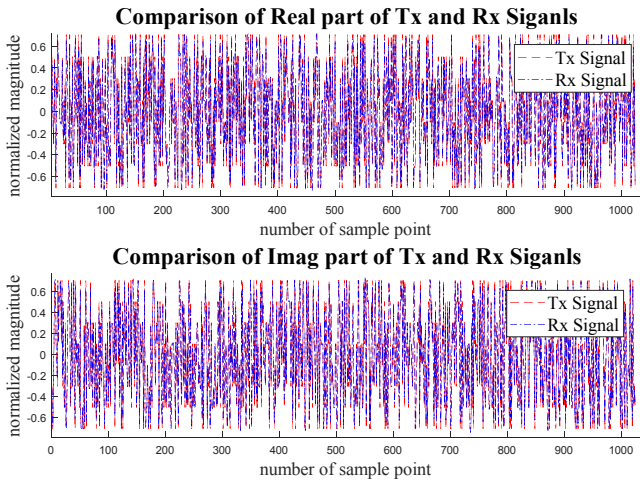


Fig. 12. Comparison of Transmitted (Tx) and Received signals' for the 64 QAM input signal (Rx) real and imaginary parts.

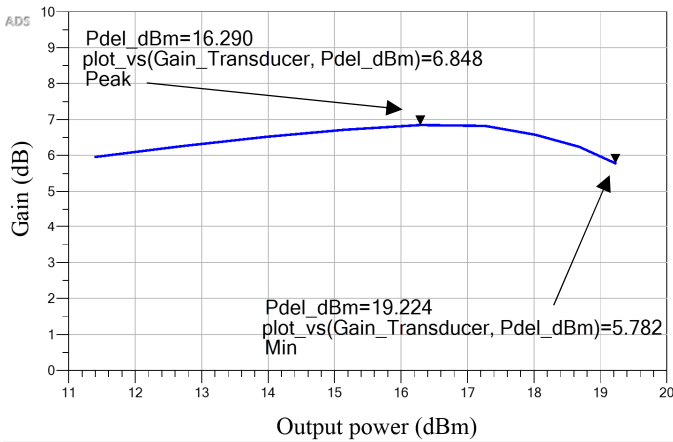


Fig. 13. Power sweep performed on the 4-way Doherty amplifier indicating a flat gain response with in 1.1 dB of deviation.

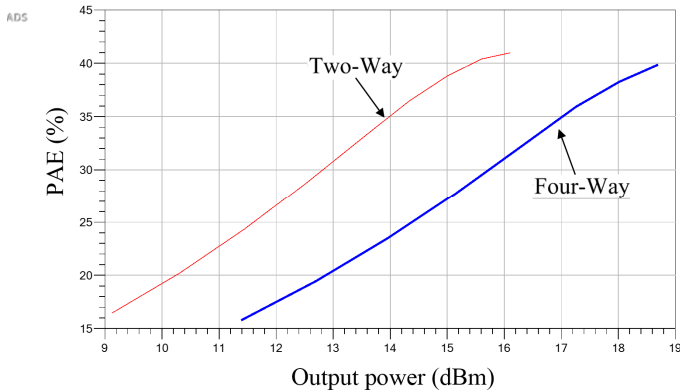


Fig. 14. Comparison PAE with relation to output power of Two-way and Four-way digitally driven Doherty amplifiers under single tone input conditions.

#### IV. DISCUSSION

Comparing Fig. 7 and Fig. 14 similar to the two-way design it is possible to trade-off between the characteristics of the DPA

by performing final modifications on the peaking amplifier bias level. E.g. favor efficiency over output power. It is also possible to have different bias levels for each of the different of individual peaking amplifier branches to facilitate signals with higher peak to average ratio. For the proposed design, plot of gain against power sweep results in a flat response with a maximum deviation of 1.1 dB. Fig. 14 portrays a comparison of two-way and four-way designs with respect to their individual PAE performance calculated for power sweep. As seen by Fig. 14 for an application that requires more output power and efficiency having higher order of amplifiers offers better performance. Fig. 11 shows the transmitted and received constellation diagram, which indicates an acceptable movement of the received constellation around the intended location with relative to the input signal constellation. Furthermore, in Fig. 11, Fig. 12 depicts the overlapping of real and imaginary parts of the transmitted and received signal. These are also in good agreement with one another. Notably in the current design, during low power drive the carrier amplifier is presented with an output impedance of 6.25 Ohms, which then translates into 100 Ohms after the impedance inverter function. This implies that the carrier amplifier undergoes an impedance transformation of ratio 1:4 under the current design criteria. However, for the purpose of considering traditional 1:2 impedance transformation ratio it is possible to anticipate a reduction in linearity. [1], [8] This issue can be addressed by having two identical carrier amplifiers and two identical peaking stages designed by performing the calculations mentioned in the current design.

#### V. CONCLUSIONS

A design to implement an N-way Doherty power amplifier for Ku band applications has been presented in this work. The performance of the N-way design was extensively tested using unmodulated single-tone and a 64 QAM signal with 800 MHz bandwidth. With the emergence of low-earth orbit satellite constellations where a large power output is not a requirement, the presented design provides a viable option for ground station transmission as shown by its performance within spectral mask limits for satellites communications.

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