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Research Article

Software-Defined Radio Demonstrators: An Example and Future Trends

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Software-defined radio requires the combination of software-based signal processing and the enabling hardware components. In this paper, we present an overview of the criteria for such platforms and the current state of development and future trends in this area. This paper will also provide details of a high-performance flexible radio platform called the maynooth adaptable radio system (MARS) that was developed to explore the use of software-defined radio concepts in the provision of infrastructure elements in a telecommunications application, such as mobile phone basestations or multimedia broadcasters.

1. Introduction

In recent years the technologies required to implement the concept of software-defined radio (SDR) have matured, and the SDR Forum presents a tier-based taxonomy for the capabilities of various SDR systems [1]. Systems are now appearing that offer flexibility and adaptability to system developers—providing advantages when addressing the issues of constrained spectrum resources, increasingly rapid changes in wireless standards, and cost-effectively developing products for niche markets [2, 3]. As the required technologies have matured, we are now seeing SDR implementations delivering wide bandwidth applications with a high quality of service, for example, in mobile data communications such as WiMAX-e. In the future it can be imagined that SDR architectures will be increasingly used to deliver telecommunication services such as mobile telephony, digital TV and radio broadcasts and heterogeneous combinations such as streaming video in the mobile environment.

As spectrum is a finite-shared resource that is increasingly congested with existing users, obtaining access to spectrum for the delivery of new services is increasingly difficult. Frequency agile SDR systems offer a solution where the flexible SDR radio can avail of an unused slice of spectrum, temporarily, to deliver the service. Originally this concept met strong resistance from existing spectrum holders and the regulators, however, recently there has been increasing interest from the regulators (who can allow greater diversity of services) and from spectrum holders (who can utilize their spectrum more profitably). One initiative that supports this trend is the developing discussions in Europe on "Wireless Access Platforms for Electronic Communications Services (WAPECS)" where it is proposed that some services may opportunistically use spectrum, if available, in regional and temporal bases [4]. Though at an early stage, these initiatives suggest new opportunities for telecommunication services.

In this paper we will present an overview of the challenges in designing an SDR platform that can be used for research or deployment. We will discuss the issues that need to be addressed and the current state-of-the art in software-defined radio demonstrators. This will then be followed by a detailed description of the maynooth adaptable radio system (MARS), its design criteria, architecture, and some use cases. Finally the paper will be concluded with some comments on the future direction of experimental SDR platforms.

2. Design Criteria for SDR Platforms

Software-defined radio platforms are integrated systems of software and hardware that enable SDR applications to be

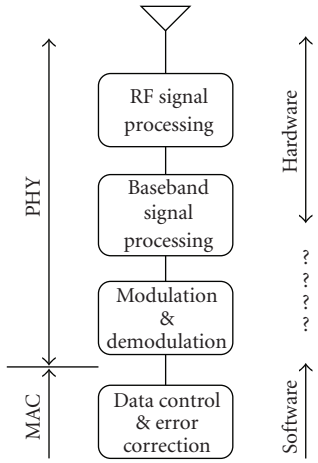

Figure 1: Partitioning between software and hardware in an SDR system.

developed and evaluated. Of the two, the software aspects are relatively more mature, and current work in this area focuses on performance enhancement and cognitive radio techniques. The hardware aspects of a platform consist of the radio-frequency (RF) elements, some baseband signal processing and communications link to the software-based signal processing element—perhaps a DSP, FPGA, or a general purpose processor (GPP). One aspect of the software-defined radio concept is that flexibility can be delivered through software. An often overlooked corollary is that the hardware performance to support that flexibility is more challenging than for a single-mode implementation, and optimal solutions remain elusive [5]. This section will comment on some of these issues and how they impact on the hardware architecture of software radio platform.

2.1. Partitioning of Resources. The software-defined radio philosophy represents a trend in electronic devices from transistors to software. This has been facilitated by the rapid increase in software capabilities and processing power. In software-defined radio the argument is to implement as much of the radio as possible in software and to control the remaining hardware features. However, the choice of where the partition between hardware and software has a fundamental impact on the design of any SDR platform [6, 7].

One desirable partitioning of functionality is to take all signal processing into the software domain and that only I- and Q-sampled data is passed into the hardware domain. In this scenario the hardware element of the system need undertakes no signal processing. This places a severe performance requirement upon the software processing element, particularly where bandwidths in excess of 1 MHz need to be supported. Alternatively some of the software processing load may be allocated to customized hardware (often in the form of an embedded FPGA or a specialist DSP device). In this scenario the load is shared but FPGAs are expensive and arguably offer less flexibility. One of the important issues to consider when choosing the partitioning is the data communications protocol between the different elements. For unprocessed IQ signals, for every 1 MHz of spectrum, that is, being supported a data link capacity of 40 Mbps is required, assuming 16 bit samples and 8 b/10 b encoding. This is doubled for duplex transceivers. This severely limits the bandwidth capabilities of platforms that are required to connect to standard interfaces on general purpose computers. More complex, higher performance links are possible that will allow greater bandwidths to be supported, for example, Gigabit Ethernet or PCIexpress. Alternatively if on-board processors are included, some local processing could greatly minimize the data throughput requirements.

2.2. Frequency Flexibility. Software-defined radios come in two varieties—those that are modulation scheme (or waveform) flexible within a specific frequency range, or those that are waveform and frequency agile. Implementations of the former are more common as it does not require any significant modification to traditional hardware. Modern mobile wireless systems (UMTS, IEEE 802.16) are often implemented in this manner. Frequency agility offers many more benefits such as flexible use of spectrum or dynamic adaptation to different wireless networks. Frequency flexibility places several severe constraints on the design of the supporting radio frontend (RFE).

(i) Programmable carrier frequency generation.

(ii) Antenna, filter, and passive network designs.

Frequency selection requires the ability to generate a carrier frequency within the required range. This is normally achieved through the use of a local oscillator. The local oscillator can be generated in many different ways depending on the degree of flexibility and phase noise performance required [8]. These two criteria tend to be inversely related, however there is continual improvement in this area and with careful design; performance and flexibility can be achieved.

Frequency agility places more severe constraints on the design of the passive elements within a radio: the antenna; filters; matching networks. Normally a radio is designed with a narrowband or multiband perspective—multiband is where a finite set of narrowband signals are used. In this scenario filters can be designed to select the band of interest and minimize the effect of other potentially interfering signals or noise. Similarly antennas and matching networks for the low-noise amplifiers and power amplifiers are optimized for maximum gain in the band of frequencies of interest. Where multiband systems are required, the common approach is to switch between the appropriate narrowband solution. Providing flexibility over a wider band means that traditional filter solutions cannot be used and to date useful programmable flexible filters do not exist. Wideband antennas and matching networks can be designed but they are suboptimal. This implies a reduction in efficiency depending on the degree of flexibility required. The lack of frequency selectivity has a significant impact on

the issue of interference, energy efficiency, and sensitivity of the final design.

2.3. Interference Management. Frequency flexible radio receivers cannot have the same band select filtering as traditional radios and are vulnerable to interference, both from external sources and self-generated phase-noise from a local transmitter. Considering the external sources first, a wideband radio receiver covering any of the communications ranges (e.g., 700–950 MHz or 1800–2500 MHz) will be exposed to legitimate transmissions from a variety of sources—mobile phone transmissions, WiFi, television. To implement a standards compliant radio receiver, it is necessary to be able to function in the presence of other transmissions to the required level of sensitivity. For example, in GSM, you must be able to receive a −98 dBm signal in the presence of a 0 dBm blocker. Requirements such as these have significant impacts on the design of your RF receivers. In a radio receiver it can be shown that reduced filter performance can be achieved at the expense of increased analog-to-digital conversion sensitivity. In the absence of filtering, it can be shown that at least 14 bits of dynamic range are required for an acceptable bit-error rate, and 16 bits would be desirable. Achieving 16 bits analog-to-digital conversion for bandwidths greater than 10 MHz is difficult and expensive in terms of power and cost. SDR platforms must decide whether they attempt to be standard compliant or best effort. For ease of implementation, most platforms ignore the interference issue, and the user selects a frequency range with minimal interference.

The second issue of self-generated interface is more challenging. Modern transmitters are good at controlling phase noise and spurious out-of-band components and, in many scenarios, the receive and transmit bands are sufficiently distant to enable robust filtering. This is important as there can be over 120 dB difference in power levels in a mobile phone handset or 150 dB for a GSM basestation. In the absence of such filtering, transmitter phase noise can leak into the receive path and swamp any received signal. This is problematic as the transmitter and receiver are coincident and thus unlike external transmissions will not be attenuated by distance. This issue is currently without a good solution. The issue can be minimized if a TDD-communication scheme is selected.

2.4. Transmitter, Receiver or Transceivers. There are many applications where it is not necessary to implement a transceiver system. If true, then many issues are greatly simplified: improved data throughput; no concerns on self-generated noise; lower cost. Receiver-only applications are popular in the cognitive radio space and in multimedia receivers. In cognitive radio one of the main challenges is in spectrum sensing and identification of existing communication schemes. This is a receiver-only application and benefits from any reduction in self-generated noise. For broadcast applications, such as television, the operators require only transmitters and receivers for the clients. However, for most wireless communications, bidirectionality is required and a full-transceiver system will be needed.

3. Review of Existing SDR Platforms

There are a large number of experimental SDR platforms that have been developed to support individual research projects. A selection of these platforms is included in [9–21]. The various experimental SDR platforms have made different choices in how they have addressed the issues of flexibility, partitioning, and application. To highlight the variety of architectures, four popular platforms will be discussed briefly prior to introducing the maynooth adaptable radio system.

3.1. Universal Software Radio Peripheral (USRP). The USRP is one of the most popular SDR platforms currently available and it provides the hardware platform for the GNU Radio project [8, 9]. The first USRP system, released in 2004, was a USB connected to a computer with a small FPGA. The FPGA was not only used primarily for routing information but also allowed some limited signal processing. The USRP could realistically support about 3 MHz of bandwidth due primarily to the performance restrictions of the USB interface. The second generation platform was released in September 2008 and utilizes gigabit Ethernet to allow support for 25 MHz of bandwidth. The system includes a capable Xilinx Spartan3 device which allows for local processing. The radio-frequency performance of the USRP is limited and is more directed toward experimentation rather than matching any communications standard.

3.2. Kansas University Agile Radio (KUAR). The KUAR platform was designed to be a low-cost experimental platform targeted at the frequency range 5.25 to 5.85 GHz and a tunable bandwidth of 30 MHz [11]. The platform includes an embedded 1.4 GHz general purpose processor, Xilinx Virtex2 FPGA and supports gigabit Ethernet and PCI-express connections back to a host computer. This allows for all, or almost all processing, to be implemented on the platform, minimizing the host-interface communications requirements. The platform was designed to be battery powered thus allowing for untethered operation, The KUAR utilizes a modified form of the GNU Radio software framework to complete the hardware platform.

3.3. NICT SDR Platform. The Japanese National Institute of Information and Communications Technology (NICT) constructed a software-defined radio platform to trial next generation mobile networks [12]. The platform had two embedded processors, four Xilinx Virtex2 FPGA, and RF modules that could support 1.9 to 2.4 and 5.0 to 5.3 GHz. The signal processing was partitioned between the CPU and the FPGA, with the CPU taking responsibility for the higher layers. An objective of this platform was to explore selection algorithms to manage handover between existing standards. To this end, a number of commercial standards were implemented, for example, 802.11a/b/g, digital terrestrial

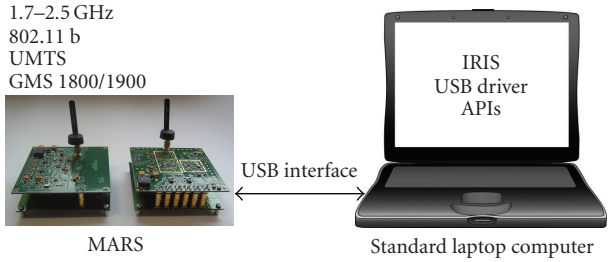

Figure 2: MARS architecture.

broadcasting (Japanese format), wCDMA, and a general OFDM communication scheme.

3.4. Berkeley Cognitive Radio Platform. This platform is based around the Berkeley emulation engine (BEE2) which is a platform that contains five high-powered Virtex2 FPGAs and can connect up to eighteen daughterboards [13]. In the Cognitive Radio Platform, radio daughterboards have been designed to support up to 25 MHz of bandwidth in an 85 MHz range in the 2.4 GHz ISM Band. The RF modules have highly sensitive receivers and to avoid self-generated noise operate either concurrently at different frequencies (FDD) or at the same frequency in a time-division manner (TDD). This cognitive radio platform requires only a low-bandwidth connection to a supporting PC as all signal processing is performed on the platform.

4. Maynooth Adaptable Radio System

The maynooth adaptable radio system (MARS) has been in development since 2004 and had the original objectives of a programmable radio front-end that was to be connected to a personal computer (PC) where all the signal processing is implemented on the computers general purpose processor (Figure 2) [14]. The platform was to endeavor to deliver a performance equivalent to that of a future mobile telephony base station and the wireless communication standards in the frequency 1700 to 2450 MHz. The software framework selected for initial development was the IRiS framework (Implementing Radio in Software) from our collaborators in Trinity College Dublin. This section will present some of the design criteria, issues encountered, our solutions, and then some results from the final implemented system.

The platform high-level objectives drive a range of technical design choices.

Future Base stations. Most 2 G base stations supported a frequency band no greater than 5 MHz, adjustable within the full GSM band. However, there is strong interest in a base station that could simultaneously support distinct and separated bands of frequencies—enabling base station sharing between operators or where operators may own different bands of frequency. This drove a specification that full-band support should be explored, 70 MHz, over an approximately 700 MHz range. Since the start of the project, wideband schemes such as wCDMA, WiMAX have become increasingly popular, and bandwidths of at least 25 MHz need to be supported.

General Purpose Computer Connected. Much of the work on software-defined and cognitive radios has been undertaken by researchers who are more familiar with general-purpose processors than with FPGA or DSP devices. All available software frameworks are PC-based and for our project we utilized the IRiS SDR framework developed by our collaborators, Trinity College Dublin [15]. Similar to the USRP, it was necessary to provide an interface with a general purpose computer in which modulated baseband data is passed between the computer and the radio platform. This can be easily identified as a performance bottleneck as one must choose a standardized interface. At the start of this project, widely used high-performance interfaces were limited. The USB 2.0 standard was selected as most suitable despite its obvious performance limitations. The platform design was designed to be modular so that this performance bottleneck could be removed when higher performance interfaces became available.

Communication Modes between 1700 and 2450 MHz. This range of frequencies is comparatively narrow but is the most congested frequency range for personal communications. As a project specification we identified the following communication modes that were to be supported:

$$\begin{matrix} \text{GSM1800} & \text{PCS1900} \\ \text{802.11 b} & \text{UMTS(wCDMA).} \end{matrix} \quad (1)$$

In addition, the Irish communications and spectrum regulator (ComREG) licensed to our university two 25 MHz bands of spectrum at 2.1 and 2.35 GHz.

4.1. Design Issues. To determine the RF system specifications it was necessary to analyze the individual parameters and spectral masks for each standard and integrate them to produce a single worst-case specification. The primary parameters of interest for the design of the platform are receiver sensitivity, receiver third-order intermodulation product (IP3), receiver noise figure (NF), transmitter power levels, and transmitter phase noise. These parameters determine the blocking performance of the receiver, the spectral and spurious masks of the transmitter, and the expected receiver bit error rate.

One of the most challenging requirements is that of capturing the minimum allowable signal in the presence of blockers. Under the assumption that strong filtering does not exist (as the system is frequency flexible), the radio system must have sufficient dynamic range for digital signal processing to extract the desired signal in the presence of blockers and interferers. Figures 3 and 4 show typical interference profiles for the GSM and wCDMA standards. The GSM standard (at all frequencies) presents the most challenging requirement as it requires successful reception of a −104 dBm signal (in the base station, −102 dBm for a GSM/GPRS handset) in the presence of a 0 dBm blocker. As

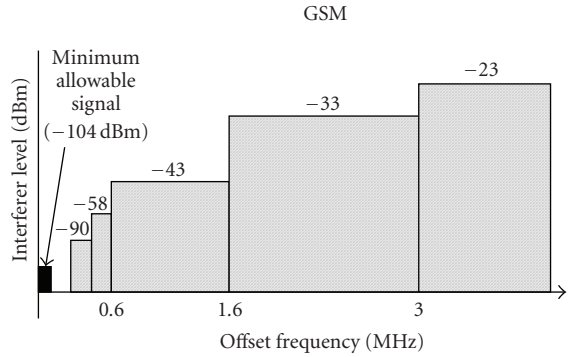

Figure 3: GSM receiver interference profile.

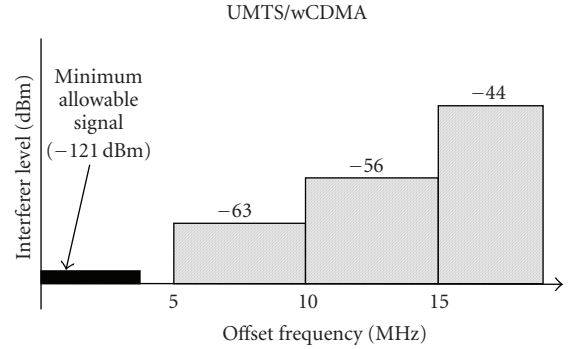

Figure 4: wCDMA receiver interference profile.

Table 1: RF specifications for various standards.

	GSM	UMTS	802.11 b
Noise figure (dB)	9	9.6[2]	9[3]
IIP2 (dBm)[1]	43	8.0	10
IIP3 (dBm)	−18	−21.0	−18

[1] IIP2 is required for zero-IF or low-IF architectures
[2] Assuming a processing gain of 25 dB
[3] Assuming a processing gain of 10.4 dB

our signal capture band is targeted at a complete communication band (e.g., the complete GSM band), blockers of that magnitude can be expected in the receive bandwidth of our platform. To capture the smallest required signal in the presence of such a blocker would suggest an analog-to-digital converter with dynamic range of over 106 dB, assuming an ideal receive signal chain. As a first-order approximation this is acceptable though a more detailed analysis shows that for a given bit-error rate, a lower dynamic range can be used [22].

The following table displays the receiver requirements for each of the communication standards. A composite specification for the receiver can be calculated by taking the most stringent requirement.

For the MARS platform, it was decided to go with a direct conversion architecture for both receiver and transmitter (Figure 5). Selecting an appropriate intermediate frequency in a frequency flexible system is difficult and thus a direct-conversion architecture allows one to avoid this issue. On the other hand, this approach places additional constraints

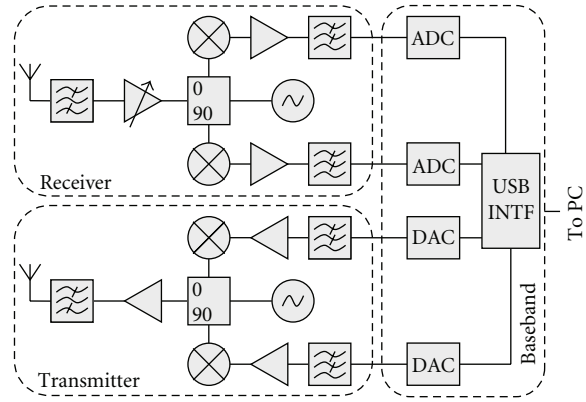

Figure 5: MARS platform architecture.

on the receiver, with signal chain performance dependent on linearity and to a large degree on IIP2 performance. In addition there have historically been issues with local-oscillator leakage resulting in dc distortion in the receiver. As most communication schemes have content at and near dc, this has been a reason to avoid direct conversion architectures in favor of low-IF or heterodyne solutions. Recently-released products have shown significant improvements and direct-conversion solutions are increasingly viable.

Given our direct-conversion architecture, the performance of the data-converters is important. We used 16 bits data converters in each direction so as to provide the necessary receive sensitivity and to minimize out-of-band transmit noise. The performance bottleneck of the overall platform is that of the USB connection which is limited to a sustained throughput of 256 Mbps. Our ideal target bandwidth of 70 MHz would require a data rate of approximately 10 Gbps—beyond the scope of any standard PC interface. In 2006, the best choice we had available was USB 2.0 which had a maximum sustained throughput of about 380 Mbps, allowing us a bandwidth of about 3 MHz (simplex) or 1.5 MHz (duplex). Modifying the sample resolutions allows us to double our throughput. It is acceptable to reduce the transmitter resolution as typically 60 dB of SNR will suffice, yielding a 25% increase in throughput. This was the fundamental performance bottleneck for our platform. There are only two solutions: place a processor or FPGA on the board or use a higher performance link. For the initial development, these options were not followed and the RF performance was throttled to match the USB interface. A modular design for the RF and baseband units was followed so that the overall platform could benefit from improvements in the data link throughput.

The following sections detail some of the components selected. In many cases it is easier to select wideband components rather than frequency agile components. With wideband components the complexity then resolves to the quality of the local oscillator, the data converters, and the passive structures (filters and matching networks). Local oscillators are a mature technology and phase-lock-loops (PLLs) are excellent at delivery agility and low noise. The

passive structures remain the most difficult and this issue is addressed by keeping any filters as relaxed as possible.

4.2. Receiver. In a direct-conversion receiver architecture, there is a direct tradeoff between RF band select filtering and the performance requirements of the analog-to-digital converter (ADC). In the absence of strong filters, the ADC must have sufficient resolution to support the dynamic range required to separate interferers from weak signals. An ADC with a signal bandwidth of 70 MHz and 106 dB (in excess of 17 bits) resolution is highly challenging but devices available at the time of development were capable of delivering 16 bit performance at high speeds though with high power consumption. We selected a family of pin-compatible ADCs from Linear Technologies, Calif, USA that can deliver up to 105 MSps (LTC220* family). This will enable lower performance ADCs to be used seamlessly where the baseband signal processing cannot support higher speeds.

The RF low-noise amplifier selected was the Freescale MBC13720. This part is a low-noise amplifier with bypass switch. It generates a gain of 12 dB and noise figure of 1.55 dB at a frequency of 2.4 GHz. The LNA is able to operate in a frequency range from 400 MHz to 2.4 GHz. It features two enable pins to control the amplification stage which are software-controlled. The gain at this stage had limited programmability. For noise-mitigation maximizing early-stage gain is the preferred option, with greater gain control available at the baseband stage.

The performance of the demodulator is important in a direct-conversion architecture. The AD8347 device, from Analog Devices was chosen. It is a direct quadrature demodulator with RF and baseband automatic gain control (AGC) amplifiers. Its noise figure (NF) is 11 dB at maximum gain and it provides excellent quadrature phase accuracy of 1° and I/Q amplitude balance of 0.3 dB. This high accuracy is achieved by the polyphase filters employed by the local oscillator quadrature phase splitter. The dc offset problem is minimized by an internal feedback loop. Any remaining dc-offset effects could be corrected by digital correction but this was not implemented in the current prototypes.

In a frequency flexible system an agile local oscillator is required. Often a clock-data recovery circuit would be used to lock onto the transmission frequency, however in an SDR architecture a band of frequencies are captured and clock-recovery is undertaken digitally. The primary criteria for the local oscillator, in an SDR RF front-end, are agility and low-phase noise. We selected a low-power delta-sigma Fractional-N PLL from national semiconductor (LMX2470) with the MiniCircuit VCO ROS-2500. The sigma-delta modulated fractional-N divider has been designed to drive close-in spur and phase noise energy to higher frequencies. The modulator order is programmable up to fourth order, permitting us to alter the phase noise characteristics at different frequency offsets. The device can operate in the range 500–2600 MHz with a phase noise of −200 dBc/Hz. It is optimally operated in a smaller range but this can be adjusted by changing the local oscillator frequency.

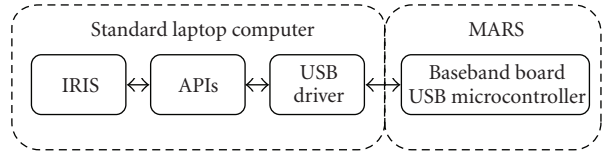

Figure 6: Computer to MARS transceiver interface.

4.3. Transmitter. The three main components in a direct conversion transmitter are the power amplifier, modulator, and the digital-to-analog converter (DAC).

The modulator chosen is the analog devices AD8349. It is a quadrature modulator that is able to operate with an output frequency range from 700 MHz to 2700 MHz. It features a modulation bandwidth from dc to 160 MHz and a noise floor of −156 dBm/Hz. Dual different IQ inputs are provided from the DAC and to improve the noise performance the local oscillator (LO) drive. The output power generated by the modulator is within the range of −2 to +5.1 dBm.

The power amplifier is constructed as a two-stage element: a fixed gain power amplifier and a digitally controlled variable gain amplifier. The power amplifier used is the MGA-83563 from (Avago, Calif, USA) which is a broadband high linearity amplifier. It works in the frequency range of 40 to 3600 MHz and achieves a small signal gain of 20 dB with a noise figure of 4.1 dB. This variable gain amplifier is the Analog Devices ADL5330 which operates from 10 MHz to 3 GHz frequencies, with a gain control range of 60 dB. The combined system can deliver 22 dBm of power in 256 programmable steps.

Digital-to-analog converters are more capable than ADCs for any given technology. For this application it was possible to get a dual-path 16-bit DAC from Maxim (MAX5875) that can support output rates of up to 200 MSps. It features an integrated +1.2 V bandgap reference and control amplifier to ensure high accuracy and low-noise performance. The output rate is adjustable based on the provided clock frequency.

4.4. USB Communications. As this is a nonstandard USB application, a customized USB driver and firmware were developed to maximize throughput and deliver sustained performance. As stated, the maximum throughput of the USB link was performance limiting factor in the platform. Even though USB offers 480 Mbps, in practice sustained performance is substantially less. Sustained performance is necessary as gaps in the data flow are unacceptable and excessive buffering will introduce latency effects. A specialist Linux driver was written to ensure suitable performance, and an efficient API library was implemented to provide a robust interface with third party software engines. Figure 4 shows a high-level vision of the interconnection between the elements of the integrated radio platform.

The USB connect was provided through a USB 2.0 Cypress EZ-USB device with an on-board 8051-compatible microcontroller (Figure 6). The function of the microcontroller was to route the data between the general purpose

interface (GPIF) of the USB device and the data converters. Through the use of USB endpoints, it was also possible to implement a control channel for reconfiguring the system. This control plane can be accessed during operation; but to maximize data throughput, it is recommended that it be only used between communication sessions.

The main software elements of our platform were some embedded code running on the USB microcontroller, an optimized Linux USB driver and an API library providing an interface with IRIS. Linux was selected due to its superior real-time performance and access to low-level device drivers. The principal challenges were first to provide high-speed and continuous data transfer without data loss and second to enable the reconfigurability of the hardware devices. High-speed data transfer without data loss was achieved by using optimized techniques in both USB driver and embedded code. Due to their ability to be queued, the USB driver utilizes USB request blocks (URBs) as the data structure for transmitting or receiving information [23, 24]. This queue of URBs guarantees that there will be always information waiting to be processed in the communication channel, which causes maximum usage of bandwidth and a continuous stream of information. Using the bulk transfer communication mode guaranteed delivery of data, solving the data loss problem. With this optimized driver, it was possible to achieve a maximum sustained throughput of 256 Mbps, an improvement over other driver implementations but substantially less than the 480 Mbps peak transport. Finally hardware reconfiguration is obtained through API functions, for example, for configuring the sampling rate, the local oscillator frequency, and the receive chain gain control.

4.5. Software Radio Framework. The software radio framework utilized in our system is the IRIS software radio framework. IRIS has been under development at Trinity College Dublin since 1999. It is a highly flexible and highly reconfigurable software radio platform for a general purpose processor running either Windows or Linux.

The IRIS architecture is illustrated in Figure 7 and comprises of DSP components which are configurable through an XML file. Examples for such components are modulators, framers, or filters. Each of the components has a set of parameters and an interface to the control logic, which allow for reuse in different radio configurations. The control logic is a software component designed for a specific radio configuration, that is, it is aware of the full radio chain while the processing components are not. This control logic can subscribe to events triggered by radio components and change radio parameters or reconfigure the radio structure. This enables the IRiS framework to support cognition through this control mechanism.

To design a radio with IRIS, an Extensible Markup Language (XML) configuration file is written that specifies the radio components, their parameters, and connections. Optionally the radio designer can implement a control logic manager for dynamic radio reconfiguration. On start up the XML file is parsed and the run-time engine creates the radio by instantiating and connecting the specified components.

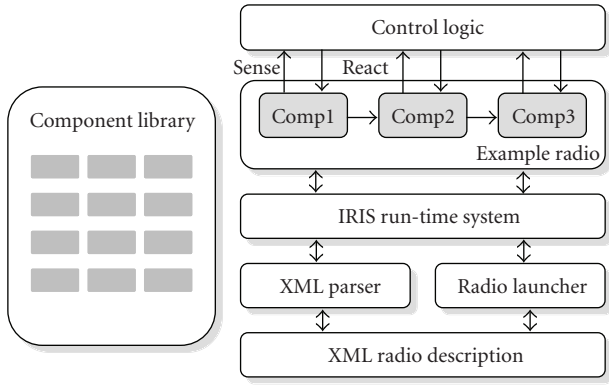

Figure 7: IRIS architecture.

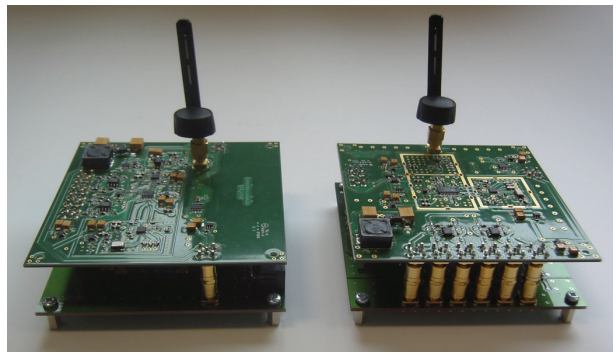

Figure 8: MARS receive and transmit boards.

The run-time engine then loads the control logic and attaches it to the components. Finally the radio is started, and blocks of data generated by the source component will be processed by each of the components in the radio chain. The control logic can react to events triggered by components, with anything from diagnostic output to a full reconfiguration of the radio.

4.6. Final Design. The implementation of the MARS platform was as two separate simplex elements: a receive-only and a transmit-only boards (shown in Figure 8). Duplex operation was avoided due to the limitations of the USB throughput. A version of the baseband board exists that allows for duplex operation but at half the bandwidth. As the MARS platform is part of an ongoing research project into software radio platforms, there have been subsequent improvements on the design which will be detailed later.

5. Performance and Use Cases

The MARS platform has been tested under a number of use cases—for example,

(i) Spectrum sensing.

(ii) Still image and video transmission.

(iii) Novel communication schemes.

(iv) Interoperability testing with the USRP.

To test the proposed SDR platform together with IRIS we successfully transmitted an image [25]. To isolate platform artifacts, a USRP and an MARS platform were used interchangeably as transmitter and receiver. The IRiS software engine has appropriate software interfaces for the two platforms. The IRiS software engine read a bit-map image, framed the data using a simple structure, with appropriate data whitening and error correction encoding. Differential quadrature phase shift keying (DQPSK) was used to modulate the data into four symbols. To limit the spectral footprint of the signal, it is upsampled and filtered with a root raised cosine pulse shaper. The resulting IQ samples were delivered over USB to the radio front-end. At the receiver, the MARS platform demodulates the data and delivers unprocessed IQ samples over USB to the software engine. IRiS then undertakes filtering, clock data recovery, and demodulation. The data is then deframed and reconstructed into the image. In this experiment we used a 1 MSps transfer rate. In this mode of operation we could operate over six times faster, but are limited primarily by the processing performance of the PC or laptop used. The results of this experiment are shown in Figure 9 where the resulting image and constellation diagram are presented. The constellation diagram provides an indication that the error vector magnitude is acceptably small and good communication is possible.

In another example, a video sample was transmitted and received using MARS platforms (Figure 10). A DBPSK modulation scheme was used. The transmitted signal bandwidth was approximately 300 kHz with an IQ sample rate of 2 MSps. This proved acceptable for video transmission but higher throughput could be obtained with higher order modulation schemes. The error vector magnitude suggests that a more dense constellation diagram could be implemented without significant impairment of performance. The limitation on using a higher modulation scheme lies in the software engine and this is likely to improve with time and processing power.

The strength of the MARS platform is in the quality of the RF elements of the circuit. Deliberate effort went into designing a high-quality receive chain in accordance with the requirements of the various standards. Table 2 presents the characteristics of the MARS platform in context to the other SDR testbed platforms. Though more powerful and capable systems exist, the MARS platform should be compared with the USRP for complexity and performance. In that context, it offers a similar level of baseband capacity with superior radio frontend performance. The two are interchangeable and offer users the ability to assess the performance of their software radio schemes independently of a specific hardware implementation and associated artifacts.

6. Future Trends

The first generation of available SDR platforms occurred around 2004–2006. Technology has progressed since then and there have been significant improvements in signal processing performance, connectivity, and in the quality of RF components such as mixers and data converters. With current capabilities it has become possible to implement most narrowband communication schemes (e.g., GSM) though not without significant effort and expertise. However, in recent years there has been a movement toward wider band solutions such as wCDMA and OFDM technologies. The effect is that SDR platforms are challenged by increasing bandwidths, reducing minimum signal strengths, and reducing maximum allowable error vector magnitudes. Application specific SDR platforms can be constructed with a combination of available technologies. General purpose experimental SDR platforms still face challenges and will be driven by three trends:

(i) Increased capacity platform interfaces.

(ii) An increasingly diverse range of processors.

(iii) Increased on-board processing capability.

The USRP2 from Mark Ettus is the first of the next generation of SDR platforms, and these trends are visible in the new design: significant on-board FPGA and a gigabit Ethernet connection.

6.1. Increased Platform Interfaces. The first generation of SDR platforms either used Ethernet or USB to provide connectivity to computers and other users. Ethernet can now commonly offer 1 Gbps, but existing SDR platforms used only 10/100 Mbps links which in practice delivered less than half that when routing overheads are considered. USB 2.0 offered a superior performance with 480 Mbps and a maximum sustained rate of 256 Mbps. In practice, to deliver 25 MHz of bandwidth to a duplex transceiver, a minimum of 2.4 Gbps would be required and a more conservative estimate would suggest 4.8 Gbps [26]. This problem is exacerbated when considering multiple element systems such as in the MIMO variant of 802.11(n). This problem can be partially solved by improving the interface communication speeds to the platform. Preserving compatibility with generic computers, multigigabit Ethernet and PCIexpress are likely to be seen in future platforms. PCIexpress was used in the KUAR platform as an internal protocol; but with PCIexpress in most computers, it has become feasible to use it as a communication interface. PCIexpress is used in graphics cards and is optimized for streaming data. In version 2.0, it offers 4000 Mbps in each direction per lane. This is sufficient for encoding 25 MHz of bandwidth, however it is possible to combine multiple PCIexpress lanes and increase performance. Most computers have at least two lanes as an expansion port, and this is likely to increase in the future. If you access the graphics bus, up to 32 lanes are available, providing 128 Gbps of bidirectional data. Alternatively, newer forms of gigabit Ethernet offer up to 100 Gbps which is also sufficient for most applications. One common trend in all these schemes is the move to optical connections. This is a trend being encouraged by developments in the mobile telephony base station industry, where fibre-optic links deliver electrical isolation, ability to place RF elements away from the processing unit, and provide an upgradeable communications infrastructure. One

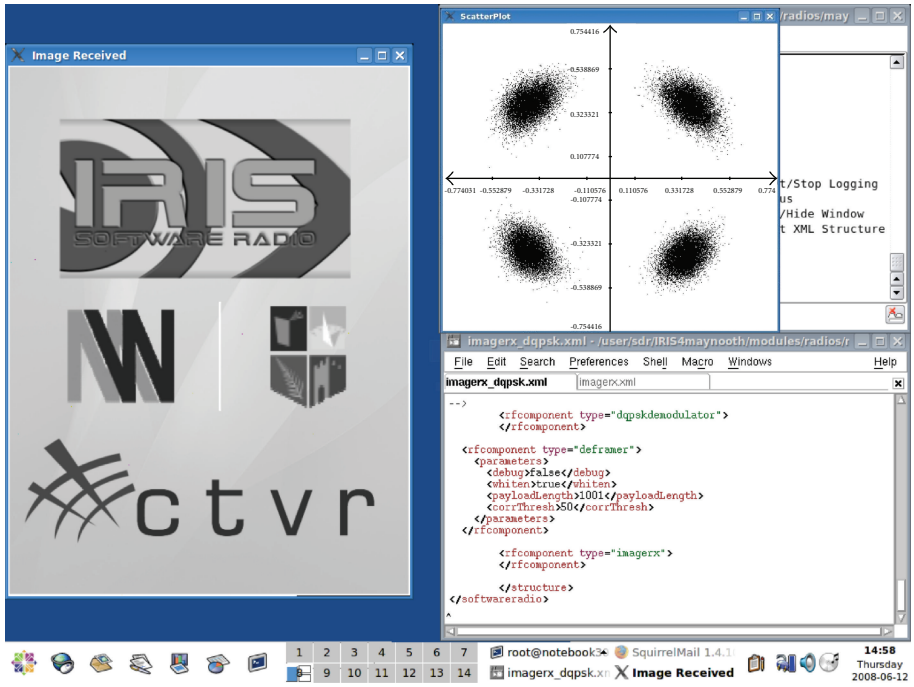

Figure 9: Transmitted image with constellation diagram.

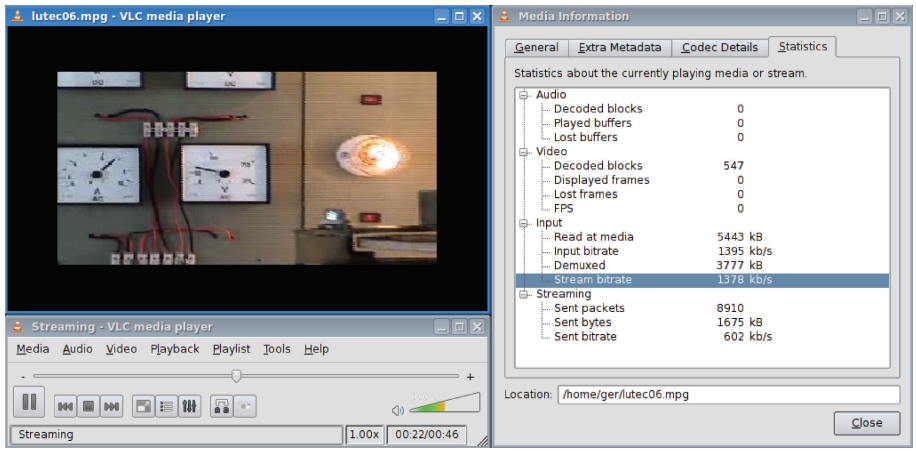

Figure 10: Example of video being received using the SDR platform with performance statistics.

implication of the increasing communications capacity is the requirement for increased on-board processing capacity.

6.2. Increased on-Board Processing Capability. The concept of placing the majority of the signal processing off-board on a computer was a valid concept that derived from the software engineering/computer science researchers who were active from the earliest days. This concept is exemplified by the commercial products developed by (Vanu, Inc. Mass, USA) and by the GNU radio architecture. This approach faces two challenges: modern communication schemes expect a very low-latency response, particularly in the initial handshaking events—which is very difficult to do when passing the data over a link to a separate processor; secondly general purpose processors are not optimally suited for many of the computational intensive aspects of a communications scheme, for example, inverse-FFTs. Specialists DSPs and FPGAs offer superior performance for many of these functions and these can be used to reduce latency by processing signals closer to the antenna prior to transport to a processing unit. This approach partitions the signal processing optimally to the available processor architectures and has the benefit of reducing the quantity of data needed to be transported and maximizing the system capacity. One extreme is to place one or more processors on board and allow the board to be functionally independent of any external source (e.g., the KUAR and BEE2 platforms). However, general purpose processors still offer superior flexibility and ease of use when developing new systems, but with higher speed connections

Table 2: Comparison of available SDR platforms.

	MARS	MARS3	KUAR	USRP	USRP2	BEE2	NICT
Year of release	2007	2009	2005	2005	2008	2007	2005
RF bandwidth (MHz)[(1)]	70	25	30	5	25	25	25
Frequency range (GHz)[(2)]	1.7–2.5	1.7–2.5	5.25–5.85	2.3–2.9[(4)]	2.3–2.9[(4)]	Fixed (2.45)	1.9–2.4 5.0–5.3
Processing partition	Off-board	Mixed	On-board	Off-board	Mixed	On-board	On-board
Processor architecture	GPP	FPGA	GPP FPGA	GPP	GPP FPGA	FPGA	GPP FPGA
Connectivity	USB	PCIexpress GigEthernet	USB Ethernet	USB	GigEthernet	USB Ethernet	USB Ethernet
No. of antennas or RF paths	2	16	2	4	2[(3)]	16	2
Standards aware (RF)	yes	yes	no	no	no	no	yes
Standards aware (baseband)	yes	yes	no	yes	yes	yes	yes
Strengths	Low cost	Large bandwidth		GNU radio integration	Large bandwidth	Processing power	Standard compliance
Weaknesses	Limited bandwidth		Frequency range	Limited bandwidth	Complexity		Limited availability

[(1)] Assuming no baseband or connectivity restrictions.
[(2)] Within a single RF board.
[(3)] Extendable through linking multiple platforms.
[(4)] Wide selection of frequency ranges available.

and wider bandwidths, partitioning of processing functions between the computer, and the SDR hardware platform appears unavoidable.

6.3. Diverse Range of Processors. Typical implementations of software-defined radio (SDR) systems include a general-purpose processor (GPP), a digital signal processor (DSP), or an FPGA, though dedicated DSP chips are being challenged by FPGAs with embedded DSP cores [27]. FPGA-based systems can deliver the performance but at the cost of increased design complexity. General purpose processors are less effective at physical layer processing but excel at the higher layers and are more accessible to the general software designer. Neither is optimal and this has resulted in a broader range of processor types being developed and used for software-radio applications. These can be broadly, and not exclusively, categorized as complex multicore systems; specialist floating-point calculators such as found in graphics chips.

Multicore systems are common with many computer processors containing multiple cores. These are, however, multiple versions of the same core. A heterogeneous multi-core system could contain a mixture of embedded FPGAs, DSPs or general purpose processors, with functions being allocated to match the strengths of a specific core. Examples of these devices include recent generations of FPGAs are now including dedicated DSP slices and complete processor cores, but are programmed using traditional FPGA design tools. Another example is the Sandbridge Sandblaster processor which contains multiple DSP cores and an ARM9 processor, and is treated as a DSP device [28]. Future SDR platforms will likely take advantage of this trend to deliver increased capacity, with the likelihood of the increasingly complex FPGAs being utilized first due to their relative maturity.

The other interesting development is the use of graphics chips to deliver the floating point processing power needed for wideband physical layer processing. Graphics chips are dedicated floating point processors which are optimized to deliver sustained performance. As part of a commodity market, it is difficult to match their processing power per cost ratio and they come with a well-developed software development environment. One of the most powerful devices is IBM CELL processor as used in the Sony Playstation3. The CELL processor is another multicore device and is designed to excel at parallel processing. It has a theoretical maximum performance of 204.8 GFLOPS (single precision)—sufficient for any software-defined radio [29]. There is already an initiative to port GNU radio to the cell processor to avail of this capability [30].

7. Future Development

The development of the MARS platform was an exploration of the challenges in implementing a base station-orientated reconfigurable platform. As such it has provided us with many insights in how the technical issues are subtly different than those experienced in handheld designs. As part of an ongoing research project, we are currently working on the

next generation of the MARS platform. The MARS platform did not include any on-board processing power, the next platform, MARS2 is in testing and will include a Xilinx Spartan3 device to enable local processing. Though this will still use a USB connection, it will allow us to avail of the greater capabilities of the RF boards. Most of our current activity is focused on the third generation of the MARS platform. This platform is focused on supporting a wider bandwidth and to have substantial localized processing. The key characteristics of this design are as follows

(i) A PCIexpress connection to a computer, providing up to 4 Gbps connectivity.

(ii) A baseband processor board with one or more Virtex4 processors, capable of supporting 8 transmit and receive paths (16 in total).

(iii) Fibre-optic CPRI/OBSAI [31, 32] links for distribution of data to remote RF boards

(iv) Remote RF boards that are enhancements of existing MARS boards with fibre-optic links, gigabit Ethernet and USB as back.

(v) Flexible RF performance supporting 25 MHz of bandwidth.

This platform is significantly more complex than before but it is designed to be modulator so that the superior RF frontends can be used in isolation or as part of a network of links boards. Though the bandwidths are substantially higher, the platform will remain compatible with the IRiS and GNUradio software frameworks. First prototypes of the new platform are expected in the summer of 2009.

8. Summary

Though software-defined radio offers many compelling benefits to radio system designers, there remains many open questions on how to effectively implement and manage flexibility in a wireless system. Software radio platforms and testbeds offer researchers and developers the ability to develop their applications in advance of designing customized hardware. In recent years there have been substantial improvements in technology, and low-cost platforms are now possible though few are generally available.

In this paper, we presented a brief overview of the state-of-the art of SDR platforms and the future technology trends in this area. We also presented an experimental platform developed at the National University of Ireland, Maynooth. This platform is currently being used by our collaborators and we wish to share this platform with new collaborators to develop a broader community of users and diverse applications.

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Computational methodologies of signal processing and analysis based on 1D-4D data are commonly used in different applications in society. In particular, image processing and analysis methodologies have enjoyed increased deployment in automated recognition, human-machine interfaces, computer-aided diagnostics, robotics surgery, and biomechanics analysis.

Image processing and analysis is fundamentally a multidisciplinary area, combining elements of informatics, mathematics, statistics, psychology, mechanics and physics, among others. One of the more important applications of image processing and analysis can be found in medical imagery, which continually promotes new research and development. Present trends include using statistical or physical procedures on medical images in order to have different objectives, such as organ segmentation, shape reconstruction, motion and deformation analysis, organ registration and comparison, virtual reality, computer-assisted therapy, or biomechanic analysis and simulation.

The research related with analysis and simulation of biomechanical structures has been a source of many challenging problems, involving geometric modeling, numerical modeling, biomechanics, material models for living tissues, experimental methodologies, and mechanobiology, as well as their application in clinical environments. A critical component for true realistic biomechanical analysis and simulations is to obtain accurately, from images, the geometric data and the behavior of the desired structures. For that, the use of automatic, efficient, and robust techniques of image processing and analysis is required.

The main objective of this Special Issue on *Image Processing and Analysis in Biomechanics* is to bring together recent advances in the field. Topics of interest include, but are not limited to:

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Special Issue on Microphone Array Speech Processing

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Significant knowledge about microphone arrays has been gained from years of intense research and product development. There have been numerous applications suggested, for example, from large arrays (on the order of >100 elements) for use in auditoriums to small arrays with only 2 or 3 elements for hearing aids and mobile telephones. Apart from that, array technology has been widely applied in the areas of speech recognition and more recently surveillance. Traditional techniques that have been used for microphone arrays include the fixed spatial filter as well as optimal and adaptive beamforming. These techniques model input or calibration signals as well as localization information for their design. Today contemporary techniques using blind signal separation (BSS) and time frequency masking techniques have attracted significant attraction. Those techniques are less reliant on array modeling and localization, but more on the statistical properties of speech signals such as sparseness, non-Gaussianity, nonstationarity, and so forth. The main advantage that multiple microphones add from a theoretical perspective is the spatial diversity, which is an effective tool to combat interference, reverberation, and noise when used according to the theoretical assumption. Combining spatial information with time-frequency information and perceptual cues will lead to innovative techniques and new methods, which will provide improved communication capabilities in challenging acoustic environments.

To further enhance current research and to promote new applications, this special issue aims to collect and present the latest research efforts in signal processing methods and algorithms for microphone arrays.

Topics of interest include, but are not limited to:

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- Multichannel dereverberation techniques
- Microphone array-assisted multichannel acoustic echo cancellation
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Special Issue on
Advanced Signal Processing for Cognitive Radio Networks

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Cognitive radio is widely expected to usher in the next wave in wireless communications. In December 2003, the Federal Communications Commission (FCC) of the US government issued authorized cognitive radio techniques for spectrum sharing/reusing and approved the use of fixed and mobile services in TV bands. In October 2008, the FCC further approved the use of mobile white space devices in TV bands, and many governments worldwide have also moved to support this new spectrum usage model. This has been accompanied recently by a significant upsurge in academic research and application initiatives, such as the IEEE 802.22 standard on wireless regional area networks (WRANs) and the Wireless Innovation Alliance including Google and Microsoft as members, which advocates unlocking the potential in the "white space" of television bands.

However, cognitive radio networking is still in the early stages of research and development. To achieve full "cognition" and reliable communication over a wireless network, there are still tremendous technical, economical, and regulatory challenges. Signal processing plays a major role in cognitive radio networks. The aim of this special issue is to present a collection of high-quality research papers in advanced signal processing for cognitive radio including theoretical studies, algorithms, protocol design, as well as architectures, platforms, and prototypes which use advanced signal processing techniques. Topics of interest include, but are not limited to:

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- Cooperative spectrum sensing and communication
- Resource allocation for spectrum sharing
- Exploiting multiantennas for spectrum sharing
- Channel and environment learning techniques for cognitive radio
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