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Microstrip unequal Wilkinson power divider with 1:11 division ratio

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In this paper, a 1:11 unequal microstrip Wilkinson power divider (WPD) is presented. Power division is a necessary function in most of the wireless/wireline communication systems. To design 1:11 WPD using an easy-to-fabricate microstrip technology, microstrip line having a very high characteristic impedance (Z_c) value of 315 Ω is needed. Realization of this value is impractical because too thin line is required. Defected ground structure (DGS) provides the hosting microstrip line with high inductance and modest capacitance values simultaneously. As a result, very high impedance could be implemented using practical lines. Novel analytical calculation method is developed to compute Z_c of microstrip line loaded with DGS. It is found that circular-patterned DGS could be used to realize the required microstrip line. The designed WPD is fabricated and measured at centre frequency (f_c) equals 1 GHz. The measurements of insertion and reflection losses of the fabricated circuit as well as the isolation between the output ports are in a good agreement with the simulated responses of the designed circuit.

Keywords: passive components; Wilkinson power divider; microstrip circuits; defected ground structure

1. Introduction

The fast evolving of radio frequency (RF) and microwave technology requires different passive and active circuits/components with stringent requirements. Among diverse passive RF devices, the power divider (PD) is indispensable component in power amplifiers [1], phased array antenna [2], mixers [3] and many other circuits. These circuits are widely used in communications and radar systems for decades. As the division ratio goes high, the design and implementation of the PD becomes much difficult.

Wilkinson power divider (WPD) [4] is the most popular type amid the PDs configurations. WPD features two main advantages, the first, it has straightforward design procedure. Secondly, its realization in printed planar technologies is very simple. On the other hand, planar microstrip technology has many advantages such as ease of fabrication, low fabrication cost and facility of integration with integrated circuits.

The purpose of unequal WPD, shown in Figure 1, is to split the power of the input with prespecified ratio between two output ports, ideally without losses. Generically, the WPD power division ratio is 1:k^2, where $k^2 > 1$. Other properties of the WPD are that all ports are matched, the two output terminals are isolated from one another, and that it is reciprocal. The aforementioned features are reflected in the *S*-Parameters matrix of unequal WPD, as stated in (1),

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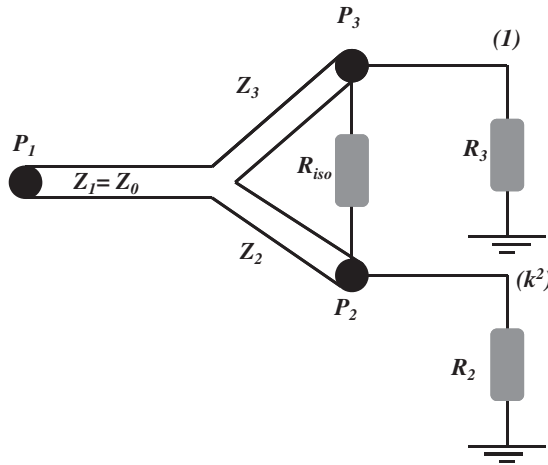*Corresponding author. Email: htaher@eeng.nuim.ie

Figure 1.   Topology of 1:k^2 unequal WPD.

$$[S] = \begin{bmatrix} 0 & -\frac{j\sqrt{k^2-1}}{k} & -\frac{j}{k} \\ -\frac{j\sqrt{k^2-1}}{k} & 0 & 0 \\ -\frac{j}{k} & 0 & 0 \end{bmatrix} \tag{1}$$

As k^2 exceeds 3, microstrip-based WPD begins to lose its advantage, where, at these designs, very high Z_c microstrip lines are demanded. It is well known that, as the value of Z_c is increased, the line width becomes much thinner. Consequently, implementation of high Z_c line is cumbersome, and in many cases, is impossible when value of k^2 exceeds 5.

   To overcome this problem, different techniques are used to implement the high Z_c line. Among these techniques, defected ground structure (DGS) is used to increase the microstrip line inductance.[5] As a consequence, Z_c of the specific line could be increased without narrowing its width. In [6], the authors obtain 1:4 dividing ratio using mender-line DGS. The dividing ratio is increased to 1:6 using rectangular DGS pattern.[7] Alternative techniques are used to increase the dividing ratio. A 1:7 unequal WPD is fabricated using grounded coplanar waveguide to achieve the high impedance sections [8], on the other side, coupled lines with two shorts are utilized to obtain 1:10 ratio.[9] Arbitrary dividing ratios are also reported. The authors employ Vias, stubs [10] or lumped components [11] to obtain the required ratio. However, the highest fabricated dividing ratio using both techniques is 1:9. Cascaded PD stages are used to obtain 1:11 division ratio.[12] However, the design suffers from the wide circuit area.

   Among the previously mentioned techniques, a DGS pattern underneath the microstrip line is the easiest methodology to design WPD. Moreover, since there is no need to Vias, stubs or lumped elements, it is easily realized and wider operational bandwidth could be obtained. As it is previously mentioned, the highest obtained division ratio with DGS patterns is 1:6. Nevertheless, there is still scope for increasing the division ratio using new DGS geometries.

In this work, simple circular DGS pattern is investigated to further increase Z_c value of microstrip line. New analytical calculation method to calculate the Z_c value of microstrip line loaded with circular DGS is derived and used. It is turned out that making use of this pattern, a microstrip line with value of Z_c of 315 Ω is realized. Accordingly, a 1:11 WPD with circular DGS pattern prototype is designed, fabricated and experimentally measured at f_c equals to 1.0 GHz. To the authors' knowledge, this is first implementation of 1:11 unequal WPD using only DGS unit fabricated with microstrip technology.

This paper is organized as follows; the developed technique for calculating Z_c of microstrip line is elaborated in section two. Parametric study of Z_c of microstrip line loaded with circular DGS pattern is presented in section three. The design procedure of the 1:11WPD is elucidated in section four accompanied by the measurement results of the fabricated circuit. Conclusions are drawn in section five.

2. Developed extraction method for Z_C of transmission line

Two techniques [6,13] are usually used to compute Z_c of microstrip line from *S*-parameters' behaviour of the line. The value extracted from the former technique is frequency dependent. Concerning the latter technique, it is impossible to extract Z_c when the electrical length (θ) of the microstrip line under the investigation approaches $\pi/2$. This region is very critical in designing WPD.[4] Consequently, robust calculating methodology of Z_c is still required. The set-up used to find value of Z_c is shown in Figure 2, where (β) is the propagation constant and (l) is the physical length of the line. On the other hand, Z_0 is the terminating impedance at input/output ports, and that is normally 50 Ω in practice.

ABCD parameters of lossless line can be expressed in terms of line parameters as in (2),

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_c\sin\theta \\ jY_c\sin\theta & \cos\theta \end{bmatrix} \tag{2}$$

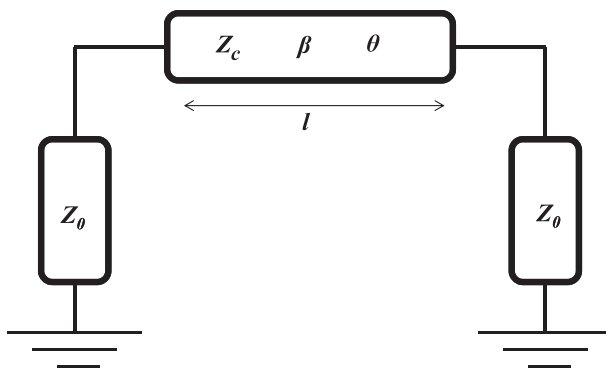where Y_c is the characteristic admittance of transmission line.

Figure 2. The used circuit diagram to find Z_c.

On the other hand, reflection and transmission coefficients at port one are S_{11} and S_{12}, respectively. They are obtained from *ABCD* parameters as follows [14],

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3}$$

$$S_{12} = \frac{2 * (AD - BC)}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{4}$$

From (2), the quantity $AD - BC$ equals one. Recalling that, Z_0 equals 50 Ω. As a consequence, the denominator of (4) takes the following form,

$$A + \frac{B}{50} + 50C + D = \frac{2}{S_{12}} \tag{5}$$

Substituting from (5) into (3). Also, substituting with the values of *A, B, C* and *D* from (2), all into (3), following equation is obtained,

$$2\frac{S_{11}}{S_{12}} = \frac{jZ_c \sin \theta}{50} - \frac{j50 \sin \theta}{Z_c} \tag{6}$$

Taking the imaginary part of the both sides of (6), equation of Z_c is obtained as in (7),

$$\frac{Z_c}{50} - \frac{50}{Z_c} = \frac{2}{\sin \theta} Im \frac{S_{11}}{S_{12}} \tag{7}$$

A quadratic equation of Z_c is acquired as in (8),

$$Z_c^2 - \left(\frac{100}{\sin \theta} Im \frac{S_{11}}{S_{12}}\right) Z_c - 2500 = 0 \tag{8}$$

The standard quadratic equation has the following form,

$$rZ_c^2 + sZ_c + t = 0 \tag{9}$$

Determinant of (8) equals to $s^2 - 4rt$ is always positive and has two real roots. Out of the two Z_c values, one is the physical solution and selected, while the other is rejected. The obtained solution is always physical and reliable especially in proximity of $\pi/2$ lines.

To validate the new methodology, frequency behaviour of Z_c of microstrip line without DGS having 50 Ω characteristic impedance at 1 GHz is calculated. The substrate used in this work is Rogers 5870 with a dielectric constant (ε_r) of 2.33 and a thickness (h) equals to 1.575 mm. Consequently, the width of simulated line (w) is 4.59 mm and its length (l) is 55 mm which corresponds to one-fourth guided wavelength ($\lambda_g/4$). The S-parameters of the line under test are obtained with time-domain finite integration technique using CST microwave studio package. Concerning the utilized boundary conditions (BC) of the problem, the perfectly matched layer is adopted as the utilized BC. It modifies the equations in the buffer region to damp the

waves as they travel through it. The goal is to attenuate these waves to a level where they can be ignored when they return to the domain of interest. The computational advantages of the PML over other absorbing boundary conditions include its applicability to various numerical methods and it relative ease of implementation.

As shown in Figure 3, the presented methodology predicts with high accuracy the Z_c value. In the next section, the novel technique is employed to investigate Z_c of microstrip line loaded with circular DGS pattern.

3.   Parametric study of Z_c of microstrip line loaded with circular DGS pattern

Circular DGS pattern in microstrip technology is shown in Figure 4. The radius of the circular DGS is a. To study the dependence of Z_c on the variation of a, the value of a is altered between 15 and 18 mm with 1-mm step. Concerning w and l, their values are fixed to 0.30 and 47 mm, respectively. In the existing case, l corresponds to $\lambda_g/4$ length. Figure 5 shows the frequency behaviour of Z_c as function of different values of a. As depicted in the graph, value of Z_c is directly proportional to a, with slight dependence on the frequency. The reason is that as a is enlarged, the perimeter of the circle is increased and the current path is prolonged. As a result, more inductance is added to the total inductance (L). Concerning the value of the capacitance added by the circular DGS, it is very small and does not effectively contribute to the total capacitance (C). Since the value of Z_c is defined as $\sqrt{L/C}$, therefore, Z_c value of the loaded microstrip line is noticeably augmented.

In quasi-TEM approximation, microstrip line, the electric field lines are tied vertically to the ground plane. Magnetic field in this mode is closed around the strip. Propagation of the electric and magnetic fields can be modelled using distributed capacitance and inductance of the transmission line in the form of lumped element. Therefore, to confirm this analysis, both electric field (capacitance) and surface current density (inductance) distributions on the ground surface are examined at operating frequency of 1 GHz and θ approximately equals to $\pi/2$. As depicted in Figure 6, most of the effective electric field exists underneath the microstrip line in small portion of the circular DGS. Consequently, modest value of capacitance contributes in overall capacitance of the line.

Regarding the surface current density distribution, shown in Figure 7, a considerable amount exists around the whole circumference of the circular DGS. Consequently, much inductance is added to the total inductance of the hosting microstrip line.
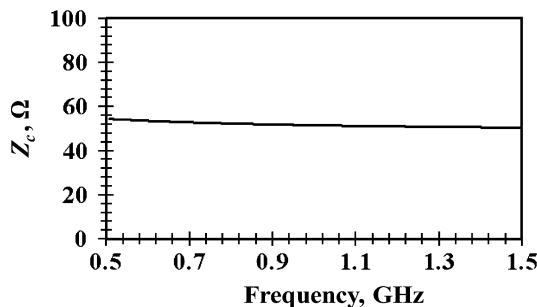

Figure 3. Z_c of 50 Ω microstrip line calculated with the developed technique.
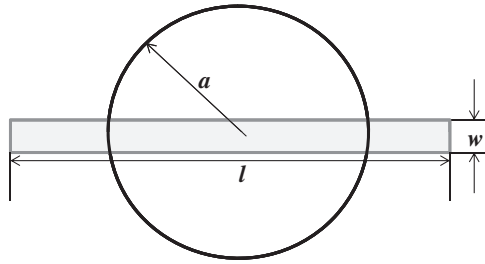
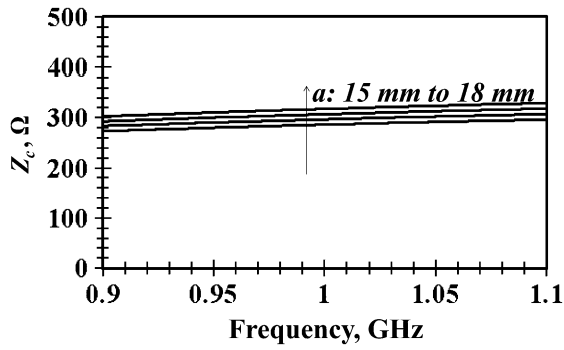Figure 4.   Circular DGS pattern on the ground of the microstrip line.

Figure 5. Z_c of microstrip line loaded with circular DGS pattern. *a* varies from 15 to 18 mm and *w* = 0.3 mm.
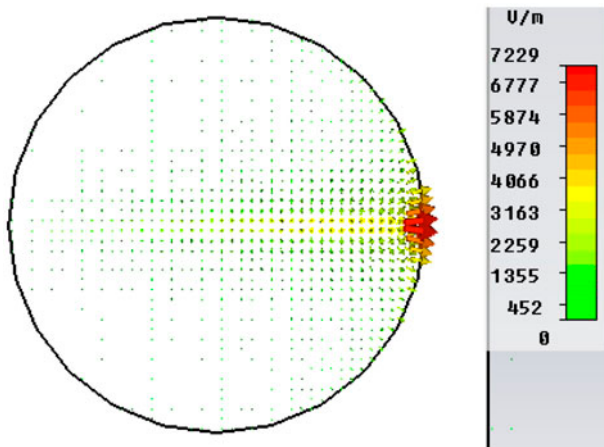

Figure 6.   Electrical field distribution on the ground of microstrip line loaded with circular DGS pattern, f = 1 GHz, $\theta = \pi/2$.
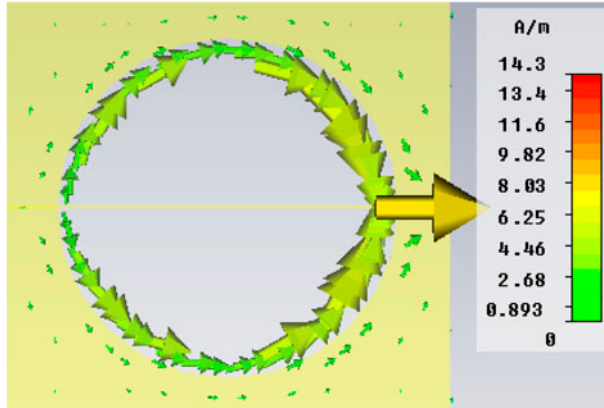
Figure 7. Surface current density distribution on the ground of microstrip line loaded with circular DGS pattern, $f = 1$ GHz, $\theta = \pi/2$.

The effect of changing value of w on the obtained Z_c value is studied as well. The value of w is increased from 0.30 to 0.90 mm with a step of 0.20 mm, while, a and l values are fixed to 18 and 47 mm, respectively. The obtained behaviour is shown in Figure 8. It is clearly depicted that, as w is increased, value of Z_c of the line is decreased. This result agrees well with the physical behaviour of any transmission line.

In the next section, the performed parametric study is exploited to build microstrip 1:11 WPD.

4. Design and practical implementation of 1:11 WPD

Figure 9 shows the layout of the proposed 1:11 WPD realized in microstrip technology. Resistances R_2 and R_3, shown in Figure 1, are transformed to 50 Ω using Z_{L2} and Z_{L3} $\lambda/4$ lines for convenient measurements. It is known that the characteristic impedances of the four $\lambda_g/4$ transmission lines and R_{iso} are given by [10],
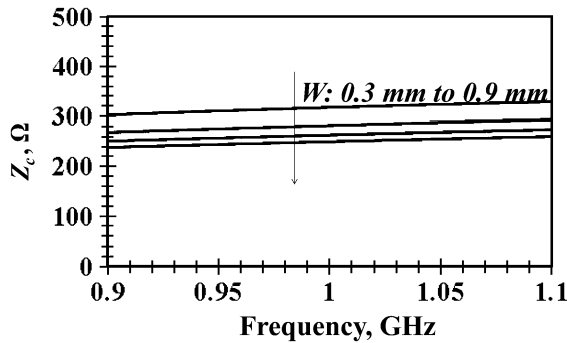

Figure 8. Z_c of microstrip line loaded with circular DGS pattern. w varies from 0.3 to 0.9 mm and $a = 18$ mm.
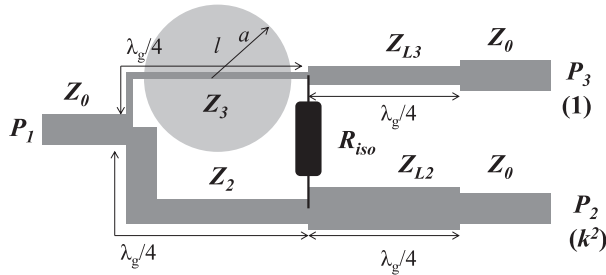
Figure 9.   Layout of the microstrip 1:11 WPD.

$$Z_2 = Z_0 \sqrt{\frac{1+k^2}{k^3}} \qquad (10)$$

$$Z_3 = Z_0 \sqrt{k(1+k^2)} \qquad (11)$$

$$Z_{L2} = \frac{Z_0}{\sqrt{k}} \qquad (12)$$

$$Z_{L3} = Z_0 \sqrt{k} \qquad (13)$$

$$R_{iso} = Z_0 \frac{1+k^2}{k} \qquad (14)$$

Using (10) to (14), the impedance values of a 1:11 WPD is listed in Table 1. As previously mentioned, it is impossible to implement traditional microstrip with Z_c equals to 315 Ω. Therefore, this line is implemented using circular DGS investigated in preceding section. From the parametric study, microstrip line with w equals 0.3 mm and l has a length of 47 mm, and circle has a equals 18 mm, can provide such a high Z_c value. It is worth noting that traditional microstrip line with w equals 0.3 mm has Z_c equals 164.5 Ω, i.e. circular DGS beneath microstrip line adds 151 Ω to the value of Z_c without narrowing the width of the line.

To reduce the circuit area, the topology is modified to the layout shown in Figure 10. The lines Z_{L2} and Z_{L3} are bent around Z_2 and Z_3, respectively. Due to the bends and junction effects of the modified circuit layout, the CST microwave simulator is used to fine tune the structure dimensions to obtain the required power division ratio at 1 GHz. The final dimensions of the design are listed in Table 2.

To validate the design, the modified WPD is fabricated using standard printed circuit board technology. This technology yields circuits having the following advantages:

Table 1.   Characteristic impedance and resistor values of 1:11 WPD.

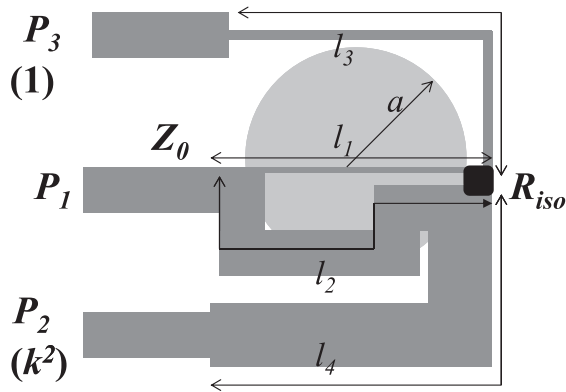| Z_2 (Ω)	Z_3 (Ω)	Z_{L2} (Ω)	Z_{L3} (Ω)	R_{iso} (Ω)
28.60	315.4	27.40	91.06	181

Figure 10. Modified and adopted layout of 1:11 WPD.

Table 2. Modified lengths values of 1:11 WPD.

l_1 (mm)	l_2 (mm)	l_3 (mm)	l_4 (mm)	a (mm)
43.40	60.60	62.75	64.5	17.5

low weight, low volume, low fabrication cost and lastly but not least can be easily combined with microwave integrated circuits. The fabricated circuit, shown in Figure 11, is measured using a vector network analyzer. A thru-open-short calibration method is used to de-embed the *S*-parameters of the WPD from the measured data. The simulated and measured results of insertion loss (S_{21}, S_{31}) and isolation between the output ports (S_{23}) are depicted in Figure 12. On the other hand, simulated and measured return losses (S_{11}, S_{22}, S_{33}) are plotted in Figure 13.

As shown in Figure 12, the ratio between $|S_{21}|$ and $|S_{31}|$ is literally 1:11 over 0.80 GHz to 1.2 GHz range. The simulated $|S_{21}|$ and $|S_{31}|$ values amount to be –0.38 dB and –10.70 dB, respectively, at 1 GHz which equal exactly to the theoretical quantities. Concerning the measured quantities, they perfectly follow the corresponding simulated quantities and their values at 1 GHz are –0.60 dB and –11 dB. Moreover, simulated $|S_{23}|$ reaches –26 dB at 1 GHz, while, the corresponding measured quantity is –24 dB.

Regarding the simulated return loss, shown in Figure 13, they have the following values at the centre frequency, $|S_{11}| = -26$ dB, $|S_{22}| = -28$ dB and $|S_{33}| = -36$ dB. The corresponding measured behaviour slightly deviates from the simulated ones. The reason for the slight difference between the theoretical and measurement results attribute to the inherent inevitable losses any microstrip circuit experiences such as conductor and dielectric losses. It is noteworthy that, the transition from coaxial to microstrip line also shares in these losses. The measured phase of S_{21} and S_{31} and the difference between them are displayed in Figure 14. The difference is 3.75° at 1 GHz and does not exceed 4.6° at 1.2 GHz.

To compare with similar works, there is only one available fabricated 1:11 WPD and is published in [12]. It is noteworthy that WPD also designed at 1 GHz on the substrate with ε_r of 3.66. Our WPD exhibits very compact structure compared to it, where,
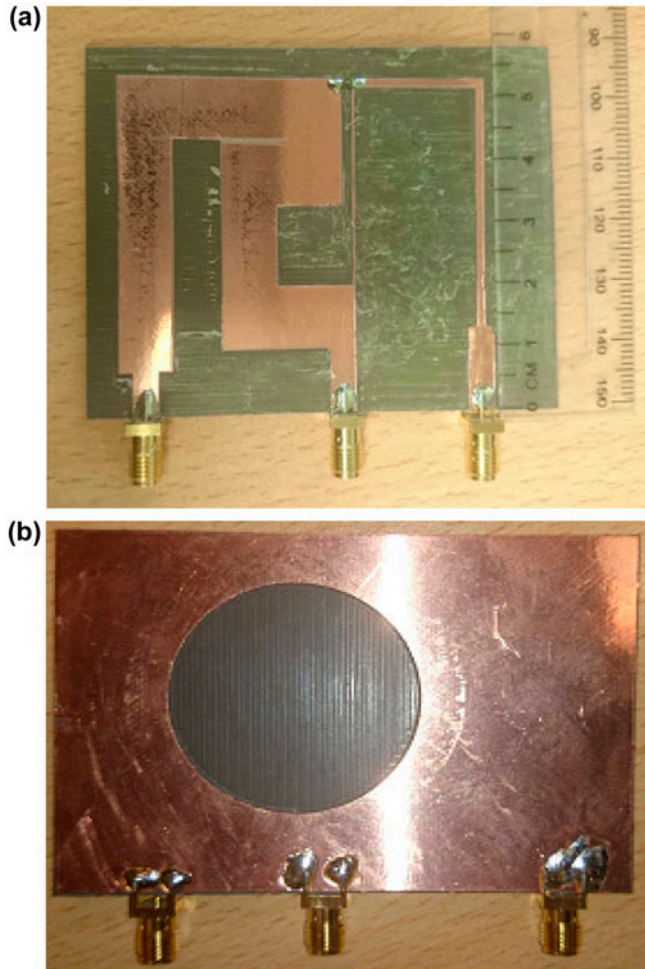
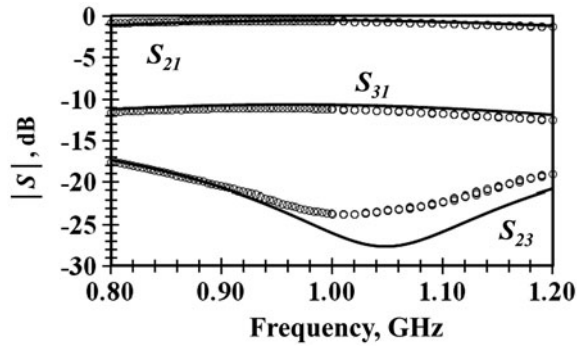Figure 11.   Photograph of fabricated 1:11 WPD (a) top (b) bottom.

Figure 12.   Simulated transmission and isolation coefficients (–) and the corresponding measured quantities (°) of the designed 1:11 WPD.
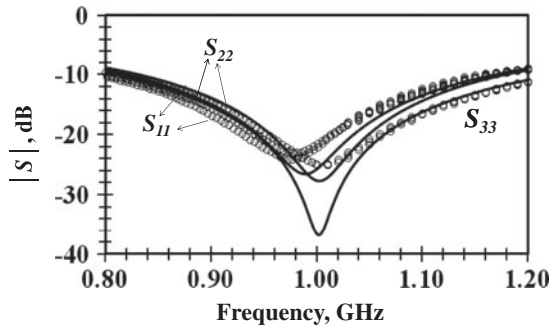
Figure 13. Simulated reflection coefficients (–) and the corresponding measured quantities (°) of the designed 1:11 WPD.
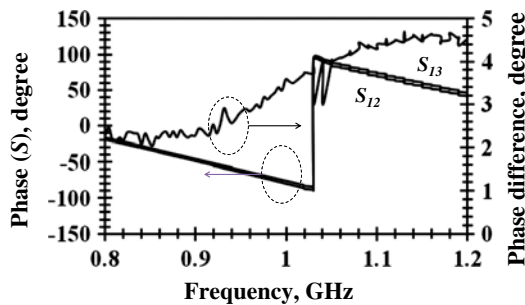

Figure 14. Measured phase of the transmission coefficients and their difference.

DGS WPD has $0.18\ \lambda_0 \times 0.22\lambda_0$, while the WPD of [12] has $0.37\ \lambda_0 \times 028\lambda_0$. On other words, the presented design has an area equals to 38% from the area of the circuit with the same specifications that is demonstrated in [12].

5. Conclusion

Compact, easy to design and fabricated without using any lumped elements, Vias or even stubs, a 1:11 WPD is presented. Simple circular DGS underneath traditional microstrip line is utilized to realize 315 Ω line which is required to build WPD. In the same context, new analytical methodology is proposed to calculate Z_c of any transmission line utilizing only its *S*-parameters measurements. The measurement results are in agreement with simulated results of the fabricated circuit. The realized WPD can be applied to any of the popular industrial, scientific and RFID communication systems.

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Disclosure statement

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