A MULTI-MODE VIDEO DRIVER FOR A HIGH RESOLUTION LCoS DISPLAY

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Abstract: *This paper describes the design of a display driver for Liquid Crystal on Silicon (LCoS) microdisplays. These are high resolution reflective display devices which allow up to 1280x1024 pixels on an area of 3.75 cm^2, and are typically refreshed at 120Hz. The required driver consists of a digital section capable of taking the common display formats such as SVGA and new formats, SXGA, and processing these to a common 120Hz RGB signal, requiring an output rate of 160 megapixels/second. This signal is then converted to a 10 bit accurate analog current which, when amplified, controls the LCoS device. This paper will discuss the new features added in the digital domain and the challenges of third-party IP integration of analog components.*

1.0 Introduction

Liquid crystal on Silicon (LCoS) microdisplays are a new technology which can provide a high resolution, low power, alternative to traditional CRT or LCD light engines. LCoS displays work on the principle of reflecting light onto a screen, given three different light sources a colour composite image can be formed. These devices can provide 1280x1024 pixels on an area of 3.75 cm^2. This when held 1" from the eye is equivalent to a 19" screen. With the use of high grade optics, LCoS devices can also be used as a cost effective replacement for large CRT screens. For good performance and to support multiple video formats, a microdisplay refresh rate of 120Hz has been targetted. In SXGA mode this would require each pixel to settle within 6 ns. However physical limitations on the refresh-rate of microdisplay pixels mean that more time is required, and this can be obtained by driving groups of pixels in parallel. Any mismatch, either in timing or value in these parallel paths will need to be minimised to prevent display distortion. This was a major consideration throughout the design of the microdisplay driver.

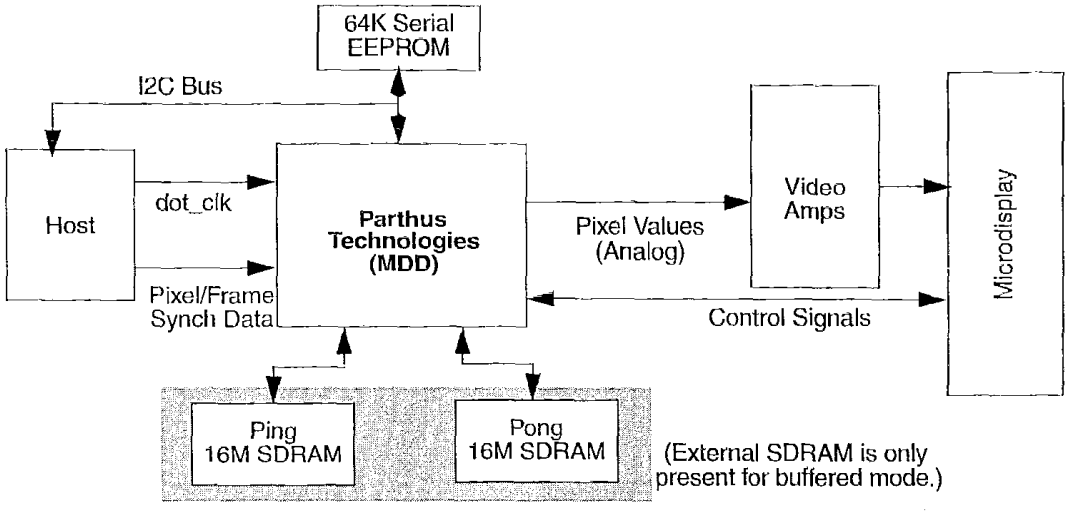

Figure 1: Position of the display driver within the system

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The system requirements are for a device that can drive a microdisplay at a refresh rate of 100 Hz, maintain interactive control of the performance of the signal path from the display driver to the microdisplay pixels, and the ability to buffer the video image in SDRAM when needed for lower frequency video modes. The display driver also has the ability to obtain its initial settings either through an I2C compatible interface or from an EEPROM. To ensure portability of the display driver, programmable Look-Up-Tables (LUT) for gamma-correction, multiple frequency, mode support and performance monitoring have been implemented in the digital domain.

2.0 Digital Design

The main function of the digital portion of the driver ASIC (MDD) is to accept video data in a given format and to condition the signals for use with the microdisplay. If the input data is less than the required frequency of the microdisplay then the signals are buffered and frames are repeated as necessary to maintain the output signal frequency. The driver is capable of supporting modes where each input frame can be repeated up to three times.

The Data Management Macros (DMM) generate the column, row and frame control signals required by the microdisplay. It also controls the storage and retrieval of frames in the external SDRAM. The size of the surrounding black ring is dynamically modified according to the size of the incoming format. The size of the incoming frame is user-definable from 2x4 to 1280x1024 (SXGA) and the position of the frame can be controlled with user-programmable x-y image offsets.

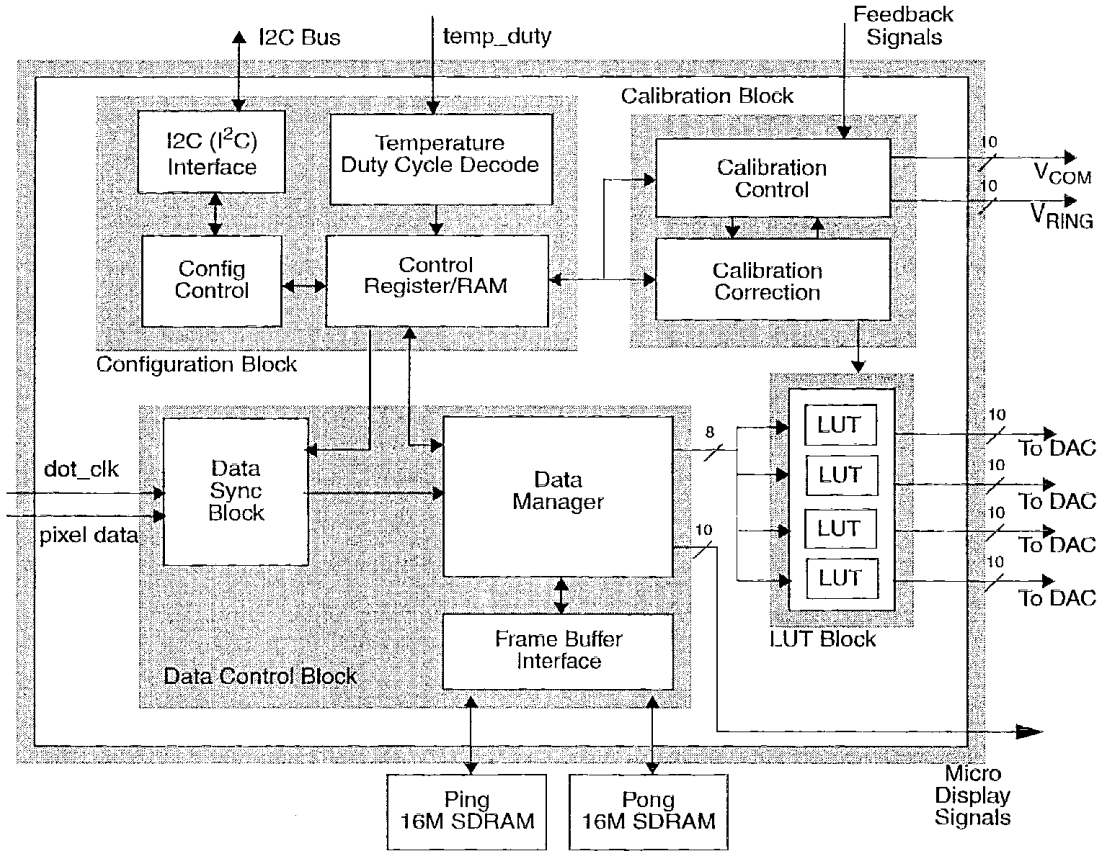

Figure 2: The main digital functional blocks

Combined with the flexibility of input frame rates and the size of the individual frames, the MDD driver is capable of driving the microdisplay with a very wide range of input formats, from low frequency high resolution signals (suitable for portable applications) to high frequency high resolution signals which could be used in monitors and television screens.

Pixel data from the DMM is applied to four Look Up Tables (LUT) which perform gamma correction by mapping each 8-bit value to a stored 10-bit value. It is possible at this point to dynamically adapt the LUT coefficients to ensure that system performance is maintained over process and temperature. The pixels are applied to the Digital to Analog Converters (DACs) which drive off chip.

The I2C interface provides control and programmability to these digital macros. This may be used to communicate with the host microprocessor and with an external EEPROM. The EEPROM is used to load initial system default values. An EEPROM has been selected as it provides the flexibility needed to ensure the driver may be used across different applications. The I2C interface to the host can then be used for user selectable options, such as varying the brightness or gamma correction and selecting video modes.

3.0 Analog IP Integration

For this design, analog blocks were available for both the video DACs and the PLL. This was advantageous as these blocks were silicon proven on our target process. The main challenge for the analog team was to examine, evaluate and integrate these analog blocks and to ensure that the system performance was obtained.

The four video rate DACs are 10 bit accurate current-mode DACs with up to 18 mA full-scale (nominally 12 mA) output drive at 40 MHz. The two slower DACs were specified to the same 10 bit resolution, at 200 Hz and a maximum current output of 2.25 mA (nominally 1.5 mA). The interchannel matching had to remain within 3%, with an INL less than 3 LSBs. Significant channel mismatch would introduce visible display distortion. Care needed to be given to the reference current distribution network, the design and layout of the DACs to ensure matching. Minor changes to the slower DAC design was required to maintain linearity over the spread of process, voltage and temperature required for this application. To facilitate the adjustment of the DACs, a complex analog behavioural model was developed for both the DACs and the load. This allowed us to efficiently test the DACs for skew, settling and interchannel interference under a wide range of conditions. Even though this was not a pure IP integration, there were significant savings in both time and effort.

The PLL was provided as a complete IP block. No changes were needed to either the design or the layout of this block. The PLL can provide a clock signal in the range 140-160 MHz with less than 100 ps(rms) jitter. The clock signal from the PLL is then fed to a custom analog block which provided the opportunity for gating the signals for test purposes. Another function of this custom block is to introduce a programmable delay of up to 25ns, with 32 steps, each step accurate to within 0.5ns. This could be used to retard or effectively advance various clock signals. This is needed to counter any transport delays between the data signals from the DACs and the digital control signals.

Analog IP integration was an important element in the design of the MDD ASIC. Using analog IP requires more testing than corresponding digital blocks, and minor modifications to the designs

should be expected. However as time-to-market was a critical feature, using silicon proven analog macros both speeded up the design process and reduced risk.

4.0 System Level Verification

The combination of off-chip devices, complex digital blocks and extensive analog components meant that system level verification was always going to present a challenge. Given the number of interfaces, the video input, the EEPROM/I2C interface, the connections with the SDRAM and the DACs, it was essential that some mechanism would be developed to verify the functionality of each interface and the performance of the relevant blocks. At the block level, pure digital or pure analog simulations could be performed but at the system level some form of mixed-mode analysis was required.

The ideal solution would be to use a tool such as spice-verilog to perform a full functional simulation of the design. However such simulations are very time-consuming and given the start-up times for both the digital, and analog blocks such as the PLL, it was decided that this would not be a viable verification technique.

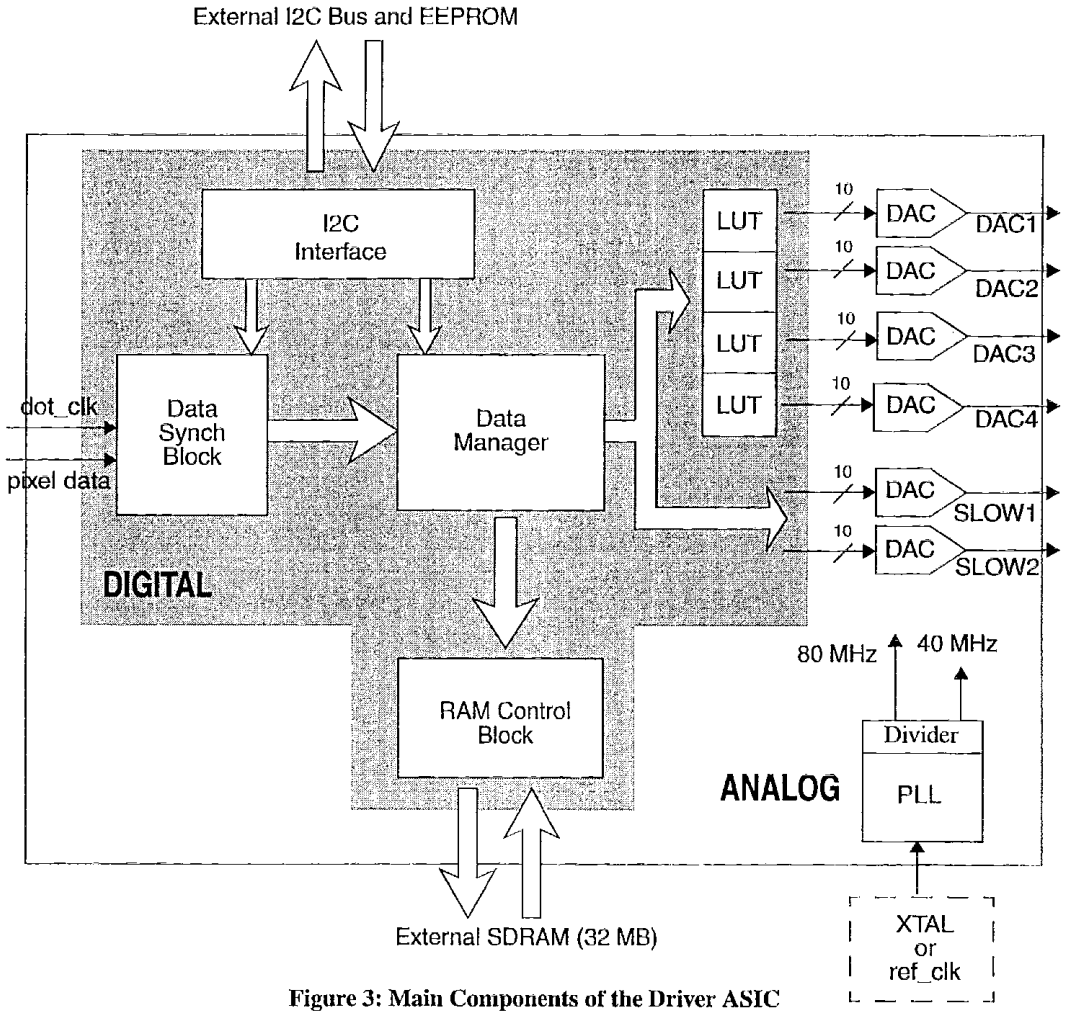

Figure 3: Main Components of the Driver ASIC

The solution chosen was to avoid a full toplevel simulation and use a two-step approach. The first step was to verify the functionality of the digital sections and their interfaces. The digital section had the most variety of function and hence the fastest simulation techniques available needed to be used, i.e. pure digital behavioural event driven simulations. To this end behavioural verilog was used to develop models for each of the analog components and off-chip components. Appropriate analog behaviour was modelled using first order approximations, digital gate and path delays were available from layout. Using this approach allowed a wide range of tests to be performed. The second stage of the top-level verification was to generate a minimal verilog model of the digital blocks. This model was sufficient to exercise the analog sections in a reasonable manner. Using spice-verilog it was then possible to examine the behaviour of the analog section under realistic conditions.

Using this two-step approach, the digital and analog sections were tested independently yet their common interfaces were tested twice, ensuring confidence in the integrity of the design.

5.0 Results

A flexible multi-mode video driver for a microdisplay was developed and brought to tape-out in a timely manner through the use of analog intellectual-property and efficient simulation techniques. First silicon has been returned functional. The digital section has been tested successfully on full SXGA frames at 80 MHz with an output sample rate of 160 MSamples/second. The DACs were measured with an INL of approximately 0.5 LSBs and a DNL of 0.3 LSBs, with interchannel matching better than 1.5%.

Acknowledgements

The authors wish to acknowledge the design team: Roger Maher, Mark Jacob, Frank Kavanagh, Ronan Farrell, David Farrell, Mary Downes, Dave Matthews, Andrea Deering and Tom Collins. This work was completed in collaboration with Three-Five Systems, whose help throughout the project was much appreciated.

Table 1: Device Characteristics

Process	0.25 µm CMOS
Active Area	33 mm^2
Power Supply	3.3 V
Frequency	80 MHz
Power Consumption	<500 mW
DAC linearity (meas)	0.5 LSBs

Figure 4: Die Layout