Wideband 0.18μm CMOS VCO Using Active Inductor with Negative Resistance

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Abstract— This paper presents a wideband voltage controlled oscillator topology based on an active inductor generating negative resistance. The proposed architecture covers a frequency band between 1.325 GHz − 2.15 GHz with average in-band phase noise of −86 dBc/Hz at 1 MHz offset from the carrier frequency. Power consumption of the oscillator core is 28 mW from a 1.8 V supply. The circuit has been simulated in Eldo RF (Design Architect IC, Mentor Graphics) using UMC 0.18 μm 1P6M Salicide RF CMOS model libraries.

I. INTRODUCTION

In recent years, the design of voltage controlled oscillators has become the subject of extensive research. Due to increasing demands for reconfigurable communication systems such as software defined radio (SDR), new wideband VCO architectures are required. Existing CMOS LC VCO topologies, despite their popularity, suffer from a relatively narrow tuning range, the use of nonlinear varactors, a relatively large die area and low Q factor values.

Among many existing methods, oscillator tuning range may be maximized using active inductors (gyrators) in place of passive counterparts [2]–[7]. In addition, as no bulky spiral inductors are employed, the overall required die area is reduced. Further size reduction may be achieved if negative resistance is generated by the same gyrator circuit, eliminating the requirement for an additional energy restorer. This approach, previously proposed in GaAs MESFET technology [3] has not been extensively explored in CMOS technology as yet.

The paper presents a new, small signal model of a CMOS active inductor, showing that for certain conditions a negative resistance generation is possible. In comparison with simulation results, the proposed inductor model is very accurate, achieving an average mismatch less than 10% for all considered parameter values. Based on this, a novel, wideband voltage controlled oscillator architecture is proposed and results from a circuit simulation are presented.

II. ACTIVE INDUCTOR WITH NEGATIVE RESISTANCE

A simple grounded active inductor with resistive feedback [1], [2], [5] is shown on Fig. 1. The feedback resistance R_f increases Q factor of the presented topology [1] and sets the inductance value [2] . All previously published CMOS oscillators utilizing this type of gyrator, employ an additional energy restorer to cancel resonant tank losses. Under certain conditions, however, the presented gyrator introduces a negative resistance at the input. In this section, the new, small signal model of the active inductor is proposed (Fig. 2), giving a practical insight into the negative resistance generation mechanism.

In order to simplify the small signal analysis, the bulk and corresponding source leads are connected and both transistors are considered to be the same. Thus small signal model parameters are equal: $C_{in1} = C_{in2} = C_{in}$, $C_{out1} = C_{out2} = C_{out}$ and
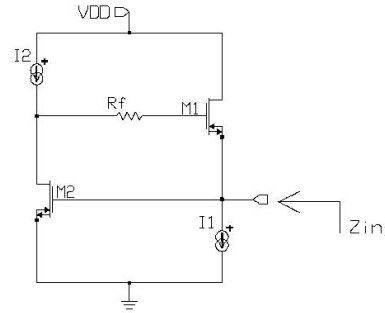

Fig. 1.   Simple grounded active inductor with resistive feedback.

$C_{gd1} = C_{gd2} = C_{gd}$. Both C_{in} and C_{out} represent an approximation of a more complex capacitance structure in four terminal transistor model. The rest of the parameters are typical MOS components: gate to drain capacitances, output conductances g_{out1}, g_{out2} and transconductances g_{m1}, g_{m2}. Both transistors are biased using ideal current sources.

Implementing a node voltage analysis using the above assumptions, the input impedance $Z_{in}(s)$ of the circuit from Fig.2, can be derived as:

$$Z_{in}(s) = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (1)$$

where all coefficients a_n and b_m are given in Table I.
Substituting $s = j\omega$ in (1) and grouping terms:

$$Z_{in}(j\omega) = \frac{a_0 - a_2\omega^2 + ja_1\omega}{b_0 + b_2\omega^2 + j(b_1\omega - b_3\omega^3)} \quad (2)$$

$$= \mathrm{Re}(Z_{in}) + j\mathrm{Im}(Z_{in}) \quad (3)$$

where:

$$\mathrm{Re}(Z_{in}) = \frac{(a_0 - a_2\omega^2)(b_0 - b_2\omega^2) + a_1\omega(b_1\omega - b_3\omega^3)}{(b_0 - b_2\omega^2)^2 + (b_1\omega - b_3\omega^3)^2} \quad (4)$$

and

$$\mathrm{Im}(Z_{in}) = \frac{a_1\omega(b_0 - b_2\omega^2) - (a_0 - a_2\omega^2)(b_1\omega - b_3\omega^3)}{(b_0 - b_2\omega^2)^2 + (b_1\omega - b_3\omega^3)^2} \quad (5)$$

If (4) and (5) satisfy following inequalities:

$$\mathrm{Re}(Z_{in}) < 0 \qquad \text{and} \qquad \mathrm{Im}(Z_{in}) > 0 \quad (6)$$

the input impedance of a gyrator becomes equivalent to a negative resistance and an inductive reactance connected in series. For a given transistor size, equations (4) and (5) are both functions of the feedback resistance R_f, the signal frequency and the biasing
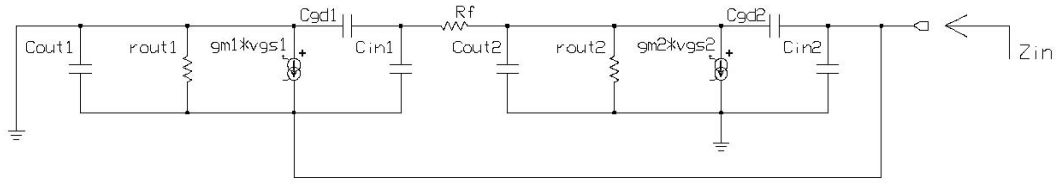
Fig. 2. Proposed small signal model.

a_2	$R_f \left(C_{gd}+C_{in}\right)\left(C_{gd}+C_{out}\right)$
a_1	$R_f g_{out1}\left(C_{gd}+C_{in}\right)+2C_{gd}+C_{in}+C_{out}$
a_0	g_{out1}
b_3	$R_f\left[2C_{gd}^2\left(C_{in}+C_{out}\right)+C_{in}^2\left(C_{gd}+C_{out}\right)+\right.$ $\left.+C_{out}^2\left(C_{gd}+C_{in}\right)+4C_{gd}C_{in}C_{out}\right]$
b_2	$R_f\left[C_{gd}\left(g_{m1}\left(C_{gd}+C_{in}\right)+g_{m2}\left(C_{gd}+C_{out}\right)\right)+\right.$ $+g_{out1}\left(C_{gd}C_{in}+\left(C_{gd}+C_{in}\right)\left(C_{gd}+C_{in}+C_{out}\right)\right)+$ $\left.+g_{out2}\left(C_{gd}+C_{in}\right)\left(C_{gd}+C_{out}\right)\right]+$ $+3\left(C_{gd}C_{in}+C_{in}C_{out}+C_{gd}C_{out}\right)+$ $+C_{gd}^2+C_{in}^2+C_{out}^2$
b_1	$R_f g_{out1}\left[g_{out2}\left(C_{gd}+C_{in}\right)+g_{m2}C_{gd}\right]+$ $+g_{m1}\left(C_{gd}+C_{in}\right)+g_{m2}\left(C_{gd}+C_{out}\right)+$ $+g_{out1}\left(C_{gd}+2C_{in}+C_{out}\right)$ $+g_{out2}\left(2C_{gd}+C_{in}+C_{out}\right)$
b_0	$g_{out1}g_{out2}+g_{m1}g_{m2}+g_{out1}g_{m2}$

Fig. 3. Input resistance as a function of R_f and frequency.

Fig. 4. Input reactance as a function of R_f and frequency.

conditions. The following analysis of the small signal model shows that requirement (6) can be fullfilled over a relatively wide band of frequencies.

III. MODEL ANALYSIS

For the frequency analysis two different cases have been considered: a changing value of the feedback resistor R_f and varying bias conditions of the one of transistors.

In the first case, transistors have been biased with the same current value, equalizing the following model parameters: $g_{m1}=g_{m2}=g_m$ and $g_{out1}=g_{out2}=g_{out}$. The feedback resistance R_f and frequency values have been swept between 1 kΩ – 10 kΩ and 0.5 GHz – 5 GHz respectively. Based on this, Fig. 3 and Fig. 4 present the calculated input resistance and reactance in comparison with the simulation results from Eldo RF. It can be seen that for a given W/L and g_m, negative resistance and inductive reactance have been generated within a wide frequency band, for all considered R_f values. For instance, for $R_f = 4$ kΩ negative resistance is observed between 1.3 GHz and 4 GHz but in the same time inductive reactance is present between 1 GHz and 3 GHz. Thus, the practical
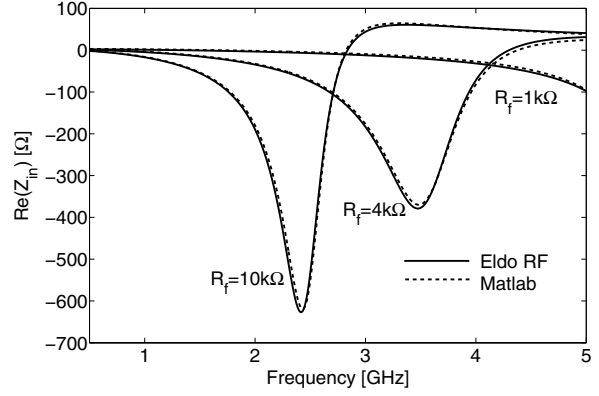
range of signal frequencies is limited only to 1.3 GHz – 3 GHz. For higher frequencies, the inductor reaches its self resonance frequency (inversely proportional to R_f value [2]). Because of the relatively large R_f values necessary to obtain negative resistance (in this case, a few times larger than the output resistance of MOS transistor), the inductor tuning method presented in [2] may be difficult to implement in practice.

In the second case, for constant R_f and biasing current of M_2, the drain current of M_1 is varied and corresponding NMOS conductances are no longer equal i.e.: $g_{m1}\neq g_{m2}$, $g_{out1}\neq g_{out2}$. Fig. 5 and Fig. 6 show input resistance and reactance respectively, for $R_f = 4$ kΩ. All curves have been calculated and measured for three different values of M_1 drain current I_{D1}: 1.4 mA, 1.9 mA and 2.4 mA. It is shown that for constant W/L, R_f and M_2 drain current, inductor impedance is adjusted by I_{D1}. The negative resistance is still available at the input, as long as requirement (6) is fulfilled for the given R_f value. In both cases the obtainable series negative resistance values are very high (100 Ω – 600 Ω, peak) and sufficient to cancel any resonant
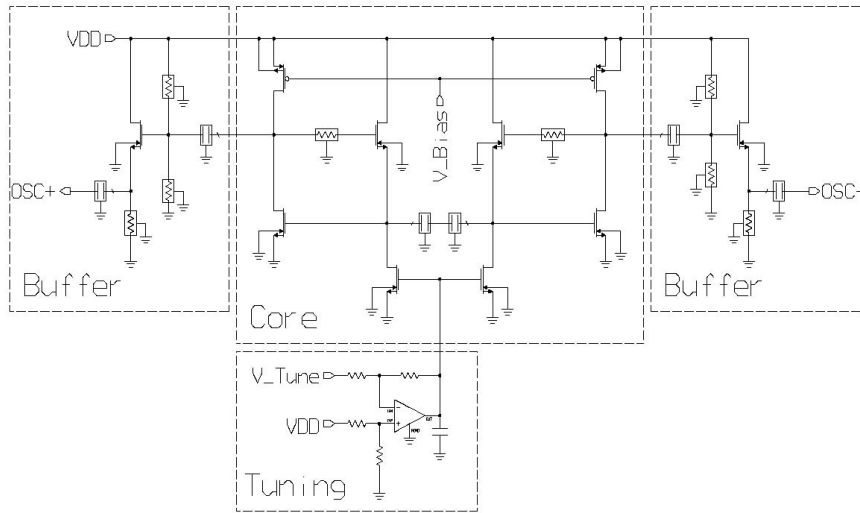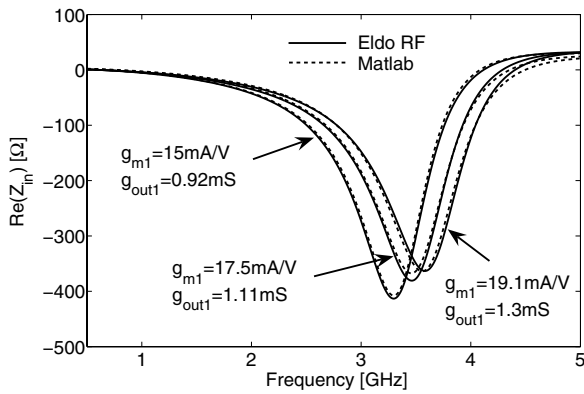
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Fig. 7.   Proposed VCO architecture.

Fig. 5.   Input resistance as a function of g_{m1}, g_{out1} and frequency.
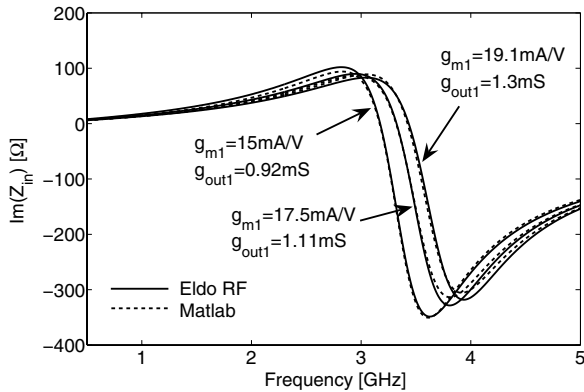

Fig. 6.   Input reactance as a function of g_{m1}, g_{out1} and frequency.

tank losses. The observed inductance values (around 3 nH to 12 nH) are also typical for RF oscillators. These features show that a new CMOS VCO architecture, consisting of only an active inductor and a fixed capacitor, is possible.

IV. OSCILLATOR DESIGN

Fig. 7 depicts the proposed VCO topology using an active inductor with negative resistance. A differential architecture has been chosen

due to its ability to minimize even harmonics in the oscillator output signal. The circuit consists of two identical active inductors connected through the tank capacitance. In practice, a single capacitor may be used, however due to a non-reciprocal model, it has been replaced by two identical capacitors connected in series. The signal from the VCO is extracted through source followers which provide a high impedance load to the core. The buffers have been biased separately from the core to ensure a constant quiescent point for both amplifiers, independent of biasing conditions of the tank. Oscillator tuning is achieved by adjusting the gate voltage of both NMOS current sources. Since oscillations have been observed for gate voltages between 520 mV and 900 mV (380 mV span), the presented tuning method results in a very large oscillator gain, $K_{VCO} = 2171$ MHz/V. To minimize gain, a subtracting amplifier has been applied. By adjusting the feedback resistor values and reference voltage, the tuning voltage range can be scaled up from 0 V to 1.8 V ($K_{VCO} = -458.3$ MHz/V, amplifier inversion).

In comparison with the theoretical analysis, nonideal current sources have increased inductance and decreased the self resonance frequency. To overcome this, M_2 transistors have been made larger than M_1 and the feedback resistance R_f value has been reduced. The body effect causes deviations between the results of the small signal analysis and the Eldo RF simulations. However, the circuit behavior and all qualitative results of the theoretical analysis are still valid.

V. SIMULATION RESULTS

This section presents results of VCO circuit simulations, using both Eldo RF steady state analysis of autonomous circuits (SST Oscill) and steady state noise analysis (SST Noise). The following plots depict the oscillator tuning curve (Fig. 8), the estimated output power together with the phase noise level (Fig. 9) and the calculated differential output spectrum (Fig. 10). All presented results have been obtained for a differential load of 50 Ω and $V_{DD} = 1.8$ V. The phase noise level has been estimated at 1 MHz offset from the oscillation frequency. During all simulations, DC power consumption of the oscillator core has not exceeded 28 mW.

A wide frequency band of 825 MHz has been covered with good linearity of the tuning curve (Fig. 8), especially in comparison with other typical varactor-tuned oscillators. Average signal power and phase noise level values of −12 dBm and −86 dBc/Hz (1 MHz offset)

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have been achieved respectively (Fig. 9). In addition, the harmonic balance simulation (carried out for 6 harmonics), shows that the differential output signal consists of odd harmonics only (Fig. 10). Thus, simple filtering may be applied to achieve the wanted spectrum shape. Table II presents comparison between previously published active inductor CMOS VCOs and this design. While presenting a poorer tuning range than other circuits, a typical performance for active inductor oscillators has been achieved without the use of an additional energy restorer.

TABLE II
COMPARISON OF VARIOUS ACTIVE INDUCTOR CMOS VCO

Publication	[4]	[5]	[2]	This work
Technology	$0.35\mu m$ CMOS	$0.25\mu m$ CMOS	$0.18\mu m$ SiCMOS	$0.18\mu m$ CMOS
Frequency [GHz]	$1.1 - 2.1$	$0.8 - 3$	$0.5 - 2$	$1.325 - 2.150$
Tuning range	62.5%	115%	85.7%	47.5%
Phase noise [dBc/Hz]	$-88*$	$-91**$	$-78**$	$-86**$
Output power [dBm]	—	—	-29 to -20	-16 to -9
Additional energy restorer	Yes	Yes	Yes	No

$* - $ at 600kHz frequency offset; $** - $ at 1MHz frequency offset
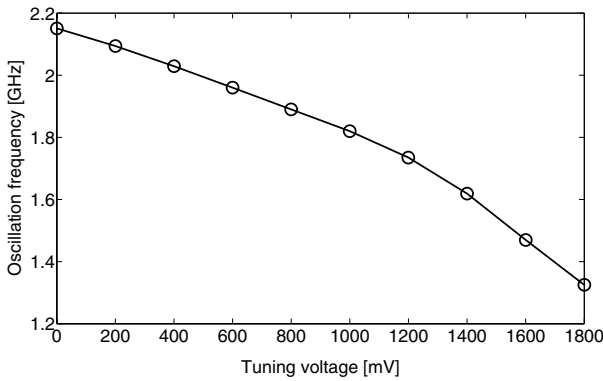

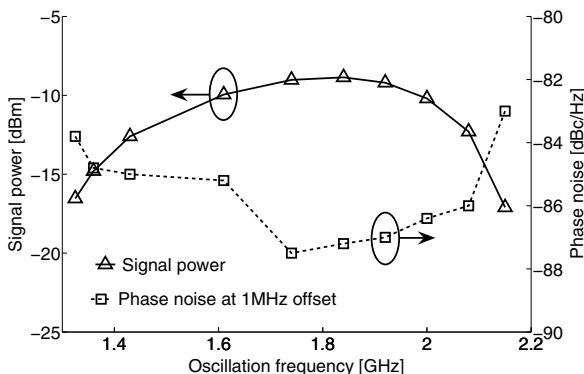Fig. 8. VCO tuning curve.

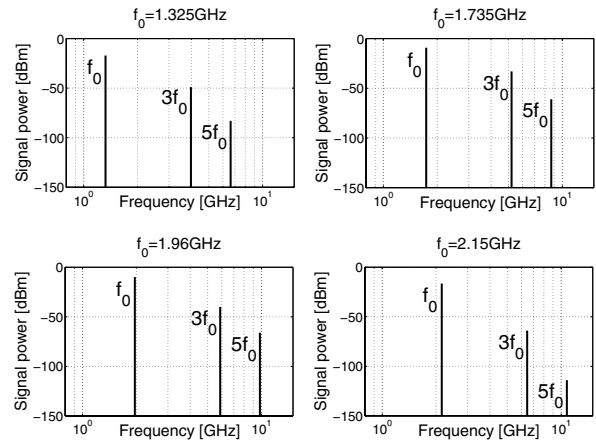Fig. 9. Output power and phase noise.

Fig. 10. Spectrum of the differential output signal.

VI. CONCLUSION

In this paper we have presented a novel CMOS VCO architecture that achieves a wideband performance without the use of an additional energy restorer. A highly accurate small signal model of the active inductor has been proposed, providing a practical insight into the negative resistance generation mechanism in a simple CMOS gyrator. While the overall performance has yet to achieve that required for existing wireless telecommunication systems, this new architecture offers a novel approach for subsequent development.

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