# An Efficient Parallel Structure for ΣΔ Modulators for use in High Speed Switching Power Amplifiers

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***Abstract: Switching amplifiers using Sigma-delta modulators have proven to be highly efficient but require high switching speeds. Implementing complete digital systems at the switching speed has prevented their use in higher speed applications. In this paper we propose a methodology for the parallelisation of sigma-delta modulators allowing for the partition of the switching amplifier into a low-speed and high speed sections. This will enable switching amplifiers to be used effectively at higher frequencies, and specifically for wireless applications.***

## I. INTRODUCTION

Switching amplifiers operate by taking a binary digital signal and using this to control a power switch. If the switching is sufficiently fast, it is possible to gain a highly accurate representation of the original signal while the noise is distributed over a wide bandwidth. As a switched system, these amplifiers theoretically have perfect efficiency and, in practice, efficiencies of 85-90% have been demonstrated [1]. These systems have been used for many years in dc voltage conversion applications, such as switched-mode power supplies. In recent years they have been increasingly used for higher frequency applications where energy efficiency is important [2,3], such as embedded-medical and portable consumer electronics.

Switching amplifiers require a stream of on/off signals that represent the desired signal. Historically pulse-width modulated signals have been used. However sigma-delta modulators are now widely used as the spectral characteristics of the pulse-density modulated output offers superior spectral characteristics and requires a lower switching frequency for a given signal bandwidth. Figure 1 shows the architecture of a sigma-delta modulator based switching amplifier. It consists of three main components, a sigma-delta modulator that takes a high resolution narrow-bandwidth signal and converts it into a high speed low-resolution 1-bit signal. This high-speed bitstream faithfully replicates the spectral characteristics of the input signal within the band of frequencies of interest, but has transferred much of the quantisation noise outside of the band of interest where it can be easily removed by filtering. The switch, or a 1-bit digital-to-analog converter, converts the digital bits to a switched analog signal, which is then filtered to retrieve the final signal. The output power of this device depends solely on the switching stage. There is an optional feedback path from the output of the switch to the input of the modulator whereby information about the performance of the switching stage can be used to pre-distort the input signal. This guarantees a high level of linearity in the output signal.

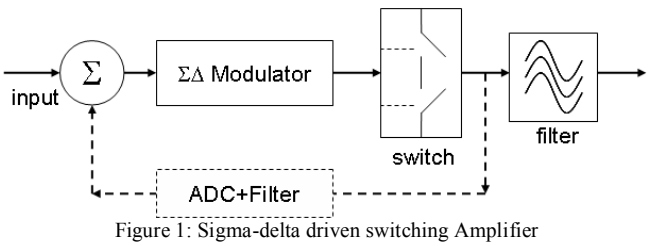


Figure 1: Sigma-delta driven switching Amplifier

Sigma-delta modulators come in many flavours but can be broadly characterised according to their signal transfer functions [5]. The most common type, low-pass systems, has a low-pass signal transfer function and where quantisation noise is removed from the passband to the higher frequencies (as shown in Figure 2a). To ensure minimal noise in the signal band, a high oversampling ratio is normally required. A factor of 16 or greater is normally used, and up to 1024 in very high resolution systems [6]. Bandpass systems have a signal passband at some non-zero frequency and the there is a co-incident notch in the noise transfer function (Figure 2b). For implementation reasons, the most common choice of passband frequency is that of one quarter that of the switching frequency, implying a fast

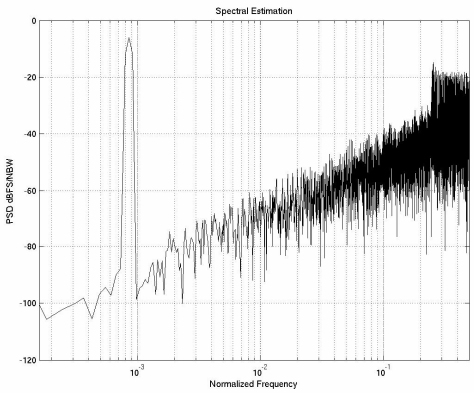


Figure 2a: Spectral output of a lowpass ΣΔ modulators

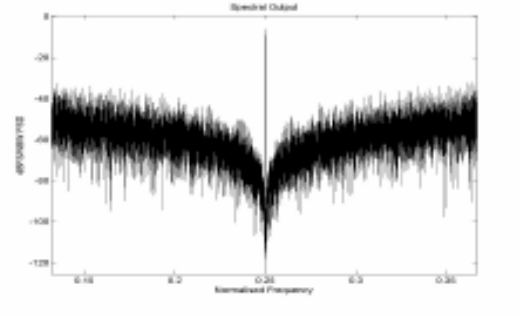

Figure 2b: Spectral output of a bandpass ΣΔ modulators

switching frequency for typical wireless applications. Where sigma-modulators are used in switching amplifiers, low-pass systems are commonly called Class-D amplifiers and Class-S refers to amplifiers with a bandpass signal transfer characteristic [3, 4].

Common to both architectures is the need for a high switching frequency. A high switching frequency implies that the full modulator must operate at this high frequency, even though the input signal may be of much lower bandwidth. While single switching stages can be designed to operate at the frequencies exceeding 10 GHz [7], implementing complex modulators at these frequencies is difficult. To date, these implementation challenges have made achieving practical higher frequency switching amplifiers difficult to achieve. If this issue could be resolved, there is significant interest in using these power amplifiers in wireless communications and in video signal drivers. In the following section we propose a new architecture that will enable higher bandwidth switching amplifiers to be achieved by partitioning the amplifier into two stages: a high-speed switch; and a parallelised, low-speed modulator.

## II. PROPOSED ARCHITECTURE

Modern digital systems, whether implemented on an FPGA or in custom IC designs, are inherently suited to parallel operations, provided that there are no iterative or feedback loops. Using this feature, we propose that it is possible to divide the power amplifier into low and high speed sections [8]. The low-speed section will consist of a number of sigma-delta modulators operating in parallel to achieve a time-interleaved output, and where a multi-bit word is passed to the high speed section, as shown in Figure 3.

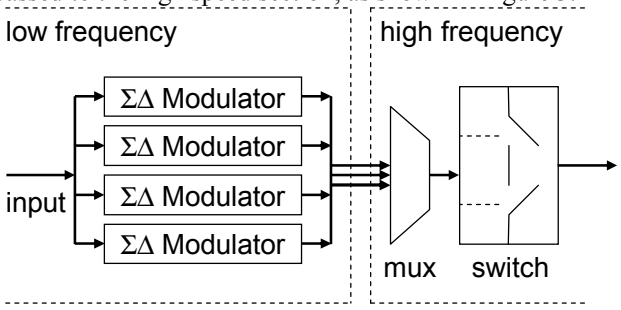

Figure 3: Proposed parallel architecture

The high speed section would consist of a de-multiplexor and a high-speed switch. This section is technically feasible in existing technology. High frequency switching circuits are regularly used in many existing circuits, such as in the digital divider logic of a high frequency phase-lock-loop or that of a SerDes device.

As the sigma-delta modulator outputs are single-bit, a multi-bit word can be simply constructed from the time-interleaved outputs, allowing for a low-frequency signal path to the switching stage (Figure 4). This word can then be subsequently converted to a stream of 1-bit outputs, either through a simple de-multiplexor of a queue structure. If implemented correctly, the parallelised output bitstream will retain the same spectral characteristics as that of a serial bitstream, onced passed through the de-multiplexor.

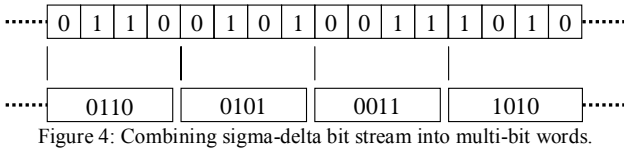

Figure 4: Combining sigma-delta bit stream into multi-bit words.

A common technique in sigma-delta modulators is time-interleaving, and it has been used extensively in analog-to-digital converters to help reduced the individual modulator operating frequency. In these systems however the output of the modulator is entering the digital domain and algorithms convert multiple single-bit outputs into a single high frequency multi-bit signal. For a switching amplifier this is not acceptable as the outputs of the modulators as the final output must remain a 2-level (1-bit) signal so as to drive the switching stage. An alternative approach that can reproduce the appropriate 1-bit outputs for a number of consecutive cycles in required.

Sigma-delta modulators are highly non-linear systems that can produce complex behaviours, ranging from limit cycles, aperiodicity and chaotic behaviour [9]. However all sigma-delta modulators have the characteristic of being deterministic provided the initial conditions and the input values are known, and in the absence of noise. In a digital implementation, all these criteria are known and noise and rounding error issues are avoided. This allows the creation of expressions that provide the future output of the modulator. If the individual bits in the high-speed bitstream are defined as $y_n$, then a 4-channel parallel architecture can be implemented as follows

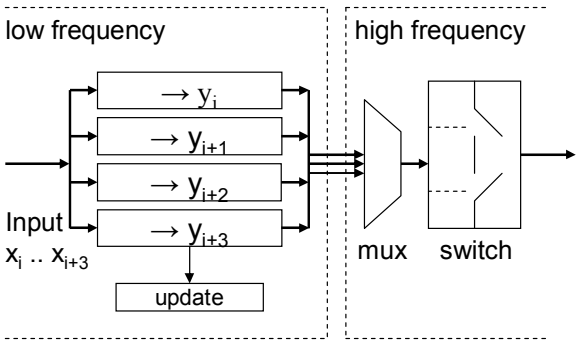

Figure 5: Modified parallel architecture

Using the architecture of Figure 5, each modulator would be provided with the same initial conditions (which are the values of the internal integrators of the modulators) and the next four input values. These input values may be assumed the same where the input is slowly changing, but this is not a requirement. The first modulator constructs the normal output. Subsequent modulators are predicting ahead, using the same initial conditions. Once the outputs have all been calculated, the final state of the internal variables of the most advanced modulator are then used to update all other modulators, thereby advancing them all to the next starting point.

The complexity of the calculations for prediction future outputs gets more complex the further we are required to look ahead. Thus there is a limitation between computational complexity and the number of parallel

modulators that can be used. In addition, the expressions for the future outputs of the modulator can only be implemented efficiently if these outputs can be expressed in closed form, based only on the inputs and the initial conditions.

## III. Predictive Equations for 2nd Order LowPass Sigma-Delta Modulator

While most sigma-delta modulators are implemented with a set of feedback paths, it is possible to develop for many modulator implementations explicit expressions for future output states [10]. To demonstrate the viability of this approach, a set of predictive expressions will be developed for a second-order lowpass sigma-delta modulator. This modulator has been selected for purposes of clarity though the approach taken is applicable to all sigma-delta modulator architectures.

In common with most sigma-delta modulators, the second-order lowpass sigma-delta modulator can be characterised by a set of coupled difference equations:

$$u_n = x_n + u_{n-1} - \mathrm{sgn}(v_{n-1}) \quad (1)$$

$$v_n = u_n + v_{n-1} - \mathrm{sgn}(v_{n-1}) \quad (2)$$

These coupled equations are equivalent to the block diagram shown in Figure 6, where $u$ and $v$ are the values held by two discrete time integrators. The *sgn* function returns the sign of the value, or in 2's complement digital systems, the most significant bit.

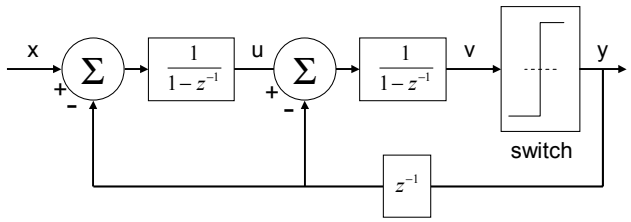


Figure 6: Example of a second order sigma-delta modulator

Taking (1) and (2), it is possible to extrapolate future values of $u$ and $v$ in the following manner [5]:

$$\begin{aligned} u_{n+1} &= x_{n+1} + u_n - \mathrm{sgn}(v_n) \\ &= x_{n+1} + (x_n + u_{n-1} - \mathrm{sgn}(v_{n-1})) - \mathrm{sgn}(v_n) \\ &= (x_{n+1} + x_n) + u_{n-1} - (\mathrm{sgn}(v_{n-1}) + \mathrm{sgn}(v_n)) \end{aligned} \quad (3)$$

and this can be extended to $j$ steps

$$u_{n+j} = \sum_{i=0}^{j} x_{n+i} + u_{n-1} - \sum_{i=0}^{j} \mathrm{sgn}(v_{n+i-1}) \quad (4)$$

This expression requires only the initial value of $u$ and the sequence of sign bits generated by the value of $v$. However the value of $v$, and the resulting sign bits can be directly expressed.

$$\begin{aligned} v_{n+j} &= \sum_{i=0}^{j} u_{n+i} + v_{n-1} - \sum_{i=0}^{j} \mathrm{sgn}(v_{n+i-1}) \\ &= \sum_{k=0}^{j} \left( \sum_{i=0}^{k} x_{n+k} - \sum_{i=0}^{k} \mathrm{sgn}(v_{n+i-1}) \right) \\ &\quad + (j+1) u_{n-1} + v_{n-1} - \sum_{i=0}^{j} \mathrm{sgn}(v_{n+i-1}) \end{aligned} \quad (5)$$

While this coupled expression appears complicated several simplifications may be made. One assumption can be that the input is slowly changing and thus assumed to be constant, which is true when using high oversampling ratios. Another simplification is that many of the terms repeat, and may be used subsequently in many locations. This feature which is repeated many times will enable an efficient implementation to be constructed.

## IV. Example of a Two Parallel ΣΔM System

To illustrate the operation of the predictive equations, a system comprising of two parallel modulators will be explored. This small number has been chosen for clarity. The required outputs for the bitstream are given by the sign-bit of the value of the second integrator ($v$). The expressions for the second integrator can be quickly obtained from (4) and (5).

$$\begin{aligned} v_n &= (x_n) \\ &\quad + (u_{n-1} + v_{n-1}) \\ &\quad - 2\,\mathrm{sgn}(v_{n-1}) \end{aligned} \quad (6)$$

$$\begin{aligned} v_{n+1} &= (x_{n+1} + 2x_n) \\ &\quad + (2u_{n-1} + v_{n-1}) \\ &\quad - (3\,\mathrm{sgn}(v_{n-1})) \\ &\quad - (2\,\mathrm{sgn}(x_n + u_{n-1} + v_{n-1} - 2\,\mathrm{sgn}(v_{n-1}))) \end{aligned} \quad (7)$$

The first-stage integrator values are given by

$$u_n = (x_n) + (u_{n-1}) - \mathrm{sgn}(v_{n-1}) \quad (8)$$

$$\begin{aligned} u_{n+1} &= (x_{n+1} + x_n) \\ &\quad + (u_{n-1}) \\ &\quad - (\mathrm{sgn}(v_{n-1})) \\ &\quad - (\mathrm{sgn}(x_n + u_{n-1} + v_{n-1} - 2\,\mathrm{sgn}(v_{n-1}))) \end{aligned} \quad (9)$$

While this may appear complex, upon investigation the equations collapse into relatively simple implementations. It should be noted that for all sigma-delta modulators it is only necessary to know the initial conditions with which the integrators have been started ($u_{n-1}$ and $v_{n-1}$). In our short-sequence development, these values refer to the values of the integrators at the start of the sequence, and will need to be updated at the start of each new sequence. If $u_{n-1}$ and $v_{n-1}$ are known, then we also know their sign bits. It can also be assumed that both input signal values are known at the start of the sequence, and may in some applications be considered equal. This has not be assumed for this example.

While modern HDL synthesisers are capable of producing an implementation directly from an equation such as given in (6-9), a more efficient approach would be to use a multi-step approach where terms within the larger equation are pre-calculated and subsequently used. This does incur a latency penalty but would ensure high-speed operation as path lengths are kept small. It will also allow significant savings as many terms are repeated, for example ($x_n$+$u_{n-1}$), or ($u_{n-1}$+$v_{n-1}$). As we predict further steps ahead, the value of using multiple-stages to pre-calculate common terms becomes increasingly valuable. A simplistic rule-of-thumb

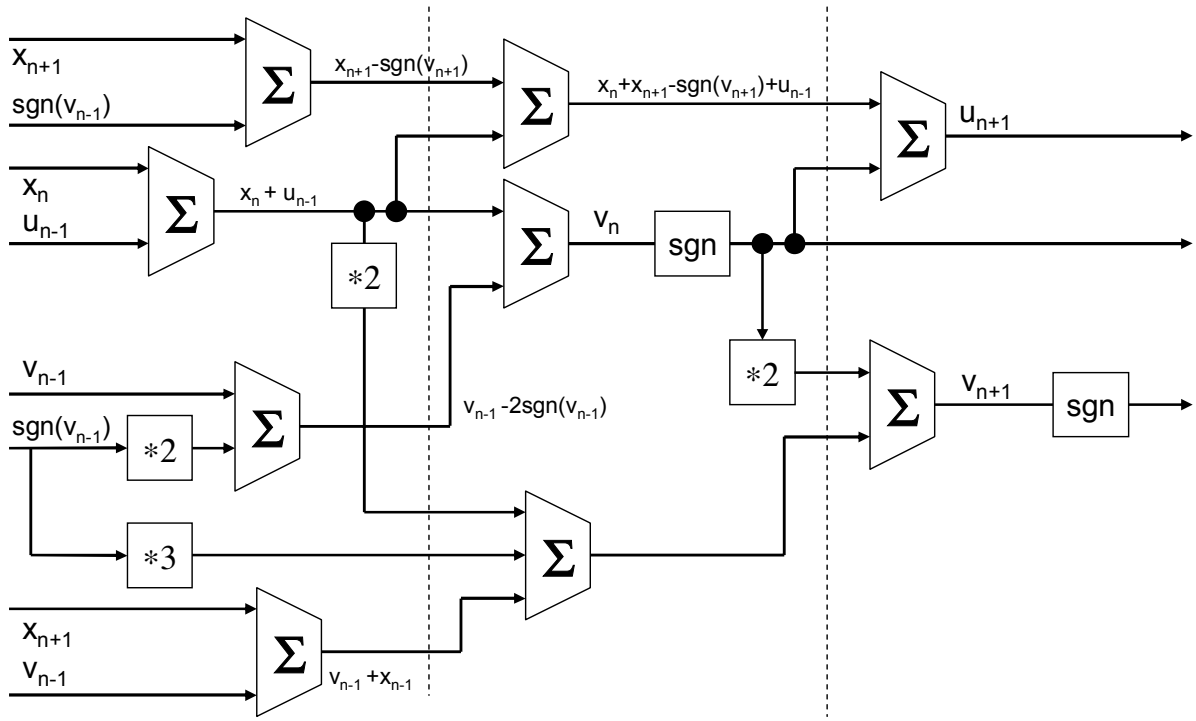


Figure 7: Illustrative Implementation with 3-adders in the forward path

would suggest that an efficient implementation may be achieved when (n+1) stages are used, where n refers to the number of additional bits being predicted (or the number of parallel modulators).

The required outputs for the switching amplifier stage are produced by equations (6) and (7). However at the end of each cycle, the initial conditions, $u_{n-1}$ and $v_{n-1}$, for the start of that cycle need to be updated. The value of $v_{n-1}$ is already known, but it will also be necessary to calculate $u_{n-1}$ separately using equation (9). The intermediate value of $u$ given by (8) is not required and does not need to be calculated.

## V. Example Implementation Architecture

This methodology for predicting the outputs of a sigma-delta modulator is well suited to FPGA or digital-logic implementation, rather than a traditional DSP. Digital logic allows for parallel processing of input signals allowing us to prepare a number of common terms in a single cycle. In the more linear structure of a software programme, true parallel processing is difficult. One criterion for assessing the efficiency and speed of an implementation is to consider the number of adders in the forward path. Figure 7 shows one illustrative structure for an efficient implementation where there are only three adders in the forward path with several of these adders only operating on the sign bit. A more compact structure with less, but larger, adders could be constructed but this could be speed restricted. It can be observed that this approach is less computationally efficient than a normal implementation of a sigma-delta modulator. This can be considered acceptable as the power consumption of additional low-speed adders are small compared to the alternative of running a single modulator at the full speed switching speed.

## VI. Conclusion

In this paper a two-stage partitioned structure for switching amplifiers is presented, using a parallel structure for sigma-delta modulators. This will enable high speed switching amplifiers to be achieved without requiring the modulators to operating at the switching speed. A methodology for developing closed-form equations for the future outputs of a sigma-delta modulator has been provided which are amenable to implementation in digital systems. This approach will enhance the efficiency of high frequency switching amplifiers; allow higher speed operation, and greater integration with existing digital systems.

## VII. References


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