An Efficient Parallel Structure for ΣΔ Modulators for Use in High Speed Switching Power Amplifiers

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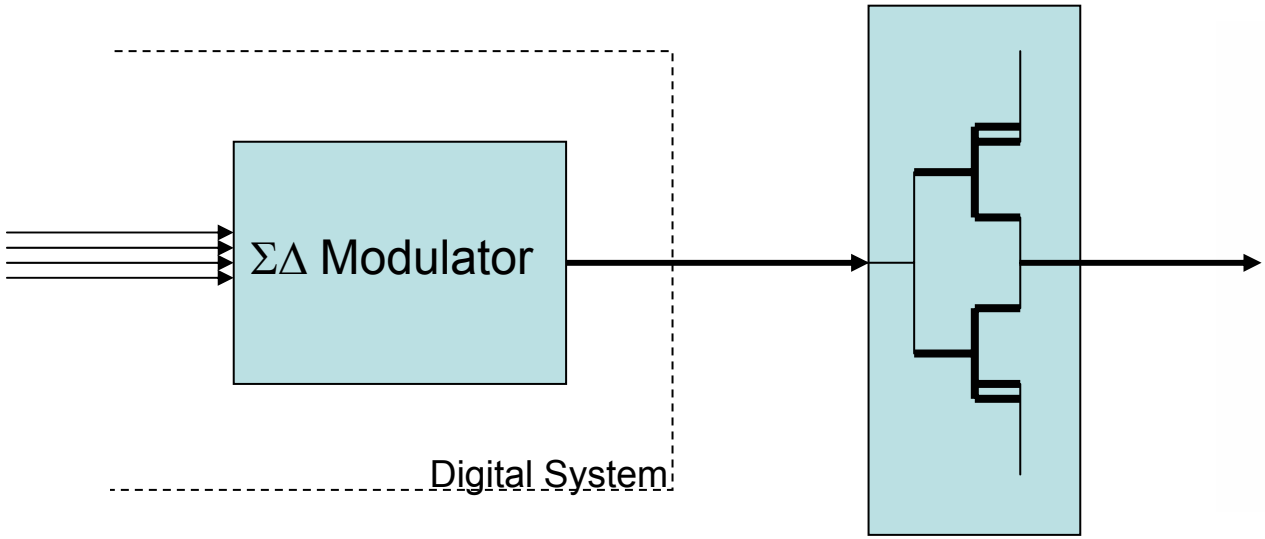
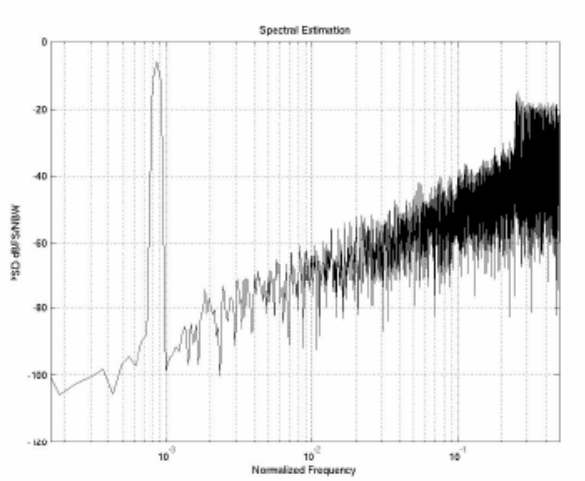
Class D Power-Amp



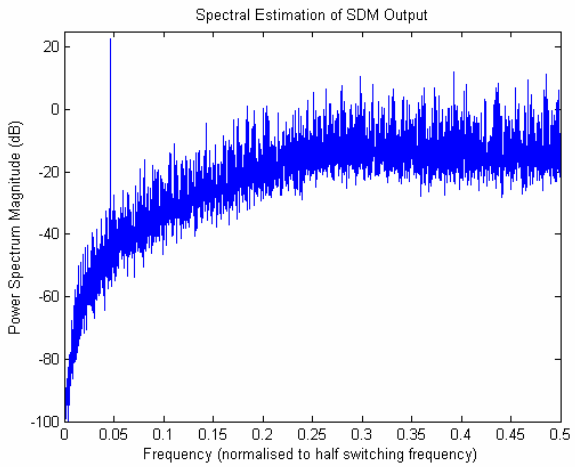


Hi-resolution digital Data → Conversion To single-bit output → Power Switches → Output to be filtered

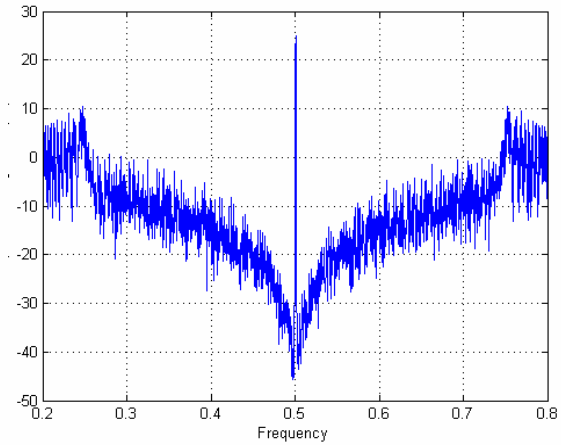
A sigma-delta modulator allows a high resolution narrowband signal to be represented by a wide bandwidth, low resolution signal

If that signal is passed to a suitable switch, then the original high resolution narrowband signal can be generated

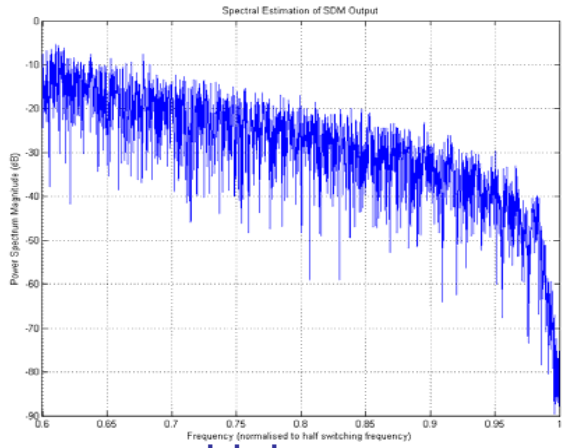
ΣΔ Modulator Flavours



low-pass
(f_{sw}=multiples of f_{in})
(easiest to build)



band-pass
(f_{sw}≈ 4 f_{in})
(harder to build)



high-pass
(f_{sw} ≈ 2 f_{in})
(easier to build)

The rate at which the switch changes is an important design criteria

ΣΔ modulators come in 3 forms, depending on their signal transfer function

In the most common LP case, we switch at a multiple of the input frequency

In the BP/HP cases, the switching frequency is at a fixed multiple (2 or 4).

Benefits and Challenges

Benefits

- Excellent noise-rejection in the signal band
- Ideally perfect linearity
- Ideally 100% efficiency
- Mostly digital, requires very few analog components
- Easily adaptable to different power and signal frequencies

Challenges

- Low Resolution output must have a high bit rate/switching frequency, preventing use in most modern communication schemes

Typical Requirements

Performance demands a high switching frequency. However the switching frequency determines the speed of the digital processors and the speed of the power switch.

Application	Low Pass	Band (High Pass)
AM Radio	16 MHz	4 (2) MHz
FM Radio	1.6 GHz	400 (200) MHz
GSM-400	7.2 GHz	1800 (900) MHz
Analog TV	~8 GHz	2.8 (1.4) GHz
GSM-900	14 GHz	3.6 (1.8) GHz
UMTS/3G	30 GHz	7.6 (3.8) GHz

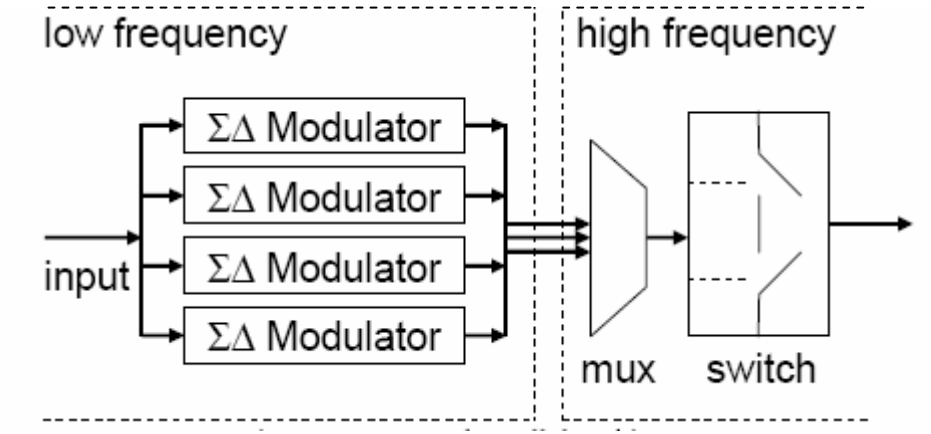
Analog switches can operate at these and higher frequencies
Digital logic becomes very difficult and expensive past 500 MHz

The range of applications could be extended if the digital processing requirements could be relaxed.

Proposal: Parallel Converters

Inspired by SERDES technology, it is possible to construct a specialist switch that converts a multi-bit word into a serial stream of 1/0 bits

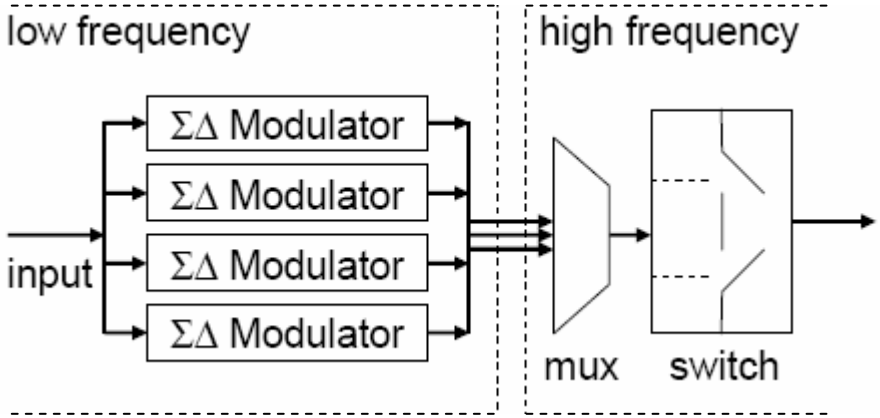
These can then drive the power switch.



The multi-bit word will be produced by a bank of low-speed parallel ΣΔ modulators, and delivered off-chip as a low-frequency parallel data link.

Proposal

STANDARD DIGITAL LOGIC



SERDES INSPIRED CIRCUITS

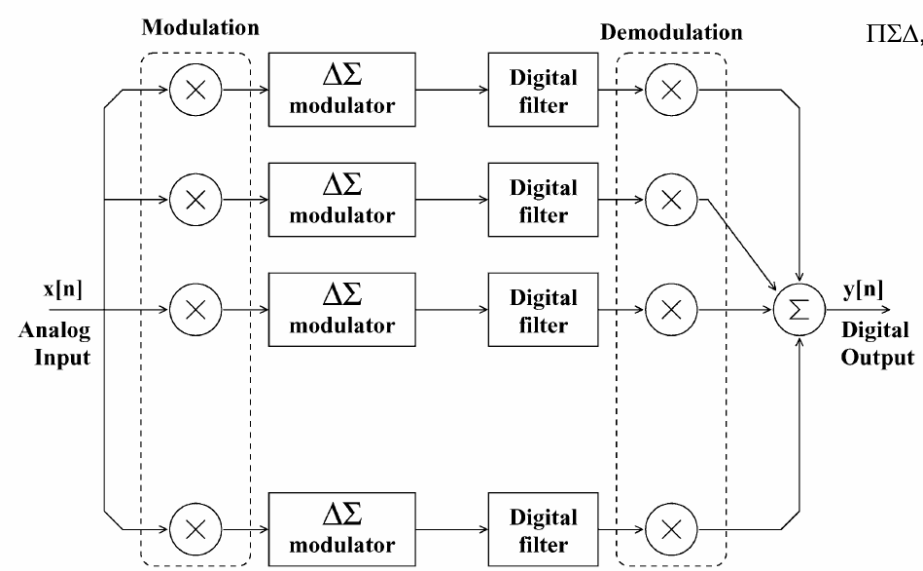
Advantages:

- avails of inherent parallel capability of digital logic
- significant lower-frequency digital systems
- little, and well-known, analog circuit design
- few high-speed noise-sensitive paths

Disadvantages:

- increased digital area

Time-Interleaved ΣΔMs



ΠΣΔ, Fiez, Trans CAS, 2004

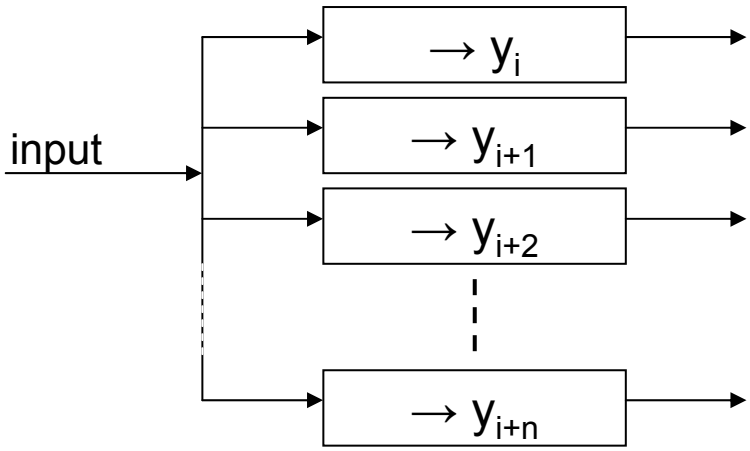
Most existing techniques require digital filtering and addition of outputs

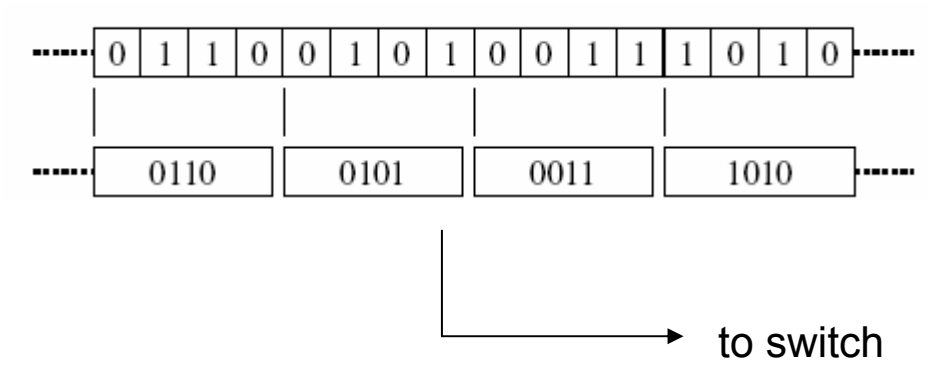
The output is a multi-bit signal.

Well suited for ADC type applications

Unsuitable for our power-switching application

Time-Interleaved ΣΔMs

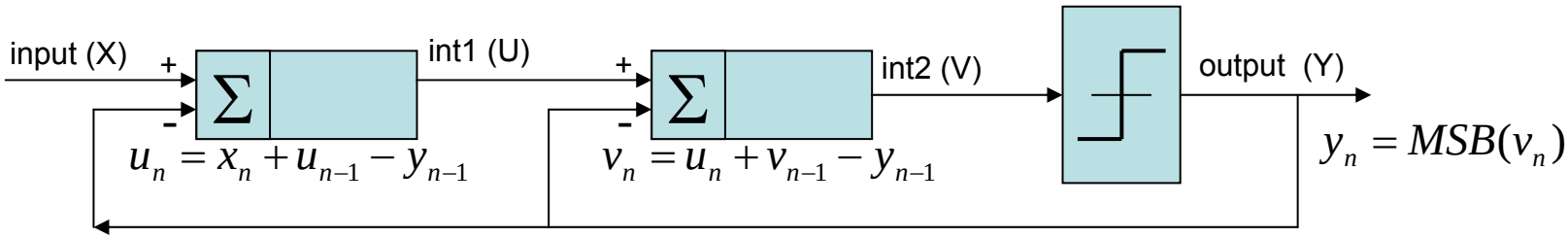


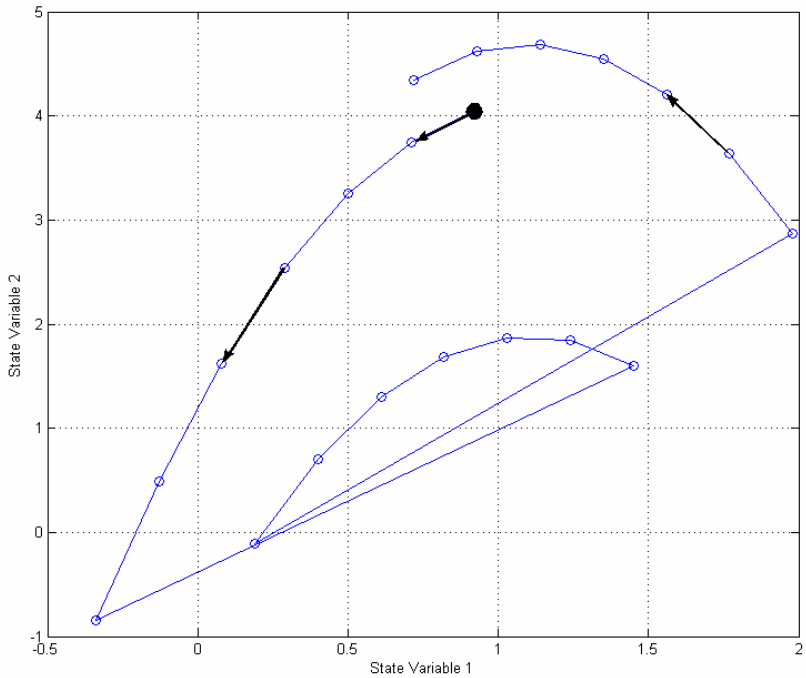


We require a system that

- perfectly produces the next n single-bit outputs concurrently
- has the exact same outputs as if done sequentially
- no change in modulator output signal spectrum

Characteristics of ΣΔM





For all sigma-delta modulators, the behaviour may appear complex

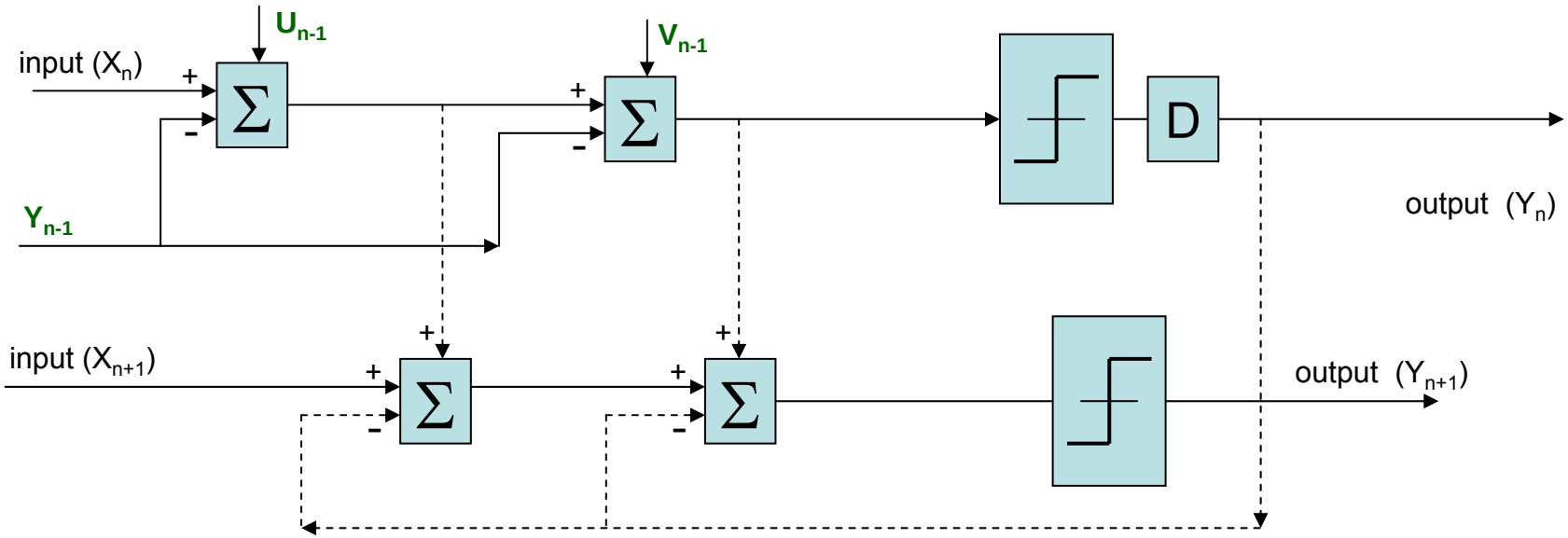
But it is deterministic and all future states can be determined if the

input

initial conditions (u,v)

are known

Future Prediction – Brute Force



We can concatenate modulators to generate the future steps, however

- feedback paths mean that historical calculations must be preserved
- this will mean that additional cycles must be used to calculate future outputs (2 cycles for 1 step look-ahead)
- no speed gain as can only operate at half the clock speed

Future Prediction

Mathematically we can unravel the feedback looks

$$u_n = x_n + u_{n-1} - y_{n-1}$$
$$v_n = u_n + v_{n-1} - y_{n-1}$$

$$u_{n+1} = x_{n+1} + u_n - y_n$$
$$v_{n+1} = u_{n+1} + v_n - y_n$$

this can be fully extrapolated to any number of steps ahead, without recursion

$$\begin{aligned} v_{n+1} &= (u_{n+1}) + (u_n + v_{n-1} - y_{n-1}) - y_n \\ &= (x_{n+1} + u_n - y_n) + (x_n + u_{n-1} - y_{n-1} + v_{n-1} - y_{n-1}) - y_n \\ &= (2x_n + x_{n+1}) + (2u_{n-1} + v_{n-1}) - (2y_n + 3y_{n-1}) \end{aligned}$$

$$y_n = MSB(x_n + u_{n-1} + v_{n-1} - 2y_{n-1})$$

input signals (known)

Initial conditions (known)

Future Prediction

$$v_n = (x_n) + (u_{n-1} + v_{n-1}) - (2y_{n-1})$$

$$v_{n+1} = (2x_n + x_{n+1}) + (2u_{n-1} + v_{n-1}) - (2y_n + 3y_{n-1})$$

$$output = y_n = MSB(v_n)$$

The values of the future outputs can be easily calculated at the cost of some additional adders.

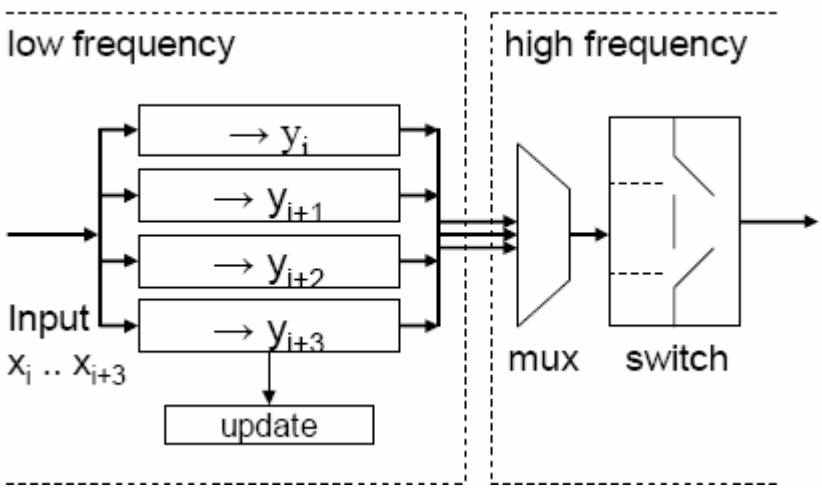
However we can note

- input could be considered to be constant, valid if is changing slowly (narrowband) compared to the switching frequency.

- u_{n-1}, v_{n-1} and y_{n-1} are initial conditions, and thus known in advance

- y_n is a one bit value and thus easily calculated

Characteristics of ΣΔM



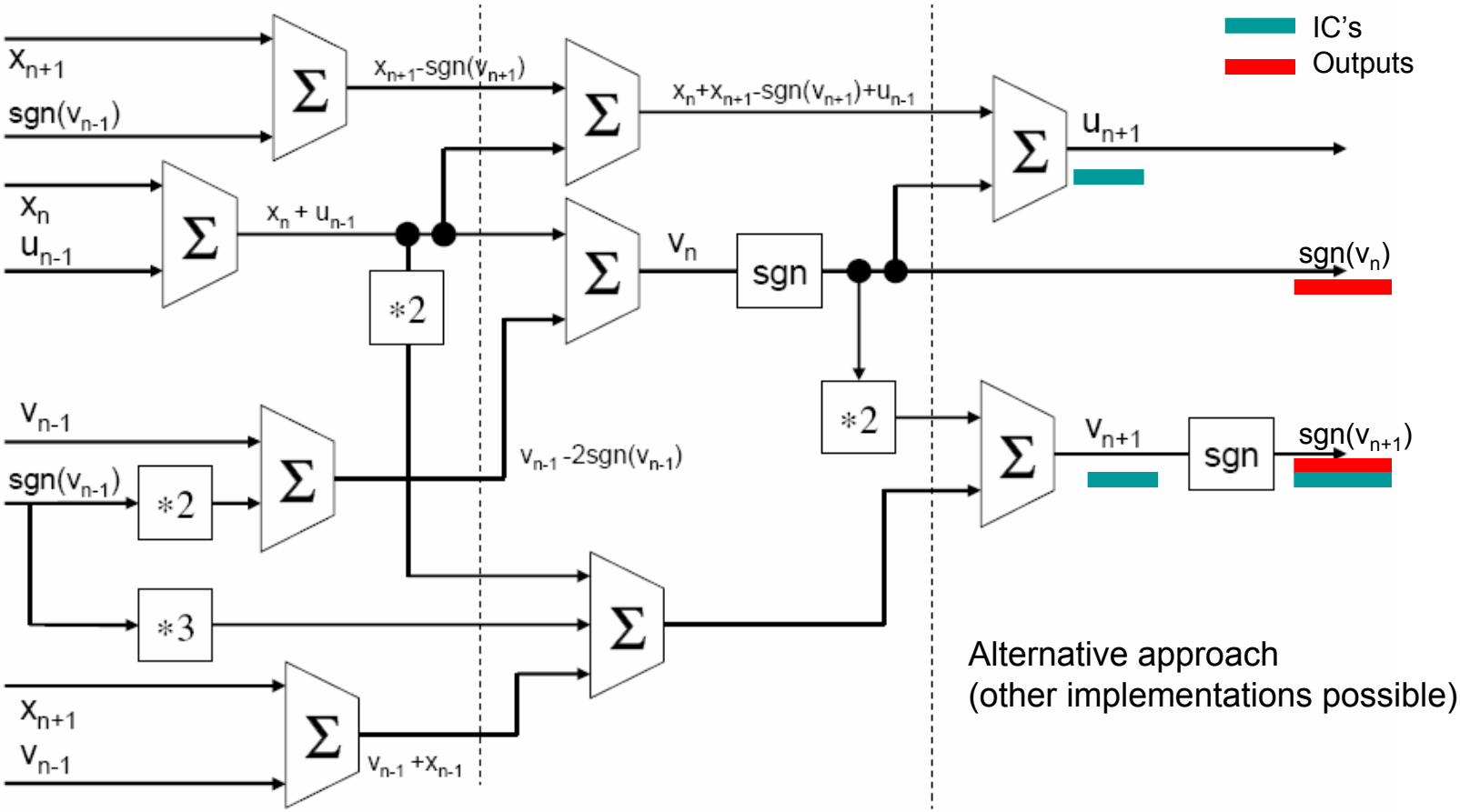
Final implementation could be best implemented as a series of adders, incurring a latency penalty

The most advanced integrator outputs are used as the initial conditions for the next sequence

Repeat the cycle.

Without any feedback paths, no historical calculations need to be preserved, can operate at full clock speed.

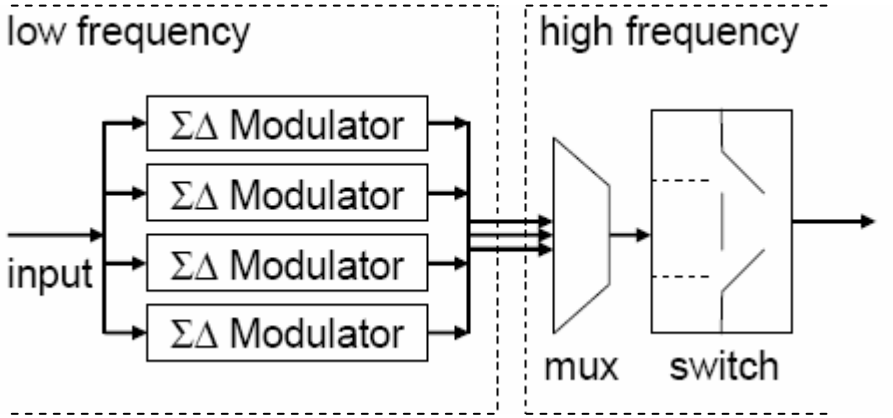
One possible implementation



Increased number of adders (9), similar latency as before

Purely feedforward, allowing for effective throughput enhancement

Conclusions



Effective high-throughput parallelisation of ΣΔ modulators is possible

Demonstrated for lowpass, but can be done for all modulators (BP and HP)

Avoids the issues of high speed digital processing for high speed switching systems, simplifying design challenges.

Enables class-D amplifiers for a wider range of applications.

Questions??

and

Thank you!