A Reconfigurable Platform to drive High Frequency Class S Power Amplifiers using Multi-Gigabit Transceivers

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Abstract

In this research work we present a reconfigurable platform that implements all the digital processing and RF carrier generation for the class S Power Amplifier proposed by the Institute of Microelectronics and Wireless Systems. This amplifier is a combination of a lowpass or bandpass sigma-delta modulation stage in series with a frequency shifting stage and a switch mode amplifier followed by a band pass filter. The reconfigurable platform is parameterizable, scalable and it has been optimized for reconfigurable devices. It takes advantage from the Multi-Gigabit serial links embedded into the new FPGAs to synthesize binary RF signals, and from the parameterizable soft cores that the FPGA vendor provides. The implementation results for a stand-alone and for a tiny Wishbone compatible System-on-Programmable-Chip versions are presented. The design is validated with data measured in the simulation and in the prototype.

1 Introduction

All power amplifiers are inherently nonlinear and traditionally the approach to linear RF power amplification is to back-off the output power of a Power Amplifier (PA) until distortion is reduced to an acceptable level. The process of backing-off the power significantly reduces the output power and efficiency but ensures linearity.

Numerous alternatives for linear power amplification have been proposed with each having various degrees of success. Envelope Elimination and Restoration (EER) is one method used [12]. One problem with this architecture is that intermodulation distortion can arise as a result of the significant difference between the delay in the RF phase path and the envelope magnitude path. Another efficient and linear PA design combines a square wave modulator with a switch mode PA such that the modulator transforms the varying envelope signal into square waves allowing the PA to be driven as a switch. Two different modulators used for this type of PA are RF Pulse-Width Modulator (RF-PWM) [7] and $\Sigma\Delta$ modulator [3]. In general the $\Sigma\Delta$ modulator is preferred since the PWM is not linear in itself and is more likely to require predistortion. As seen in [5], a bandpass $\Sigma\Delta$ modulator can be used directly with the PA. In this case the $\Sigma\Delta$ modulator is clocked at 4 times the RF frequency to modulate the RF signal and drive the PA. Serious design challenges are faced such as feedback in the $\Sigma\Delta$ modulator at 4 times the RF frequency. As a result this technique severely limits the maximum possible carrier frequency. In a polar transmitter a low-pass modulator can be used to switch the drain current on/off. For this implementation the switching rate must be close to the RF frequency, but switching at such high frequencies is difficult because of the large currents and large parasitic capacitances. In summary, either a complex modulator structure is chosen and must be driven at 4 times the RF frequency or alternatively the modulator has a simple structure, but must handle large currents and large parasitic capacitance. In both of these cases the implementation is close to impossible for RF frequencies [9].

In order to avoid these limitations, a novel class S-PA is proposed by the research group of the Institute of Microelectronics and Wireless Systems (IMWS) [8]. It is composed of a combination of a lowpass or bandpass sigma-delta modulation stage in series with a frequency shifting

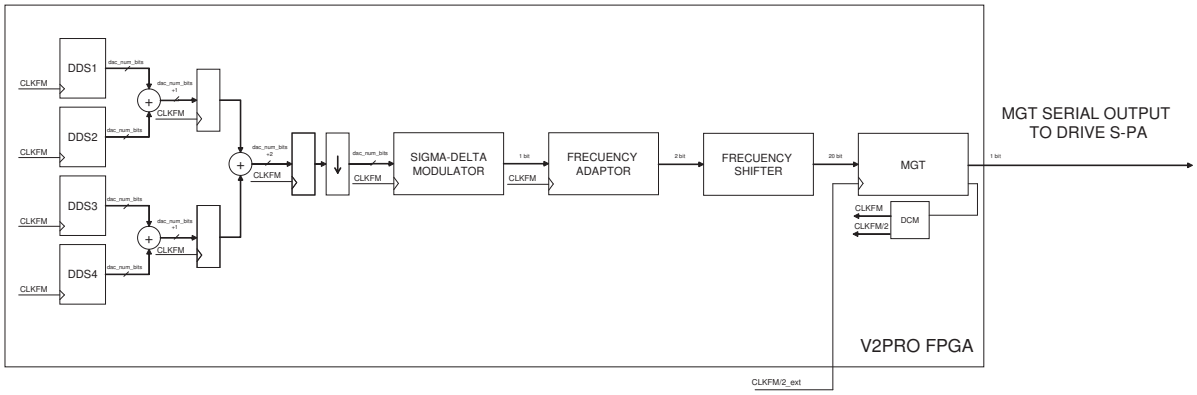

Figure 1. Block diagram of the reconfigurable modulator.

stage and a switch mode amplifier followed by a band pass filter. The principle of operation is similar to the conventional class S-PA, the primary difference between the two is the use of a frequency shifting stage in the proposed amplifier. The frequency shifting stage in the design takes the output of a $\Sigma\Delta$ modulator and shifts the desired signal to the RF carrier frequency using digital mixing. Because of the frequency shifting operation, the $\Sigma\Delta$ modulator can use a sample frequency lower than the final output signal sampling frequency of the power amplifier. This enables the implementation of the modulator on currently available FPGAs. Another possibility made available with the proposed architecture is the option to use a lowpass modulator instead of a bandpass modulator, since it is the frequency shift stage that controls the carrier frequency of the output signal.

Taking into account the level of flexibility needed to experiment and verify this approach, a reconfigurable system is proposed for the prototype. Apart from proving the concept and validating and simulating the theoretical results, the purpose of this prototype is to explore a commercial and low cost solution. In the same field of research, many of the reported approaches are only validated by simulation [3–5]. And if a prototype or a testing method is reported, they are more focused on concept proof: A downscaled frequency prototype based on standard components is used in [9]. In [6] a pattern generator with and external serializer is employed for testing purposes. However, FPGAs are gaining acceptance for prototyping in the RF research field: In [2] a Virtex-4 FPGA is used for the generation of the envelope $\Sigma\Delta$ modulation (EDSM), but not for the RF carrier section. In [17] a Multi-Gigabit transceiver is used for the generation of RF-PWM modulation.

In this paper we present a novel architecture to drive the class S PA proposed by the IMWS. It is parameterizable, scalable and it has been optimized for reconfigurable devices. It generates, modulates, shifts and serializes the signal up to real RF carrier frequencies. It takes advantage of

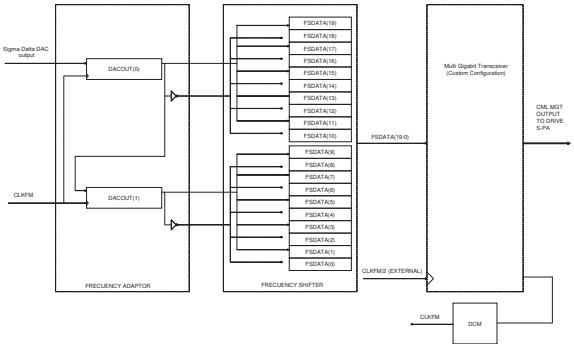

Figure 2. Functional sections of the frequency adaptor and frequency shifter modules.

the Multi-Gigabit serial links embedded into the new FPGAs to synthesize binary RF signals, and from the parameterizable soft cores that the FPGA vendors provide.

The remainder of this paper is organized into four sections. In section 2 the circuit architecture is presented. Section 3 summarizes the implementation results in terms of FPGA resources and maximum achievable frequencies. In Section 4, the results obtained in the HDL Behaviorial simulation are contrasted with the measured data in the prototype. The paper ends in Section 5, with the conclusions and future work in this topic.

2 Architecture description

Figure 1 represents the block diagram of the reconfigurable modulator instantiated for the generation of four fixed tones.

The input signal of $\Sigma\Delta$ modulator is generated by four Direct Digital Synthesizers (DDS). The netlists and the models for these circuits are generated automatically by the

Xilinx Core Generator [14, 15]. The main DDS parameters that can be selected in the compilation stage are: Clock rate, Spurious Free Dynamic Range (from 18 up to 115 dB) and frequency resolution of the output signal. Depending on the selected parameters, the bit width of the output signals changes to achieve the resolution needed. The HDL description of the proposed architecture automatically adjusts the different parameters that depend on that width. For example, the bit width of the $\Sigma\Delta$ modulator.

The outputs of the DDS are mixed in the circuit and the signal additions are pipelined in order to achieve the maximum admissible clock rate for the $\Sigma\Delta$ modulator. The architecture is scalable, so the number of DDS can be easily modified. Although these DDS have multichannel capabilities, for this platform the parallelization is preferred to not limit the frequency and quality of the generated sine wave.

The DDS modules and the $\Sigma\Delta$ modulator run at the same `CLKFM` frequency, that should be as high as possible to enhance the behavior of the $\Sigma\Delta$ modulator for a given signal input frequency. As has been presented in Section 1, the class S PA proposed by IMWS needs a bitstream that runs at the RF carrier frequency. To achieve that goal in the RF Ghz range, the proposed system takes advantage from the RocketIO-MultiGigaBit Transceiver (MGT) hard core [16] embedded into the Virtex-II FPGA families [13].

Although the common application of these MGTs is the high speed digital data communication using standard formats (XAUI, Aurora, Fibre Channel, etc.), in this application the MGT is configured in a custom mode that will act as 20 bit shift register (hard fixed value). This hard core is clocked with a `CLKFM/2` signal. Thus, it multiplies by 10 the frequency of the one bit $\Sigma\Delta$ modulator output.

Figure 2 depicts the modules involved in the frequency shifting and adaptation stage. The `Frequecy adaptor` module takes two bits from the $\Sigma\Delta$ modulator to adapt the data rate to `CLKFM/2` frequency. The output of these flip-flops is interspersed at the input of the MGT with the negated value for each bit pair. When the pattern is serialized by the MGT, the differential Common-Mode-Logic (CML) signal at the output of the MGT is the Gigahertz signal needed to drive the class S PA.

In order to achieve the maximum flexibility and scalability for the proposed platform, an alternative architecture has been designed. Figure 3 summarizes the enhancements that have been added:

- The reconfigurable modulator has been standardized to the Wishbone specification [1] using a Wishbone wrapper. The addition of a standard interface enables seamless integration of the module into the design of more complex SoPC.
- The DDS modules have been generated with programmable frequency and offset capabilities.
- The value of the frequency and offset input for the DDS are written by a Wishbone master module that integrates a soft PicoBlaze microprocessor [1] and a UART. Its software is stored in the internal dedicated memory of the FPGA and the processor is implemented using general purpose FPGA logic. Depending on the software stored, the modulation can be controlled autonomously (for example a fixed pattern) or by commands send by an external host and received through the serial channel.

[1] Wishbone SoC interconnection architecture for portable Intellectual Property cores [10] is a standard specification for data exchange between IP cores. It defines the interfaces, what bus topologies are allowed and signaling. It is absolutely royalty free and is used to share open projects [11]. It provides high levels of robustness and flexibility.

3 Implementation results

Table 1 summarizes the implementation results for '4 tones Stand-alone Implementation' and '4 tones Wishbone SoPC Implementation'. In the first case, a raw four tones modulator has been implemented and in the second case, a Wishbone System-on-Programmable-Chip (SoPC).

For both implementations the configuration of the different modules is as follows:

- 14 bit first order $\Sigma\Delta$ modulator.
- 215 Mhz clock rate for the DDS modules and $\Sigma\Delta$ modulator.
- DDS modules configuration:
  - 14 bits output width.
  - 34 bits frequency data width (32 bits for the '4 tones Wishbone SoPC Implementation')..
  - 34 bits accumulator width (32 bits for the '4 tones Wishbone SoPC Implementation')..
  - 11 bits phase angle width.
  - 80 dB Spurious Free Dynamic Range.
  - 0.024 Frequency Resolution (0.06 for the '4 tones Wishbone SoPC Implementation').
  - The DDS modules generate 4 sine vawes with the following frequencies: 1 Mhz, 1.2 Mhz, 1.4 Mhz and 1.6 Mhz. So the bandwidth for this test is 0.6 Mhz.

The implementation results support the viability of the proposed system to validate and implement the novel class S PA approach of the IMWS. For the '4 tones Stand-alone Implementation' less than the 3% of the FPGA general purpose resources are used, and for the '4 tones Wishbone

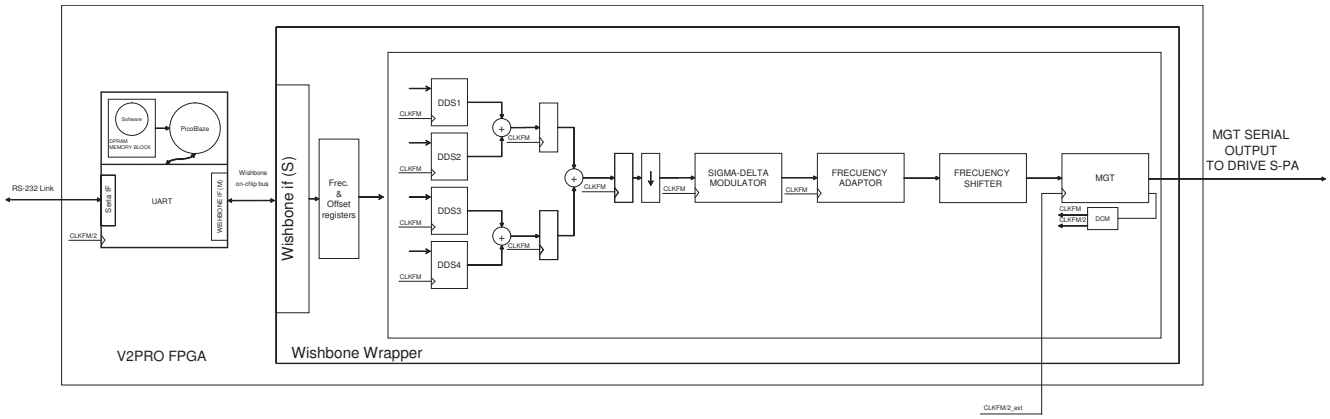

Figure 3. Design standardization and microprocessor addition.

SoPC Implementation' about 6%. Thus, taking into account that the implementation that has been presented is highly optimized and there are lot of resources free, diverse enhancements can be proposed: The replication of the proposed architecture (7 times) to use the remaining 7 MGTs in order to implement a multi-channel transmitter; or, the integration of the Wishbone compatible transmitter in a more complex SoPC.

Compared to other approaches, our prototype is capable of achieving high RF frequencies without frequency downscaling, like in the prototype proposed in [9], or without the use of external components for the frequency shifting stage like it is proposed in [2].

For both implementations that has been reported, the target board is the XUP Virtex-II Pro Development system. The low cost of this board for research groups enables the possibility of having multiple prototypes and future expansions and enhancements of the proposed system.

4 Design Validation

Although the analysis of the class S PA approach of the IMWS group is beyond the scope of this paper, in order to illustrate the functionality of the proposed reconfigurable system some preliminary results are presented.

In conjunction with the prototype based on the XUP board, the whole system allows simulation using Modelsim. The MGT channels are simulated using Synopsis Smartmodel library. The testbenchs capture the input and output at the $\Sigma\Delta$ modulator and the MGT channel in binary files. The FFT representation of those sampled signals is generated using MatLab. All this process has been automated in a 'Virtual Platform' that speeds up the different experiments.

Figure 4(a) shows the output of the $\Sigma\Delta$ modulator for the implemented versions (four tones at 1, 1.2, 1.4 and 1.6 Mhz and a 215 Mhz clock frequency for the DDS and $\Sigma\Delta$ modulator). These representations have been obtained using the 'Virtual Platform'.

The screen-shoot of the Spectrum Analyzer (Figure 4(c)) represents the desired modulation in the RF frequency generated in the MGT channel. Figure 4(b) depicts the simulation results for the same configuration measured in the MGT channel of the prototype.

5 Conclusions

In this paper a novel reconfigurable platform has been presented. It not only fulfills the requirements of the experimental class S PA approach of the IWMS group, but it offers an excellent resources/speed trade-off as well.

The enhanced Wishbone standardized core in conjunction with the tiny microprocessor offers a suitable solution for complex modulators and for SoPCs that are able to drive directly the amplifier circuit.

The proposed platform allows simulation using Modelsim. The 'Virtual Platform' includes the HDL description, models and testbenches needed to analyze all the main signals using MatLab.

The data measurements made on the XUP Virtex-II Pro Development board prove the theoretical approach with a preliminary configuration. Future works includes: the implementation of highest order $\Sigma\Delta$ modulators, the experimentation with other high speed communication channels for low-cost FPGA families and enhancements in the frequency shifting stage.

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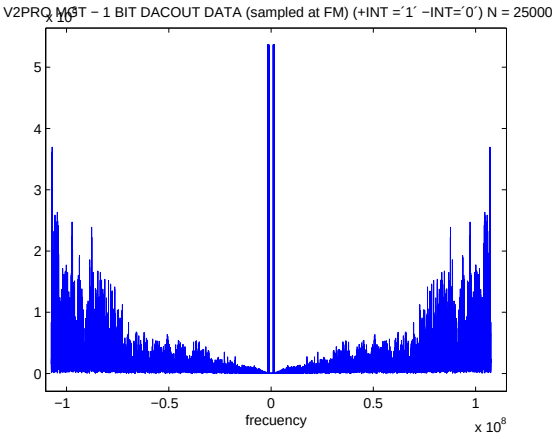
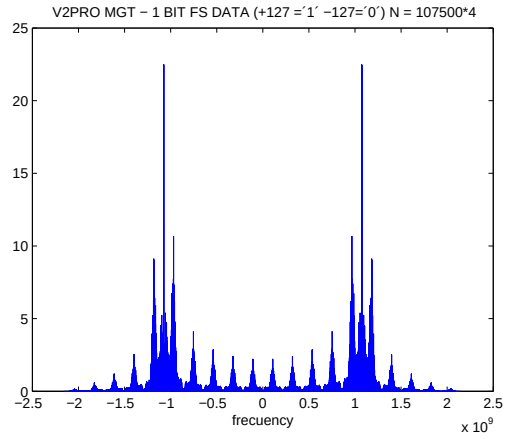
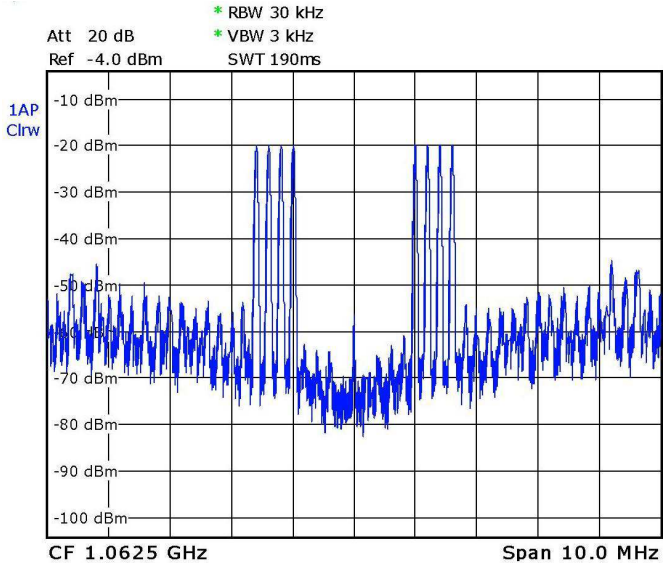


(a) FFT of the signal at the output of the $\Sigma\Delta$ modulator (Virtual Platform).



(b) FFT of the signal at the MGT channel (Virtual platform).



(c) FFT of the signal at the MGT channel (Prototype). RF Frequency 1.0625 GHz. MGT channel at 2.125 Gbps.

Figure 4. FFT of the involved main signals.

Table 1. Class S PA MGT driver Reconfigurable Platforms implementations.

Resources	4 tones Stand-alone Implementation	4 tones Wishbone SoPC Implementation
4 input LUTs	599 (2%)	1.012 (3%)
Slice Flip-Flops	853 (3%)	1.303 (4%)
Virtex-II Slices	520 (2%)	855 (6%)
18K BlockRAMs	4 (2%)	5 (3%)
Digital Clock Managers	1 (12%)	1 (12%)
Multi-Gigabit Transceivers	1 (12%)	1 (12%)
Maximum FM clock	215 MHz	215 MHz
Maximum FS clock (RF frequency)	1.075 GHz	1.075 GHz
Multi-Gigabit Transceiver Data Rate	2.15 Gbps	2.15 Gbps

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