Detection of Coupling Effects in Nanoscale Digital Logic

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Summary

Integrated circuit design is entering an era of truly nanoscale transistors with minimum device geometries now at 32nm and soon to be at 25nm. While actual transistor and logic gate sizes are many times the minimum lengths possible, logic elements are becoming increasingly small and more closely packed together. There is now an increasing possibility of getting coupling errors where nearby logic gates and wires can induce an erroneous response in a logic gate. This has been a significant problem in memory systems for many years where techniques to test for this fault mechanism are well developed. In logic test, there are few methodologies or technologies for detecting this new category of errors.

1 Introduction

Due to the decrease in scaling of integrated circuits, the high switching frequencies and the decreasing voltage signal levels, the impact of logic gates and wires upon their neighbouring components is increasing. Such crosstalk issues can introduce errors or faulty outputs. Such issues have been very common in dense memory structures for many years and similar behaviour has been observed in logic circuits since the early 1990's [1]. With device geometries now approach 25 nm, these coupling errors are likely to become more prominent. Design guidelines can be used to minimise the potential for interference, however due to manufacturing tolerances, or through unexpected design issues, it is possible that occasional logic cells may be vulnerable to these errors. It is therefore important to determine which manufactured chips are vulnerable to these flaws or coupling errors.

There are two categories of techniques that can be use to test chips: functional; or structural testing. Functional testing is based on the premise of testing the operation of the chip. In this way it is possible to ascertain if the function is preserved, however with increasingly complex devices, it has become difficult to capture the full range of possible uses. Structural testing works on the premise of determining if the device has been manufactured. This approach has been proven to be effective and at reasonable cost. Scan testing is the dominant technique and is based on developing chains of flip-flops with intervening combinational logic. By exercising the combinational logic it is possible to ascertain if all devices are working correctly. It is also possible to do this at-speed in order to capture dynamic effects such as delays. This approach cannot detect coupling effects as the choice of combinational logic used is based on the Boolean function rather than their physical proximity to each other. Existing techniques for testing for coupling errors have been functional tests on buses, and thus suffer from lack of scalability to the wider chip design.

2 Proposed Work

We proposed to explore techniques that could be used to expand scan-type test methodologies to detect crosstalk or coupling errors in dense nanometer digital logic. The test methodology must take into account of several key aspects.

- the physical layout of the device must be included in the test selection.
- These faults occur at high switching speeds

The methodology that we propose to follow is to develop a simulation-based model of nanometre digital logic so as to assess the sensitivity of logic gates to coupling errors. With this knowledge we will explore selection criteria for scan chains and assess the excitation patterns that may trigger these events. The objective is to retain compatibility with scan architectures so as to require minimal additional test infrastructure.

Publications

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