A Practical Class S Power Amplifier for High Frequency Transmitters

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Abstract- Digital signal processing (DSP) techniques are being incorporated in the design of modern power amplifiers (PA) and as the speed of DSP advances it is envisioned that DSP will develop to a point where algorithms will provide signals at RF particularly for switching amplifiers. The digital transmitter has many potential benefits such as the absence of aging or tuning problems, reconfigurability, programmability as well as ease of integration and testing. In this paper a new class S RF power amplifier architecture is proposed for use in high frequency transmitters and is not restricted by the requirement for the square wave modulator to have a sampling rate of 4 times the carrier frequency.

I. INTRODUCTION

Radio frequency (RF) power amplifiers (PA) are an important part of wireless transceivers used in a wide range of wireless devices from mobile phones to base stations. In these systems PAs are among the dominant consumers of power. The function they perform is to convert DC power into power at RF frequencies and ideally this is performed efficiently and linearly. However, all power amplifiers are inherently nonlinear and traditionally the approach to linear RF power amplification is to back-off the output power of a PA until distortion is reduced to an acceptable level. The process of backing-off the power significantly reduces the output power and efficiency but ensures linearity.

Numerous alternatives for linear power amplification have been proposed with each having various degrees of success. More recent efforts have focused on the use of polar transmission techniques to enable improvements in power efficiency while still providing linear operation. Envelope elimination and restoration (EER) is one method used, shown in Fig.1.

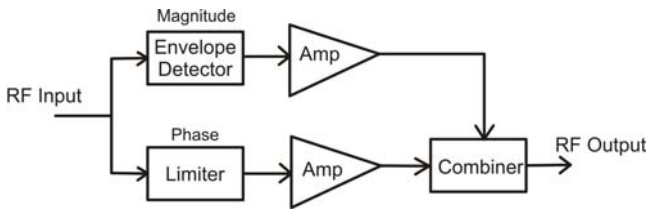


Figure 1. Envelope elimination and restoration architecture

In the case of EER the envelope of the RF input is 'eliminated' by a limiter to generate a constant amplitude phase signal and at the same time an envelope detector extracts the magnitude of the input. The magnitude and phase signals are then amplified separately and recombined to 'restore' the desired RF output. The key advantage of the EER approach is that the RF PA always operates as an efficient switched mode amplifier and the EER architecture as a whole can linearize the switched-mode RF PA without compromising its efficiency. One problem with this architecture is that intermodulation distortion can arise as a result of the significant difference between the delay in the RF phase path and the envelope magnitude path. Also, special care must be exercised in the design of the limiter circuit. A number of other transceiver structures split the RF input signal and subsequently recombine them such as envelope tracking and linear amplification using nonlinear components (LINC). Similar considerations must be taken into account for these designs.

Another efficient and linear PA design combines a square wave modulator with a switch mode PA such that the modulator transforms the varying envelope signal into square waves allowing the PA to be driven as a switch. Two different modulators used for this type of PA are RF pulse-width modulator [1] and ΣΔ modulator [2]. In general the ΣΔ modulator is preferred since the PWM is not linear in itself and is more likely to require predistortion. As seen in [3], a bandpass ΣΔ modulator can be used directly with the PA. In this case the ΣΔ modulator is clocked at 4 times the RF frequency to modulate the RF signal and drive the PA. Serious design challenges are faced such as feedback in the ΣΔ modulator at 4 times the RF frequency. As a result this technique severely limits the maximum possible carrier frequency. In a polar transmitter a low-pass ΣΔ modulator can be used to switch the drain current on/off. For this implementation the switching rate must be close to the RF frequency, but switching at such high frequencies is difficult because of the large currents and large parasitic capacitances. In summary, either a complex ΣΔ modulator structure is chosen and must be driven at 4 times the RF frequency or alternatively the modulator has a simple structure, but must handle large currents and large parasitic capacitance. In both of these cases the implementation is close to impossible for RF frequencies [4].

This paper presents a class S PA with relaxed design requirements for the ΣΔ modulator. This is accomplished by performing a frequency shifting operation between the ΣΔ modulator block and the switch mode PA stage. It is shown that by doing this a sampling rate of only twice the RF frequency can be used. Section II gives a detailed description of the main functional blocks of a typical class S PA. Then in Section III the principle of operation of the new

class S PA is explained. Finally, Sections IV and V present the results and conclusions of this work respectively.

II. The Class S Power Amplifier

A class S power amplifier architecture has previously been developed for audio frequency applications and has more recently advanced into RF and microwave frequencies. Typically a class S PA consists of a square wave modulator, switch mode PA and bandpass filter (BPF), a high level description of one is shown in Fig 2.

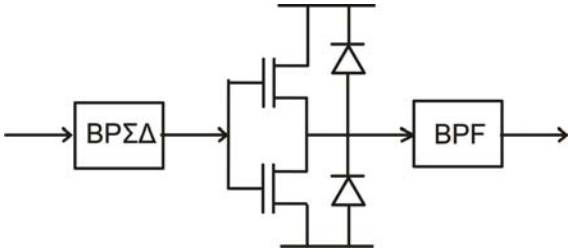


Figure 2: Class S power amplifier

The ΣΔ modulator stage is used to convert a multi-bit input signal into a 1-bit signal. The primary reason for using a ΣΔ modulator is to move the quantization noise outside of the desired signal band. The performance of the ΣΔ modulator depends mainly on two parameters: the order of the modulator and the oversampling ratio (OSR) of the input signal. The order of the ΣΔ modulator is a trade-off between low-in-band quantization noise on one side and high-out-of-band quantization noise, increased implementation complexity and higher possibility for instability on the other. The OSR denotes the ratio of the sampling frequency to two times the input signal bandwidth. In general, increasing the OSR decreases the level of the in-band noise [5].

The ΣΔ modulated 1-bit signal is suitable for use with a switch mode power amplification stage. Switch mode power amplification can provide considerably better power efficiency compared to conventional power amplifier topologies such as class A, B or AB for example. In an ideal case the current-voltage product is zero and 100% efficiency is possible. In reality non-ideal switches mean that this is not possible, however, efficiencies of higher than 90% have been reported at audio frequencies [1].

Since over a narrow bandwidth the bandpass ΣΔ modulator is linear and the switch mode amplifier is linear for a digital signal the filtered output of the PA in theory will be linear.

III. Principle of Operation

Using the class S PA of Fig. 2 the operation of a conventional class S amplifier can be described as follows: An RF signal is converted to a binary signal by means of a bandpass ΣΔ modulator. The modulator is an A/D converter in which the quantization noise is spectrally shaped to lie outside the frequency range containing the desired signal [6]. The binary signal is then fed into a switch mode amplifier and finally the signal is bandpass filtered. For implementation reasons bandpass ΣΔ modulators or their equivalent are required in order to transmit the high frequency signals used in popular wireless applications.

The trouble with this approach is that the sampling rate or clock frequency for the amplifier is set to 4 times the required RF carrier frequency. Modern wireless systems contain large digital cores. Integration of the power amplifier can be made much easier if in the case of a class S PA, the ΣΔ modulator can be implemented using an FPGA or other programmable device and connected directly to the switch mode stage. At RF and microwave frequencies such clock frequencies are prohibitively large cannot be implemented in this way using current FPGA technology.

The RF PA proposed in this paper provides a solution to this integration problem. Our class S PA is described as a combination of a lowpass or bandpass sigma-delta modulation stage in series with a frequency shifting stage and a switch mode amplifier followed by a BPF, as shown in Fig 3. The principle of operation is similar to the conventional class S PA of Fig. 2, the primary difference between the two is the use of a frequency shifting stage in the proposed amplifier.

The frequency shifting stage in the design takes the output of a ΣΔ modulator and shifts the desired signal to the RF carrier frequency using digital mixing. Because of the frequency shifting operation the ΣΔ modulator can use a sample frequency lower than the final output signal sampling frequency of the power amplifier. This enables the implementation of the ΣΔ modulator on currently available FPGAs. Another possibility made available with the proposed architecture is the option to use a lowpass ΣΔ modulator instead of a bandpass ΣΔ modulator, since it is the frequency shift stage that controls the carrier frequency of the output signal.

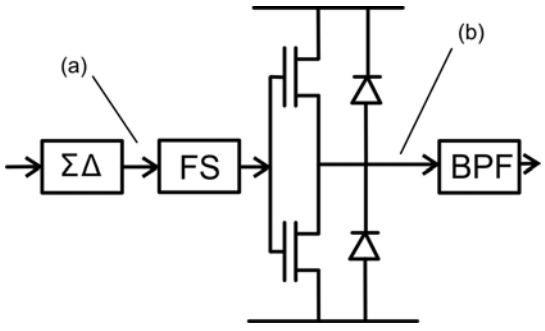
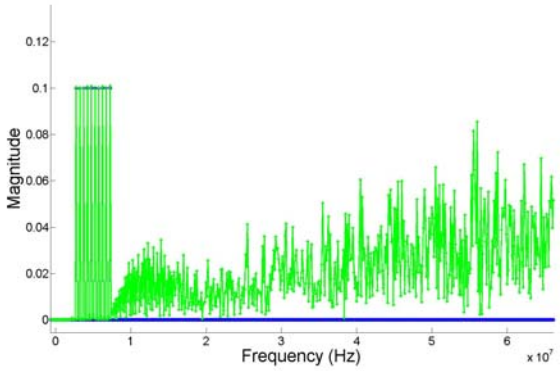


Figure 3: Proposed Class S power amplifier

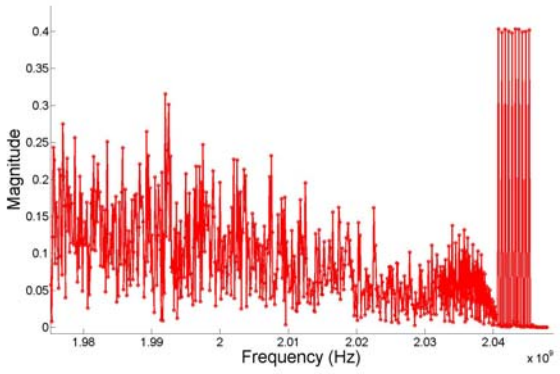
Class S PAs have the potential to offer improvements in efficiency at RF and microwave frequencies compared with current power amplifiers. The area of class S amplifiers is still at a very early stage of development but as the area matures and faster FPGAs and power switching devices become available there is the potential for more widespread use.

IV. Simulation and Results

The proposed class S PA used in this case has a 4th order lowpass ΣΔ modulator followed by a frequency shifting stage. In the system level simulation, the ΣΔ modulator output is then connected to a switch mode high frequency amplifier and finally a bandpass filter.



(a)



(b)

Figure 4. (a) Output signal from ΣΔ modulator (b) Frequency shifted output from high-speed ΣΔ modulator block

As a proof of concept this novel structure was modelled at system level in Simulink using a 4th order lowpass ΣΔ modulator. A sampling frequency of 256MHz was used for the ΣΔ modulator stage. The output of the modulator is shown in Fig. 4(a) and the desired modulated signal with a bandwidth of 5MHz from this stage is subsequently shifted in frequency and centred on a carrier frequency of 2.043 GHz. This high frequency 1-bit signal is used to drive the RF switch mode amplifier stage and the resulting output signal is shown in Fig 4 (b). This signal can finally be filtered to remove the unwanted frequency components.

V. Conclusions

The high frequency switch mode architecture presented here has a theoretical efficiency of 100%. Previously an implementation of a class S PA for high frequency was limited greatly by a requirement for the clock frequency to be 4 times that of the carrier frequency. In this paper a method is proposed to provide approximate bandpass ΣΔ operation, which can be realised with the FPGA technology currently available. For high frequencies, the class S PA is a realistic solution to the problem of achieving high efficiency and linear power amplification.

Acknowledgment

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