On Time-Interleaved Analog-to-Digital Converters for Digital Transceivers

Michael Soudan*, Ronan Farrell†, Ludovic Barrandon‡
Centre for Telecommunications Value Chain Research
Institute of Microelectronics and Wireless Systems
National University of Ireland, Maynooth, Co Kildare, Ireland
Email: *msoudan@eeng.nuim.ie, †rfarrell@eeng.nuim.ie, ‡lbarrandon@eeng.nuim.ie

***Abstract*— This paper presents a transceiver model that comprises two time-interleaved analog-to-digital (A/D) converter systems to sample the inphase and quadrature signals in a digital receiver. Random data is used as the information signal and quadrature modulation is employed as the modulation scheme. A polyphase filter bank is derived as a representation of the time-interleaved A/D converter system, thereby modelling its converter mismatch. Furthermore, filter bank theory is used to design reconstruction filters that mitigate aliasing and distortion and achieve matched filtering in a single post-processing scheme, therefore reducing the digital implementation complexity of the receiver. Simulations results are presented to illustrate the performance degradation due the usage of non-ideal A/D converters and to verify the propose reconstruction scheme. Finally, an analysis of the required synthesis filter complexity is presented for different error magnitudes as a guideline for the filter bank design.**

I. Introduction

A trend in the design of digital communication systems is to minimise the analog components in favour of digital signal processing, as typified by the software-defined radio concept [1]. This requires the analog-to-digital (A/D) converter to move towards the antenna in the receiver chain, demanding ever increasing performance. Though direct analog-to-digital conversion after the antenna would be favorable in terms of receiver flexibility, the required A/D converter performance is far beyond todays state-of-the-art technology [2]. A compromise between the all-digital and the traditional processing can be achieved by using receiver systems such as the low-IF and direct conversion architectures. However the A/D converter is seen as one of the most challenging components for such radio systems demanding high resolution, high sampling rates and low power consumption.

The need for high A/D converter resolution can be demonstrated by examining the sensitivity requirements of receivers, where it is necessary to detect small communication signals in the presence of strong blocking signals and background noise. The A/D converter resolution has to be sufficient to convert a weak signal while the interfering signals occupy the full input range of the A/D converter. A common metric to assess the receiver performance is the symbol error rate (SER) of the system. The second important A/D converter parameter is the minimum sampling rate that is determined by the signal bandwidth [3]. As more broadband wireless services are developed, the requirement for signal bandwidth becomes more and more demanding. The IEEE 802.16e (WiMAX) standard for example, has an option for a 25 MHz channel requiring a sampling rate in excess of 50 MSps [4]. A high resolution A/D converter with this sampling rate is expensive. One promising technique for providing this level of performance is through the use of multiple time-interleaved A/D converters [5]. While time-interleaving enables the designer to improve the overall sampling rate of the system quite easily, a degradation of the spectral purity is caused by the dissimilar characteristics of the individual A/D converters [6]. In particular, gain, offset and timing mismatch between the individual A/D converters causes spurious images of the input signal in the output spectrum of the converter system, thereby degrading its spurious free dynamic range (SFDR). Timing mismatch has attracted a lot of attention in recent years since its compensation has proven to be computationally expensive for wide-band signals [7]. This paper presents the impact of these error mechanisms, their impact on the receiver performance and a digital correction scheme for suppressing these effects. Finally, simulation results are presented to verify the proposed architecture as well as guidelines for the design of the correction system.

II. Time-Interleaved A/D converter

For A/D converters that operate in a time-interleaved manner, the overall sampling rate f_s becomes a multiple of the sampling rate of a single A/D converter f_{AD}, according to the number of employed A/D converters M. The sampling instants t_m of the individual converters, called channels, are controlled by their dedicated clock signals, where $m = [0, 1, .., L]$ indicates the channel index. The digital output of the different channels is serialized in the last stage (see Fig. 1).

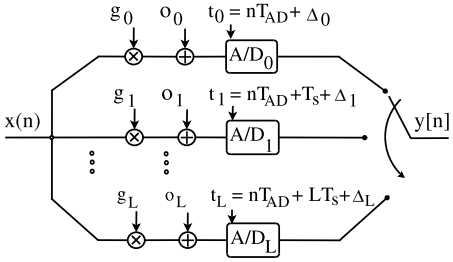

Fig. 1. Time-interleaved A/D converter system.

The non-idealities of individual A/D converters, such as the mismatch of gain g_m, offset o_m and timing Δ_m are static, or slowly changing due to component aging or temperature influence. The gain and offset errors refer to the deviation from the ideal converter transfer characteristic. These mismatch magnitudes are given as the percentage of the full-scale range (%FS) of the A/D converter. The term timing mismatch, however, refers to a constant deviation of the sampling process from the ideal sampling instant. This sampling delay is a combination of clock skew and the individual circuit response time. Typically, the magnitude of timing mismatch is normalised as a percentage of the overall sampling period of the time-interleaved system.

III. QAM Transceiver Model

Fig. 2 depicts an idealised transceiver model that employs quadrature amplitude modulation (QAM) and matched filtering to

minimize the impact of white Gaussian noise that affects the transmission channel [8]. QAM modulation was selected as the modulation scheme due to its widespread use in current and emerging technologies and low susceptibility to channel noise. To account for realistic input data, a uniformly distributed random signal is used as an input for the transmitter. On the receiver side, both I and Q signals are sampled by two dedicated time-interleaved A/D converter systems (see Section III). For the I channel, different Gaussian distributions with various standard deviations are used to characterise the gain, offset and timing mismatch errors. The mean values of all distribution are assumed to be zero. Three sets of identical but independent distributions are employed to describe the corresponding Q channel mismatch errors, since two separate conversion systems are utilized in the transceiver model. The converted I and Q signals are then filtered by the matched filters of the receiver and demodulated in the last stage.

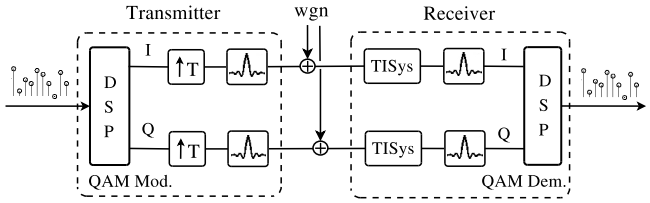

Fig. 2. QAM transceiver model.

IV. Mismatch Correction Scheme

A. System Modelling

The reconstruction of the I and Q signals can be achieved by modelling the non-ideal A/D converter behaviour as analysis filter in a filter bank [9]. Fractional delay filters are well suited for this task, since they facilitate the resampling of a signal according to a specified fraction of the sampling period. By applying windowing methods, this type of filter can be designed to model the timing mismatch among A/D converters with high accuracy. Additionally, the channels individual sampling phase and it static errors can be represented by adding a channel dependent delay and factors for the respective gain and offset error. The non-causal FIR representation of such a filter, modelling the channel with index m is given in (1), where n equals $[-K/2,\ K/2]$ for even K and $[-(K+1)/2,\ (K-1)/2]$ for odd K, respectively. The term K indicates the order of the fractional filter design.

$$H_m(n) = g_m\left(z^{-m}\ w(n)\ sinc(n+\Delta_m) + o_m\right) \tag{1}$$

The causal implementation of these filters can be obtained by adding a delay of $-K/2$ for even and $-(K+1)/2$ for odd orders, respectively. The shifted window function $w(n)$ attenuates the Gibbs phenomenon and therefore ensures an improved performance in the band of interest. By modelling the reconstruction system as a filter bank, we can employ filter bank theory to mitigate the impact of non-ideal sampling. A disadvantage of the common analysis and synthesis filter representation is that they do not operate efficiently. In the case of the analysis filter, data is filtered that is partially discarded by the consecutive decimator and the synthesis filter processes zero-padded data. A polyphase filter representation, however, operates on the decimated and not on the overall sampling rate allowing a more practical implementation. The polyphase structure of the filter bank is derived by exchanging the decimator with the polyphase analysis filter and the interpolator with the polyphase synthesis filter [10]. Furthermore, channel dependent delays need to be added to allow multiplexing and demultiplexing of input and output data, respectively (see Fig. 3).

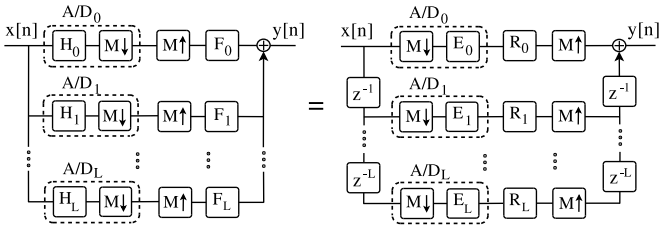

Fig. 3. Maximally decimated filter bank (left) and its equivalent polyphase representation (right).

The polyphase representations of analysis and synthesis filter that are employed in the polyphase filter bank formulation are shown in (2) and (3).

$$H_m = \sum_{k=0}^{L} z^{-k}\ E_{mk}(z^M) \tag{2}$$

$$F_m = \sum_{k=0}^{L} z^{-(L-k)}\ R_{km}(z^M) \tag{3}$$

By using definitions (2) and (3), it is possible to describe all sets of analysis and synthesis filter in the polyphase matrices E and R, respectively. The required polyphase decomposition of H and F into corresponding subfilters is shown in Fig. 4.

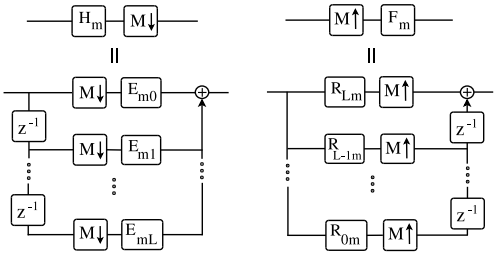

Fig. 4. Polyphase decomposition of analysis (left) and synthesis filter (right).

It is important to notice that only the derived set of synthesis filter need to be implemented in an practical application since the analysis filter behaviour is constituted by the non-ideal A/D converters.

B. Synthesis Filter Design

By suppressing aliasing and distortion errors as well as achieving polyphase matched filtering, we obtain a more efficient digital noise reduction scheme. The synergy of these two functionalities results in a single system, whose implementation and computational complexity is more favourable. The perfect reconstruction criteria for this system is given in (4), where c is a scalar value, and G is the polyphase formulation of the root-raised-cosine filter.

$$R\ E = c\ z^{-d} G \tag{4}$$

The polyphase decomposition of G follows the definition of (2). The polyphase synthesis filter are obtained by (5), where vector q represents the determinant of E. Here, P is the delayed product of the polyphase matrices G and the adjoint matrix of E (see (6)).

$$R = \frac{1}{q}\ P \tag{5}$$

$$P = c\, z^{-d} \begin{bmatrix} G_0 & G_1 & . . & G_L \\ z^{-1}G_L & G_0 & . . & G_{L-1} \\ . & . & . & . \\ . & . & . & . \\ z^{-1}G_1 & . . & z^{-1}G_L & G_0 \end{bmatrix} \begin{bmatrix} \varepsilon_{00} & \varepsilon_{01} & . . & \varepsilon_{0,L} \\ \varepsilon_{10} & \varepsilon_{11} & . . & \varepsilon_{1,L} \\ . & . & . & . \\ . & . & . & . \\ \varepsilon_{L,0} & \varepsilon_{L,1} & .. & \varepsilon_{L,L} \end{bmatrix} \quad (6)$$

The polyphase elements of R as described in (5) are recursive and have a common denominator given by the determinant of E. Typically, these filters are unstable since the roots of the recursive part lie outside the unit circle in the z-plane. To ensure the stability of the polyphase filters, it is necessary to approximate the subfilter characteristics of R using finite impulse response filters (FIR). This approximation for a single polyphase subfilter can be obtained by solving (7) where Q is the Toeplitz matrix of q. The scalars $R_{mk}(n)$ and $P_{mk}(n)$ refer to the n^{th} coefficient of the respective polyphase subfilter. The number of taps of the subfilters of P is indicated by N.

$$\begin{bmatrix} P_{mk}(0) \\ . \\ . \\ P_{mk}(N-1) \\ 0 \\ . \\ . \\ 0 \end{bmatrix} = \underbrace{\begin{bmatrix} q(0) & 0 & . . & 0 \\ . & . & . . & . \\ . & . & . . & . \\ q(N-1) & q(N-2) & . . & q(0) \\ 0 & q(N-1) & . . & q(1) \\ . & . & . . & . \\ . & . & . . & . \\ 0 & 0 & . . & q(N-1) \end{bmatrix}}_{Q} \begin{bmatrix} R_{mk}(0) \\ . \\ . \\ R_{mk}(N-1) \end{bmatrix} \quad (7)$$

The least squares solution to this problem is given in (8), where Q^T indicates the transpose of matrix Q.

$$R_{mk} = (Q^T\ Q)^{-1} Q^T\ P_{mk} \quad (8)$$

It is interesting to notice that the pseudoinverse matrix is constant for the approximation of all polyphase subfilters of P, since it only depends of the determinant q. This fact reduces the complexity of the design as this pseudoinverse facilitates the approximation of all polyphase subfilters of P. It can be concluded, that the major difference between the unstable synthesis filter design that achieves perfect reconstruction as shown in (4) and its stable approximation in (8) is the least-means-squares approximation of the inverse of vector q.

V. Simulation Results

The model presented in Section III has been simulated using 1000 uniformly distributed data points as an input sequence for the quadrature amplitude modulator. In this section, the presented figures-of-merit such as SER and signal-to-noise ratio (SNR) show the average value of at least 500 simulations to provide results of sufficient statistical significance. The specified standard deviations g, o and Δ were used to select the respective mismatch magnitudes of the individual converters for every simulation. Using these mismatch values, the analysis filter were designed according to (4) employing a delayed Hann window. The modulation and demodulation of the information signal and the transmitter matched filter design were carried out in Matlab. The roll-off and oversampling factor and the filter delay were selected to be $[0.2, 2, 16]$ for the matched filter design, respectively. Its finite length of 65 taps introduced an mean-squared-error of 54.8 dB for a random 64 QAM signal, when no other noise source affected the transceiver. 14-bit A/D converters were employed in the time-interleaved system, unless stated otherwise. The root-raised-cosine filtering was performed by the polyphase synthesis filter designed as described in Section IV for all simulation results presented in this section.

Fig. 5 shows the symbol error rate against the energy per bit to noise power spectral density ratio (E_b/N_0) for 4, 16 and 64 QAM. The dashed lines indicate the symbol error performance, when the A/D converters do not introduce aliasing or distortion errors due to channel mismatch. The solid lines show the additional impact of gain, offset and timing mismatch error on the SER. The respective standard deviations of these errors were set to be $[5\%, 0.5\%, 5\%]$. As depicted in this figure, the 4 QAM system is hardly affected by the mismatch errors due to the great Euclidean distance of its constellation points. However, an increasing number of constellation points in combination with the specified mismatch errors increases the symbol error rate of the 16 and 64 QAM modulation system significantly. To reduce this performance penalty, each root-raised-cosine filter was replaced by a proposed filter bank (see Fig. 2). The order analysis filter were designed for a filter order of 8. The coefficients of the resulting synthesis filter design had 65 taps after limiting their accuracy to 14-bit. Therefore, the filter bank performed the same number of filter operations as the root-raised-cosine filtering alone would require. As a consequence did the reconstruction of the mismatch affected I and Q signals not introduce additional filter operations.

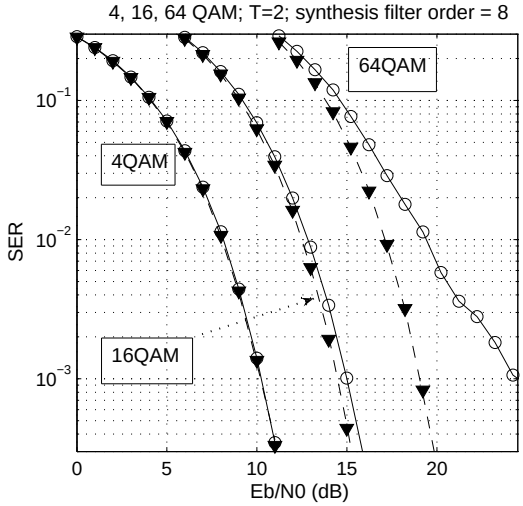

Fig. 5. Symbol error rate against E_b/N_0 for 4, 16 and 64 QAM with (solid lines with circular markers) and without mismatch errors (dashed lines). The SER of the reconstructed signal is indicated by triangles. ($[g,\ o,\ \Delta] = [5\%,\ 0.5\%,\ 5\%]$).

The SNR performance of a 64 QAM system, that has proven to be the most susceptible to converter mismatch, is investigated in Fig. 6. The necessarily finite number of taps used for the matched filter design, causes the performance of the corrected and uncorrected system to saturate at a value of 54.8 dB. The SNR value of the uncorrected architecture that is represented by the consecutive mesh, deteriorates by about 14 dB, even for a small timing mismatch of 2.5%. However, the transceiver with 16 tap analysis filters achieves a SNR of more than 50 dB even for very large mismatch errors. A low filter order of 6 still obtains a SNR increase of 23 dB for large mismatch errors.

Fig. 7 illustrates the numerical robustness of the proposed system. The solid lines indicates least-mean-squares contour lines for a SNR

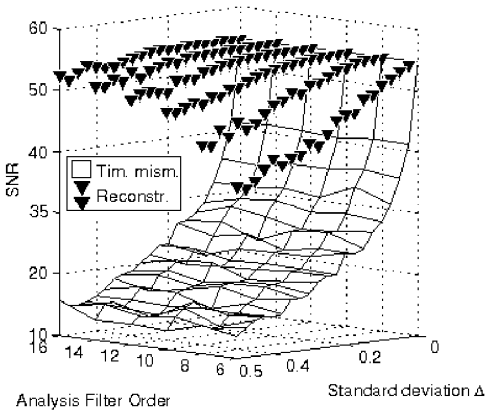

Fig. 6. SNR(dB), of a 64 QAM system, against the standard deviation (Gaussian distributed) of the timing mismatch ($\Delta = [0\%, 2.5\%, ..., 50\%]$) and the order K of the analysis filter ($K = [6, 8, 10, 12, 14, 16]$).

of 50, 45 and 40 dB, when the synthesis filter coefficients use the 52 bit floating point accuracy. The dashed and dashed-dotted indicate the contour for 14-bit and 12-bit accuracy, respectively. The impact of limited filter length increases for more complex analysis filters and larger mismatch magnitudes.

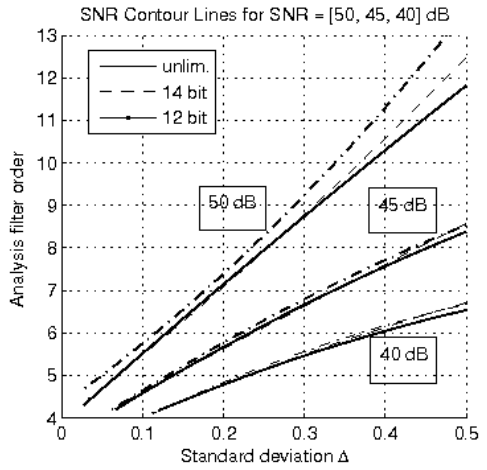

Fig. 7. SNR(dB) least-mean-squares contour plot for unlimited coefficient and 14-bit length.

VI. Conclusion

In this paper, we presented a transceiver model employing a quadrature amplitude modulation scheme and time-interleaved A/D conversion.

The impact of A/D converter non-idealities such as gain, offset and timing mismatch on the digital receiver performance was investigated. The figures-of-merit degradation has been demonstrated for different quadrature amplitude modulation schemes. The respective simulation results showed that A/D mismatch severely increases the receiver symbol error rate for higher order quadrature amplitude modulation systems. To overcome these performance penalties, a filter bank correction scheme was derived. This system facilitates the reconstruction of the inphase and quadrature signals and performs matched filtering at the same time, allowing a less complex implementation. The investigated figures-of-merit, such as symbol-error-rate and mean-squared-error, indicated a substantial performance increase of the system, even for large timing mismatch errors. Furthermore, design guidelines have been presented that show the required filter bank complexity for a specified mismatch standard deviation. Finally, the numerical robustness of the proposed design was demonstrated.

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