Low-Power Sliding Correlation CMOS UWB Pulsed Radar Receiver for Motion Detection

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Abstract— **This paper presents a low-power coherent receiver for UWB pulsed Radar for motion detection. Due to accuracy of the radar motion detection, coherent detection scheme is adopted in the receiver. To relax the stringent requirement of timing synchronization, sliding correlation detection is proposed. The clocking step which determines detection resolution is determined by 2ns which is half of a pulse width or equivalent to 30cm. Receiver is designed in 0.13-μm CMOS process from 1.5 V supply. The pulse center frequency is 4GHz. The receiver includes a high voltage gain LNA, a analog correlator, a sampling comparator and a Flip Flop. The whole receiver excluding an LNA consumes 0.9 mA of DC current and 10pJ/pulse at the pulse rate of 16MHz. The active size is 600 x 380 μm^2.**

I. Introduction

FCC recently regulated a large low power 3.1 to 10.6GHz spectrum which opens up many interesting applications of Ultra wideband (UWB) [1] technology. Short range UWB radar is one of them. The motivation to develop the UWB pulsed radar for movement detection is the high resolution of short UWB pulses while being able to maintain system low power, low complexity, and low cost. Several approaches have been done so far for the radar. Architecture varies from traditional direct conversion architecture to the direct sampling using oscilloscope. The technology of choice is also vast, from SiGe HBT [2], InP-HEMT [3] to CMOS [4]. Detection types can be Doppler [4] or spectrum sensing, digital sampling [3] or correlation [2]

As a compromise of the requirement, technology challenge and technical aspect, the architecture shown in Fig. 1 is chosen. Correlation using analog approach using CMOS technology is implemented together with a smart system clock timing. The proposed RF receiver is shown in Fig. 1 consisting of a high gain differential wideband LNA, an analog correlator, a comparator and Flip Flop (FF). Designed in 0.13-μm CMOS process, the receiver proves the functionality and shows the feasibility of low power low cost and effective UWB radar for motion detection.

II. System Operation

A. System consideration

So far, several works have been reported to develop UWB pulse radar transceivers. There are two data demodulation schemes for UWB pulse system, coherent [2] and non-coherent demodulations. Non-coherent receiver [3]
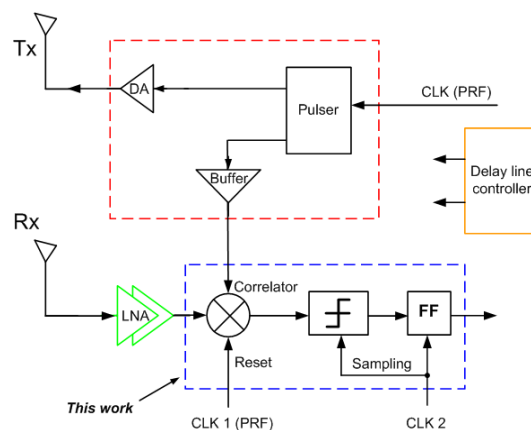

Figure 1. Transceiver architecture of the UWB pulse radar.

is not suitable for radar detection in the jamming environment though the architecture is simple. False alarm and misdetection may happen due to any reflected signals, both from tracking objects or surrounding ones. In the coherent transceiver, the correlation process requires the shape matching of the pulses generated in the receiver and the received pulses. It is complex but can meet the precise timing synchronization between transmitter and receiver, which is useful for the radar accuracy.

The whole receiver circuit for implementation is shown in Fig. 1. Correlator is the key building block in the coherent receiver. Its performance determines the receiver front-end gain, resolution, required template amplitude thus the power consumption. As can be seen from Fig. 1, a template pulse generator is provided from the transmitter. The template pulse will be correlated with the incoming pulse which is amplified by the high gain LNAs.

Sampling comparator is adopted to provide better immunization with DC offset, better resolution and overcome the delay of comparator input. However, the tradeoff when using sampling comparator is the involvement of clock generation circuit. From Fig. 1 we can see two clocking signal, CLK 1 and CLK 2, are needed

B. Receiver Operation

Fig. 1 shows the receiver chain (Rx) for the UWB-based Radar transceiver. This work includes a Correlator (Multiplier + Integrator), Comparator, Flip Flop circuit and the Reset and Sampling clock generators. The operation frequency of the receiver is in the UWB low band with

center frequency of 4 GHz and pulse bandwidth 500MHz. At the receiver input, reflected pulses from detected object will be amplified by a high gain LNA to the high enough level for the correlator to process the comparison of input pulse with template pulse. After correlation, the output is converted to DC and accumulated in a capacitor which acts as an integrator. The voltage output of correlator will go though the comparator. A given threshold is set for comparison. The output of sampling compartor will be smoothed using Flip Flop (FF). At the output, the data is recovered in correspondence with the input pulses.

In order to test the operation of the receiver, the triangular enveloped pulse generators are used to act as the input pulses and template pulses. The envelope will feature the triangular shape for high amount of sidelobe rejection. Its duration is about 4ns width to ensure 500 MHz of spectrum.

The operation of the receiver strongly depends on the clock timing setup. The timing diagram of CLK1 and CLK2 in respect with system clock is shown below in Fig. 2. From the system analysis, the pulse repetition frequency (PRF) is chosen as 1MHz. The choice of PRF is important, which is the consideration to satisfy the transmission spectral mask, link budget calculation. From the system clock (CLK), CLK1 is generated with the same PRF but delayed 20n to create a buffer time for Reset clock.
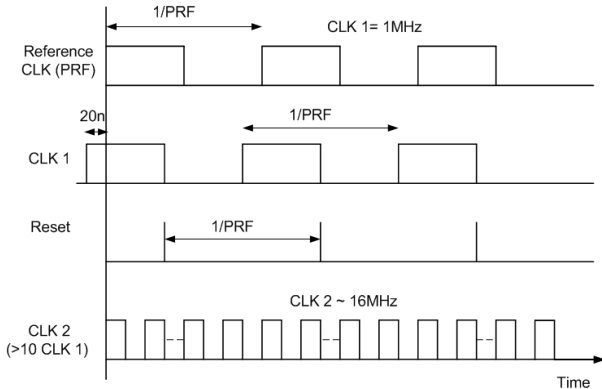

Figure 2.   System clock timing.

CLK1 function is to generate the Reset clock for the correlator. The Reset clock has the same PRF as CLK, it happens before each period of correlation to reset the previous correlation product to low level and ready for the new correlation cycle. CLK2 function is to generate the Sampling clock for Comparator and FF. It period is chosen about 10 times smaller than the CLK.

The design goal focuses on the simplicity, low power and low cost. Correlator block is the center in the receiver design. It involves the design constraint and performance of the receiver as well as the radar system.

III.   RECEIVER CIRCUIT DESIGN

A.   Multiplier

For the coherent receiver, the incoming signal will be compared with the template one in phase. To realize the

comparison, multiplication method is often applied. The product of the multiplication will be proportional to the degree of correlation between the two signals, input and template.

To satisfy the wide bandwidth in the UWB pulsed radar system, the Gilbert-cell based multiplier [5] is a strong cadidate. The multiplier includes the transconductance stage and switching stage. Both of the stages can provide gain to the output product. Bias is important for the multiplier to operate. The circuit is required to operate in saturation bias condition

B.   Analog Correlator

An analog correlator in principle consists of a multiplier and an integrator. The multiplier circuit and its operation have been discussed above. To provide an optimal solution, the compact design is approached, merging an integrator with the multiplier. A capacitor will be used as an integrator to accumulate the output product of multiplication.

In Fig. 3, the double balanced Gilbert cell is used for multiplication, which can meet the wide bandwidth requirement. The current product of multiplication will be converted to the voltage using PMOS load, which consists of diode connected and cross-connection. The positive feedback causes higher gain. The correlation gain depends on three factors, which are the amplitude of the template pulse, the delay between the input and template pulses and the gain of the multiplier. With the PMOS cross- and diode-connected load, the current consumption is small while the gain is high enough for a given minimum detectable input pulse.
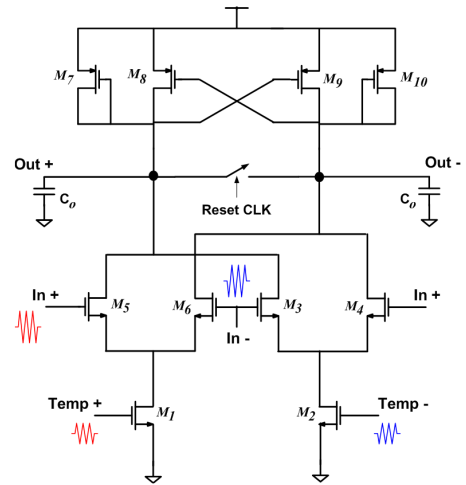

Figure 3.   Proposed analog correlator: merging multiplier with integrator

The output current will be integrated using the capacitor C_0 at the output node. Since the speed of integration or charging time is inversely proportional to the value of the capacitor, the capacitor is preferred to be used with small value. The best solution is to take advantage of the parasitic capacitance at the output node. When the input pulse arrives, the multiplication happens with the template pulse which is always available for every cycle. The positive

output will be charged to High level voltage while the negative stay at the Low level.

The sizing and bias is extremely important for the correlator block. For the proper bias, the proposed correlator just gives an output the two states: High and Low, regardless of the input signal level as long as it is higher the minimum detectable level. This unique feature is very suitable and applicable for system using comparator. Because the comparator just compares with the threshold level and responds the binary output.

Across of the differential output, a switch is inserted. It consisted a single transistor with the gate is controlled by Reset clock signal. The switch will be triggered every period. When the switch is ON, the two differential outputs are shorted, making the output go back to the same Low logic level. When the switch is OFF, the two outputs are not affected, staying at the High logic level when correlation is detected.

C. Sampling Comparator

The sampling comparator consists of the latch comparator and the D-Flip Flop (FF) block, shown in Fig. 4. In order to drive the sampling comparator, a clock signal (CLK2) is needed. CLK2 will go though a differential clock generator circuit to generate the complementary clock for the two D-FFs.
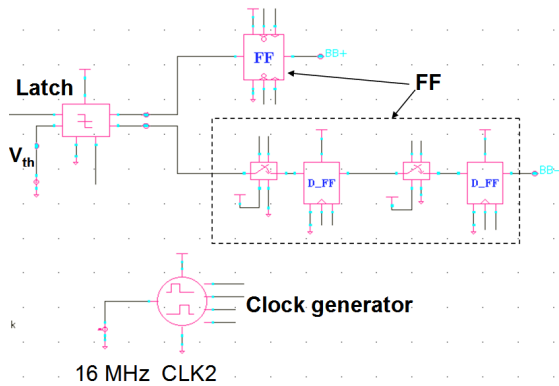

Figure 4.   Sampling comparator with the inside view of Flip Flop block.

1) Latch Comparator

The choice of comparator type should be in line with the design target of low complexity and low power consumption. In this regards, dynamic latched comparator is the most suitable candidate. The schematic of dynamic comparator used in this design is shown in Fig. 5. It consists of a core latch and the inverters at output. Dynamic latched comparator dissipates only dynamic current, during the generation phase. Clock signal (CLK) acts as latch signal.

The cross-coupled transistor is positive feedback circuit which realizes the regeneration. The cross-coupled transistors help to speed up the decision at the output of latch. It also makes the comparator with smaller amount of hysteresis. From the simulation, the comparator's resolution is in the range of a few 10mV, which is small enough for
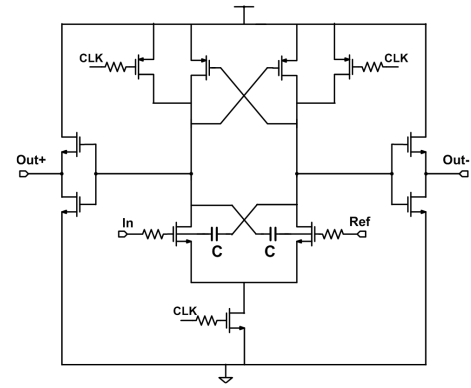

Figure 5.   Dynamic comparator schematic.

this design and optimum value for the tradeoff of power consumption.

Extra capacitor is cross-inserted between the body of one transistor and drain of the other transistor in differential pair to remove the overshoot of clock and kick-back noise. The noise as well as some offset product during multiplication may degrade signal to noise ratio (SNR). To overcome this drawback, the ambient noise will be estimated and represented as the threshold voltage for the comparator to restore the input data out of the noise.

2) D-FlipFlop

Conventional D-Flip Flop (FF) block [6] is used after the latch. The FF function is to smooth the output of the sampling comparator.

IV.   SIMULATION RESULTS

The UWB pulse radar system is designed using 1.5 V supply. The triangular-shaped pulse generator is used at the input to act as the incoming signals. High gain LNA is not covered in this work but added for whole receiver operation simulation. Fig. 6 shows the pulse train obtained at the output the correlator when the OOK pulses are applied at the input. The template pulse amplitude is 800 mVpp, which is high enough for the correlator operation.
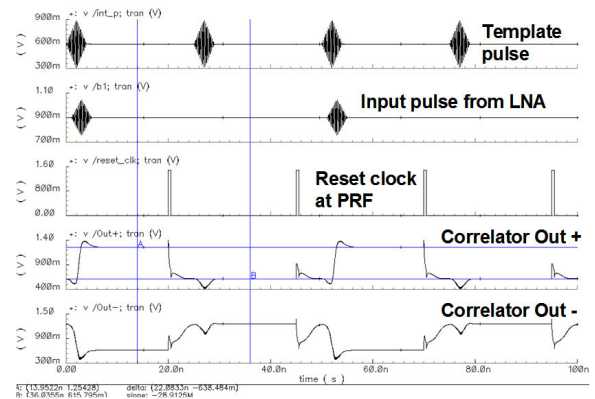

Figure 6.   Transient simulation of the correlation.

The correlator has a distinctive feature. That is the output is locked either at the High or Low level which depends on the correlation is achieved or not, respectively. In Fig. 6, the

output correlation process is shown. The correlation current is charged up to the peak level during the pulse duration and is hold for the comparator to process it. The peak level is constant, which is determined by the initial DC bias condition of the multiplier circuit. Only the rising slope or charging speed is proportional to the amplitude of input pulse, its delay with template pulse and the gain of multiplier. In this design, the minimum detectable input of correlator is 20mVpp. The difference of the high and low voltage level is around 400mV. The correlator is design to be able to operate when the maximum offset between the input and template pulses is 2ns, which is based on the system operation and minimum range step.
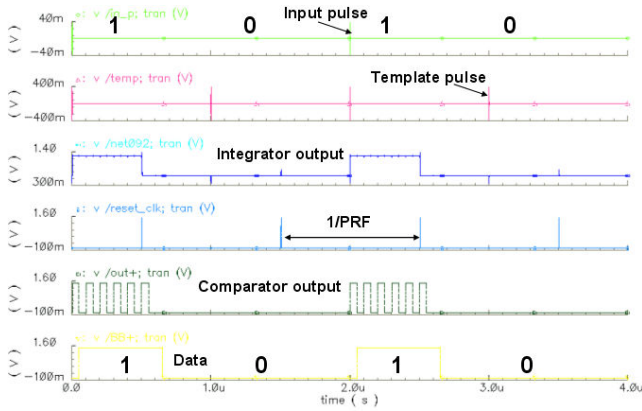

Figure 7.   System with input and output transient simulation.

Fig. 7 shows the timing diagram of the receiver. Input pulses come at the twice frequency of the template. This is done on purpose, to observe the difference of the correlation and without correlation. Only when the pulses from input and template present at the same time or with a delay of less than 2ns, the multiplication happens. The correlator will process these pulses and generate the output products, marked as Integrator ouput. As can bee seen from Fig. 7, the correlator's output is from 800mV to 1200mV, which is large enough for the comparator to process. The output of correlator is compared with threshold level Vth using the sampling comparator. The final data output go through the FF to smooth the pulse data. Rx output signal is acquired in response to the input data.
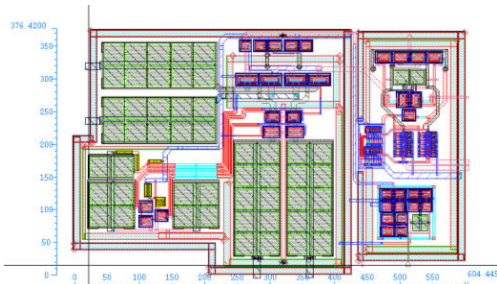

Figure 8.   Layout of the designed receiver, excluding LNA.

The layout photograph of the receiver without LNA is shown in Fig. 8. It core size is 600 x 380 um^2. The receiver performance is summarised in Table I.

TABLE I: PERFORMANCE SUMMARY

Analog Correlator		Comparator + FF	
Template pulse amplitude	800mVpp	Threshold level	900mV
Minimum input pulse amplitude	20mVpp	Minimum offset	30mV
Minimum offset	2ns	Average power dissipation	10pJ/pulse
Pulse bandwidth	500MHz	Sampling rate	16MHz
Pulse center Freq.	4GHz		
Current Consumption	0.9mA		
Supply voltage	1.5V		
Process	0.18μm		

V.   CONCLUSION

A fully integrated coherent CMOS UWB Radar receiver in 3-5 GHz band is presented. The proposed receiver's circuit blocks are designed to provide the high sensitivity and accuracy for moving detection radar application. In the receiver, a high gain LNA with 70dB of voltage gain is added for system simulation. Correlator with Gilbert cell based multiplier is adopted. The parasitic capacitance at the correlator output is used for integration, which simplify the circuitry. Dynamic latched comparator is used to save the power. The sampling approach is used for comparator to improve its performance against delay, noise. Designed in a 0.18-μm CMOS technology from 1.8 V supply, overall performances of the receiver is good. Basic functionality of receiver is simulated with corner simulation. Minimum detectable pulse of correlator is 20mVpp. DC current consumption is around 0.9mA while average dynamic power dissipation is 10pJ/pulse. The receiver without LNA shows a very compact die size of 0.24 mm^2.

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