is 1.25 dB with a return loss better than 28 dB. Two transmission zeros are observed with attenuations over 40 dB at approximately 1.43 and 1.93 GHz, respectively. Meanwhile, the measured 3-dB relative bandwidth is about 9.35%. Figure 3(b) describes the measured in-band group delay. The wideband responses, shown in Figure 3(c), illustrate that the first spurious pass-band is located at 3.18 GHz, i.e. about $2f_0$. When comparing the measurements with predicated results, one can see that a good agreement between them can be observed.

4. CONCLUSION

In this article, a compact dual-mode patch resonator for band-pass filter applications has been studied. A demonstrator filter using a dual-cross slot has been designed, fabricated and tested. Measured data indicate the filter has a minimum pass-band insertion loss 1.25 dB as well as a pair of transmission zeros close to the pass band. The filter has a size reduction to 26.7% as compared to the conventional patch resonator. The design concept is validated, theoretically and experimentally, with good consistency.

REFERENCES

1. J.-S. Hong and M.J. Lancaster, Microstrip filters for RF/microwave applications. Wiley, New York, 2001, Ch. 11.
2. I. Wolff, Microstrip bandpass filter using degenerate modes of a microstrip ring resonator, Electron Lett 8 (1972), 302–303.
3. B.T. Tan, S.T. Chew, M.S. Leong, and B.L. Ooi, A dual-mode bandpass filter with enhanced capacitive perturbation, IEEE Trans Microwave Theory Tech 51, (2003), 1906–1910.
4. A. Görür, A novel dual-mode bandpass filter with wide stopband using the properties of microstrip open-loop resonator, IEEE Microwave Wireless Compon Lett 12, (2002), 386–388.
5. A. Gorur, Description of coupling between degenerate modes of a dual-mode microstrip loop resonator using a novel perturbation arrangement and its dual-mode bandpass filter applications, IEEE Trans Microwave Theory Tech 52, (2004),671–677.
6. S. Amari, Comments on description of coupling between degenerate modes of a dual-mode microstrip loop resoantor using a novel perturbation arrangement and its dual-mode bandpass filter applications, IEEE Trans Microwave Theory Tech 52, (2004), 2190–2192.
7. S.-W. Fok, P. Cheong, K.-W. Tam, and R. P. Martins, A novel microstrip square-loop dual-mode bandpass filter with simultaneous size reduction and spurious response suppression, IEEE Trans Microwave Theory Tech 54, (2006), 2033–2041.
8. S.J. Fiedziuszko, J.A. Curtis, S.C. Holme, and R.S. Kwok, Low loss multiplexers with planar dual mode HTS resonators, IEEE Trans Microwave Theory Tech 44, (1996), 1248–1257.
9. J.-S. Hong, and S.-Z. Li, Theory and experiment of dual-mode microstrip triangular patch resonators and filters, IEEE Trans Microwave Theory Tech 52, (2004), 1237–1243.
10. L. Zhu, P.-M. Wecowski, and K. Wu, New planar dual-mode filter using cross-slotted patch resonator for simultaneous size and loss reduction, IEEE Trans Microwave Theory Tech 47, (1999), 650–654.
11. O. Akgun, B.S. Tezekici, and A. Görür, Reduced-size dual-mode slotted patch resonator for low-loss and narrowband bandpass filter applications, Electron Lett 40, (2004),1275–1276.
12. L. Zhu, B.C. Tan, and S.J. Quek, Miniaturized dual-mode bandpass filter using inductively loaded cross-slotted patch resonator, IEEE Microwave Wireless Compon Lett 15, (2005), 22–24.
13. W.-H. Tu and K. Chang, Miniaturized dual-mode bandpass filter with harmonic control, IEEE Microwave Wireless Compon Lett 15, (2005) 838–835.
14. IE3D Manual, Zeland Software, Fremont, CA, 2001.

9.1 dBm IIP3 36 dB GAIN CONTROLLABLE LNA FOR WCDMA IN 0.13-μm CMOS

Tuan Anh Phan,[1] Ronan Farrell,[1] and Sang-Gug Lee[2]
[1] Institute of Microelectronics and Wireless Systems, National University of Ireland, Maynooth, Kildare, Ireland; Corresponding author: aphan@eeng.nuim.ie
[2] Information and Communications University, Daejeon, Korea

Received 13 September 2008

ABSTRACT: *This article presents a low-power, high-linearity cascode-type low noise amplifier (LNA) with 36 dB of variable gain for the WIDE Code Division Multiple Access systems. By enhancing the substrate resistance of a common gate transistor along with adopting multiple-gate technique, the linearity is significantly improved. Shunt-current steering is adopted for smooth gain control. Step gain mode is used to further increase the gain control range. The main common source transistor is disabled in attenuation mode, saving unwanted power consumption. Measurements show maximum gain of 12.3 dB with S_{11} of -19.5 dB, and S_{22} of -14 dB. The total gain control range is 36 dB. NF is measured as 2 dB and two-tone test shows 9.1 dBm of IIP3. Implemented in 0.13-μm CMOS technology, the LNA consumes only 1.6 mA at maximum gain mode and only 0.2 mA in attenuation mode from 1.2 V supply. Its die size is 0.3 mm^2.* © 2009 Wiley Periodicals, Inc.
Microwave Opt Technol Lett 51: 1385–1388, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24320

Key words: *LNA; variable gain control; high linearity; CMOS; WCDMA; low-power*

1. INTRODUCTION

WIDE Code Division Multiple Access (WCDMA) receiver systems require high linearity due to cross modulation distortion (XMD) [1]. Once the signal-to-noise ratio (SNR) is degraded at the low noise amplifier (LNA) by XMD, designing the following stages to satisfy linearity and power consumption requirements may be difficult. Also, to achieve a wide system dynamic range of over 80 dB, the LNA must have several gain modes so as not to saturate the following stages. Besides those main challenges, the LNA should have a good performance with high enough gain, low noise figure (NF), and low power consumption.

There have been several efforts to improve the linearity performance of the LNA for CMOS technology. Feed-forward cancellation technique introduced in [2] is useful for differential application, but it requires an additional external power splitter which would be a cost increase. The active postdistortion technique [3] and derivative super-position (DS) [4] are quite effective but with the cost of higher noise. The modified derivative superposition (MDS) method is attractive because it can increase linearity significantly with wide DC operating range [5]. In this method, however, it is not easy to control the opposite phase of third order product to obtain the desired high level of linearity. Thus, a new technique to further increase the linearity is introduced.

In this article, a high-linearity variable gain cascode-type LNA for WDCMA systems is presented. The linearity is significantly improved when the DS method is adopted together with enhancing the substrate resistance of common gate transistor without any performance penalty in power consumption, noise, and gain. To extend the gain control range, smooth and step gain control techniques are combined. Implemented in 0.13-μm CMOS process with Deep N-Well, the proposed LNA obtained 9.1 dBm of IIP3

and 36 dB of variable gain range while consuming only 1.6 mA at 1.2 V supply.

2. LINEARITY IMPROVEMENT APPROACH

The cascode-type LNA can be considered as two cascaded stages consisting of the common source (CS) and common gate (CG) transistors. The role of a preceding CS transistor is to provide the gain and suppress the noise through input matching. This transconductance device linearity is usually more important because it introduces more nonlinearity products to the output more than the cascode device (CG). Therefore, most of the linearization techniques have focused on the transconductance device as mentioned in the previous section. In this article, the approach is different. We assume that the transconductance has been fully linearized and the subsequent CG stage, which acts as current buffer, is the bottleneck of the linearity. Moreover, if we treat the transconductance and cascode devices as the two cascading stages, the subsequent cascode device will dominates the overall linearity performance at the output. Thus, the overall LNA linearity will be maximized when both the CS and CG are linearized, especially the CG.

So far, most of the linearization methods for a CMOS LNA have focused on the CS stage. The most effective technique is derivative superposition (DS). This method cancels out the negative third-order derivative of the main field-effect transistor's (FET's) dc transfer characteristic by paralleling the auxiliary FET biased near the weak inversion region with the positive one. In this design, DS is adopted but the linearity does not satisfy the system

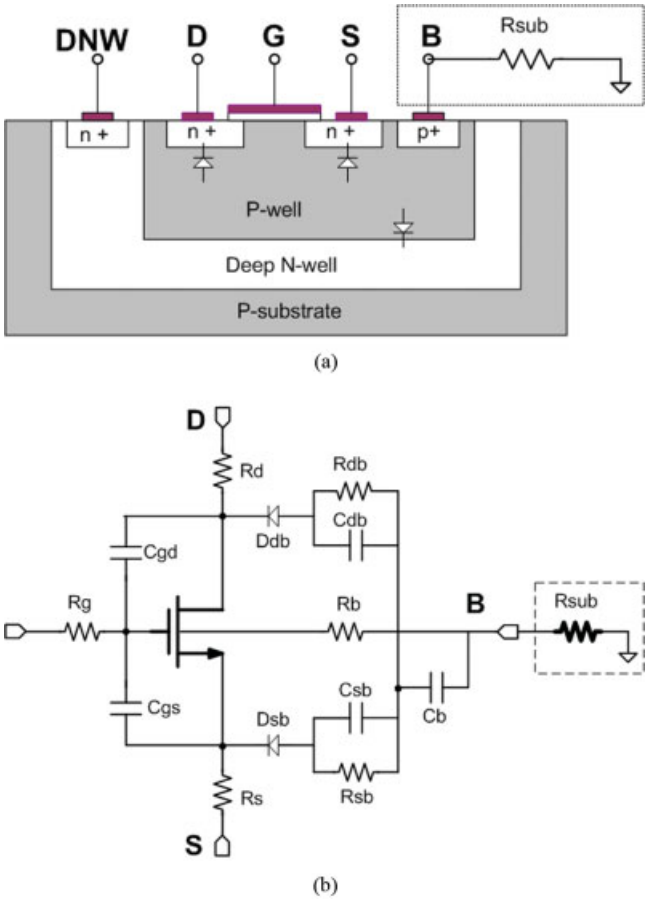

Figure 1 (a) Cross-sectional view and (b) substrate model of MOSFET. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

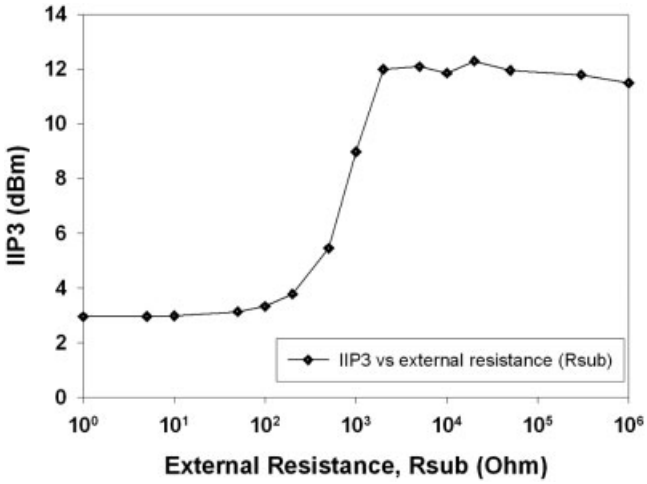

Figure 2 Simulation of IIP3 performance vs. the value of R_{sub}

requirement because it is hard to adjust the bias and FET's size to achieve complete IM3 cancellation.

Therefore, to obtain further linearity, a linearization technique at the CG by adopting substrate resistance enhancement is proposed. The model of a NMOSFET in a deep *N*-well process is shown in Figure 1 with presence of an external resistor R_{sub} between bulk terminal and ground. From the substrate model shown in Figure 1(b), a strong signal may turn on the parasitic source-bulk (D_{sb}) or drain-bulk (D_{db}) diodes, which clips the signal itself. That effect reduces the power handling capability or linearity of the MOSFET device. Because of that, the linearity can be improved by bootstrapping the bulk voltages [6, 7], which is realized by floating the bulk at RF. By isolating the bulk from ground with R_{sub}, distortion source cannot interfere the main signal path.

In contrast, the body and source of common source FETs are tied together to minimize the body effect and substrate resistance. Because it is well known that the higher the substrate resistance of CS transistor, the lower are its output resistance and transconductance, thus reducing the maximum available gain.

Figure 2 presents the linearity performance (IIP3) of the LNA versus the external substrate resistance (R_{sub}) by simulating with different R_{sub} values. When R_{sub} goes from 700 to 4 KOhm, the linearity shows a sharp increase in IIP3. With R_{sub} over 4 KOhm, linearity performance is saturated and not much improved compared to the IIP3 at 4 KOhm of R_{sub}.

3. LNA TOPOLOGY AND CIRCUIT DESIGN

The proposed LNA schematic using cascode topology is shown in Figure 3. Inductive load peaking (R_L, L_L) is used for wideband design. M_m and M_{ex} are the main and auxiliary FETs for DS technique, respectively. L_G, C_{GS}, and L_S are input the matching network. C_{GS} is used to reduce the size of M_m for noise and input simultaneous matching with power constraint.

The R_{sub} is inserted between the body of CG transistor and ground. Thus the body is highly isolated from ground, avoiding any feedback loop which may cause the signal distortion. It also helps reducing the resistive losses in the conductive P-well between D and S because the bulk resistance is open to the ground. In this design, R_{sub} is selected as 5 k Ohm.

Continuous gain control is realized by steering the signal away from the load through a branch consisting of C_{couple} and M_{steer}. C_{couple} is for DC blocking and AC signal coupling. As the M_{steer}

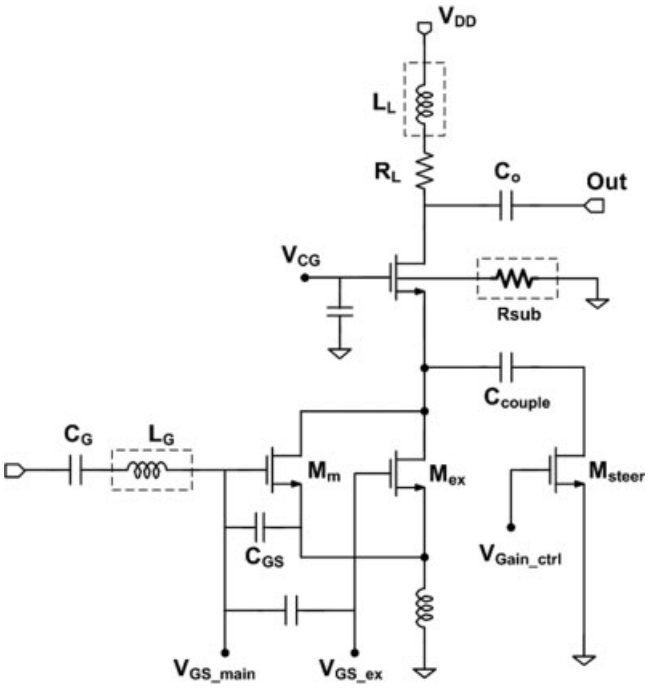

Figure 3 Proposed high linearity variable gain LNA

is ON, low on-resistance creates another path for signal to the ground apart from the main signal path to the output. Thus, depending on the amount of signal steered away, the signal appearing at the output can be controlled. To increase the range of gain control, step gain control is combined with continuous gain control. Four step gain modes are obtained corresponding with the ON/OFF operation of M_m and M_{steer}. That is maximum, medium, attenuation, and minimum gain modes when M_m is ON and M_{steer} is OFF, both M_m and M_{steer} are ON, M_m is OFF and M_{steer} is OFF, and M_m is OFF and M_{steer} is ON, respectively.

In the DS method, the subthreshold-biased FET (M_{ex}) generates more noise than the saturation-region biased one [2]. Hence, the auxiliary FET is designed with small size to minimize parasitic capacitance and noise contribution.

4. EXPERIMENTAL RESULTS

The proposed LNA is designed and fabricated in TSMC 0.13-μm CMOS technology using 1.2 V supply.

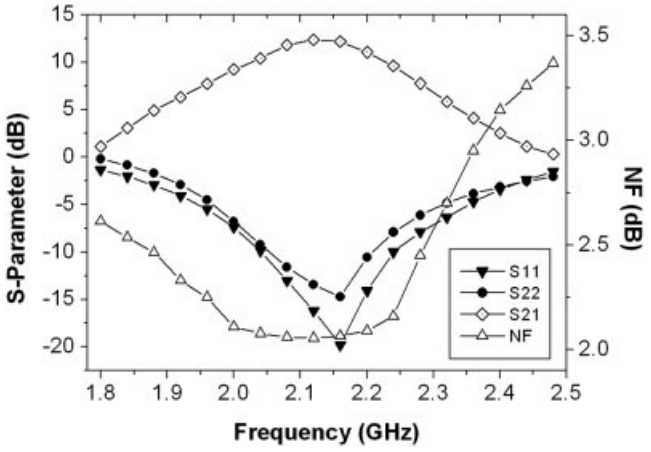

Figure 4 Measured S-parameters and NF of the LNA

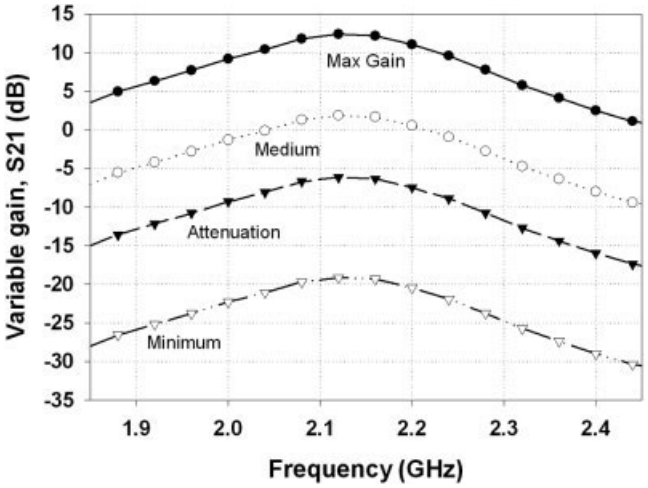

Figure 5 Measured variable gains of the LNA

Measurements show 12.3 dB of gain with good input and output matching. The measured S-parameters are shown in Figure 4. The NF is measured at 2 dB, which is slightly higher than simulation. This is due to slight reduction of measured power gain when compared with simulation.

Four gain modes (maximum, medium, attenuation, and minimum) are realized by turning ON/OFF the bias $V_{GS\ \ main}$ for M_m and $V_{Gain\ \ ctrl}$ for M_{steer} as aforementioned. In each gain mode, smooth gain tuning is achieved varying $V_{Gain\ \ ctrl}$ to adjust the mount of current steering. As a result, a wide range of 36 dB gain control is obtained as shown in Figure 5.

In Figure 6, the measured linearity performances of the LNA adopting DS technique with and without the R_{sub} are provided. Two-tone test at 2.135 and 2.145 GHz shows a high linearity performance as analyzed and expected. Though, the performance is little lower when compared with the simulation results shown in Figure 2. Measured IIP3 is 9.1 dBm showing more than 10 dB of improvement when compared with the case without using R_{sub}.

P1dB is improved slightly by 1 dB. The overall LNA consumes only 1.9 mW, which is suitable for low power applications. Chip die photo is shown in Figure 7 and performance is summarized in Table 1.

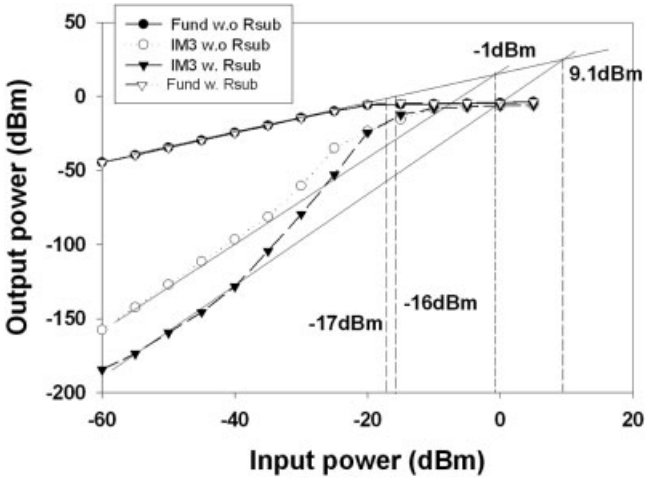

Figure 6 Measured IIP3 of the LNA with and without R_{sub} of 5 KOhm

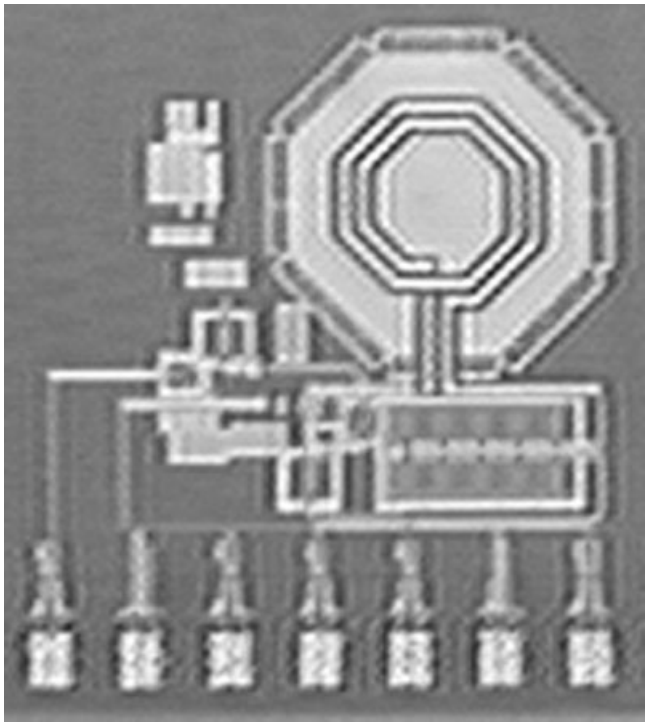

Figure 7 Die photo of the LNA

5. CONCLUSION

A simple but effective technique for linearity enhancement of an LNA with variable gain control in WCDMA systems is proposed. Linearity is significantly improved when the substrate of the common gate transistor is floated. Smooth and step gain controls are jointly realized by using current steering and turning ON/OFF the main transistor, respectively. As a result, a wider range of gain control is achieved. The LNA is also optimized for low power consumption. Implemented in 0.13-μm CMOS process, measurements show 9.1 dBm of IIP3 with an extra substrate resistance, improved by more than 10 dB. 36 dB of gain control range is obtained. S_{11}, S_{22}, and NF are -19.5, -14, and 2 dB, respectively. The LNA dissipates 1.6 mA from 1.2 V supply, and die size is 0.3 mm^2. The proposed LNA is well suited for high-linearity, low-power applications like WCDMA.

ACKNOWLEDGMENTS

The authors would like to thank Science Foundation Ireland for their generous funding of the research through the Centre for Telecommunication Value-Chain Research (CTVR). This work was supported in part by the Korea Science and Engineering Foundation (KOSEF) through the Ministry of Science and Technology (MOST).

TABLE 1 Summary of the LNA Performance

Parameters	Measurement
Power gain (dB)	12.3
Variable gain range (dB)	-24
S_{11}/S_{22} (dB)	$-14/-19.5$
NF (dB)	2.05
IIP3 and P1dB (dBm)	-1 and -17 without R_{sub} 9.1 and -16 with R_{sub}
Power dissipation (mW)	1.9
Supply voltage (V)	1.2
Process	0.13-μm CMOS

REFERENCES

1. V. Aparin and L.E. Larson, Analysis and reduction of cross-modulation distortion in CDMA receivers, IEEE Trans Microwave Theory Tech 51 (2003), 1591–1602.
2. Y. Ding and R. Harjani, A +18 dBm IIP3 LNA in 0.35 μm CMOS, IEEE Int Solid State Circuits Conf, San Francisco, CA (2001), 162–163.
3. N. Kim, V. Aparin, K. Barnett, and C. Persico, A cellular-band CDMA 0.25-μm CMOS LNA linearized using active post-distortion, IEEE J Solid State Circuits 41 (2006), 1530–1534.
4. T.W. Kim, B. Kim, and K. Lee, Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors, IEEE J Solid State Circuits 39 (2004), 223–229.
5. V. Aparin and L.E. Larson, Modified Derivative superpostition method for linearizing FET low-noise amplifiers, IEEE Trans Microwave Theory Tech 35 (2005), 571–581.
6. M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance, IEEE Trans Microwave Theory Tech 54 (2006), 31–39.
7. Q. Li and Y.P. Zhang, CMOS T/R switch design: Towards ultra-wideband and higher frequency, IEEE J Solid State Circuits 42 (2007), 563–570.

WIDE-BAND LOW-LOSS CPW-BASED COMPOSITE RIGHT/LEFT-HANDED TRANSMISSION LINE

Nemat Dolatsha and Mahmoud Shahabadi
Photonics Research Lab., School of ECE, Univ. of Tehran, Kargar Ave.North, 14395–515 Tehran, Iran; Corresponding author: n.dolatsha@ece.ut.ac.ir

Received 13 September 2008

ABSTRACT: *In this article, a coplanar waveguide (CPW)-based composite right/left-handed transmission line (CRLH TL) is introduced. The structure is realized by parallel-plate series capacitors (C) and shunt CPW stub inductors (L). Using a symmetric configuration for the unit cells along with searching for optimum values of LC components, we reduce the insertion loss and achieve wider LH-bandwidth. For the symmetric CRLH TL, a LH-passband extending from 1.3 to 4 GHz and a RH-passband extending from 4 to 6.5 GHz are measured.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1388–1390, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24319

Key words: *metamaterial; composite right/left-handed (CRLH); transmission line (TL)*

1. INTRODUCTION

Materials with simultaneously negative permittivity and permeability were theoretically studied by Veselago in 1967 [1]. Composite right/left-handed transmission lines (CRLH TLs) with antiparallel phase and group velocities are a class of these materials realized by cascading series capacitors and shunt inductors. There are also wanted and unwanted series inductors and shunt capacitors which should be accounted for at higher frequencies. Some novel devices such as phase-advance phase shifters [2] and backward-wave antennas [3] based on the CRLH TLs have been reported.