

Modeling and design of a low-cost constant current electronic load

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Abstract—Electronic loads are very useful tools for various applications in an electronics laboratory, but their high cost and lack of precise mathematical representation in the literature is a significant limitation. In this sense, this work presents the design and modeling of low-cost direct current (dc) analog electronic load. Design recommendations are presented in terms of a comprehensive design procedure. The related equations are presented, giving a broader understanding of the principles of operation. Three distinct test scenarios are analyzed, whereas the equipment relies on low-cost components.

Index Terms—electronic load, modeling, constant current, low-cost, design

I. INTRODUCTION

Electronic loads are devices capable of absorbing power and, therefore, have the opposite role to that of a power supply. An electronic load can simulate and maintain different specified load values, emulating an adjustable resistance, so that it is possible to draw different values of current from a power supply. This functionality makes electronic loads ideal tools for various studies with different types of voltage and current sources.

Some of the applications of electronic loads include testing the following components: photovoltaic modules to obtain current versus voltage curves (I - V) [1], [2]; fuel cell operation [3]; battery load test [4]; verification of efficiency of DC-DC converters [4]; loading of switched sources in order to measure noise levels at different operating points [5], [6]; among other applications.

Despite being a very useful tool, the typically high cost makes the use of such devices prohibitive for certain audiences. A query to the Digi-Key Electronics page performed on 19/07/2023 shows that some commercial models have values between US\$685 (B&K Precision model 8540) and US\$1318 (Teledyne LeCroy model T3EL150302P).

Two most common ways to design an electronic load are found in the literature. The first and most complex one employs static power converters and a control loop [7]. This option is very useful for cases where the amount of energy spent on tests is very large and needs to be recovered. As some works show, this topology and its control circuit allow

part of the energy to be returned to the grid [8], [9]. Despite this, the number of components for creating a static converter is greater, consequently increasing its cost, in addition to the control circuit also adding additional cost and complexity to the project [10]. For these reasons, this type of construction will not be used in this work.

The second option is a circuit topology that has changed little since its inception [11], [12], using a MOSFET-type transistor (metal oxide semiconductor field effect transistor) or IGBT (insulated gate bipolar transistor) [4], so this device is controlled by negative feedback with an operational amplifier (Op. Amp.). Due to the low number of components, as well as reduced cost and complexity, this will be the topology chosen for the work.

There are four operating modes for commercial electronic loads: constant current (CC), constant voltage (CV), constant resistance (CR), and constant power (CP). In this work, the circuit is presented in CC mode, since this is the most common operating mode for such a device [4].

From this scenario, it is defined as the objective of this study to present in general lines the project and an experimental prototype of an CC analog electronic load. The contributions consists of creating the circuit with common and low-cost components. In addition, the work presents the theoretical foundation in a more analytical way, given the lack of information in the literature works in the modeling of electronic loads [13] [14] [15], enabling further studies with of such devices. The different design decisions and the corresponding equations are also discussed in order to help in similar designs.

II. THEORETICAL FOUNDATION

In this section, all the concepts necessary to carry out the project are presented.

A. Basic circuit of an electronic load

The basic circuit of an electronic load is presented in Fig. 1 and consists of a N-type enhancement MOSFET, controlled by an Op. Amp. in negative feedback.

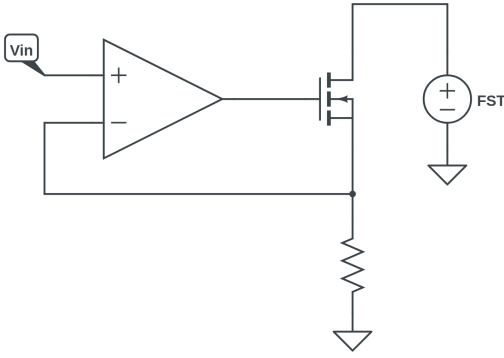


Fig. 1. Basic circuit of an electronic load.

As shown in Fig. 1, the topology resembles a voltage follower, modified by the addition of the FET device. By the virtual short-circuit principle, it is known that the voltage at both Op. Amp. inputs is the same (V_{in}) and, therefore, the operation of the circuit can be described according to (1):

$$I_D = V_{in}/R_S \quad (1)$$

where I_D is the drain current, V_{in} is the user-set voltage, and R_S is the sensing resistor resistance.

In functional terms, it can be stated that the device converts its voltage signal at the input into a corresponding value of current to be drawn from the source under test (SUT), positioned on the right. For this reason, this mode of operation is called CC.

B. Limitations of MOSFET

As with any other circuit, it is important to check the operating limits of the chosen MOSFET: voltage between drain and source (V_{DS}), voltage between gate and source (V_{GS}), breakdown limit ($V_{BD DS}$) and so on. Special care must be taken with the maximum drain current (I_D), this value is usually defined in the datasheet. This parameter is determined by two factors: the capacitance of the semiconductor itself and the limit of the device package. The first limit is theoretically calculated using thermal resistances and assuming that the package remains at a given temperature. The second limit is known for each specific type of encapsulation, being found through reliability tests and safety margins already added when this value is informed by the manufacturer [16]. For the first case, the maximum dissipation capacity of the semiconductor P_{MAX} is determined as:

$$P_{MAX} = \frac{T_{J MAX} - T_C}{R_{\theta JC}} \quad (2)$$

where $T_{J MAX}$ is the maximum temperature allowed in the junction, T_C is the encapsulation temperature and $R_{\theta JC}$ is the thermal resistance between the junction and the encapsulation.

Next, determine the maximum current I_{MAX} :

$$I_{MAX} = \sqrt{\frac{P_{MAX}}{R_{DS(on)}}} \quad (3)$$

where $R_{DS(on)}$ is the conduction resistance between drain and source of the MOSFET.

This expression is extremely important, as it shows that the maximum current is determined by means of theoretical calculations that assume a constant temperature in the device casing, which is problematic, especially in situations of high power dissipation, i.e., high values of I_D and V_{DS} simultaneously. Contrary to what other works claim, it is made explicit here that it is not possible to maintain an operating point with such a theoretical maximum current value presented in the datasheet. To determine the voltage and current values to which the device can be subjected, the safe operating region of operation of the device must be consulted. The SOA (safe operating area) presents information for the component should be used. The SOA corresponds to the different regions in which the component can be used, as well as their respective limits. There are five possible device limitations represented in the SOA, so a full description of each can be found in [17]. For the present work, the curve that presents the behaviour in direct current is the only relevant information.

C. Thermal instability

In addition to the aforementioned efforts, other failures that typically occur in MOSFETs must also be considered, as shown in the literature [18]. The main factor leading to such failures are the assumptions on which the datasheet is built. As mentioned earlier, some assumptions are unrealistic, such as maintaining the package temperature at a constant value. This leads to incorrect inferences of other device information, which will not be in the SOA as expected. The presence of such non-representative data in the datasheet is mentioned in [19]. When using the device outside the SOA, it will be subject to the phenomenon of thermal drift, which is the operating region where its power dissipation capacity is lower than the power to which the element is actually subject. In such circumstance, the device gets damaged.

The occurrence of the hot spot is another phenomenon that is not considered in the theoretical determination of SOA. As shown by [20], the MOSFET does not always have a negative coefficient between its drain current and its temperature. In Fig. 2, we have the $I_D - V_{GS}$ curve of a MOSFET, which allows us to elucidate this point.

It is possible to notice in the curve of Fig. 2 that there are three regions of interest. The curves meet at a first point (at about 70 A), which marks the zero temperature coefficient (ZTC). At this point, the drain current does not change as a function of temperature. On the left of the ZTC, it is possible to notice that curves of higher temperature present a higher drain current, indicating a positive coefficient of I_D versus V_{GS} , that is, heating the device leads it to drain higher values of drain current. To the right of the ZTC, there is the opposite behaviour, that is, a negative temperature coefficient, so that an increase in temperature leads to a reduction in the drained current. The effect of the positive temperature coefficient may cause an accumulation of the electric current in the silicon, leading to more heating. After this event, the semiconductor

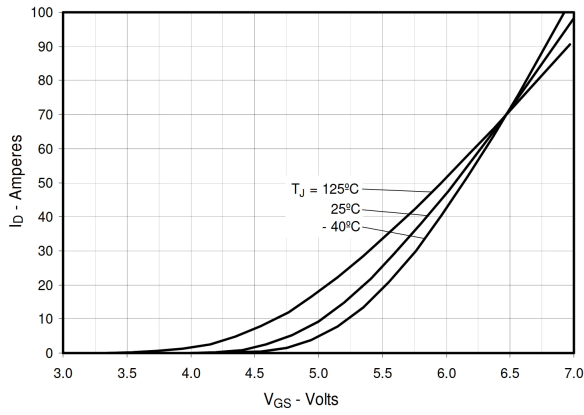


Fig. 2. Curve $I_D - V_{GS}$ - Extracted from the MOSFET model IXTT80N20L datasheet from IXYS.

may be damaged. This phenomenon is called hot spot, as shown in Fig. 3.

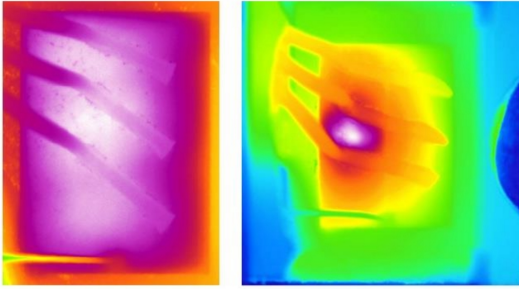


Fig. 3. Uniform temperature (left) and occurrence of hot spot (right). [21]

In short, from the fact that manufacturers do not disclose their testing methodologies for each device in a clear and accessible way, it is not possible to determine whether an SOA corresponds to the true behaviour of the device. As far as the authors could verify, it was not possible to find in the literature an exact method to overcome the unreliability of this information. In the following section, some practical recommendations are shown to alleviate all the aforementioned inconveniences.

III. CIRCUIT ASSEMBLY CRITERIA

In possession of the fundamental concepts and the basic topology of the circuit, it is necessary to define the components. In this section, the impacts that each of these aspects causes on the circuit are presented, leaving the designer to adapt the instructions according to his specific needs.

For the choice of MOSFET, given the difficulties presented above, some recommendations are shown. First, the chosen device must have operating limits greater than the maximum values of the magnitudes to which it will be subject. The maximum value of V_{DS} , for example, must be greater than the highest voltage of the source to be tested. Other maximum operating limits should also be evaluated at this initial stage.

If the device does not have the minimum capacity defined in this first analysis, it should be substituted.

A device with low thermal impedance should be chosen, aiming at a better thermal performance. A consultation of device datasheet shows that the lower the temperature to which the component is subjected, the greater the possible value to obtain for the drain current (I_D).

In scenarios where system reliability is an imperative requirement, it is recommended to obtain devices that are guaranteed by their SOA, which is usually indicated with the warning Guaranteed FBSOA (Forward Bias Safety Operating Area) printed on the device datasheet, or performing failure tests to determine the actual SOA of devices [19]. MOSFETs built with the purpose of continuous operation under conditions of high power dissipation are usually called linear MOSFETs [22]. As an example, there is the Linear L2 series from the IXYS manufacturer, which guarantees a SOA at a more realistic temperature of 75 °C for the encapsulation. Linear MOSFETs are a good choice for similar projects like shown in this work.

It is good practice to add safety margins to the design, with 20% being a common value for the current and voltage given as thresholds in the SOA for the device [19]. It is also recommended to add a margin of 20 °C to the [19] maximum junction temperature.

The control voltage (V_{in}) of Fig. 1 of the Op. Amp. can be obtained in different ways. In this work, a simple voltage divider consisting of a resistor and a potentiometer is recommended. Pay attention to the choice of resistance values, so that the polarization current of the Op. Amp., no matter how small, does not produce a significant load effect on the voltage divider. If the voltage node is used for other purposes (such as supplying other circuits) and suffers a load effect, it is recommended to use a series linear regulator (like a 78XX) to stabilize the supply voltage delivered to the voltage divider.

The offset voltage (V_{OFFSET}) in a Op. Amp., which can be seen as a voltage source of unknown polarity in series with one of the input terminals, can cause problems when you want to obtain very low current values. Once the Op. Amp. reference value is set to zero ($V_{in} = 0$), this effect takes on a major role and causes a voltage drop at least equal to the offset voltage across the sensing resistor. The minimum possible current value can be determined by knowing the sensor resistor values and the expected offset voltage by means of the component datasheet according to ((4)):

$$I_{MIN} = V_{OFFSET}/R \quad (4)$$

For illustration purposes, considering $R = 0.1 \Omega$ and using a Fairchild Op. Amp. LM741 with a maximum offset voltage of 6 mV, in the worst case, a minimum current of 60 mA. This analysis is important, as it may indicate the impossibility of the load being used in conditions of very low current, such as CR2032 batteries, or even the simulation of the load of very low power circuits, such as microcontrollers. To work around this problem, just use the device's offset correction terminals,

or even adopt an Op. Amp. model with a low offset voltage value.

Once the electrical power supplied to the FET is converted into thermal energy, its dissipation is essential to keep the device temperature within its maximum nominal values [23]. It is possible to calculate the junction temperature of the device using (5):

$$T_J = T_A + P(R_{\theta JC} + R_{\theta CD} + R_{\theta DA}) \quad (5)$$

where T_A and T_J are the ambient and junction temperatures, respectively; P is the power dissipated by the device; $R_{\theta JC}$, $R_{\theta CD}$ and $R_{\theta DA}$ are the thermal resistances from the junction to the device package, from the package to the heat sink and from the heat sink to the environment, respectively.

Since an electronic load is constantly exchanging electric energy to thermal energy a thermal analysis is imperative. Further details may be of interest such as low thermal resistance values for components and forced ventilation.

When choosing the voltage sensor resistor for the feedback, it is important to observe the relationship of this component with its temperature coefficient. Once the MOSFET reaches the user-given desired operating point, the resistance drift caused by heating the resistive element alters that operating point. In this regard, lower resistances and/or lower temperature coefficients in the sensing resistor would be desirable. The sensor resistor value also limits the maximum current that can be drawn from the SUT, since this element is in series with the circuit. On the other hand, a higher resistance value has the advantage of distributing the power dissipation between the transistor and the resistor. There is also concern about the robustness of the feedback signal. Low values may generate a feedback signal on the order of mV or less. In this scenario, some noise could contaminate the signal and cause the load to operate in an oscillatory manner, making it impossible to obtain a constant SUT current value. The decision on which of these parameters are most important for the equipment is up to the designer.

IV. EXAMPLE PROJECT

To demonstrate the recommendations of the previous section, calculations are shown for a project with the following specifications: voltage range between 0.5 V and 20 V; current range between 10 mA and 500 mA; and maximum power of 10 W. These values were arbitrated by the authors since there are no significant literature to compare the values to. As a starting point, the project starts with the basic circuit of Fig. 1, obtaining the input voltage from a voltage divider with a resistor and a potentiometer as suggested. The values of each of the components must be calculated using (1). For this application, a 100 k Ω resistor and a 1k Ω linear potentiometer are used. Since the highest voltage V_{DS} to which the circuit will be subjected is equal to 20 V, it is verified that the MOSFET IRFZ44N meets the specifications with a value of $V_{BD DS}$ greater than 20 v.

To find the power dissipation measures that must be taken, it's used (5) to determine the maximum thermal resistance. A

safety margin of 20°C is also used as previously suggested. The equation results in a maximum thermal resistance of 6.5 °C/W. This value indicates that the sum of all thermal resistances must not exceed this limit. Starting from the thermal resistance values found in the MOSFET datasheet, with a resistance between junction and encapsulation of 1.5 °C/W, a heat sink must be adopted whose value is less than or equal to 5 °C/W minus the value of the interface resistance between both components (arbitrated as 0.5°C/W). Choosing a model with thermal resistance equal to 4.35 °C/W and adding a fan to help with cooling ensures safe operation of the MOSFET for all operating regions with a total thermal resistance of 6.35 °C/W.

To reach the desired current range, it is necessary that the sensor resistor be calculated for the worst case, that is, when working with the lowest SUT voltage and the highest current is desired, that is, 0.5 V and 500 mA , respectively. For this purpose, use (6).

$$R_S \leq \frac{V_{MIN}}{I_{D MAX}} - R_{DS(on) MIN} \quad (6)$$

Based on the MOSFET datasheet, the minimum value of $R_{DS(on)}$ is 22 m Ω . The minimum voltage specified for the project is 0.5 V and the maximum current is 500 mA, so the sensing resistor value must be at most 0.978 Ω . Power must also be considered, so the resistor must have a dissipation capacity given by (7):

$$P_{DISS} \geq 1.2(R_S \times I_{D MAX}^2) \quad (7)$$

A margin of 20% is added to the power rating of the resistor. With the values in hand, we obtain from (7) a value of 0.03 W. The resistor available to the authors at the time of the project has a specification of 0.1 Ω - 5 W and, therefore, will be used in the circuit. Due to the large margin in dissipation capacity, the analysis with the resistor temperature coefficient will not be performed for this example project. If this analysis is necessary, the evaluation of the resistance deviation as a function of temperature is indicated by means of (8):

$$R = R_0(1 + \alpha(T - T_0)) \quad (8)$$

where R is the resistance at the temperature to be calculated, R_0 is the resistance at room temperature, α is the temperature coefficient, T is the temperature relative to the value R and T_0 is the ambient temperature.

The last element to be determined is the Operational Amplifier. As mentioned, the offset can be compensated for by the device's own offset terminals when available. The power supply available to the circuit is adjustable, so there are no restrictions on the choice. Thus, a simple model LM741 component was chosen for the circuit. With all the components selected, the final circuit obtained can be seen in Fig. 4.

All the results of the following section were obtained from the circuit discussed, presented in Fig. 4.

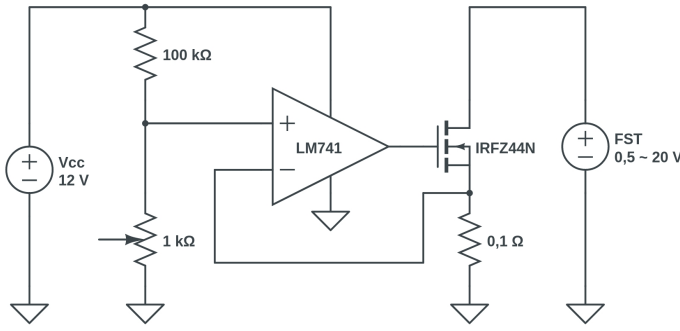


Fig. 4. Electronic load prototype.

V. RESULTS

In this section, the results related to the project are presented, such as cost estimation and experimental tests, envisioning some of the possible scenarios for using the electronic load.

A. Costs

The cost of the project boils down to its components: Op. Amp. LM 741 (R\$ 1.67); MOSFET IRFZ44N (R\$3.74); Resistor 0.1 Ω (R\$ 0.85); 100 k Ω resistor (R\$ 0.06); Potentiometer of 1 k Ω (R\$ 1.95). The total cost of the project was R\$ 8.27 or US\$ 1.72. The total cost of the project is low, considering that general-purpose components that are easily found commercially were used. To give a more appropriate evaluation on the cost comparison the price/watt of this work circuit and the refereed commercial units cited in the introduction are presented. This work proposal reached a value of 5.81 W/\$, the entry level model 8540 presents a value of 0.22 W/\$, and the more advanced model T3EL150302P a value of 0.23 W/\$. The proposed models presents a complete product case and displays, but the difference presents itself to a factor of begin 25 times more expensive for functionalities that may even not be useful for other research endeavours.

B. Test N. 1: Operation Check

Tables I and II show the current values, power dissipated in the MOSFET and equivalent resistance between drain and source obtained from tests with a SUT of 5 V and 20 V, respectively. Thus, it is intended to show the ability of the circuit to maintain different current values even with different SUT voltage values. As can be seen, the proposed circuit is capable of fulfilling all the previously mentioned design specifications. In the sequence, some examples of application for the electronic load are demonstrated.

C. Test N. 2: Battery Discharge Curve

A characteristic curve usually presented in battery datasheets is its discharge curve. As the name implies, the test aims to obtain the characteristic discharge curve of the energy storage element, for example, to determine its capacity. In Fig. 5, there is the discharge curve obtained in a different test, for an alkaline battery connected to the circuit. The test

TABLE I
TEST AT 5 VOLTS

MOSFET current	Power	$R_{DS}(eq.)$
10 mA	49.99 mW	499 Ω
50 mA	249.75 mW	99.9 Ω
100 mA	499 mW	49.9 Ω
200 mA	996 mW	24.9 Ω
300 mA	1.491 W	16.57 Ω
500 mA	2.475 W	9.9 Ω

TABLE II
TEST AT 20 VOLTS

MOSFET Current	Power	$R_{DS}(eq.)$
10 mA	199.9 mW	1999.9 Ω
50 mA	999 mW	399.9 Ω
100 mA	1.99 W	199.9 Ω
200 mA	3.99 W	99.9 Ω
300 mA	5.99 W	65.6 Ω
500 mA	9.97 W	39.9 Ω

lasted approximately 11 h, being performed with the electronic load adjusted to a current of 200 mA. It should be noted that this curve is in accordance with the one found in the battery datasheet, once again showing the correct operation of the circuit. The measurements presented were performed using the analog reading function (analogRead) of an Arduino Uno.

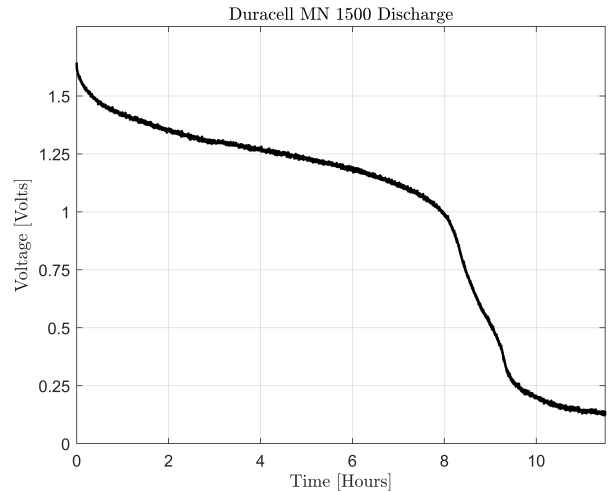


Fig. 5. Battery discharge curve - DURACELL MN1500.

D. Test N. 3: Noise measurement on a switched power supply

Switched mode power supplies (SMPS) usually have mechanisms to keep their voltage level constant even when subjected to loads of different powers. On the other hand, their respective noise level increases proportionally depending on the load. Table III shows the peak voltage values corresponding to the noise level obtained when testing a switched power supply model HP 0957-2146, with 16 V output and current limit of 625 mA, considering six different current values. Once

again, the test results denote the effectiveness of the proposed circuit in acting as an electronic load.

TABLE III
NOISE ON A SMPS OUTPUT

Current	Noise (peak voltage)	$R_{DS(eq.)}$
10 mA	11 mV	1599.9 Ω
50 mA	13 mV	319.9 Ω
100 mA	14 mV	159.9 Ω
200 mA	15 mV	79.9 Ω
300 mA	17 mV	53.2 Ω
500 mA	20 mV	31.9 Ω

VI. CONCLUSION AND FUTURE WORK

In this work, the basic design concepts for an analog electronic load in DC mode were presented. The design suggestions were explained considering their impact on the operation of the circuit, as well as the equations that relate the design parameters and their operating limits.

The main contributions of this work include:

- illustrated design decisions with their respective equations and comments on their effects;
- development of a prototype with reduced cost and complexity;
- development of an intuitive project road map.

In future works, it is intended to expand the concepts discussed here in order to also include the following aspects:

- modeling for transient regime and modification for alternating current operation;
- development of a prototype based on microcontrollers aiming to add new functionalities;
- inclusion of other electronic load operation modes;
- to discuss the increase in power dissipation capacity of the circuit.

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