



# Frequency Domain Multiplexing for Microwave Kinetic Inductance Detectors: Comparing the Xilinx ZCU111 RFSoc with the New 2x2 RFSoc Board

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## Abstract

The Xilinx ZCU111 Radio Frequency System on Chip (RFSoc) is a promising solution for reading out large arrays of microwave kinetic inductance detectors (MKIDs). The board boasts eight on-chip 12-bit / 4.096 giga samples-per-second (GSPS) analogue-to-digital converters (ADCs) and eight 14-bit / 6.554 GSPS digital-to-analogue converters (DACs), as well as field programmable gate array (FPGA) resources of 930,000 logic cells and 4,272 digital signal processing (DSP) slices. While this is sufficient data converter bandwidth for the readout of 8,000 MKIDs, with a 2 MHz channel-spacing and a 1 MHz sampling rate (per channel), additional FPGA resources are required to perform the DSP needed to process this large number of MKIDs, due to a mismatch between the data converter bandwidth relative to the FPGA resources of the ZCU111. A solution to this problem is the new Xilinx RFSoc 2x2 board. This board costs only one fifth of the ZCU111 while still providing the same logic resources, albeit with only a quarter of the data converter resources. Thus, using multiple RFSoc 2x2 boards would provide a better balance between FPGA resources and data converters, allowing the full utilization of the RF bandwidth provided by the data converters, while also lowering the cost per pixel value of the readout system; from approximately €2.50 per pixel with the ZCU111 to €1 per pixel with the 2x2.

**Keywords** Microwave kinetic inductance detectors · Kinetic inductance detectors · MKIDs · KIDs

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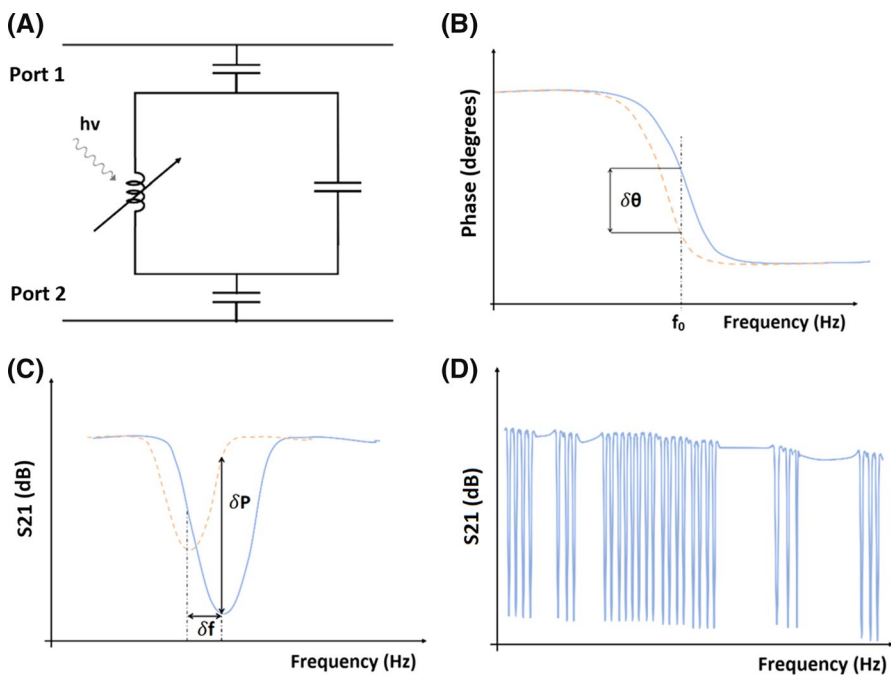
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## 1 Introduction

Microwave Kinetic Inductance Detectors (MKIDs) are low temperature detectors based on superconducting LC resonators [1] which exploit the kinetic inductance effect, with a wide range of applications [2]. Figure 1 displays their basic detection principle. Incident photons which strike the detector's inductor break superconducting Cooper pairs, and cause an increase in inductance, which causes the resonant frequency of the resonator to shift according to:

$$f_0 = \frac{1}{\sqrt{LC}} \quad (1)$$

When monitoring a single frequency, this shift in resonant frequency can be seen as either a change in the amplitude or the phase of the resonator's transmission. Because this shift is proportional to the number of quasi-particles formed, which is itself proportional to the energy of the incident photon, the phase shift is also proportional to the energy of the incident photon. This, along with the extremely low bandgap of superconductors, compared to semiconductors, allows the energy of



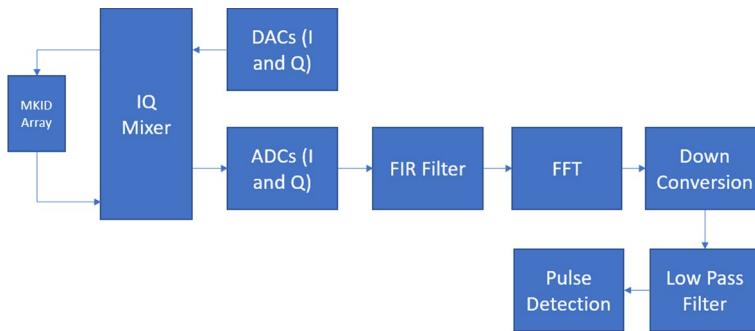
**Fig. 1** (Color figure online) MKID Detection Principle: A photon with energy  $h\nu$  strikes an MKID's inductor, which acts as its absorbing element (A). This causes a shift of both its phase (B) and amplitude (C). The energy of the incident photon can be resolved from these shifts. By fashioning an array of MKIDs, each with a unique resonant frequency, 1000s of MKIDs can be read out on a single feedline with minimal crosstalk between detectors (D)

incident photons to be determined by monitoring the phase of the probe signal driving an MKID, giving MKIDs their intrinsic energy resolution which is one of their key benefits.

While other low temperature detectors, such as transition edge sensors (TESs) (e.g. [3]) or metallic magnetocalorimeters (MMCs) (e.g. [4]), also have intrinsic energy resolution, they are difficult to scale up to large arrays, because they are not resonators, typically requiring the use of, for example, Superconducting Quantum Interference Devices (SQUIDS) to be multiplexed [5, 6]. MKIDs, however, which are resonators by their very design, can be designed as an array, whereby each resonator has a unique resonant frequency, suitably spaced from nearby frequencies, allowing a large array to be read out on a single feedline by using frequency domain multiplexing (FDM), without the need for any additional resonant components [1].

A benefit of this FDM readout is the minimisation of the required low temperature electronics. Typically, an array of thousands of MKIDS requires only a single high electron mobility transistor (HEMT) amplifier on a single feedline. However, this simplicity at low temperatures comes at the cost of requiring quite complex room temperature electronics capable of performing the complex digital signal processing (DSP) needed to separate the whole bandwidth of the array into a series of channels, with one channel for each pixel in the array, in order to monitor each resonator. In this project, MKIDs are being designed for the 4 to 8 GHz octave, with 2 MHz spacing between MKIDs.

In order to be read out, MKIDs need to be driven at their resonant frequency,  $f_0$ , given by Eq. (1). This is achieved by using digital-to-analogue converters (DACs) to generate a comb of signals at, typically, MHz frequencies. Signals are generated with both in-phase and quadrature (I and Q) components. Any imbalance in phase or amplitude between these I and Q components can be compensated using digital methods. These are signals of equal frequencies, one of which (Q) lags behind the other (I) by  $90^\circ$ . An IQ mixer board then upmixes these tones to GHz frequencies, such that there is a single tone for each MKID in the array, with the frequency of each tone being tuned to that of the corresponding MKID. The upmixed signal passes through the MKID array and upon exiting the MKID array is amplified at the 4 K stage by a HEMT amplifier, and at room temperature by a room temperature amplifier. After being amplified at room temperature, these signals are downmixed back to MHz frequencies using the same IQ mixer electronics and local oscillator (LO) as was used for the up-conversion, before being finally re-digitized by analogue-to-digital-converters (ADCs). The FPGA logic is then used to perform the channelization DSP on this digitized data. Channelization divides the entire frequency span into a series of equally spaced frequency bins, such that each frequency bin captures a single tone that couples to a single MKID in the array. This is done by applying a finite impulse response (FIR) filter and fast Fourier transform (FFT) to the digitized data, to achieve a polyphase filter bank (PFB). Each of these bands is then digitally downconverted (DDC) to 0 Hz, before a low pass filter is applied to remove any other tones. Each of these bands are then sampled at MSPS sampling rates and monitored for phase pulses which signify photon events. [7] Fig. 2 displays a possible implementation of an MKID readout system. Note that this is only one possible FDM implementation, and the number of resources utilized could be



**Fig. 2** (Color figure online) Possible MKID Readout Implementation

reduced by optimizing the FDM firmware design. It should also be noted that this implementation is for single photon counting MKIDs. For lower energy photons, it is impossible to detect individual photon pulses, and instead changes in photon flux are measured. As such, MKIDs operating in the far-infrared would require different readout methods.

Thus, in order to carry out this signal processing for large arrays of MKIDs, room temperature electronics consisting of DACs, ADCs, an FPGA and an IQ mixer board are required. MKID readout systems which have already been implemented to read out large arrays of pixels include the ROACH 1 [8, 9] and ROACH 2 [9, 10] boards. However, for even larger, next generation arrays of MKIDs, more powerful FPGA boards and faster data converters are required. One promising solution which is being explored at DIAS is the Xilinx ZCU111 Radio Frequency System-on-Chip (RFSoc) [11].

## 2 Xilinx ZCU111 RFSoc

The ZCU111 [11] is a radio frequency system-on-chip (RFSoc) developed by Xilinx. It boasts FPGA resources of 4,272 DSP slices and 930,000 logic cells. What is particularly appealing about this board is that it does not require external data converters, having eight on-chip 12 bit / 4.096 GSPS ADCs and eight on-chip 14 bit / 6.554 GSPS DACs on the same system-on-chip (SoC) as the FPGA. The on-chip format of the data converters and FPGA greatly reduces the size of this MKID readout system. Each feedline requires two ADCs and two DACs in order to sample both the I and Q components of the resonators' transmission. Thus, each feedline requires a pair of ADCs and a pair of DACs. With an ADC sampling rate of 4.096 GSPS and a pixel spacing of 2 MHz, this allows for 2,000 pixels to be read out on a single feedline, with the possibility for four feedlines. Thus, the ZCU111 has sufficient data converter resources to read out upto 8,000 MKIDs. However, while this is ample data converter resources to read out an array of 8,000 pixels, the FPGA resources are estimated to only be sufficient for processing approximately 4,000 pixels. This value is based on extrapolating from the pixel counts of the ROACH 1 and ROACH

2 boards, relative to the number of DSP Slices used in their firmware designs (see Table 1). Note that, while the ROACH 1 has 640 DSP slices, 319 are utilized in its firmware. Thus, the ZCU111 has the FPGA resources to only use half of the bandwidth of each ADC/DAC pair. Thus, in order to fully utilize the RF bandwidth provided by the ZCU111's data converters, additional FPGA resources are required.

### 3 Xilinx 2x2 RFSoc

The 2x2 RFSoc [12] is a low cost alternative to the ZCU111 released by Xilinx and HiTech Global as part of their University Programme. It should be noted that this board is only available to universities. While it contains the same FPGA resources as the ZCU111, it has only a quarter of the data converter resources, containing only two on-chip 12 bit / 4.096 GSPS ADCs and two on-chip 14 bit / 6.554 GSPS DACs. Significantly, the 2x2 board costs only one fifth of the price of the ZCU111, driving down the cost-per-pixel value of a potential MKID readout system. As it has an abundance of FPGA resources, relative to the data converter resources, the full 4.096 GSPS bandwidth of the ADC/DAC pairs can be used, in contrast to with the ZCU111, meaning that each board can read out 2,000 pixels.

### 4 Cost Per Pixel Values

One important metric which is used to evaluate MKID readout systems is their cost-per-pixel value. For example, the ARCONS [13] and DARKNESS [14, 15] arrays used ROACH 1 and ROACH 2 boards, respectively, to read out arrays of optical MKIDs, with cost per pixel values shown in Table 1.

As explained in Sect. 2, while the ZCU111 has ample data converter resources for reading out up to 8,000 pixels, the actual number of MKIDs which it is estimated to be capable of reading out is confined by the FPGA resources to  $\sim 4,000$  pixels. This is based on scaling up the pixel counts achieved by ROACH 1 and ROACH 2 relative to their FPGA resources. Thus, a single ZCU111, costing  $\sim \text{€}10,000$ , has a cost per pixel of  $\text{€}2.50$ .

However, the 2x2 RFSoc, having four times the FPGA resources relative to data converter resources, when compared to the ZCU111, allows for the entire RF bandwidth of the data converters to be used. Thus, a single 2x2 RFSoc, capable of

**Table 1** Readout Board Comparison

| Board     | Total Cost (€) | Pixel Count | Approx. Cost/<br>Pixel (€/pixel) | Logic Blocks | DSP Slices |
|-----------|----------------|-------------|----------------------------------|--------------|------------|
| ROACH 1   | 4,000          | 256         | 16                               | 7,360        | 640        |
| ROACH 2   | 4,000          | 1,000       | 4                                | 326,400      | 1,120      |
| ZCU111    | 10,000         | 4,000       | 2.50                             | 930,000      | 4,272      |
| 2x2 RFSoc | 2,000          | 2,000       | 1.00                             | 930,000      | 4,272      |

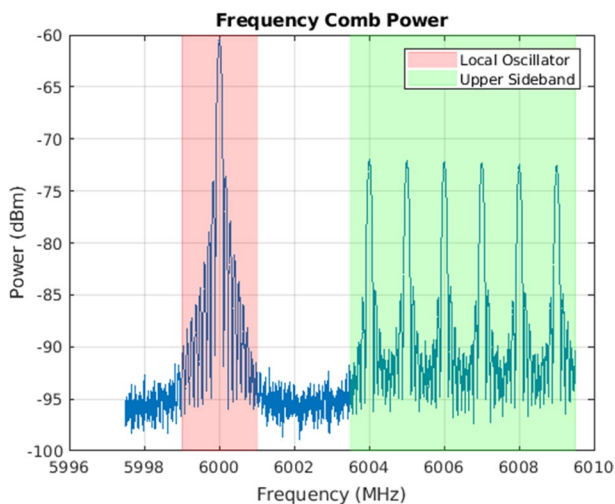
reading out 2,000 pixels and costing  $\sim$  €2,000, will have a cost per pixel of €1. This is summarised in Table 1. It should be noted that the costs detailed in this table for the ZCU111 and 2x2 RFSoc board are the costs for which they were purchased for this project. As of May 2022 the ZCU111 is priced at  $\sim$  € 10,300, and the 2x2 RFSoc is priced at  $\sim$  € 2,060.

## 5 Development Progress

Work is ongoing in the development of firmware and software for the reading out of arrays of MKIDs using the ZCU111. Moreover, a pair of 2x2 RFSoc's have been acquired and development will continue on these. As both boards use the same FPGA, adapting the firmware and software from the ZCU111 to the 2x2 should not cause any serious challenges.

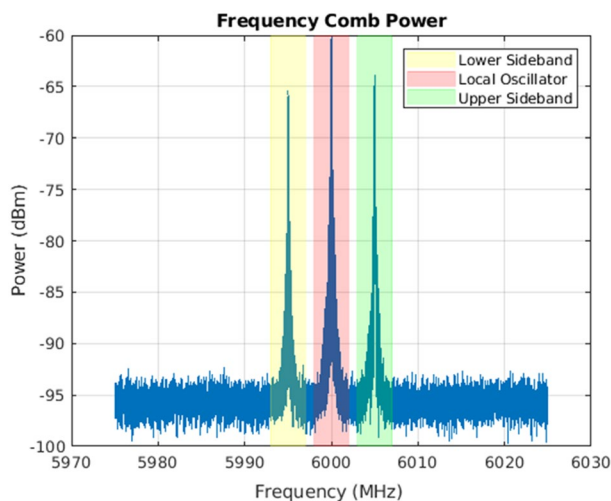
The firmware for the board is developed using Xilinx's Vivado package and the accompanying software is written in Python using the PYNQ framework. PYNQ uses Jupyterlab Python, running on the RFSoc, to create user friendly notebooks for writing to and reading from the Vivado generated firmware.

Current firmware developed for the ZCU111, using Xilinx Vivado, can be used to generate frequency combs using the board's DACs which are upmixed to GHz frequencies using an intermediate frequency (IF) mixer board. Similarly, signals which are downmixed back to MHz frequencies by the same mixer board are digitized by the boards ADCs. Programmable finite impulse response (FIR) filters and fast Fourier transforms (FFT) are then applied to these digitized signals, separating the frequency span into a series of channels. Xilinx's LogiCORE IP FIR Compiler [16] and FFT Compiler [17] are used to achieve this. This FFT compiler implements the Cooley-Tukey FFT algorithm [18]. Other FFT implementations are also available, which may improve resource utilization, such as the BxBFFT[19]. Clocking at 409.6 MHz, the signals are, typically, channelized using a 1024 tap FFT and 25 tap bandpass low pass FIR filter. The current firmware design is utilizing 24076 logic blocks, and 9 DSP slices. Estimates for the fraction of these resources used up by each part of the firmware were determined by compiling three separate firmware designs; one for controlling the data converters, one for implementing the FIR filter, and one for implementing the FFT. From these it is estimated that the data converters use approximately 13500 logic blocks and 0 DSP slices, the FIR filter uses approximately 4900 logic blocks and 2 DSP slices, and the FFT uses approximately 5800 logic blocks and 9 DSP slices. Figure 3 shows a frequency comb generated by the ZCU111's DACs at MHz frequencies and upmixed with the 6 GHz LO by the IF mixer board and measured using a vector network analyzer (VNA). Note that while it would have been preferable to use a spectrum analyzer for these measurements, there was not one available, and thus, instead a VNA was used in receiver mode. The frequency comb is generated by synthesising a sinusoid in Python for each frequency in the comb. Each of these sinusoids are then added together to generate the total frequency comb. This combined signal is then sent to the firmware where it is outputted by the DACs. These frequencies, as well as the power of the tones can be edited in Python by the user, without having to edit the firmware.



**Fig. 3** (Color figure online) Frequency Comb Generated at MHz Frequencies and Upmixed to  $\sim 6$  GHz Range Using ZCU111. Note that the relatively low powers outputted by the DACs are due to full range of the DACs not being used

Figure 4 shows a single 5 MHz tone upmixed to either side of the LO, thus giving the upper and lower sidebands. Upmixing a signal of frequency  $f_{\text{tone}}$  with a LO of frequency  $f_{\text{LO}}$  will generate frequencies at  $f_{\text{LO}} \pm f_{\text{tone}}$ , thus giving a signal at either side of the LO. As it is planned to operate on both sides of the LO, it is important to ensure that these sidebands don't degrade our performance by clashing



**Fig. 4** (Color figure online) Single Tone Upmixed to Either Side of 6 GHz Local Oscillator Using ZCU111

with resonators on the opposite side of the LO [10]. For example, a tone generated to probe a 6100 MHz resonator could interfere with another resonator at 5901 MHz. Thus, an ideal image reject mixer will suppress the unwanted sideband, mitigating this effect [20].

## 6 Conclusion

Work has been done developing firmware and software for the Xilinx ZCU111 RFSoc, implementing code to control the board's data converters, in order to generate frequency combs, which can then be upmixed with an external mixer board, as well as implementing FFT and filtering blocks needed to perform the channelization needed to read out arrays of MKIDs. However, it is concluded that the 2x2 RFSoc board offers a better balance between data converter bandwidth and FPGA logic resources. Because of this it is concluded that the 2x2 board provides a more affordable solution for reading out large arrays of MKIDs. Thus, next it is intended to also implement this firmware which was developed for the ZCU111 on the 2x2 RFSoc to provide a cheaper readout alternative.

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**Data Availability** The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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