SPAlink: A Flexible Bitstream Link for Class S-Power Amplifiers

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***Abstract* – In this paper a multi-platform HDL description of a circuit that implements all the digital processing and RF carrier generation for the class S Power Amplifier proposed by the Institute of Microelectronics and Wireless Systems is presented. The circuit is the combination of a lowpass sigma-delta modulation stage in series with a frequency shifting stage that generates the bitstream that drives a switch mode amplifier followed by a bandpass filter. This HDL description is that it can be implemented not only on high-end FPGAs but on low-cost devices as well. The 8 parameters that define at compilation time the final implementation are presented and four implementations are discussed in this work. The design is validated with data measured in the simulation and in the prototype.**

I. INTRODUCTION

Nowadays, the reconfigurable platforms offer enough power and flexibility to face heavy computationally demanding applications like digital signal processing for wireless base stations. Apart from high cost ASIC processor-based approach, the industry and the research community has adopted the core-based design methodology for system integration using FPGAs [1]. Taking into account the fact that FPGAs do not incur non-recurring engineering charges due to their reconfigurable nature, the number and diversity of the available Intellectual Propriety (IP) cores for digital systems composition have greatly increased [2,3]. This design flow simplifies and speeds-up the design of complex systems which allows very short time-to-market and facilitates custom device design for every industry and application.

In this paper a multi-platform HDL description for reconfigurable devices that implements all the digital processing and RF carrier generation for Wireless Base Station is presented. All power amplifiers are inherently nonlinear and traditionally the approach to linear RF power amplification is to back-off the output power of a Power Amplifier (PA) until distortion is reduced to an acceptable level. The process of backing-off the power significantly reduces the output power and efficiency but ensures linearity.

Numerous alternatives for linear power amplification have been proposed with each having various degrees of success. Envelope Elimination and Restoration (EER) is one method used [4]. One problem with this architecture is that intermodulation distortion can arise as a result of the significant difference between the delay in the RF phase path and the envelope magnitude path. Another efficient and linear PA design combines a square wave modulator with a switch mode PA such that the modulator transforms the varying envelope signal into square waves allowing the PA to be driven as a switch. Two different modulators used for this type of PA are RF Pulse-Width Modulator (RF-PWM) [5] and $\sum\Delta$ modulator [6]. In general the $\sum\Delta$ modulator is preferred since the PWM is not linear in itself and is more likely to require predistortion. As seen in [7], a bandpass $\sum\Delta$ modulator can be used directly with the PA. In this case the $\sum\Delta$ modulator is clocked at 4 times the RF frequency to modulate the RF signal and drive the PA. Serious design challenges are faced such as feedback in the $\sum\Delta$ modulator at 4 times the RF frequency. As a result this technique severely limits the maximum possible carrier frequency. In a polar transmitter a low-pass modulator can be used to switch the drain current on/off. For this implementation the switching rate must be close to the RF frequency, but switching at such high frequencies is difficult because of the large currents and large parasitic capacitances. In summary, either a complex modulator structure is chosen and must be driven at 4 times the RF frequency or alternatively the modulator has a simple structure, but must handle large currents and large parasitic capacitance. In both of these cases the implementation is close to impossible for RF frequencies [8].

In order to avoid these limitations, a class S PA is proposed by the research group of the Institute of Microelectronics and Wireless Systems (IMWS). It is composed of a combination of a lowpass or bandpass sigma-delta modulation stage in series with a frequency shifting stage and a switch mode amplifier followed by a band pass filter. The principle of operation is similar to the conventional class S PA, the primary difference between the two is the use of a frequency shifting stage in the proposed amplifier. The frequency shifting stage in the design takes the output of a $\sum\Delta$ modulator and shifts the desired signal to the RF carrier frequency using digital mixing.

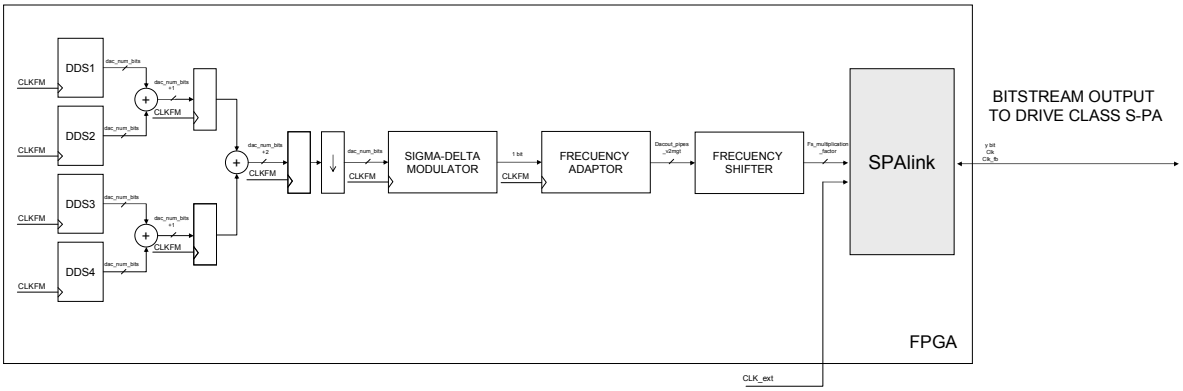

Figure 1: SPAlink block diagram.

Because of the frequency shifting operation, the ∑Δ modulator can use a sample frequency lower than the final output signal sampling frequency of the power amplifier. This enables the implementation of the modulator on currently available FPGAs. Another possibility made available with the proposed architecture is the option to use a lowpass modulator instead of a bandpass modulator, since it is the frequency shift stage that controls the carrier frequency of the output signal.

Taking into account the level of flexibility needed to experiment and verify this approach, a reconfigurable system is proposed for the prototype. Apart from proving the concept and validating and simulating the theoretical results, the purpose of this prototype is to explore a commercial and low cost solution. In the same field of research, many of the reported approaches are only validated by simulation [6,7,9] and if a prototype or a testing method is reported, they are more focused on concept proof: A down-scaled frequency prototype based on standard components is used in [8]. In [10] a pattern generator with and external serializer is employed for testing purposes. However, FPGAs are gaining acceptance for prototyping in the RF research field: In [11] a Virtex-4 FPGA is used for the generation of the envelope ∑Δ modulation (EDSM), but not for the RF carrier section. In [12] a Multi-Gigabit Transceiver is used for the generation of RF-PWM modulation.

In this paper we present a novel architecture to drive the class S PA proposed by the IMWS. It is parametrizable, scalable and it has been optimized for reconfigurable devices. It generates, modulates, shifts and serializes the signal up to real RF carrier frequencies. The 8 parameters that can be configured in compilation time define the final implementation. In a high-end FPGA, the Multi-Gigabit serial links embedded into these devices are used to synthesize binary RF signals, and in a low-cost FPGA high-speed differential links with dynamic clock adjustment capability are proposed for that task.

The remainder of this paper is organized into three sections. In Section II the circuit architecture is presented. Section III summarizes the implementation results in terms of FPGA resources and maximum achievable frequencies for the different options. In this Section results obtained from the simulation and in the prototype are presented. In Section IV, conclusions and future work in this area are covered.

II. ARQUITECTURE DESCRIPTION

Figure 1 represents the block diagram of the reconfigurable modulator instantiated for the generation of four fixed tones. The input signal of ∑Δ modulator is generated by four Direct Digital Synthesizers (DDS). The netlists and the models for these circuits are generated automatically by the Xilinx Core Generator [13,14]. This tool takes into account the target FPGA and refreshes all the output files if a different device is selected. The main DDS

Parameter	Description	Range
dac_num_bits	Bit width of of the modulator input	Same width as the DDS
fs_multiplication_factor	Multiplication factor for the frequency up-conversion	Variable for the parallel links and fixed for the MGT (20)
external_clock_feedback	External clock reference for clock compensation with parallel links	TRUE-FALSE
output_lvds	Differential or single-ended parallel link	TRUE-FALSE (Do not care for MGT)
IOSTANDARD_sel	I/O standard for the parallel link	SelectIO standards (Do not care for MGT)
VIRTEXIIPRO_MGT	Selection of the Multi-Gigabit-Transceiver high speed serial link	TRUE-FALSE (Only for V2PRO FPGA)
dacout_pipes_v2pmgt	Number of FFs needed to synchronize the output of the modulator with the serializer	2 for the MGT implementation
REF_CLK_V_SEL	Clock source for the MGT	1-BREFCLK 0-REFCLK

Table 1: HDL description parameters and generics.

parameters that can be selected in the compilation stage are: Clock Rate, Spurious Free Dynamic Range (from 18 up to 115 dB) and Frequency Resolution of the output signal.

Depending on the selected parameters, the bit width of the output signals changes to achieve the resolution needed. The HDL description of the proposed architecture automatically adjusts the different parameters that depend on that width. For example, the bit width of the ∑Δ modulator.

The outputs of the DDS are mixed in the circuit and the signal additions are pipelined in order to achieve the maximum admissible clock rate for the ∑Δ modulator. The architecture is scalable, so the number of DDS can be easily modified. Although these DDS have multichannel capabilities, for this platform the parallelization is preferred to not limit the frequency and quality of the generated sine wave. The DDS modules and the ∑Δ modulator run at the same CLKFM frequency, which should be as high as possible to enhance the behavior of the ∑Δ modulator for a given signal input frequency. As has been presented in Section I, the class S PA proposed by IMWS needs a bitstream that runs at the RF carrier frequency.
To achieve a bitstream in the RF GHz range, the proposed system takes advantage from the flexible SelectIO interfaces that the new low-cost FPGAs offer, like the Xilinx Spartan-3 family, and from ocketIO-MultiGigaBit Transceiver (MGT) hard core [15] embedded into the high-end Virtex-II FPGA families [16].

The module that implements the link to communicate the FPGA with the S PA is named SPAlink. The aim of the SPAlink is to provide a single VHDL description for the reconfigurable platform that allows implementations not only on high-end FPGAs, but on low-cost devices as well.

For the first group of FPGAs, depending on the requirements of the class S-PA circuit, different parallel links can be defined. For the second group, high-end FPGAs, the MGT is configured in a custom mode that will act as 20 bit shift register (hard fixed value). This hard core is clocked with a CLKFM/2 signal. Thus, it multiplies the frequency of the one bit ∑Δ modulator output by 10.

All the parameters (VHDL language generics) are defined at compilation time in the entity of the VHDL top level file. These generics define what portion of code of the VHDL description will be synthesized and implemented in each case.

Table 1 summarizes all the parameters that can be modified to obtain a custom implementation of the system. The flexibility that these parameters offer exploits the FPGA reconfigurability.
Figure 2 depicts the three basic architectures that can be implemented:

- **MGT link implementation:** This version uses the MGT embedded hard core

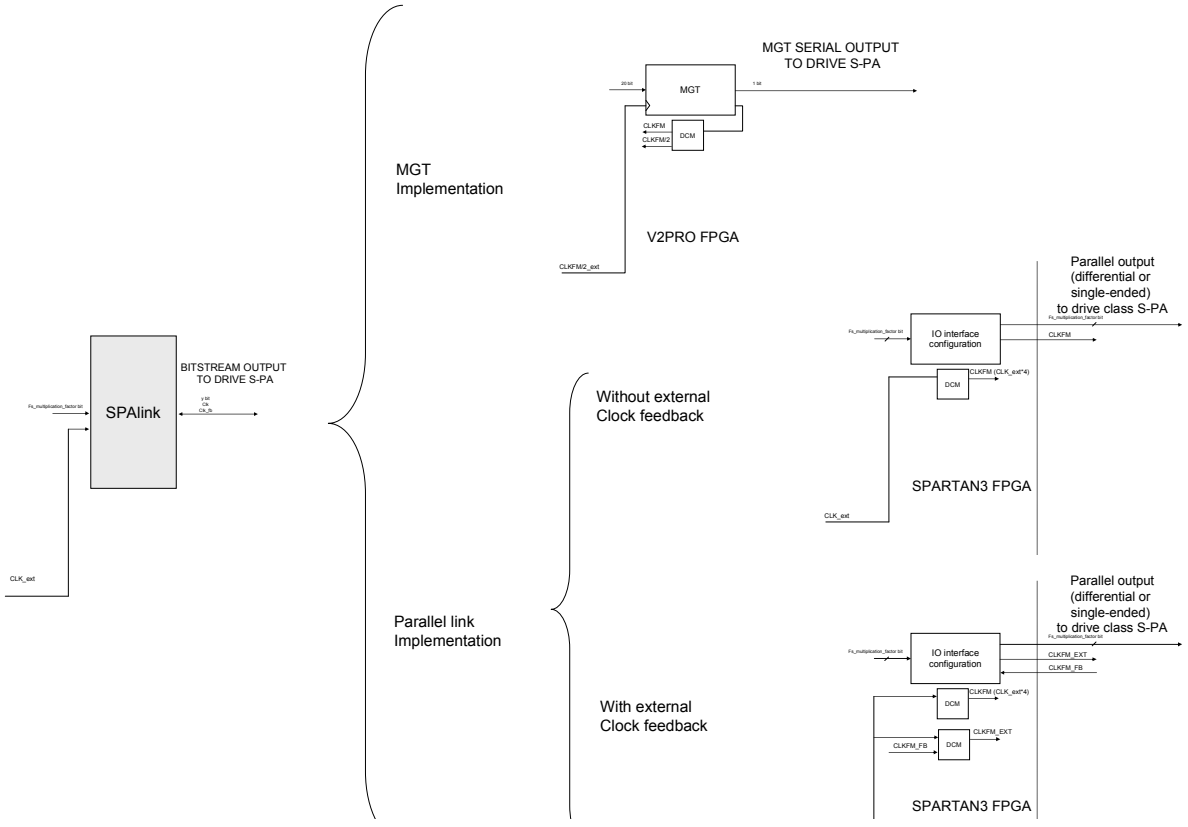

Figure 2: SPAlink basic implementations.

Resources	MGT link implementation (1st order ΣΔ modulator) Virtex-II Pro (XC2VP30FFG869-7C)	MGT link implementation (2nd order ΣΔ modulator) Virtex-II Pro (XC2VP30FFG869-7C)	Parallel link with external clock feedback implementation (1st order ΣΔ modulator) Spartan3 (xc3s200-5ft256)	Parallel link with external clock feedback implementation (2nd order ΣΔ modulator) Spartan3 (xc3s200-5ft256)
4 input LUTs	201 (1%)	215 (1%)	201 (5%)	612 (15%)
Slice Flip-Flops	233 (3%)	245 (1%)	227 (5%)	859 (22%)
Slices	136 (1%)	143 (1%)	131 (6%)	524 (27%)
BlockRAMs	4 (2%)	4 (2%)	4 (33%)	4 (33%)
Digital Clock Managers	1 (12%)	1 (12%)	2 (50%)	2 (50%)
Multi-Gigabit Transceivers	1 (12%)	1 (12%)	0 (N/A)	0 (N/A)
Maximum FM clock	216.4 MHz	207.5 MHz	190 MHz	160 MHz
Maximum FS clock (RF frequency)	1.084 GHz	1.0375 GHz	950 MHz	800 MHz
Class S PA link data rate	2.164 Gbps	2.075 Gbps	1.90 Gbps	1.6 Gbps

Table 2: Class S PA MGT driver Reconfigurable Platforms implementations.

SERDES. In this case, the link with the class S PA is a single differential pair.

- **Parallel link without external clock feedback implementation:** This option is focused on short parallel links. Also, the maximum clock frequency is limited by that path because the external clock for the parallel link is not measured and compensated internally. This option needs less connections and resources than the parallel link with clock compensation.
- **Parallel link with external clock feedback implementation:** This implementation offers the highest achievable clock frequencies for the parallel link when combined with a differential LVDS standard. The external clock for the parallel link is measured continuously by a Digital Clock Manager (DCM) inside the FPGA and synchronized with the FPGA internal clock.

III. IMPLEMENTATION RESULTS

The combination of the parameters presented in Section II allows multiple system configurations. In order to illustrate the viability of the proposed reconfigurable approach, four implementations are reported. The parameters in common to all implementations are the following:

- **DDS modules configuration:**
  - 10 bits output width (dac_num_bits).
  - 33 bits frequency data width.
  - 33 bits accumulator width.
  - 11 bits phase angle width.
  - 60 dB Spurious Free Dynamic Range.
  - 0.024 Frequency Resolution.
  - The DDS modules generate 4 sine vawes with the following frequencies: 1 Mhz, 1.2 Mhz, 1.4 Mhz and 1.6 Mhz.

The specific parameters for each pair of implementations are the following:

- **MGT link implementation:**
  - FPGA: Virtex-II Pro (XC2VP30FFG869-7C).
  - fs_multiplication_factor: 20.
  - output_lvds: N/A.
  - IOSTANDARD_sel: N/A.
  - dacout_pipes_v2pmgt: 2.
  - REF_CLK_V_SEL: 1-BREFCLK (Low jitter differential input clock for MGTs).

- **Parallel link with external clock feedback implementation:**
  - FPGA: Spartan3 (xc3s200-5ft256)
  - fs_multiplication_factor: 10.
  - output_lvds: TRUE (Differential output).
  - IOSTANDARD_sel: LVDS25 (2.5 V).
  - dacout_pipes_v2pmgt: 2.
  - REF_CLK_V_SEL: N/A.

For each option, two implementations are reported: One with a 10 bit first order ∑Δ modulator and another with a 10 bit second ∑Δ modulator.

Table 2 summarizes the implementation results for all the configurations. The maximum RF frequency that can be achieved with the selected parameters has been analyzed. The maximum achievable RF frequency (1.084 GHz) corresponds to the Virtex-II Pro MGT (1st order ∑Δ modulator) implementation while the slower RF carrier is generated by Spartan-3 (2nd order ∑Δ modulator) implementation.

In order to archive higher RF frequencies using the same devices, the complexity of the circuit can be decreased reducing the quality of the signal generated by the DDS modules and consequently the number of bits at the input of ∑Δ modulator. Another option is to increase the number of multiplication stages in the frequency up-converting stage. As a result of these modifications, the code efficiency in the RF modulation will be affected.

Depending on the application, the designer has to find a trade-off between the different parameters involved.

To aid the designer in this analysis, the system allows simulation in a `Virtual Platform' environment using Modelsim. The testbenches capture the input and output at the ∑Δ modulators and the high speed I/O channels (MGT or parallel) in binary files. The FFT representation of those sampled signals is generated using MatLab.

The implementation results support the viability of the proposed system to validate and implement the novel class S PA approach of the IMWS using conventional FPGA devices. Compared to other approaches, this approach is capable of achieving high RF frequencies without frequency down-scaling, like in the prototype proposed in [8], or without the use of external components for the frequency shifting stage like it is proposed in [11].

For the implementations that have been reported, the target boards are the Spartan-3 Diligent Development board and the XUP Virtex-II Pro Development system. The low cost of these boards for research groups enables the possibility of having multiple prototypes and future expansions and enhancements of the proposed system.

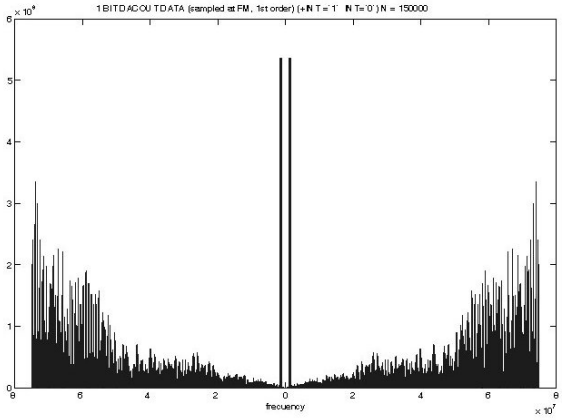

Figura 3: FFT of the signal at the output of the 1st order ∑Δ modulator (Virtual Platform).

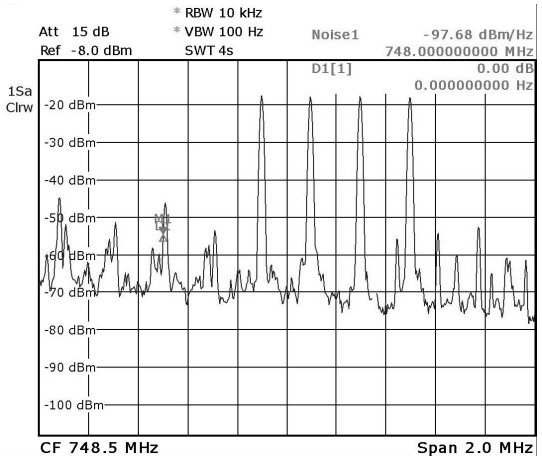

Figura 4: FFT of the involved main signals (CLKFM=150 MHz).

In order to illustrate the functionality of the proposed reconfigurable system the simulation and experimental result for a given configuration are presented. The parameters values for this application are as follows:

- **DDS modules configuration:**
  - 1st order ∑Δ modulator.
  - FM Clock=150 MHz and RF Frequency= 750MHz.
  - 14 bits output width (dac_num_bits).
  - 33 bits frequency data width.
  - 33 bits accumulator width.
  - 11 bits phase angle width.
  - 80 dB Spurious Free Dynamic Range.
  - 0.024 Frequency Resolution.
  - The DDS modules generate 4 sine vawes with the following frequencies: 1 Mhz, 1.2 Mhz, 1.4 Mhz and 1.6 Mhz.

Figure 4 depicts the output of the 1st order ∑Δ modulator for the implemented versions. These representations have been obtained using the `Virtual Platform'.

The screenshot of the Spectrum Analyzer (Figure 5) represents the desired modulation in the RF frequency generated in the MGT channel.

IV. CONCLUSIONS

In this paper a multi-platform HDL description of a circuit that implements all the digital processing and RF carrier generation for the class S PA proposed by the Institute of Microelectronics and Wireless Systems has been presented.

The 8 parameters in combination with the MGT implementation allow a huge number of experimentations and introduce new research challenges for future works in this field. The implementations using low-cost FPGAs validate the class S PA of the IMWS for commercial applications.

The proposed platform allows simulation using Modelsim. The `Virtual Platform' includes the HDL description, models and testbenches needed to analyze all the main signals using MatLab. This complete simulation flow offers a invaluable validation tool for the researchers and engineers for the tasks of parameter selection and analysis of the results.

The data measurements made on the evaluation boards prove the theoretical approach with a preliminary configuration. Future works includes: the implementation of higher order ∑Δ modulators, enhancements in the frequency shifting stage and the addition of a signal feedback for correction of Power Amplifiers non-linearities.

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