Analysis and design of oscillators based on low-voltage self-oscillating active inductors

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Abstract — **This paper presents a new consistent analysis of self-oscillating active inductors together with a complete design example of a 90 nm CMOS current controlled oscillator (CCO) for ISM applications. Using the proposed passive compensation method in place of a standard negative impedance converter, typical performance of active inductor oscillator is achieved with reduced static power consumption. The article presents a small signal, large signal and phase noise analysis of the proposed oscillator together with related design trade-offs. Theoretical results are confirmed by a simulation of current controlled oscillator designed using UMC 90 nm 1P9M RF process libraries. The proposed circuit achieves a relative tuning range of 26% with a 434 MHz carrier frequency and average in band phase noise of -92 dBc/Hz at 1 MHz offset. The maximum power consumption of the oscillator core is only 2 mW from a 1 V supply.**

Keywords — **Active inductors, negative resistance oscillator, current controlled oscillator, CMOS, RF circuits, LTI phase noise model.**

I Introduction

The design of compact integrated sinusoidal oscillators at sub-GHz frequencies is a challenge when using standard commercial CMOS process. Firstly, on-chip passive LC resonators suffer from a relatively low quality factors that inevitably increase phase noise and power consumption. Secondly, the required capacitance and inductance values in the range of few nH and pF force designers to sacrifice significant silicon area. Finally, in a modern sub-micron processes, the performance of spiral inductors and capacitors is optimised for higher frequencies at the cost of its reduction in sub-GHz band.

Historically, active inductors (capacitively loaded gyrators, Figure 1) became a potential alternative to passive tanks due to a compact size and inherent electronic control over simulated inductance [1]. This solution is not free of its own problems. Noise performance is much worse than of a passive counterpart due to the use of transistors. Also, the non-linear character of

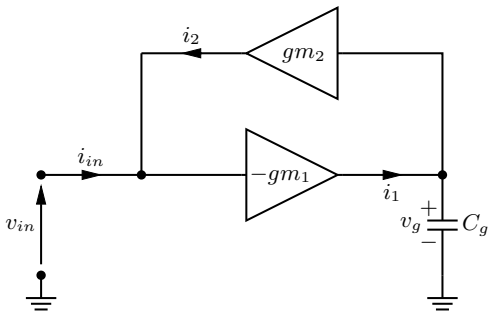

Fig. 1: Ideal active inductor.

amplifiers reduces maximum amplitude swing and the dynamic range of active resonator is restricted. Abidi [2] proves that both noise and dynamic range are inversely proportional to quality factor of active inductor. This behavior is contrary to the one of a standard LC resonators, proving that gyrators should not be considered as an analog of its passive counterparts, especially in a presence of large signals. In fact, to maximise a circuit performance, the quality factor of active

inductor resonator have to be low, as opposed to a common practice of designing high Q circuits employing spiral on-chip inductors. In terms of gyrator-based oscillators, as shown by Crainckx in [3], phase noise level of active inductor oscillator is also proportional to the resonator Q.

Low Q factor of active inductor resonator is manifested as fast attenuation of the signal. To sustain oscillations, typically an additional negative resistance is connected to the tank. This method requires static power proportional to the amount of looses in the resonator as well as the capacitance value of the tank [4]. Thus, in the case of a low Q active inductors, standard compensation methods are not power efficient, especially with modern low-voltage CMOS processes.

This paper presents an alternative method of active inductor compensation, based on passive RC components that do not require any additional static power. In Section II the concept of proposed approach is explained. Also, a small signal parameters and oscillation conditions are derived. Section III describes effects caused by large signal swings, with emphasis of amplitude stabilisation mechanisms. Section IV presents a simplified LTI (linear time invariant) phase noise model, that within its accuracy, shows a practical limitations of phase noise performance for a self-oscillating gyrator oscillator. Finally, Section V contains a complete, experimental 434 MHz CMOS CCO design with detailed simulation results.

II Active inductor with negative resistance

a) *High frequency parasitic effects of non-ideal transconductors*

Moulding [5] observed that at a high frequencies, non-ideal transconductors generate additional negative conductance. Figure 2 illustrates a gyrator-based tank, where amplifier parasitics manifest itself in a form of an arbitrary phase lag of $\phi/2$ radians of each transconductor. This is a result of finite resistive losses and the parasitic capacitances of transistors and biasing network. It is assumed that ϕ, although not negligible, is small enough to satisfy the condition of $\sin(\phi) \approx \phi$. If $\phi \leq \pi/10$ and $G_{o1} \ll gm_1, gm_2$, the input admittance is approximately equal to

$$y_{in}(j\omega) = G_{o2} + j\omega C_t + \frac{gm_1 gm_2}{G_{o1} + j\omega C_g} e^{-j\phi} = \approx G_{o2} + j\omega C_t + \frac{1}{R_s + j\omega L_s} - \frac{\phi}{\omega L_s} \quad (1)$$

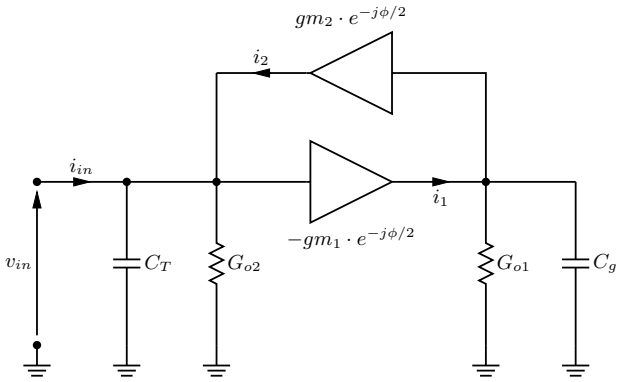

Fig. 2: Active inductor resonator with lossy transconductors.

where

$$R_s = \frac{G_{o1}}{gm_1 gm_2} \quad (2)$$

$$L_s = \frac{C_g}{gm_1 gm_2} \quad (3)$$

An additional parallel negative resistor of $-\phi/\omega L_s$ is now present in the circuit. If not sufficiently suppressed, it causes resonator peaking at higher frequencies, and in extreme cases leading to instability [6].

b) *Concept of degenerated active inductor*

By approaching the problem of non-ideal transconductors from a different perspective, the unfavorable effect causes total compensation of gyrator losses, theoretically producing oscillations without any additional active circuit. As transistor parasitics are hard to control, this compensation method can not fully rely on device non-idealities. Instead, it is possible to generate a negative resistance inside a gyrator tank with the help of an additional phase lag network, while a transconductor parasitics are kept minimal at a frequency of the interest.

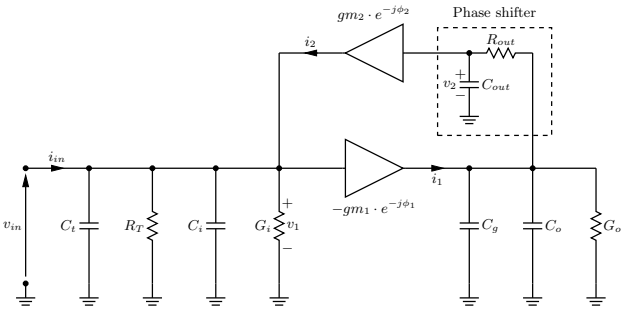

Fig. 3: Non-ideal degenerated active inductor resonator.

Figure 3 depicts a degenerated gyrator tank with an additional phase shifter at the output port of active inductor. G_i and G_o represent a total conductances at input and output nodes and consists

of resistive losses of transconductors as well as the real part of the input/output admittances of amplifiers. Similarly, C_i and C_o characterise total node capacitances due to a reactive parasitic components. Respectively, R_T and C_t represent a parallel resistance and capacitance of the resonator from additional components connected to the gyrator (output buffer, for example). The phase shifter required for negative resistance generation is achieved by using R_{out} and C_{out}. Phase shifts of both transconductors, denoted by ϕ_1 and ϕ_2, are assumed to be negligible at sub-GHz frequencies.

The choice of single phase shifter and its position in the circuit is not arbitrary. There are three possible cases: two phase shifters at each end of gyrator; a single shifter at input node; or an output shifter. From the oscillator perspective first two solutions are not optimal. Two RC circuits double the noise of a single phase shifting network. Also, the circuit suffers from a self-resonance caused by an additional product of two shifters. If a single RC network is used at the input node, the observed negative resistance tends to be more sensitive for frequency changes and has a smaller inductive bandwidth than in the case of our chosen solution.

The input admittance of the proposed active resonator with output shifter is given by

$$\begin{aligned} y_{in} &= \frac{1}{R_T} + G_i + G_{pdg}(\omega) + j\omega C_T + \frac{1}{\omega L_{pdg}(\omega)} = \\ &= \frac{1}{R_T} + G_i + \\ &+ \frac{gm_1 gm_2}{C_G\left(\omega_{z1} - \dfrac{\omega^2}{\omega_{z2}}\right)\left(1 + \dfrac{\omega^2\omega_{z2}^2}{\left(\omega_{z1}\omega_{z2} - \omega^2\right)^2}\right)} + \\ &+ j\left(\omega C_T - \frac{gm_1 gm_2}{\omega C_G\left(1 + \dfrac{\left(\omega_{z1}\omega_{z2} - \omega^2\right)^2}{\omega^2\omega_{z2}^2}\right)}\right) \end{aligned} \tag{4}$$

where

$$C_T = C_t + C_i \tag{5}$$

$$C_G = C_g + C_o + C_{out}(1 + R_{out}G_o) \tag{6}$$

$$\omega_{z1} = \frac{G_o}{C_G} \tag{7}$$

$$\omega_{z2} = \frac{C_G}{(C_g + C_o)\, C_{out} R_{out}} \tag{8}$$

Equation (4) consists of four terms: input conductance, total tank capacitance, simulated parallel inductance $L_{pdg}(\omega)$ and an additional conductance $G_{pdg}(\omega)$ with a negative factor. Note that, both simulated inductance and negative conductance depend on frequency, bias conditions, phase shifter components and circuit parasitics.

c) Oscillation criteria

In general, the criteria for oscillation of any negative resistance oscillator are divided into amplitude and phase conditions, as in the case of Barkhausen criteria for feedback oscillators [7]. The amplitude condition allows one to find parameter values for which total conductance (or resistance) of the resonator becomes negative. Similarly, a phase condition reveals circuit parameters for which a total susceptance (or reactance) of the tank is zero.

Both conditions are found directly from (4). Results can be simplified, assuming that resonator losses are dominated by a gyrator input losses $G_i + 1/R_T \approx G_i$. In simple, two transistor gyrators, where both amplifiers have the same gm and the gm to g_{out} ratio is large enough, then generally $G_i \approx gm$ is observed. In this case, the amplitude condition is approximately equal to

$$gm + C_G\left(\omega_{z1} - \frac{\omega^2}{\omega_{z2}}\right)\left(1 + \frac{\omega^2\omega_{z2}^2}{\left(\omega_{z1}\omega_{z2} - \omega^2\right)^2}\right) \leq 0 \tag{9}$$

The phase condition reveals the resonant frequency of the circuit by finding real and positive root of $\Im\{y(j\omega)\} = 0$ from (4)

$$\omega_0 = \frac{\sqrt{2}}{2}\omega_{z2}\sqrt{\sqrt{1 - 4\frac{\omega_{z1}}{\omega_{z2}} + 4\frac{gm_1 gm_2}{\omega_{z2}^2 C_G C_T}} + 2\frac{\omega_{z1}}{\omega_{z2}} - 1} \tag{10}$$

where corresponding parameters are defined by (5)-(8).

d) Tunig range

The theoretical tuning range of the proposed oscillator is defined by the parameter values for which (9) and (10) are fulfilled at the same time. Analysing total conductance from (1) it can be observed that the negative conductance decreases with frequency mostly due to a low-pass character of RC phase shifter. On the other hand, at low frequencies, the output conductance of amplifiers becomes dominant, effectively cancelling the negative conductance effect. For a wide band operation of the oscillator this conductance should be as small as possible, which in turn requires a transconductance amplifiers with large gm to g_{out} ratio. For this reason, the use of minimum size transistors is not optimal.

III Large signal behavior

In general, gyrator circuits are non-linear and increased signal amplitude inevitably leads to harmonic distortion. Kaunisto [8] shows that harmonic effects usually deteriorate the performance

of active inductor resonator far before the voltage headroom limit of the transconductance amplifier is reached. This is caused mostly by a feedback in gyrator circuit where both amplifiers start to drive each other with distorted signals. Depending on the type of transconductor non-linearities, increasing signal amplitudes cause either expansion [8] or compression [4] of simulated inductance. Thus, in the presence of large signal swing, instantaneous resonant frequency of the tank varies similarly to one of a standard LC tank employing varactors.

In the degenerated active inductor resonator, large signals cause harmonic compression of negative conductance $G_{pdg}(\omega)$ (due to odd-order harmonics). During oscillation build-up, the circuit starts to diverge from a small signal behavior and, at a certain level, the amplitude condition is violated. The resonator becomes dissipative and the oscillation amplitude settles at this point. It is observed that signal amplitude and distortion are proportional to the magnitude of negative conductance margin required to start oscillations. If the start-up margin is low, then the signal amplitude is relatively small. This in turn increases phase noise of the oscillator due to a limited RF power of the generated carrier. For an excessive margins, resulting signal becomes highly distorted before its amplitude is limited. Typically, a standard margin of 2 is a practical choice between available amplitude and resulting distortion.

IV Phase noise performance

The phase noise of self-oscillating active inductor can be modeled using LTI method used in a past by Razavi for ring oscillators [7] and by Cranickx for standard gyrator resonators [3]. Although less accurate than, the more time consuming, LTV (linear time variant) method of Hajimiri and Lee [9], it allows for a much quicker estimation of phase noise performance of the presented oscillator. To derive the proposed LTI model, noise sources have to be known as well as a corresponding noise transfer functions. To simplify analysis it is assumed that only a single MOS transconductors are used and are characterised only by a thermal noise. In the degenerated active inductor described here, three main sources can be distinguished, two from a transconductance amplifiers and the third one from a phase shifter resistor. A thorough analysis of noise properties of RC compensated resonators can be found in our previous work [4].

In the oscillator, each of the described noise sources contribute to $S_{out}(\omega_m)$ - the output noise power spectral density (PSD) of oscillator signal. To calculate phase noise at frequencies ω_m close to the carrier, each of the noise transfer functions $H_n(\omega_m)$ is linearised using Taylor series [7]

$$H_n(\omega_m)\Big|_{\omega_m \ll \omega_0} \approx H_n(\omega_0) + \omega_m \frac{\partial H_n(\omega)}{\partial \omega}\Big|_{\omega=\omega_0} \tag{11}$$

and multiplied by PSD of a corresponding noise source. The phase noise is then calculated using the formula for a normalised theoretical one-sided spectrum of oscillator signal [10]

$$L(\omega_m) = \frac{S_{out}(\omega_m)}{V_{out}^2/2} \tag{12}$$

where V_{out} is the amplitude of oscillator signal. Note that the total noise (i.e. both phase and amplitude noise) at offset frequency is calculated. This methodology combined with the results of the detailed noise analysis from our previous work [4] and model parameters from (4), the output noise PSD of a degenerated active inductor oscillator, at frequencies $\omega_m \ll \omega_0$ is given by

$$S_{out}(\omega_m) \approx \frac{kT\gamma}{\left(1+\frac{C_T C_G}{gm_1 gm_2}\cdot\frac{\omega_0^4}{\omega_{z2}^2}\right)^2}\left[\frac{gm_2}{\omega_0^2 C_T^2}+\frac{1}{gm_1}+\right.$$
$$\left.+\frac{1}{gm_1^2 R_{out}}\left(1+\frac{gm_1 gm_2}{\omega_0^2 C_T C_G}\right)^2\right]\cdot\frac{\omega_0^2}{\omega_m^2} \tag{13}$$

where k is Boltzmann's constant, T is temperature in Kelvins, γ is a process dependent noise constant and the rest of parameters are taken from (5)-(8).

The LTI model given by (13) allows us to estimate the theoretical phase noise performance of degenerated gyrators. For the parameters chosen for the circuit design presented in Section V, an estimated phase noise levels are in the range of -100 dBc/Hz at 1 MHz offset from 434 MHz carrier. In practice, the phase noise level will be at least 5 dB worse, because presented LTI model does not account neither for a time variant oscillator behavior nor a non-linear noise conversion effects. The estimated phase noise performance is limited by two factors. Firstly, as any active inductor, the proposed circuit generates significant levels of noise. Secondly, using a low-voltage power supply, active loads and harmonic distortion bound effectively available signal amplitudes.

V CCO circuit

Figure 4 depicts the proposed CCO circuit designed using UMC 90 nm 1P9M RF process libraries. The oscillator consists of a gyrator core, 1:1 matched current mirrors and an output buffer driving 50 Ω load. All of the component values are attached, including total width and length of MOS transistors.

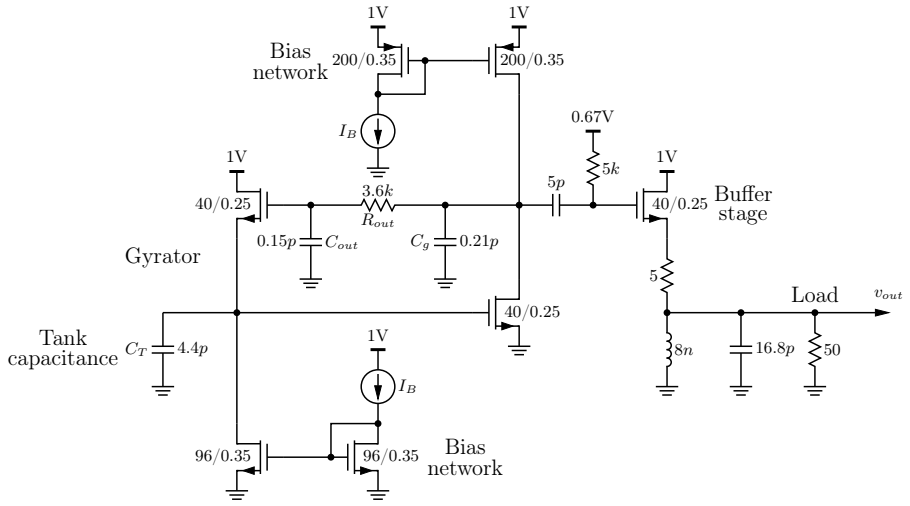

Fig. 4: ISM 434 MHz current controlled oscillator with output buffer.

a) Oscillator core

The oscillator core consists of a standard common drain and common source amplifiers connected in a feedback loop through phase shifter $R_{out}C_{out}$. Each amplifier is biased using current mirrors that for matching and noise purposes do not use minimum size transistors. R_{out} is a polysilicon resistor optimised for RF frequencies. All of the capacitors shown are high-Q MIM capacitors. Tuning of the oscillator is achieved by controlling the bias current I_B simultaneously for both mirrors, which allows to keep $gm_1 \approx gm_2$. The output buffer is connected to the output port of active inductor to exploit a larger signal amplitudes at the common source transconductor output.

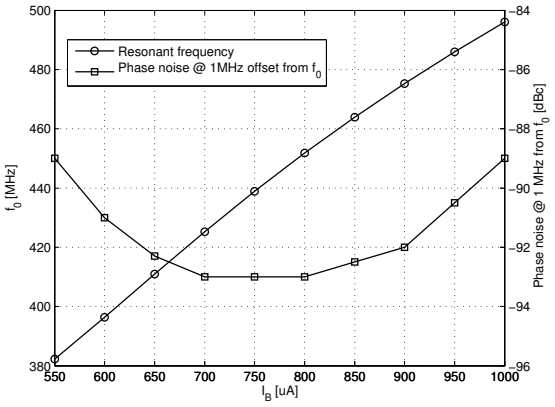

Fig. 5: Tuning curve and phase noise performance.

b) Output buffer

The output buffer is a class-A, tuned source follower with passive inductor to maximise a voltage headroom. The resonant tank is tuned to 434 MHz and modelled as off-chip due to a poor Q factor of an available spiral inductors at frequencies of interest. This external tank allows also to minimise possible buffer instability normally caused by a capacitive loads of followers. Note that this resonant tank does not affect signal generation mechanism of the core. An additional 5 Ω resistor is used to improve stability of an amplifier. Transconductance of the buffer is in the range of 20 mA/V. This causes a 3 dB power loss in the case when $gm >> 1/R_L$ but requires less static power in a presence of low impedance load.

VI Simulated results

The circuit was modelled in Eldo RF using transient and autonomous steady state simulations with noise. The results are depicted on Figures 5 and 6. Obtained tuning range of 113 MHz provides a sufficient margin for process variations and exhibits linear tuning curve. The phase noise performance is typical for an active inductor oscillators and reaches a local minimum of -93 dBc/Hz at a nominal resonant frequency and it is only 7 dB worse than predicted by a simplified LTI model from (13). The characteristic increase in phase noise at the both ends of tuning range is caused by reduced signal amplitude due to a smaller negative conductance margin at this frequencies. The low harmonic distortion of output signal is retained using class-A buffer stage by the cost of increased power consumption.

Table 1 presents various circuit parameters extracted from the simulation results. The available RF power at 50 Ω is equal to -10 dBm with only 1.5 mW of core power used to generate the signal with harmonic distortion of 2.8%. In addition, the start up time for this oscillator is short, in the range of 10 ns, which makes it an ideal candidate for on-off keying (OOK) modulation schemes.

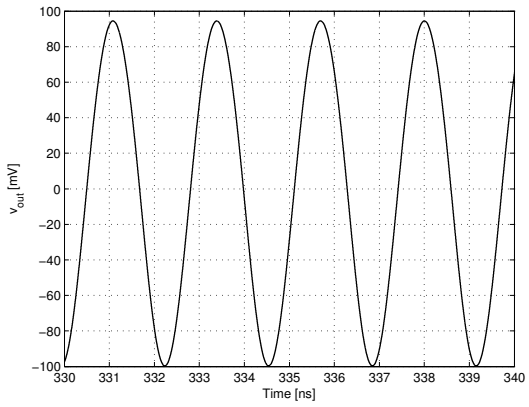

Fig. 6: Simulated output voltage at 434 MHz.

Table 1: Simulated circuit parameters

Symbol	Parameter	Value	Unit	Comments
VDD	Supply voltage	1	V	
I_B	Bias current	550	µA	min
		750		nominal
		1000		max
f_0	Frequency	382	MHz	min
		434		nominal
		495		max
Δf	Tuning range	113	MHz	
		26	%	at nominal f_0
PN	Phase noise	-93	dBc/Hz	at 1 MHz offset from nominal f_0
P_{RF}	RF power	-10	dBm	50 Ω load 3 dB buffer loss
THD	Total harmonic distortion	2.8	%	from amplitude definition
t_{up}	Start-up time	10	ns	at nominal f_0
P_B	Buffer power consumption	6.5	mW	
P_C	Oscillator core power consumption	1.1	mW	min
		1.5		nominal
		2		max

VII Conclusion

In this paper we have presented a new, consistent analysis of self-oscillating active inductors. Small signal oscillation criteria are derived, together with an explanation of a large signal behavior. A simple phase noise model is presented, providing a practical insight into the limitations an noise mechanisms of the proposed circuit. Using the presented RC compensation technique, a typical performance of a standard active inductor oscillator is achieved without the use of any additional active circuit and excessive power consumption. Theoretical results are confirmed by a thorough simulation of integrated current controlled oscillator, offering a novel approach for subsequent development of integrated oscillators.

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