Parallelization of Bandpass Sigma-Delta Modulators for Class-S Digital Power Amplifiers

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***Abstract*—In this paper a new technique of utilizing parallel sigma delta modulation for high frequency switch mode digital power amplifiers is presented. This approach allows achieving a factor of two increase of a digital logic speed for band-pass SDM with minor adjustments made. A universal scheme for a SDM system transformation is provided. Since the transformation scheme is established, a parallel low-pass SDM, expandable to a factor of four clock frequency reduction is designed. The parallelization of a low pass SDM however requires modification on the form of a Noise Transfer Function in order to preserve desired speed of a digital logic. This can affect the overall performance of the SDM. The derivation of the systems is provided through analysis of discrete time domain equations. The method is validated through simulations.**

I. Introduction

Sigma-delta modulators have been used widely in analog and digital signal conversion [2]. Recently there has been an interest in using sigma-delta modulators (SDM) for direct digital to RF conversion in switched-mode power amplifiers (SMPA), offering the potential for superior linearity and efficiency [3], [4]. One of the more challenging aspects of using modulators for digital power amplifiers is the need for high oversampling ratios and high-speed clocked outputs - for modern communication systems, the required digital processing speeds are beyond what is economically available [4]. The need for a high oversampling ratio in sigma-delta modulators is well known as a direct factor affecting the degree of noise shaping that is possible and thus the overall dynamic range.

The sampling frequency however has additional roles, namely in determining the coding efficiency [3] of a switch mode power amplifier.

Coding efficiency (1) is a term used to express the ability to extract the signal power from the overall pulse-stream. It is independent of efficiency but impacts on the sizing of the circuit implementation.

The relation between a sampling frequency and a continuous time coding efficiency is derived from a convolution of a discrete time sample with a square pulse - being the impulse response of a digital to analog converter. Power of the output signal depends on the square pulse duration T_S, which is directly related to a sampling frequency of a SDM by $T_S = 1/f_S$. Deducing from [8] for an ideal square pulse (zero rise time, zero fall time) a continuous time coding efficiency can be expressed as

$$\eta_{CT} = \frac{p_{IN}}{p_Q}\left(sinc\left(\frac{f_C}{f_S}\right)\right)^2 \quad (1)$$

Where p_{IN} is a power of an input signal, p_Q is a power of a discrete time SDM output, the f_C is a carrier frequency of the signal. The sampling frequency has therefore significant role in a sigma-delta driven SMPA, affecting the overall power efficiency of the device, Fig.1. A choice for optimal $\frac{f_C}{f_S}$ ratio usually oscillates in a range of 0.25 to 0.33 [5], [3], implying the desired sampling frequency f_S $3GHz$ to $4GHz$ for a carrier frequency $f_C = 1GHz$. A number of methods of increasing the output frequency by parallelization of SDM blocks can be found in literature. In [6], the authors developed a method of parallelization for SDM based on digital block filtering approach. It allowed the use of m SDMs connected in parallel, where each modulator worked at $1/m$ of an output bit rate. The method suffered from an increased hardware complexity. Also, the increased length of a single dsp path makes this approach unsuitable for digital implementation (FPGA). In [7], the authors utilized the SDM time domain equations to form a structure similar in principle to the digital block filtering based approach, with the advantage of a reduced complexity. Although the hardware reduction has been achieved, and the clock frequency of each modulator could be theoretically reduced by any m times, the problem of long dsp paths remains unsolved.

This paper presents an alternative mechanism for increasing the effective output rate for a given clock frequency, without requiring significant additional processing.

In the remainder of this paper, the approach derived from discrete time-domain equation of the loop filter in a SDM is presented.

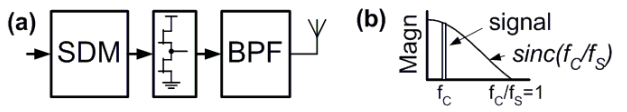

Figure 1. (a) Class S PA, (b) The effect of sampling frequency on the signal's strength

II. Derivation

When analyzing the first order SDM shown in Fig.2(a) it is observed that knowing the output and the input of the delay block at time indexes $n-1$ and n allows finding a current

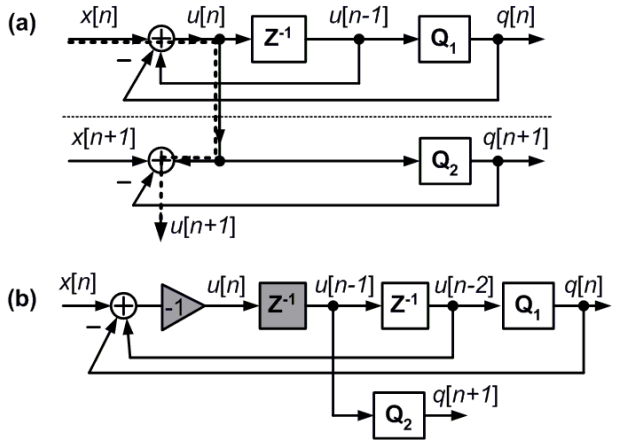

Figure 2. (a) A parallel organized SDM for processing two input samples during single clock cycle, (b) A first order SDM after bandpass transformation

and a future SDM outputs $q[n]$ and $q[n+1]$ by deploying quantizers Q_1 and Q_2. Since the one-step-ahead SDM output $q[n+1]$ is known, we can find a future input to the delay block at time $n+1$. Deducing from Fig.2(a) we obtain an explicit discrete time domain equation for $u[n]$ and $u[n+1]$ (2).

$$\begin{aligned} u[n] &= x[n] - q[n] + u[n-1] \\ u[n+1] &= x[n+1] - q[n+1] + x[n] - q[n] + u[n-1] \end{aligned} \tag{2}$$

In a similar manner the system in Fig.2(a) can be expanded by any integer number m (m positive), and therefore it has the potential of increasing a sampling frequency of a modulator by a factor of m. Although this technique seems promising there is a constraint in practice. As the m factor increases, the difference equation for each next future u expands, forcing longer computation time, and thus reducing the speed of signal processing - the long dsp path indicated by a dashed line in Fig.2(a). This limits the degree of parallelization possible, in a similar fashion to the previous techniques [6], [7]. The problem could be however avoided, if the equation for $u[n+1]$ was released from dependence of $u[n]$.

This is achieved by performing the well known low pass to band pass transformation $z \to -z^2$. In this way, we arrive at a system, shown in Fig.2(b), whose zeros are located at $\frac{f_S}{4}$, and whose $q[n]$, $q[n+1]$ values are known by deploying quantizers Q_1 and Q_2. The current and the future value of u can then be written as,

$$\begin{aligned} u[n] &= -(x[n] - q[n] + u[n-2]) \\ u[n+1] &= -(x[n+1] - q[n+1] + u[n-1]) \end{aligned} \tag{3}$$

Since values of $u[n-2]$, $u[n-1]$ are known from a previous clock cycle, (3) can be computed in two parallel signal processing paths independently.

III. BPSDM IMPLEMENTATION SCHEME

The band pass structure is generated undertaking the $z \to -z^{-2}$ transformation from the prototype low-pass modulator. This transformation adds additional delay and gain block to the low pass structure (shown in gray in Fig.2(b)). From (3) it is noted that the variable u is expressed as a function of q, x and itself delayed by two clock cycles. If one delay from each serial pair of delays in Fig.2(b) was removed, and the intermediate times indicated as $[n-1]$ omitted, by observation we can say that the obtained structure would be a result of the $z \to -z$ transformation of the first order SDM shown in upper part of Fig.2(a). As a result we arrive at system that complies with (3), and when supplied with input samples $x[n]$ at time indexes $n = 0, 2, 4, 6\ldots$ it returns the corresponding output sequence $q[n]$ at the same time indexes, $n = 0, 2, 4, 6\ldots$. To calculate the intermediate (odd) values, another, connected in parallel modulator is required. This simple example shows that two connected in parallel $z \to -z$ transformed, first order SDMs, operating at the same sampling frequency $\frac{f_S}{2}$, can replace single, band pass SDM having sampling frequency f_S.

This property can be extended to a broader class of modulators since all $z \to -z^2$ transformed SDMs can be characterized by discrete time domain equations processing either odd or even samples at the same time. To verify this statement, a general single loop SDM shown in Fig.3(a) is considered next. Its $STF(z)$ and $NTF(z)$ are given by (4).

$$STF(z) = \frac{H(z)}{1 - H(z)} \qquad NTF(z) = \frac{1}{1 - H(z)} \tag{4}$$

Now two such modulators are connected in parallel - Fig.3(b), such that each of them processes input samples having odd $(1, 3, 5...)$ or even $(0, 2, 4...)$ time indexes n.

In order to derive $STF(z)$ and $NTF(z)$ for the obtained system, the sums S_1, S_2 and quantizers Q_1, Q_2 in Fig.3(b) are moved outside of the parallel system-Fig.3(c). This can be done by noticing that the input to the quantizer in Fig.3(c) is composed from outputs of both loop filters $H(-z)$, thus it produces the same output sequence $q[n]$ as in Fig.3(b). Next, the output $q[n]$ is distributed through multiplexer to the loop filters inputs without changing them (Similar reasoning had been applied in [6]).

Now, a single loop SDM having a loop filter $\overline{H}(z)$ is obtained. The loop filter transfer function $\overline{H}(z) = \overline{H}_{OUT}(z) / \overline{H}_{IN}(z)$ is calculated in the following lines

$$\begin{aligned} U_1(z) &= \tfrac{1}{2}\left\{\overline{H}_{IN}\left(z^{1/2}\right) + \overline{H}_{IN}\left(-z^{1/2}\right)\right\} \\ U_2(z) &= \tfrac{1}{2}\left\{z^{-1/2}\overline{H}_{IN}\left(z^{1/2}\right) - z^{-1/2}\overline{H}_{IN}\left(-z^{1/2}\right)\right\} \end{aligned}$$

$$\begin{aligned} &W_1(z) = V_1\left(z^2\right), \ \ where \ \ V_1(z) = H(-z)\,U_1(z) \\ &W_2(z) = V_2\left(z^2\right), \ \ where \ \ V_2(z) = H(-z)\,U_2(z) \\ &\text{finally} \\ &\overline{H}(z) = \tfrac{\left[z^{-1}W_1(z) + W_2(z)\right]z}{\overline{H}_{IN}(z)} = H\left(-z^2\right) \end{aligned}$$

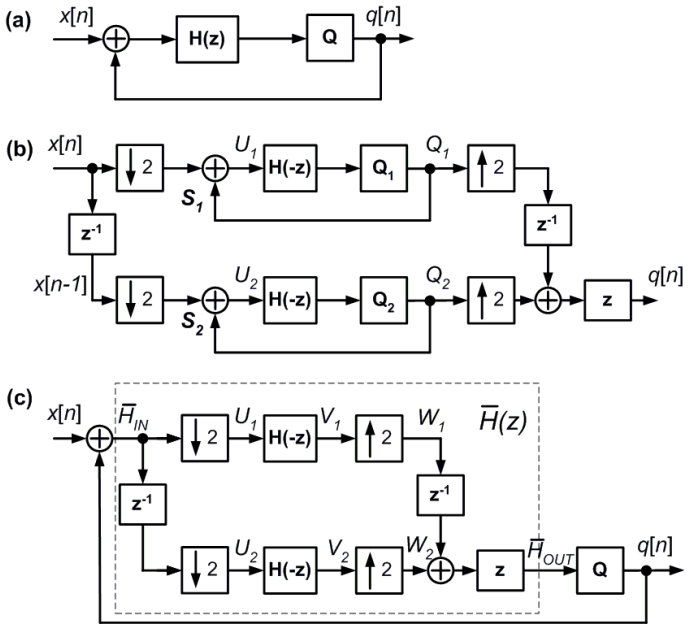

Figure 3. (a) Single Loop SDM, (b) Parallel system, (c) Modified parallel system

Which proves the stated earlier equivalence. Hence a scheme shown in Fig.4 can be applied.

For experimental verification a third order direct form IIt [1] filter has been chosen as a loop filter $H(z)$ in both structures - $z \to -z^2$ and the parallel $z \to -z$. The third order direct form IIt implemented as a loop filter in a single loop SDM is shown in Fig.6(c).

The frequency responses for both bandpass systems, whose low-pass prototype NTF has zeros and poles: $z_1 = 1$, $z_{2,3} = 0.9998 \pm 0.019j$, $p_1 = 0.77$, $p_{2,3} = 0.854 \pm 0.1972j$ are shown in Fig.5.

IV. Extension to higher factors of improvement

It can be concluded that a simple parallelization applied in a previous section, with M parallel blocks, $(M > 2)$, will increase the sampling frequency by factor of M, but also a undesired $z \to z^M$ transformation of NTF will follow. In order to avoid it, some cross connections between a parallel blocks are needed. Straight implementation of these allows reducing the speed of the digital logic put between down/up-samplers. However, an undesired effect of lenghtening dsp

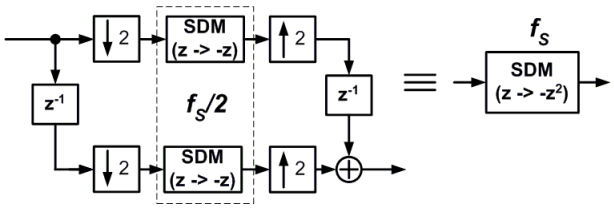

Figure 4. Two connected in parallel, $z \to -z$ transformed SDMs operating at a speed of $\frac{f_S}{2}$ are equivalent to a bandpass SDM operating at a speed of f_S

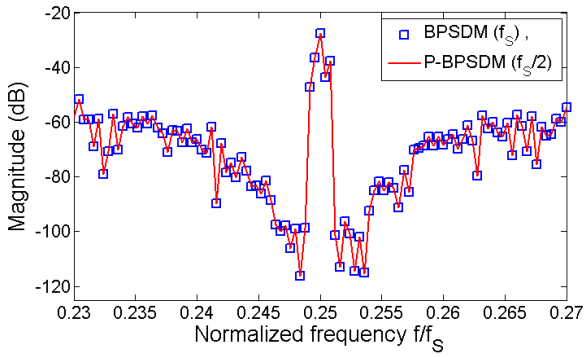

Figure 5. Frequency responses of band pass SDM (BPSDM) working at sampling frequency f_S and an equivalent parallel circuit working at $f_S/2$ (P-BPSDM)

paths seen in [6], [7] or in Fig.2(a) appear.

Learning from the described earlier parallel system, as well as from [6], [7], it can be concluded that in the case of parallelization, the discrete time domain equation of the loop filter $h[n]$ must not consist components delayed by less than M clock cycles. If these are canceled, the cross connections between the parallel SDMs may still be necessary, yet they will origin from delays blocks outputs and hence they will not impose longer computation times. This condition leads to a $H(z)$ of the form given by (5), which for the single loop SDM yields NTF of the form of (6).

$$H(z) = \frac{c_M z^{-M} + c_{M+1} z^{-M-1} + c_{M+2} z^{-M-2} \dots}{1 - d_M z^{-M} - d_{M+1} z^{-M-1} - d_{M+2} z^{-M-2} \dots} \tag{5}$$

$$NTF(z) = \frac{1 - d_M z^{-M} - d_{M+2} z^{-M-1} - d_{M+2} z^{-M-2} \dots}{1 + e_M z^{-M} + e_{M+1} z^{-M-1} + e_{M+2} z^{-M-2} \dots} \tag{6}$$

Where M is an integer, and $M \geq 2$.

Design of stable single bit SDM having the above NTF can be challenging task since (6) does not allow placing the poles and zeros freely. If, however a low pass SDM is designed with the least $M = 2$, it can be immediately extended to a factor of four clock-frequency-reduced BPSDM by simply applying the scheme from Fig.4.

Example of such a third order low-pass NTF with zeros and poles at ($Z_{1/2} = 0.5 \pm 0.01j$, $Z_3 = 1$, $P_1 = -0.624$, $P_2 = -0.176$, $P_3 = 0.8$) is given by (7). Its direct implementation with a single loop SDM and a direct form IIt structure as a loop filter is shown in Fig.6(c). The parallel structure derived from discrete time equation of the loop filter $h_{OUT}[n]$ (8) is shown in Fig.6(d).

$$NTF(z) = \frac{1 - d_2 z^{-2} - d_3 z^{-3}}{1 + e_2 z^{-2} + e_{3+1} z^{-3}} \tag{7}$$

$$\begin{aligned} h_{OUT}[n] = c_3 h_{IN}[n-3] + d_3 h_{OUT}[n-3] + \\ + c_2 h_{IN}[n-2] + d_2 h_{OUT}[n-2] \end{aligned} \tag{8}$$

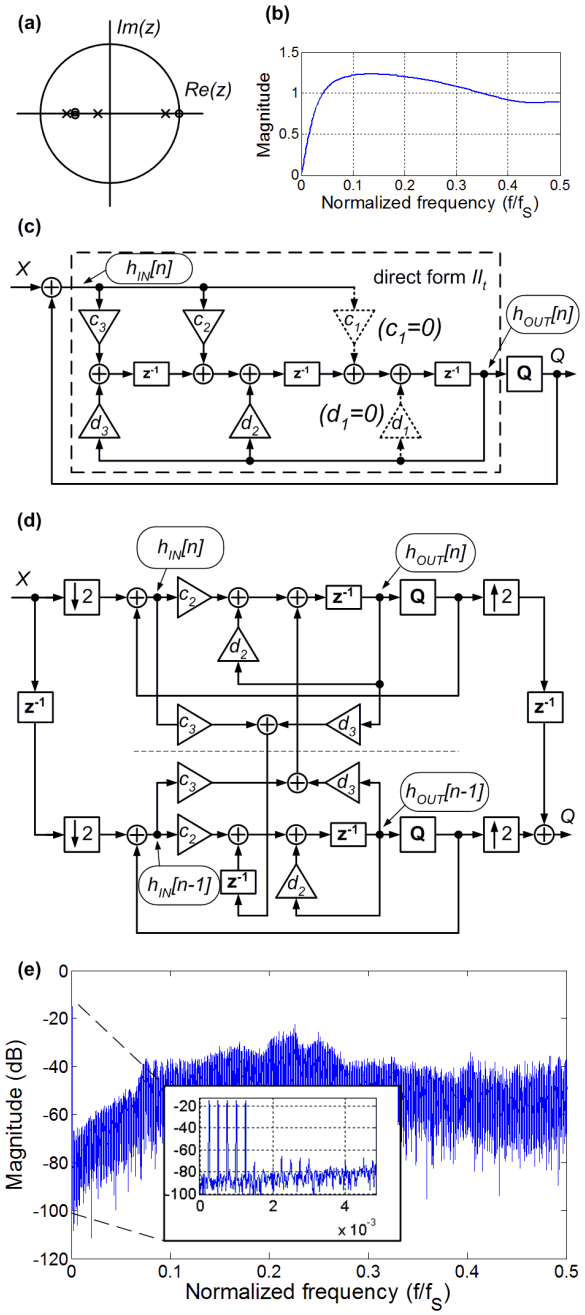

Figure 6. Two connected in parallel SDMs, creating together low pass NTF. (a) NTF zero-pole plot, (b) Noise Transfer Function (c) Direct implementation (d) Parallel implementation (e) Frequency response of the parallel low pass SDM

Observing closely Fig.6(d) reveals, that although at first glance the cross connection network seems to be complicated, no path starting from a delay output has more than three adders in cascade. This implies, that a single computation cycle can be not longer than that of structure Fig.6(c), yet it processes two input samples and returns two in a single cycle.

The zeros and poles have been chosen so that they yield a stable low-pass NTF, thus the system can be further parallel-transformed by applying scheme Fig.4.

Although it is a third order system, the single zero placed at dc implies that its performance can be at best compared with 1st order low pass SDM. The remaining two zeros appear at $Z_{1/2} = 0.5 \pm 0.01j$ and are partly compensated by NTF poles - Fig.6(a) and (b).

The obtained parallel modulator has a frequency response to a five tones input given in Fig.6(e).

V. Conclusion

A new approach to a BPSDM modulation suitable for switch mode power amplifier design has been presented. The method takes advantage of an independence between consecutive modulator states separated by one clock cycle in a low pass to band pass transformed SDM. Using this property a modulator can be split into two parallel signal processing paths, as a result doubling the speed of the digital logic. This property has been used to produce a general conversion scheme for low pass to parallel band pass SDM.

Next the attempt to double the speed of a low pass SDM has been taken. This can be a challenging task since the straight approach to parallelization leads to extended discrete time equations of the system, which in turn extends the time needed to process them. In order to avoid long cascades of adders/multipliers, a NTF of the low pass system has been modified. This solution allows to break a critical dsp path by insertion of a delay block. Although the desired speed can be achieved, some compromises in SNR performance due to the modified NTF arise.

Both approaches have been verified in simulations.

Acknowledgment

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