Reconfigurable High Frequency Class S Power Amplifier Demonstrator

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Abstract — **This paper presents an end-to-end high frequency class S power amplifier. A description of the full testbench and some important points on generation of RF outputs from FPGA devices and current mode class D design are given. Experimental measurements are provided for the prototype PA consisting of a signal generator, analog to digital converter, driver circuit, current mode class D switching stage and bandpass filter. Theory and experimentally measured results for this prototype are presented for a multi tone signal centred at 930 MHz and with a total output power of 24.7dBm.**

Index Terms — **Delta-sigma modulation, power amplifiers.**

I. Introduction

Switch-mode power amplifiers such as class D, E and F have higher theoretical efficiencies than class A or AB amplifiers. Because switch-mode PAs are nonlinear they are not direct replacements for linear PAs, though they can be used in architectures such as Envelope Elimination and Restoration (EER), LInear amplification with Nonlinear Components (LINC) or as is shown here, with ΣΔ based modulators in what is known as a class S power amplifier.

The Class S architecture in this paper utilizes a current mode class D (CMCD) switch for the high efficiency switch-mode PA stage. This class of power amplifier has published drain efficiencies of the order of 60%, 63% and 71% for designs with high power discrete devices [1-3]. Since the class D amplifier eliminates the envelope of the input signal, all information in the input signal must be encoded in the timing of the switch transitions. Maximum transistor switching frequency remains a major barrier to high efficiency implementation of the class-S PA architecture and influences the maximum possible bit rate of the input signal. The modulation strategy must therefore be optimized for both cheap implementation on a digital circuit and compatibility as a drive signal for the available transistor technology.

The type of encoder that can be used is limited due to the necessity to reconstruct the amplified version of the original input signal. A direct bandpass ΣΔ modulator can be used as the encoder as it can convert the modulated carrier signal into a binary amplitude pulse train for amplification in the class D switchmode power amplifier stage. Typically, direct ΣΔ modulation will require a system clock frequency of 4 times the carrier frequency and circuits have been presented for carrier frequencies of the order of 2.2 GHz [4].

Although it is possible to manufacture ΣΔ modulators for high frequency operation an alternative approach presented here is to implement the ΣΔ at a lower frequency on an FPGA. This implementation has several advantages including low cost, low risk and it provides a reconfigurable hardware implementation. Such a solution is suitable for integration in a software defined radio as it can be accommodated on an FPGA and requires a small fraction of total FPGA resources.

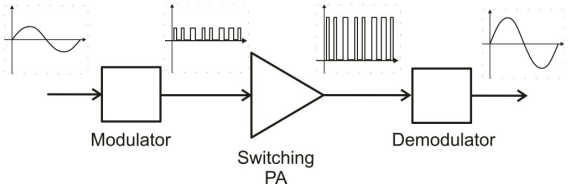

Figure 1. System view of a class S switch mode PA

In this paper we present experimentally measured results for a class S power amplifier with a high level structure similar to that shown in Fig 1. This platform operates at high frequency using a mid-range FPGA development board and a CMCD amplifier. It is shown that the clock frequency for the ΣΔ modulator can be set at a fraction of the carrier frequency of the output by adopting alternative techniques to direct bandpass ΣΔ modulation. For this demonstrator we will use a 10^{th} order ΣΔ modulator to convert the input signal to a pulse density modulated output which is up-converted and used to drive a CMCD PA. Experimentally measured results are presented for the output of the full PA.

II. High Frequency Digital Modulator

A ΣΔ modulator converts a high resolution digital input signal to a pulse density modulated output. This is done by adding an error signal whose spectral components are filtered out from the signal band, and when added to the input in the time domain creates a square wave. Digital ΣΔ modulators are used when high dynamic range, low noise and high linearity are required. ΣΔ modulators can be broadly classified in terms of order, number of output levels of the quantizer and noise transfer function.

For the end-to-end RF class S PA presented here we require a ΣΔ modulator which can convert a low frequency high resolution signal to a high frequency low resolution signal. Limitations in the implementation of high frequency

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direct bandpass ΣΔ modulators include the high clock frequency which in turn will increase the cost of developing and building such a solution, and the input signal in the direct approach is an RF signal. In this way a number of integrated circuits must be used prior to the modulator to upconvert the signal.

A combination of both the up conversion and modulation stages can now be realised on FPGA development boards. In this implementation the signal is first encoded with a band pass 10^{th} order ΣΔ modulator using a relatively low clock frequency as shown in Fig. 2. It is characterized by signal transfer function (STF) and noise transfer function (NTF) given by (1) and (2) respectively.

$$STF(z) = 1 \tag{1}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{2}$$

The loop filter employed in the ΣΔ has been introduced in [5], and it is optimized for fast operation in digital signal processors. The loop filter shown in Fig. 3 has two adders in a cascade in the longest computational path. It is constructed in such a way, that the poles of H(z) move along the unit circle as coefficients m_i change. Therefore deep notches appear in the NTF as the poles of H(z) become zeros of the NTF. This feature is used to generate power of two coefficients in the loop filter, and effectively replace multiplications by a fast operation of bit shifting. This makes the chosen ΣΔ structure suitable for fast FPGA operation. Moreover, the latency does not depend on modulator order. Here, a 10^{th} order BPΣΔ with zeros optimized around $f_{\Sigma\Delta}/4$ has been used, the structure of which is shown in Figures 2 and 3.

The modulated signal is subsequently multiplied by a +1 and -1 bit stream. Since a bit stream of +1,-1 clocked at a frequency f_{CLK} (f_{CLK} = 20 $f_{\Sigma\Delta}$, where $f_{\Sigma\Delta}$ is a sampling frequency of ΣΔ, $f_{\Sigma\Delta}$ = 98MHz) is equivalent to a frequency multiplication by a local oscillator at $f_{CLK}/2$ sampled at the nyquist rate. The spectrums of both the direct BPΣΔ approach and the digital mixing approach are shown in Fig.4.

The purpose of this signal modulator is to drive a switch mode RF power amplifier. As such the performance of the power amplifier is directly dependent on the signal driving it. Comparison of the direct approach to the digital mixing method is performed using a number of figures of merit such as dynamic range, signal passband or bandwidth (BW), maximum and minimum pulse width and coding efficiency. The dynamic range of the signal and passband of the modulator must be large enough so that when the modulated signal is filtered by the PA output network and filter stages the output signal will meet spectral mask requirements. Here we will gauge the relative difference in available signal bandwidth for each modulator and not compare it to a particular spectral mask requirement. Modulator output signal pulse widths can have a large effect on the overall performance of the class S power amplifier depending on the types of transistors used. Short and long pulse lengths in the modulator output bit stream will effect the overall performance of the class S PA depending on the gate switch on time, low frequency dispersion effects and f_T for the devices used [6]. Mean power coding efficiency, η_P, of a pulse density modulator is defined as the ratio of in-band signal power to total ΣΔ modulator output power [7].

$$\eta_P = \frac{P_{inband}}{P_{total}} \tag{3}$$

Relative performance and signal quality for both the direct and digitally mixed approaches can be calculated in Matlab. Using a fixed point simulation a close approximation to the FPGA implementation can be calculated and are found in Table I.

TABLE I. COMPARISON OF ΣΔ MODULATORS

Parameter	Direct ΣΔ	ΣΔ + Mixing
F_C	930 MHz	930 MHz
$F_{\Sigma\Delta}$	3.72 GHz	98 MHz
BW	180 MHz	9 MHz
Dynamic Range	57 dB	45 dB

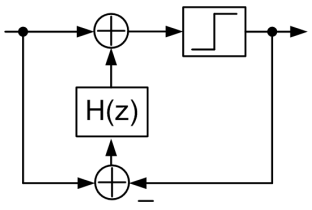

Figure 2. ΣΔ structure used

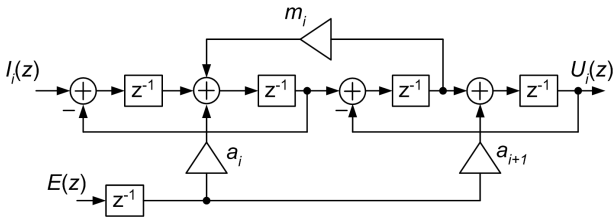

Figure 3. Computationally efficient loop filter H(z)

It is possible to change the pulse density modulator NTF by updating the modulator coefficients on the FPGA. To dynamically change the transmit frequency is also possible, however the quality of the transmit signal generated by the modulator on the FPGA will be influenced by the reference oscillator used on the FPGA board and the relationship

between its frequency and the required transmit frequency for the system.

Since the clock frequency requirements for the direct ΣΔ implementation are prohibitively large for the Virtex II pro FPGA development board only experimental results for the digital mixing approach are presented.

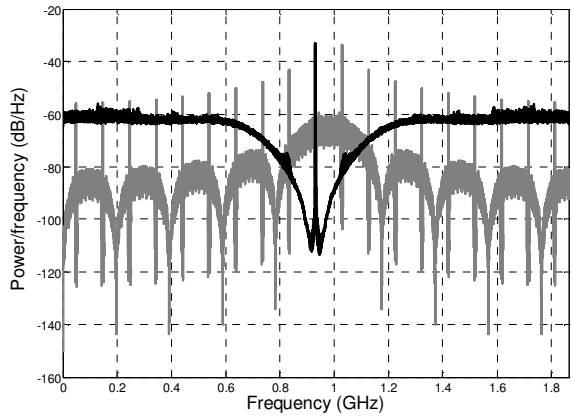

Figure 4. Plot of direct 4th order and 10th order digitally mixed bandpass ΣΔ modulators (direct approach in black, digitally mixed approach in grey).

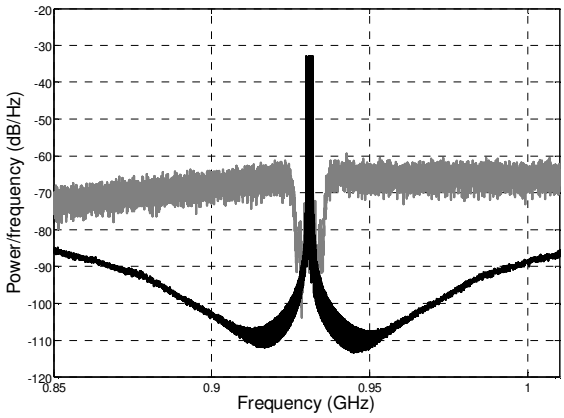

Figure 5. Magnification about the carrier frequency (direct approach in black, digitally mixed approach in grey).

III. Class-S PA Demonstrator Design

Class D, E and F switch-mode power amplifiers have been shown to offer linearity and high efficiency through the use of various PA architectures, namely: Envelope Elimination and Restoration (EER) and LInear amplification with Nonlinear Components (LINC) [8][9]. In these cases the switch mode PA accepts an analog signal already modulated on the RF carrier transmit frequency. This requires a high frequency circuit to pre-process the signal and split it into two separate paths. The class S PA is similar as it requires pre-processing of the signal using pulse-density modulation [10]. Shown in this publication, the signal into the class S PA is a high resolution digital signal at a fraction of the carrier frequency. This signal is modulated and upconverted to an RF frequency in the PA. To solve the input signal generation problem, a differential output signal directly from the multi-gigabit transceiver (MGT) on a Virtex II pro FPGA development board was used. In this way the input signal for the power amplification stage can be generated at different carrier frequencies and most importantly uses a ΣΔ modulator clocked at a fraction of the carrier frequency.

The resources required on the Virtex II pro FPGA to implement the design constitute a very small percentage of those available on the device. The signal source used for this demonstrator is implemented directly on the FPGA. 4 direct digital synthesizers are used to generate a multi tone signal having a bandwidth of 2MHz. A 10^{th} order bandpass ΣΔ modulator is instantiated in this implementation on a Virtex II pro FPGA board. The MGT of the FPGA board is used to upsample the output signal from the ΣΔ modulator.

The MGT outputs of the FPGA development board are connected to a prototype CMCD PCB board built on 4 layer FR4. The board consists of a PWD06 switch-mode driver IC from PWRF, the output of this is fed to a 3dB 180 degree splitter from Anaren to provide the differential drive signals for the class D stage. The CMCD bridge power amplifier structure consists of two pHEMT ATF52189 transistors from Avago Technologies. The differential output across the drains of the two transistors is connected to a resonant LC tank circuit tuned to 930 MHz. Finally a lumped element balun was designed and implemented to convert the signal from differential to single ended output for measurement purposes.

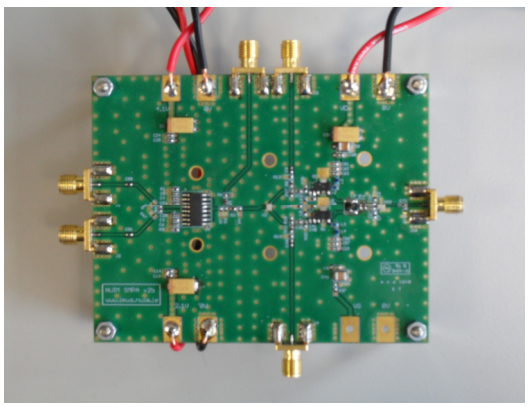

Figure 6. Photo of CMCD amplifier PCB

IV Experimental Measurements

Experimental measurements were taken for the reconfigurable class S power amplifier described in Section III. Figure 6 shows a photograph of the CMCD power

amplifier board. The FPGA development board MGT output is connected to the CMCD board by two matched semi-rigid co-axial cables. Care is taken in the PCB layout to match the two paths of the differential signal into the CMCD.

A first set of measurements was taken to determine the performance of the CMCD board for a single tone at the center frequency. An Agilent E4433B signal generator was used to generate the signal and an off-board splitter was used to convert the signal from single-ended to differential. In these tests a CMCD stage drain efficiency of 65% was recorded for a single tone at 930MHz. This result is for the CMCD stage alone and does not represent the overall system efficiency, which suffers from the power consumption of the IC used to amplify the pulse density modulated signal from the FPGA.

The second set of measurements used the output from a pulse density modulated and upconverted signal to drive the current mode class D switch. A screen capture from a Rohde & Schwarz FSL spectrum analyser of the output signal from the PCB is presented in Figure 7.

The total power contained in the output signal spectrum is 24.7dBm, 12.5dBm in the wanted signal, 24.2dBm from ΣΔ noise and 10.6dBm from images and other spurious signals.

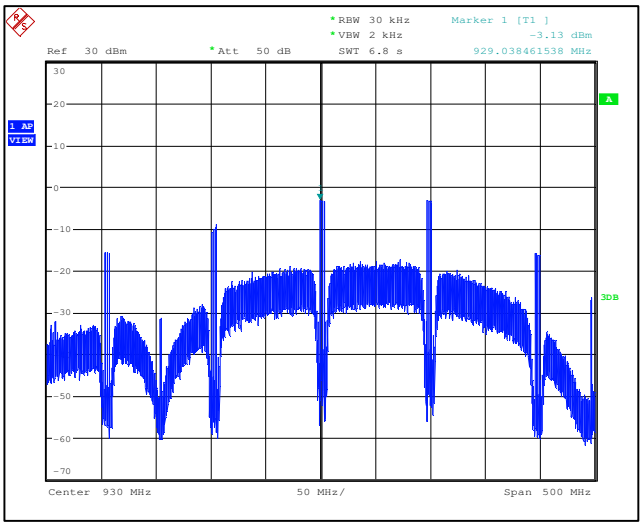

Figure 7. Measured output spectrum from CMCD board

V CONCLUSIONS

A class S power amplifier prototype that can accept a modulated data stream from an FPGA and produce an output of greater than 20dBm has been built. The modulated RF signals from the FPGA are sufficient to test the prototype CMCD board and demonstrate an end-to-end class S PA. From these results it is evident that the ΣΔ modulation scheme is critical for overall system efficiency. A high level of out of band noise power and unwanted spectral components greatly reduces the efficiency of the CMCD stage and as a result, the overall system efficiency. Further work is required to improve the performance of this system to increase the available signal bandwidth and improve the dynamic range. At present it is not possible to identify the presence of nonlinear effects from the system output. There is also an open issue of power consumption in the amplification of the digital pulse stream from the FPGA to drive the CMCD stage.

ACKNOWLEDGMENTS

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