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Design technique of broadband CMOS LNA for DC – 11 GHz SDR

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Abstract: This paper presents a DC–11 GHz CMOS low noise amplifier (LNA) for software-defined radio (SDR). The broadband performance is extended to cover the spectrum from near DC to 11 GHz by adopting extra inductors with modified resistive feedback, folded current reuse topology. Bandwidth extension is proposed by inserting pole splitting, interstage and LC ladder inductors. A source follower jointly acts as the buffer stage for broadband output matching and feed-forward path for gain enhancement as well as noise cancellation. Simulation shows power gain of 11 ±4 dB and the NF ranging from 1.8 to 3 dB in 0.4–11 GHz band. The LNA achieves an average IIP3 of −10 dBm while consumes only 5.3 mW. The proposed broadband LNA is designed in 0.18-μm CMOS process from 1.5 V supply.

Keywords: LNA, broadband, software-defined radio, low power, CMOS

Classification: Integrated circuits

References

[1] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800 MHz-6 GHz Software-Defined Wireless Receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[2] L. Shuzuo and H. C. Luong, "A 0.8 GHz–10.6 GHz SDR low-noise amplifier in 0.13-μm CMOS," *IEEE Custom Integrated Circuits Conf.*, pp. 65–68, Sept. 2008.

[3] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4 V 25 mW inductorless wideband LNA in 0.13 μm CMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 426–613, Feb. 2007.

[4] M. Ingels, C. Soens, J. Craninckx, V. Giannini, T. Kim, B. Debaillie, M. Libois, M. Goffioul, and J. Van Driessche, "A CMOS 100 MHz to 6 GHz software defined radio analog front-end with integrated pre-power amplifier," *Proc. ESSCIRC*, pp. 436–439, Sept. 2007.

[5] B. G. Perumana, J.-H. C. Zhan, S. S. Taylor, B. R. Carlton, and J. Laskar, "Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, part. II, pp. 1218–1225, 2008.

[6] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, "A DC-11.5 GHz Low-Power, Wideband Amplifier Using Splitting-Load Inductive

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Peaking Technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 7, pp. 482–484, 2008.
[7] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
[8] Z.-Y. Huang, C.-C. Huang, C.-C. Chen, C.-C. Hung, and C.-M. Chen, "An inductor-coupling resonated CMOS low noise amplifier for 3.1–10.6 GHz ultra-wideband system," *IEEE Int. Symp. Circuits Syst.*, pp. 221–224, May 2009.

1 Introduction

The numbers of wireless radio standards for various applications have been emerging rapidly. To save the cost and resources, it is necessary to realize a mobile terminals which can connect to all existing systems. The design of multi-band multi-standard RF transceiver for software defined radio (SDR) has recently gained a lot of interest as the circuitry can be configured and share the same hardware for different wireless standards [1, 2, 3, 4, 5, 6, 7].

RF front-end circuit for SDR is required to cover every communication standard even if it is a new standard. Therefore, RF front-end capable of handling different carrier frequencies operating from few hundred MHz up to 10 GHz spectrum range is highly demanded [2]. Broadband LNA is hence a key block and challenging in software defined radio (SDR) [4]. The main challenge in design such wideband LNA for SDR is to make it able to work from hundreds MHz to several GHz. Since operating at low frequency with low NF requires large transistors and low 1/f noise which opposes to GHz range operation. The required input matching inductor is also excessively large.

There are several approaches to realize the SDR wideband LNA. In [1], a differential LNA consisting of common gate (CG) and common source (CS) branches are used. It suffers severe issue of even order distortion. In [2], the cross-coupled CG with negative feedback is employed. Active source follower feedback LNA can bring down the operation frequency from 1 GHz up to 7 GHz [3]. Resistive feedback recently has become interested with advantages in terms of simplicity, occupying small chip size, and low noise figure compared to other approaches [4, 5, 6]. However, the power consumption is relative high, not adequate NF, and the bandwidth is limited given the standard CMOS process.

A technique to extend the bandwidth from DC to 11 GHz is proposed by adding extra inductors to the modified resistive feedback LNA in this work. Furthermore, with current reuse and feed-forward connection, the gain is enhanced while the noise is suppressed. The proposed LNA is designed in 0.18-μm CMOS process.

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2 Proposed broadband LNA

2.1 Resistive feedback and current reuse

The broadband LNA covering from DC to 11 GHz is proposed in Fig. 1. The wideband operation is realized in a current reuse cascode LNA with shunt peaking load by using resistive feedback with extra inductors to absorb parasitic capacitance. The LNA gain is expressed as:

$$A_v = -\left(g_m - \frac{1}{R_f}\right)(R_L//R_f) \approx -g_m(R_L//R_f) \tag{1}$$

From Fig. 1, the input impedance of resistive feedback LNA shown in Fig. 2 can be given by

$$Z_{in} = \frac{R_S//R_f}{1+A_{loop}} \approx \frac{R_S}{1+A_{loop}} \tag{2}$$

where A_{loop} is the loop gain. Since R_f is much large than R_s, from (4), input matching is achieved with $A_{loop} < 1$. The loop gain of just below unity also ensures circuit stability.

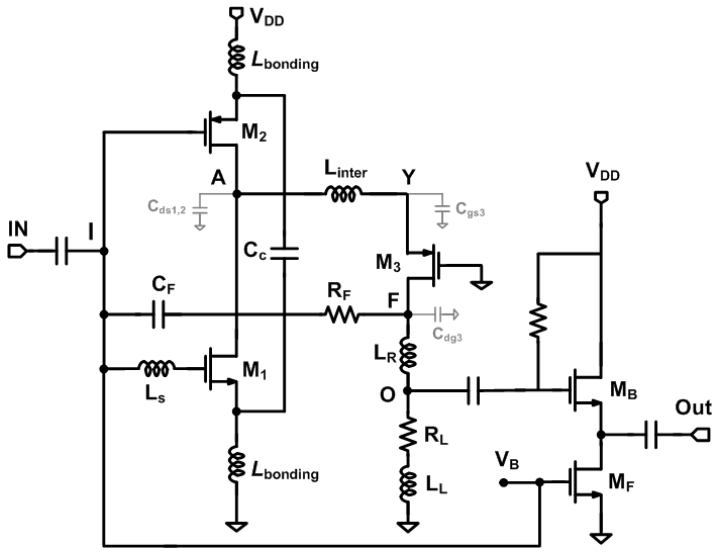

Fig. 1. Schematic of the proposed broadband LNA

To reduce the power consumption, the complementary transconductance (M1 and M2) and feed-forward connection are adopted. Cascode amplifier is used in this LNA design to provide good isolation and reduce Miller's effect to operate at higher frequencies. Moreover, the current reuse is adopted to achieve sufficient gain given power constraint.

The NF is also reduced further as the proposed topology can provide noise cancellation along signal paths. Since the noise current flowing along R_F will result in voltage noises at node O (also node F) and the gate of M_F with the same sign, the converted current noises at the output via M_B and M_F show opposite phases. Thus, the noise will be cancelled out while the signal is reinforced. The source follower buffer is used to ensure the wideband matching and for measurement purpose at the output. The gain is enhanced by feed-forwarding the input to the buffer at M_F.

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2.2 Coupling resonated inductive load

Feedback resistor R_F and the main amplifier can create a loop, which can be modified by the Miller's Theory which is shown in Fig. 2 (b). Feedback loop with R_F could play two roles in this LNA. Input impedance R1 is part of input matching network while the output impedance R2 is becoming a part of the load of the cascode amplifier.

The coupling inductor L_R is inserted to absorb the output parasitic capacitances at the load and drain of M3. Its effect is similar to the LC ladder filter, shown in Fig. 2 (a). However, to be more accurate, the inductor coupling resonated load is established with the shunt peaking load and R2 coupled by the inductor L_R as discussed in [8]. The value of L_R is carefully chosen so that the transition frequency $f_{trans} = 2\pi R_L/L_R$ falls between the operation frequency band. Thus, the gain in the middle band is improved with L_R and inductive peaking load.

3 Proposed Inductors for bandwidth extension

3.1 Input pole splitting inductor

Fig. 2 presents the small signal model of the proposed LNA shown in Fig. 1. With the insertion of a splitting inductor, L_s, at the gate of M1, the input pole is split and placed at a higher frequency. The transfer function of the LNA in Fig. 1 with L_s can be derived as

$$\frac{V_{out}}{V_{in}} = \frac{1}{1+s^2L_sC_{gs1}} \times \frac{\left\{\begin{array}{l}[1-(g_{mn}+g_{mp})R_F+s^2L_LC_{gs1}(1-g_{mp}R_F)]g_{m3}r_{ds}\\ -(1+s^2L_LC_{gs1})(1+sC_{ds}r_{ds})\end{array}\right\}R_L}{(R_F+R_L+sL_L)\times(g_{m3}r_{ds}-1-sC_{ds}r_{ds})} \tag{3}$$

Where $C_{ds} = C_{ds1} + C_{ds2}$, $r_{ds} = r_{ds1}//r_{ds2}$. As for the conventional inverter LNA with inductive peaking like in [6], the transfer function is given as

$$\frac{V_{out}}{V_{in}} = \frac{1}{1+s^2L_s(C_{gs1}+C_{gs2})} \times \frac{\{[1-(g_{mn}+g_{mp})R_F]\,g_{m3}r_{ds}-(1+sC_{ds}r_{ds})\}\,R_L}{(R_F+R_L)\times(g_{m3}r_{ds}-1-sC_{ds}r_{ds})} \tag{4}$$

From (3) and (4), the resultant poles are $\left(\sqrt{L_sC_{gs1}}\right)^{-1}$ and $\left(\sqrt{L_s(C_{gs1}+C_{gs2})}\right)^{-1}$, respectively. The pole of the proposed LNA with presence of L_s is put to higher frequency. It is also noted that, BW improvement due to the pole split does not depend on PMOS device size (C_{gs2}). Hence in the current reuse topology, PMOS device in transconductance stage can be larger without spoiling the effect of frequency improvement. As the bias current in M2 is larger than M1, PMOS is used in M3 in this LNA to steer part of the current from M2.

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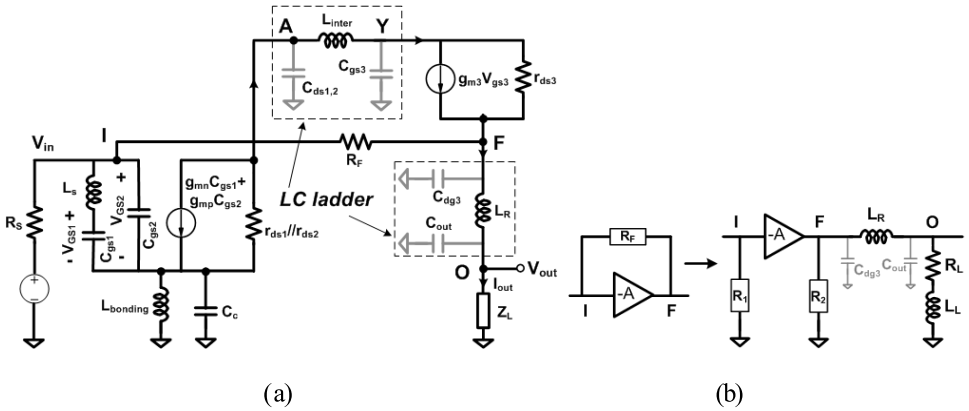

Fig. 2. Small signal model of the folded CG LNA (a), and the transfer function of LC network between node X and Y (b).

3.2 Inter-stage inductor

In CMOS technology, severe parasitic capacitance deteriorates BW significantly. The series inductor L_{inter} is inserted at node Y to broaden the BW at the bottle neck of the proposed wideband amplifier architecture, shown in Fig. 1. Without employing inductors, amplifier bandwidth is mainly determined by RC time constants of every node. In the denominator of both (3) and (4), there is a pole created by C_{ds} as $(g_{m3}r_{ds}-1)(C_{ds}r_{ds})^{-1}$. The above equations are derived without the present of L_{inter} to simplify the derivation. From the small signal equivalent circuit in Fig. 2, the three order LC ladder filter is inherently created with the presence of parasitic capacitances $C_{\text{ds1,2}}$ and C_{gs3}. The LC ladder will absorb those parasitic capacitances which limit the bandwidth of LNA, hence extend the frequency response of the LNA significantly [1].

4 Simulation results and discussion

Fig. 3 (a) presents the S21 performances of the designed LNA with the effect of L_{s}, L_{inter}, L_{R}, and L_{L}. The bandwidth is enhanced significantly with the presence of L_{s} and L_{inter}. L_{R} also improves the frequency response but at the middle band, which is analyzed above. From the simulation of S21 without L_{L}, it is observed that the gain is only degraded at low and middle frequency band, while maintain its high frequency operation. This is suitable with the impact of inductive load peaking, where R_{L} determines the gain at low frequency and L_{L} helps extend its BW. In the proposed LNA, S21 achieves its best performance with L_1 value of 1.9 nH, L_{inter} of 1.8 nH, L_{R} of 3.1 nH, and L_{L} of 4.3 n. Coupling capacitor Cc is to short the source of PMOS and NMOS devices in transconductance stage. Hence, bonding wire effect which lowers the gain at RF frequency is reduced. Fig. 3 (b) shows the improvement of gain at high frequency, thus the bandwidth as well.

The proposed LNA is simulated and designed in 0.18-μm CMOS process using 1.5 V supply. Fig. 3 (c) shows the gain and S-parameter performances from DC to 11 GHz. The power gain is above 11 dB and almost flat within

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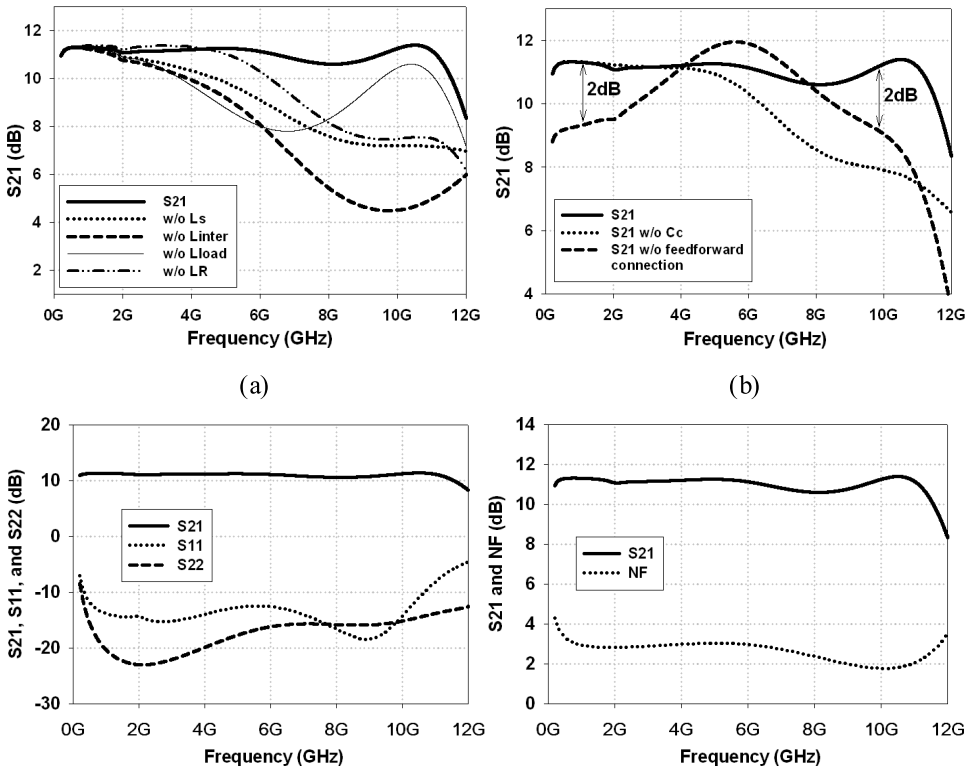

(a) (b) (c) (d)

	BW (GHz)	Power (mW)	S21 (dB)	S11 (dB)	NF (dB)	IIP3 (dBm)	Tech. μm	Topology
This work	DC-11	5.4	10.7-11.4	<-13	1.8-3	~-10	0.18	Modified.Res. Feedback
[4]	0.1-2.5	12/8	22/11	<-10	2/2.4	-10/-13	0.13	Res.Feedback
[5]	0.5-7	12	22 (Av)	<-9	2.3-2.9	-10.5	90n	Res.Feedback
[6]	DC-11.5	9.1	13.2	<-8	5.6	-10	0.13	Res.Feedback
[2]	0.8-10.6	14.4	>16	<-12	3.4-5.6	>1.6	0.13	Cross.C. CG
[3]	1-7	25	16	<-10	2.7-3	-4.1	0.13	Reactive.FB

(e)

Fig. 3. S21 performance with the effects of inductors Ls, Linter, LL, and LR on the bandwith (a), Simulated S21 with and without forward path, coupling capacitor Cc for gain and bandwidth enhancement (b), simulated S21, S11 and S22 (c), S21 and NF of the proposed LNA (d), and performance comparison table of the proposed LNA with previously published works (e).

the full bandwidth. Good input matching with S11/S22 of below −13 dB is shown in the whole band. In Fig. 3 (d), the simulated NF of the proposed LNA is achieved with minimum values of 1.8 dB. From 0.4 to 11 GHz, NF is less than 3 dB. The NF shows a gradually reducing characteristic over the whole band as frequency goes from near DC to 10 GHz. This is due to parasitic capacitances causing the deviation of noise cancellation effect at higher frequency.

Two-tone test with 2 MHz spacing is applied at various wireless stan-

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dard frequencies from 400 MHz to 10 GHz. IIP3 values vary from −14.2 to −6.3 dBm. The linearity reduction with frequency is due to loop gain roll-off [5]. Fig. 3 (e) summarizes the proposed LNA performances and compares with previously published works in wideband LNA designs for SDR. The designed LNA consumes only 5.3 mW from 1.5 V supply with good gain flatness and low NF over wide spectrum range from DC to 11 GHz, which is suitable for multiband multistandard low cost solutions like SDR.

5 Conclusion

The broadband LNA for SDR operating from near DC to 11 GHz was proposed and designed in 0.18-μm CMOS technology. Resistive feedback and folded current reuse topology is adopted in cascode LNA. The bandwidth extension is proposed by adding extra inductors to in this work. With current reuse and feed-forward connection, the power gain is high enough given the power constraint. The proposed LNA shows good gain flatness with minimum NF of 1.8 and below 3 dB in 0.4–11 GHz band. With technology scale down, the proposed LNA will even achieve better performance. It is suitable for low cost solution in realizing SDR radio which can cover various wireless standards.

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