

12 MHz to 5800 MHz Fully Integrated, Dual Path Tuned, Low Jitter, LC-PLL Frequency Synthesizer

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Abstract — This paper presents a realised prototype of fully integrated CMOS LC-PLL frequency synthesizer. The circuit delivers a wide range of clock signals between 12 MHz and 5800 MHz, with average long term jitter of only 4 ps. The primary application of the presented circuit includes high speed series data transmission links. Low power consumption of the complete synthesizer (including bias circuitry), in the range of 50mW from dual 1.2 V/3.3 V supply, is in line with energy efficient solutions for modern electronic systems. The circuit is developed using a standard RF UMC 130 nm CMOS process reducing design time and necessity for customisation of its components. Full integration of RC loop filter is obtained using dual path tuning scheme, involving two separate charge pumps, two filter paths and specially modified LC-VCO architecture. Total synthesizer area including PLL circuitry with set of programmable frequency divider, output RF drivers, two separate VCO circuits and all auxiliary bias circuitry occupies no more than 0.7 mm² of active area.

Keywords — Frequency synthesis, phase lock loop, dual path tuning

I INTRODUCTION

High speed series communication standards require low jitter clock signals to minimise the effects of sampling errors. To maintain given bit error rate (BER) for a given transmission scheme, the allowed variations in time instants when data is sampled have to be kept small. This requirement becomes quite challenging if transmission speeds reach Gbps range, which is the case for modern communication protocols as USB 3.0 or HDMI 1.3.

The low jitter clock signals are typically produced using phase lock loop (PLL) synthesizers due to their superior performance over free running oscillators. PLL loop is able to track and counter for phase variations of clock signals as long as these are slow enough to be captured. As the standard PLL synthesizer is equipped with voltage controlled oscillator (VCO) and frequency dividers, whole range of output frequencies can be produced using only a single frequency (and low jitter) reference source.

The main challenge of PLL design and integration is to deliver single chip solution for the synthesizer. The known design trade-offs for these circuits include a tuning range, jitter, chip area and power consumption. For example, to obtain output signals with low jitter, a classic resonant tank LC-VCO is preferable over ring oscillator circuits however requiring much larger chip area. Moreover, for a typical values of PLL design constraints, a low pass filter required for stable operation of the loop employs capacitors in the range up to few nF, leading to circuit integration that is not normally cost effective in many existing CMOS technologies.

One of previously published solutions for the problem of loop filter integration is known as dual path tuning (DPT). In this scheme, the single filter is substituted by two separate RC subcircuits driven from a separate charge pumps but leading to capacitance values in the range of few pF that may be now integrated on the same chip as the rest of the circuit.

This paper demonstrates in practice the simplest possible arrangement of dual path filtering using only

two capacitors and single resistor for the loop filter. Together with two separate multi-band LC-VCO cores with combined fractional bandwidth of 67% and set of programmable high speed devices, presented synthesizer is able to produce a set of 1024 unique clock frequencies with low long term jitter.

II LOOP FILTER INTEGRATION BY DUAL PATH TUNING TECHNIQUE

Figure 1 presents a classical arrangement for a second order PLL loop filter consisting of RC branch responsible for setting a transmittance zero at frequency of $\omega_z = 1/R_z C_z$ and additional capacitor C_p setting a transmittance pole at $\omega_p = 1/R_z(1/C_z + 1/C_p)$. The choice of this particular filter structure allows to ensure enough gain margin for stability of the loop at the same time providing to certain degree a control over transient response of the circuit [1]. The filter operates by translating net charge sourced or sunk by the charge pump current i_{cp} into a voltage V_t tuning a VCO circuit. The

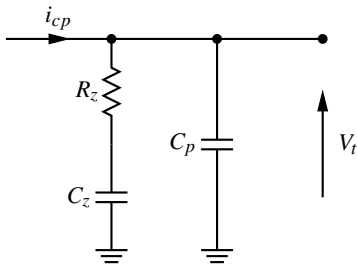


Fig. 1: Classical second order loop filter.

main problem related to the integration of the classical filter is the required size of the resistor and capacitors. For a typical values of loop parameters: VCO gain in the range of MHz/V, charge pump currents in the range of μ A and loop bandwidths less than 1 MHz, the resistance of few $k\Omega$ and capacitors of from hundreds of pF to few nF are necessary. For a typical capacitance density in CMOS process of $1\text{fF}/\mu\text{m}^2$ – $2\text{fF}/\mu\text{m}^2$, 1nF capacitor would consume more than 0.5mm^2 of active area, not mentioning reliability issues related to large metal surfaces of such capacitor. One of the so-

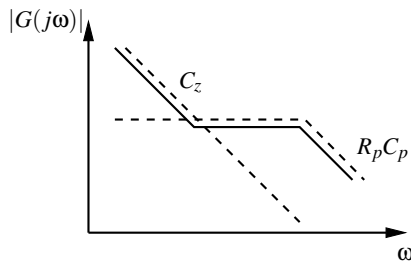


Fig. 2: Amplitude response of second order loop filter.

lutions for this problem is use of dual path tuning technique [2, 3]. Solid line on Figure 2 depicts a simplified

Bode plot of amplitude response of the classical second order filter, with single zero and single pole. Dual path tuning approach recognises that the response of the filter is a combination of transmittance functions of ideal integrator (capacitor) and a low pass RC filter, approximated by the respective dashed lines on Figure 2. Thus, instead of a single filter circuit, the same behaviour can be realised by using two separate subcircuits. Craninckx and Steyaert [3] proved that, all other things being equal, this approach yields capacitance values in the range of only few pF, relatively small in size and thus easy to integrate on the same chip as the rest of the PLL circuit.

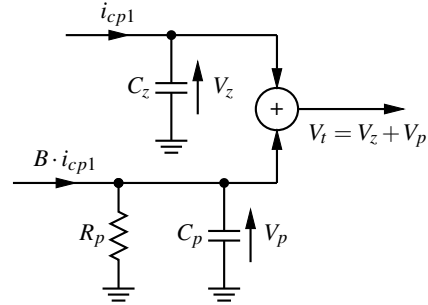


Fig. 3: Second order dual path filter.

Figure 3 depicts a generic structure of second order dual path filter [3]. The top path consists of an integrator translates a charge pump current i_{cp} into proportional tuning voltage V_z . The same rule applies to the bottom part of the filter, this time however the RC circuit is driven by the proportionally scaled version of the charge pump current, $B \cdot i_{cp}$, producing voltage V_p . These two voltages are then combined into a single tuning voltage V_t resulting in the frequency response corresponding to the solid line depicted in Figure 2.

The scaling parameter B allows to control the position of the transmittance zero [3]. A larger charge injected into $R_p C_p$ part of the filter, results in proportionally higher voltage V_p , shifting down the frequency where the corresponding curves $R_p C_p$ and C_z from Figure 2 intersect. Because the dual path filter requires two separate excitations, one being i_{cp} and its scaled version of $B \cdot i_{cp}$, this technique requires two separate charge pumps. This is not a major obstacle of the synthesizer integration as in general the charge pumps consist of a small number of transistors. Thus doubling the area occupied by two charge pump circuits, does not significantly change the total area requirements for complete PLL. The total tuning voltage has been originally combined using differential to single ended amplifier driving a tuning input of the VCO [2, 3]. This solution does not require any modifications from the existing VCO, however it consumes more power and injects flicker noise from an op-amp directly to the oscillator. Another method, presented by Chi et al. [4] assumes that the summation can be achieved in capacitance domain, connecting two outputs of the dual path

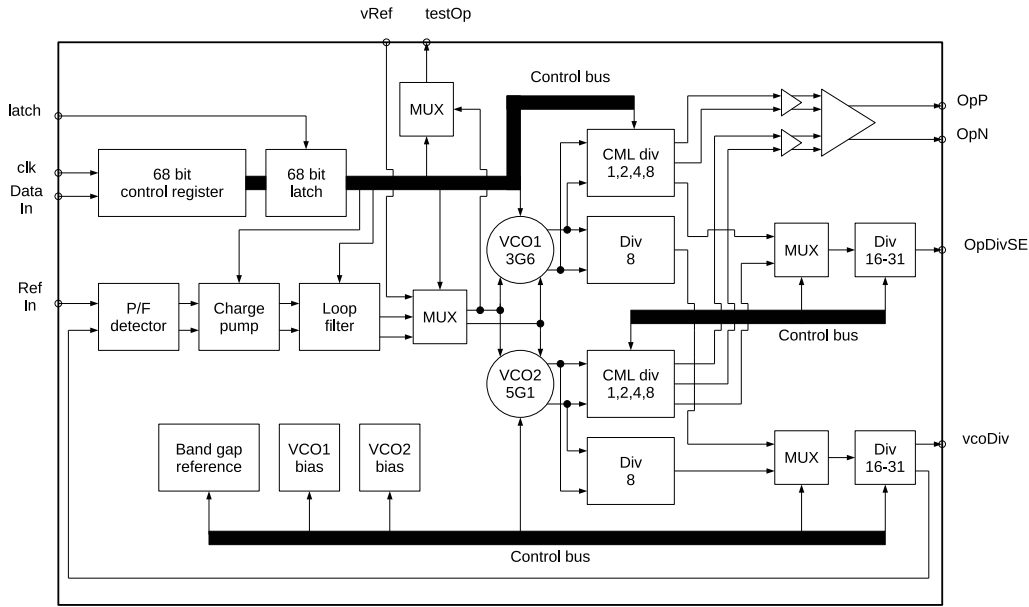


Fig. 4: Block schematics of the proposed wide tuning range PLL frequency synthesizer.

filter to a separate varactor branches in the VCO, effectively controlling oscillator behavior using two tuning voltages. This solution is passive and requires only a minor modification of the oscillator circuit.

In addition, the authors of [3, 4] use third order filters (obtained by adding another low pass RC branch) in order to meet a relatively stringent phase noise criteria of wireless standards. The reported capacitance values for this additional circuit are the range of tens of pF that inevitably increase area of the filter. As the proposed PLL synthesizer is designed for series data transmission links, as long as PLL stability margin is successfully maintained, optimised second order filter is enough to satisfy noise requirements. As a result, the presented synthesizer uses a very compact loop filter, much smaller in size than the ones from [3] and [3, 4].

III WIDE TUNING RANGE SYNTHESIZER CIRCUIT

Figure 4 presents a block diagram of the proposed frequency synthesizer. The circuit is designed with many reconfigurable parameters in mind, intended as compensation of process, voltage and temperature (PVT) variations, and for experiments with automated band preselection algorithms not discussed in this paper. The following subsections describe most of the blocks in more detail.

a) Synthesizer interface

The chip communicates with outside world using two stage 68 bit shift register. The register consists of D flip-flops triggered by external clock signal and supports MHz range speeds. The first stage of the register is responsible of storing 68 bits used to control both analog and RF functions around the chip. Note that fixed duty cycle for the clock signal driving the series

interface is not crucial. After 68 bits are sent to the first stage of the register, they are latched in the second stage. Any subsequent change in the first stage of the register does not change the state of the second stage, until another latch signal is not received by the synthesizer. The reset option has not been implemented in this prototype.

b) Phase frequency detector

The phase and frequency (P/F) detector uses a standard structure of two D flip-flops, transmission gates and NAND feedback with time delay to mitigate dead zone effects in charge pumps [1].

c) Charge pump circuit

The charge pump block consists of two parallel charge pumps used to source and sink the charge from a dual path loop filter block. Both charge pumps utilise a standard NMOS/PMOS totem pole of switches with return path to minimise charge sharing effects and improve speed. The magnitude of charge pump current can be trimmed using 8 bits from the input 68 bit control sequence. The ratio of charging currents delivered to the filter is set to $B = 9$.

d) Loop filter

Loop filter structure presented in Figure 5 corresponds to the circuit depicted in Figure 3, however instead of a summation in voltage domain, the filter has two single ended outputs V_z and V_p connected to separate varactor branches in the subsequent VCO stage. The value for the resistance can be controlled using 4 bits of the 68 bit control sequence. Five possible resistance values are available: 17 k Ω , 21.25 k Ω , 25.5 k Ω , 29.75 k Ω and 34 k Ω . The resistance tuning has been implemented in

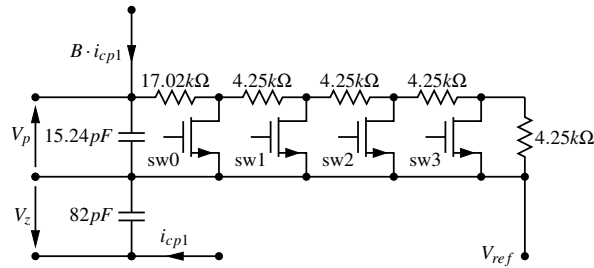


Fig. 5: On chip second order dual path filter.

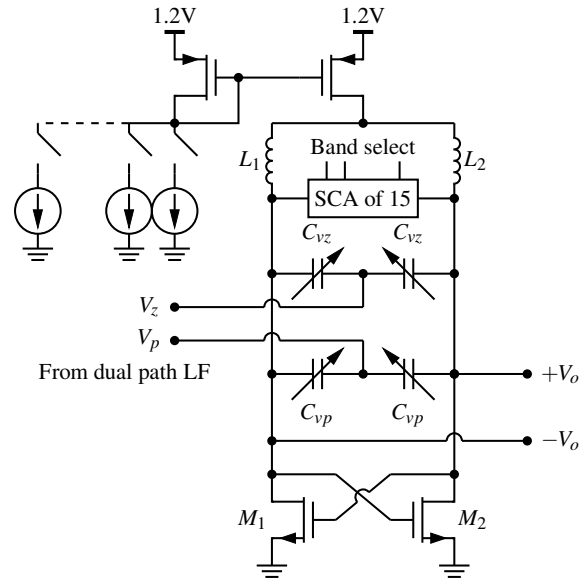
order to allow control over PLL bandwidth. If the synthesizer operates over wide frequency range, it is impossible (without additional design effort) to keep oscillator gain constant. As a result the bandwidth of the PLL can change significantly as well as noise performance of the loop. Tuning of filter resistance helps to mitigate this unwanted effect to a certain degree. The capacitor values used in this design are: 82 pF for C_z and 15.24 pF for C_p , resulting in the PLL bandwidth in the range between 100 kHz and 300 kHz.

e) Multiplexers

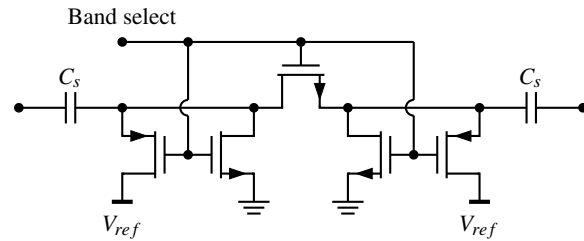
Multiplexers are used to switch some of the signals between subsequent circuit and output nodes. The multiplexer connected directly after loop filter allows to tune the selected oscillator core with externally supplied voltage or selects the tuning voltages generated by the loop filter. Respectively, this corresponds to open and closed operation of the loop. The second multiplexer allows to supply voltage from the integrator path in the filter outside the chip for measurement, which can be considered a test mode. During normal operation of the loop, this output is disconnected to prevent noise coupling directly to the oscillator core. Finally, a set of two multiplexers is used to connect RF signals from one of the two oscillator cores to the output of the synthesiser. The multiplexers are controlled using 1 bit of the 68 bit control sequence.

f) Voltage controlled oscillators

The RF signal is generated in two LC-VCO cores: a low band (LB), operating between 2900 MHz and 4200 MHz, and high band (HB), operating between 4000 MHz and 6000 MHz. This choice is dictated by low phase noise operation, low power consumption and very wide tuning range. Figure 6 depicts simplified schematics of the proposed VCOs. Each core consists of differential spiral inductor $L = L_1 + L_2$ (5.3 nH for LB, 2.9 nH for HB) connected to 15 element switched capacitor array (SCA). Each element of SCA is composed of two 45 fF capacitors connected in series through MOS switch. All the elements of SCA are thermometer coded, resulting in 16 possible tuning sub-bands for each VCO circuit. Each oscillator circuit is compensated by negative resistance pair made of NMOS transistors, biased through switch-



(a) Oscillator architecture with 15 element SCA and switchable current sources.



(b) Single element of switched capacitor array.

Fig. 6: Wide band dual path VCO.

able PMOS current mirror. When oscillator operates over wide frequency range, the quality factor of the resonator varies which in turn translates to significant changes in RF signal amplitude. To allow synthesizer robustness against PVT variations, we found that oscillation amplitude should not be lower than 450 mV for 1.2 V power supply, otherwise output dividers will not operate as intended. To mitigate this, the core can be biased with currents between 1.2 mA to 3.75 mA using 17 switchable current sources, 150 μ A each.

The dual path tuning is implemented in a similar fashion as described by Chi et al. [4]. Care has to be taken to choose proper varactor values as the tuning gain of each branch has to correspond to B ratio of charge pump currents. This is not easy task as scaling the varactor sizes does not translate to similar scaling of tuning gain, the fact omitted from [4]. Moreover, this gain varies with tuning voltage as varactors are inherently non-linear. Despite a total lack of design guidance in the literature, we were able to establish that the most practical is to estimate the varactor gain for the mid point of its tuning curve, which in the case of our circuit is equal to 600 mV. The varactors connected to the integrator path have approximately 4 times the size of their counterparts connected to $R_p C_p$ output of the

filter.

Two oscillators are designed such the lowest bands of HB core overlap with the highest tuning bands of LB core. This way it is possible to tune the RF part of the PLL continuously between 2900 MHz and 6000 MHz for the range of tuning voltages between 0 V and 1.1 V. In practice, this tuning range is somewhat smaller, as simple charge pumps used in this prototype are not rail-to-rail architectures.

g) Frequency dividers

There are two types of frequency dividers present in the prototype. Two differential current mode logic (CML) dividers (one per oscillator core) allow to extract GHz range signals from VCO directly, at the cost of increased power consumption. They also act as buffering stages to prevent excessive loading of the core. There are four possible division ratios available: 1,2,4 and 8, controlled by means of 2 bits of the 68 bit control sequence. The outputs of these dividers are connected directly to a two stage, high speed driver amplifier, delivering differential rail-to-rail signals at RF frequencies (3 GHz–6 GHz) to the chip output. At the same time the outputs of CML divider are connected to 16-31 divider made of standard cells, delivering single ended output in the range from 375 MHz down to 12 MHz. The 16-31 divider is controlled by 4 bits of the 68 bit control sequence.

The feedback divider is also of 16-31 type, connected to the VCOs through fixed-by-8 divider. This way the output signal is slowed down significantly to be compared to the reference source below 25 MHz.

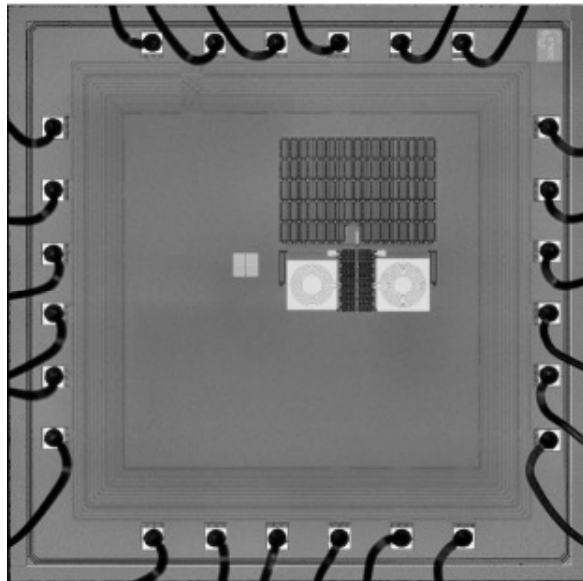


Fig. 7: Photograph of the manufactured chip.

IV IMPLEMENTATION AND MEASUREMENTS

The test chip has been prototyped on multiple project wafer (MPW) using Mini@sic UMC 130 nm mixed

mode 8-metal process through Europractice. Figure 7 presents a microscopic view of the manufactured chip, the die edge length is equal to 2.5 mm, the chip occupies a rectangle of 1 mm by 0.7 mm. The chip has been placed in QFN24 package and tested using high speed prototype board depicted in Figure 8. The test board communicates with PC computer through USB interface through FTDI 2332D chipset. The control software has been developed in LabView to facilitate an access to all of the synthesiser functions. The syn-

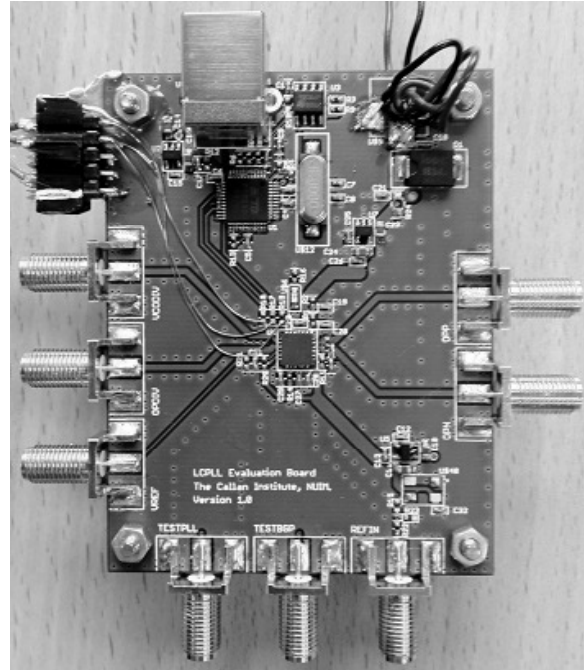


Fig. 8: Photograph of test board.

thesizer has been tested for generation of output signals for all possible division ratios that range from 1 to 248. Using reference frequency of 23.568 MHz from external signal generator, the PLL synthesizer delivers the set of unique 1024 clock signals ranging from 12.16 MHz to 5844 MHz (the RF range has been measured by RedMere, Cork using RF differential probe). The upper oscillation frequency less than 6000 MHz has been impeded by circuit parasitics and reduced voltage range from the charge pumps. Note that the arrangement of integer dividers in this prototype allows the frequency step between output clock signals to be smaller than f_{ref} , going down to as much as 400 kHz around 12 MHz.

Phase noise spectrum has been measured in order to observe PLL locking and to estimate bandwidth. Figure 9 shows two example phase noise spectra for output frequency of 49.610 MHz. Two curves show a free running and phase locked oscillator within PLL, respectively. The PLL bandwidth is equal to 200 kHz, resulting in phase noise at 1 MHz offset from the carrier better than -130 dBc/Hz. The example of power spectrum for the locked signal at the same frequency

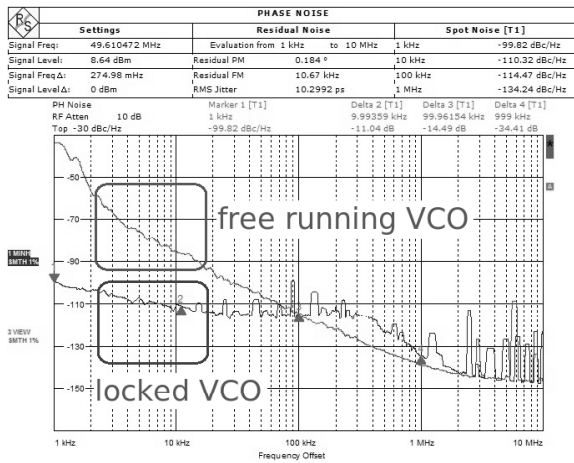


Fig. 9: Example of phase noise spectrum for 49.610 MHz output for free running and locked VCO.

is depicted in Figure 10. Note that the majority of the spurious content seen on the photograph is due to a low performance reference generator used and are below -100 dBc.

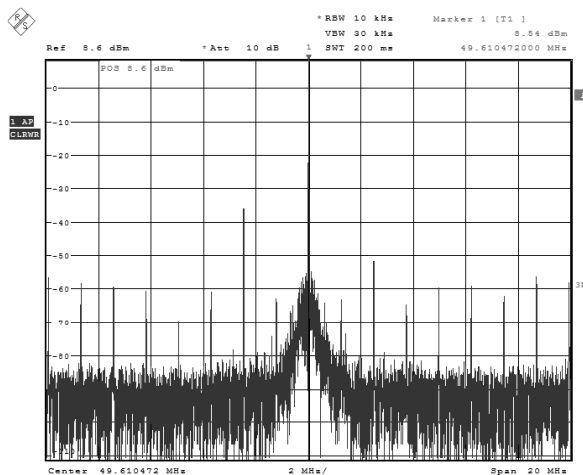


Fig. 10: Example of signal spectrum for 49.610 MHz output.

Last of the test conducted on the prototype involved measurement of long term jitter as a function of frequency and temperature. The method involved fast oscilloscope with jitter measurement capabilities and RF probe connected to the synthesizer output. 1000 randomly chosen set of results, each set consisting of 10k consecutive oscillation cycles has been collected. Using a histogram of zero level crossings distribution, long term jitter has been calculated as a standard deviation over the range of the described 1000 datasets.

At the same time the temperature test involved jitter measurements at temperatures 0, 23 and 60 degree Celsius, using the described histogram method. The worst case long term jitter of 6 ps were observed for both VCO cores at upper boundary of their tuning ranges

and the highest temperature. This can be explained by charge pumps reaching their voltage headroom and therefore increasing the static phase offset contributing to the measured jitter. When oscillators move from their extreme tuning range boundaries, long term jitter value settles at 4 ps. The measured jitter results are 1.5 ps higher from the simulated values using CppSim software [5].

V CONCLUSION

This paper presented the design of fully integrated CMOS LC-PLL frequency synthesizer with average long term jitter of 4 ps over a wide temperature range. The presented circuit has been developed using standard mixed signal UMC 130 nm CMOS process and proves validity of dual path tuning scheme combined in capacitance domain. The presented circuit occupies no more than 0.7 mm² of active area. The proposed low jitter frequency synthesizer represents important example of how wide range of fast clock frequencies can be generated using standard commercial process, large integration scale of digital blocks together with high performance RF circuitry.

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REFERENCES

- [1] F. Gardner, *Phaselock Techniques*. New York: Wiley-Interscience, 2005.
- [2] D. Mijuskovic, M. Bayer, T. Chomicz, N. Garg, F. James, P. McEntarfer, and J. Porter, "Cell-based fully integrated CMOS frequency synthesizers," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 3, pp. 271–279, Mar. 1994.
- [3] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 12, pp. 2054–2065, Dec. 1998.
- [4] C.-W. Lo and H. Luong, "A 1.5-V 900-MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications," *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 4, pp. 459–470, Apr. 2002.
- [5] M. H. Perrott, "Fractional-N Frequency Synthesizer Design Using The PLL Design Assistant and CppSim Programs," *Design*, pp. 1–26, Jul. 2008.