10 GHz, Class-B, 0.5 V, 130 nm CMOS Cross-Coupled Oscillator Design Using Open-Loop Technique

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***Abstract*— The paper presents a method for design of LC cross-coupled oscillators based on open-loop technique and its practical application leading to a high frequency CMOS oscillator prototype. Thanks to the proposed approach, main circuit parameters as loaded quality factor (responsible for phase noise performance of LC oscillator) and steady-state oscillation amplitude can be extracted, without the necessity of time consuming transient simulations. The presented method is not technology specific and allows fast calculations under changing bias conditions. The proposed 130 nm CMOS prototype operates 10 GHz from 0.5 V power supply achieving SSB phase noise of -113 dBc/Hz at 1 MHz offset from the carrier. Low power consumption of 1.09 mW RMS, has been obtained by biasing the oscillator devices to operate in class-B i.e. $V_{GS} = V_{th}$.**

I. Introduction

Rapid development of modern communication standards, both wired and wireless, constantly pushes LC oscillator design to its limits. Low power consumption and phase noise levels, together with large output signal amplitudes are must, however usually can't be obtained simultaneously. These become even more important in deep submicron CMOS circuits, where both a circuit size and available voltage headroom is limited.

The power consumption of RF oscillator can be improved by recognising that the circuit requires less energy to sustain the oscillations than to start them. Oscillator circuit has to employ a certain degree of reconfigurability that allows to decrease the power consumption while in steady state. One of the solutions assumes changing the bias of MOS transistors in the oscillator close to (class-B) or below (class-C) a threshold voltage. As a result, while in steady-state, active devices in the oscillator core stay "on" for shorter time during each period than during start-up [1], and RMS power necessary to operate the oscillator decreases.

The described method is not obvious to achieve and analyse in practical circuits. Firstly, for a successful start-up, cross-coupled oscillator requires both transistors in the core to be biased with DC current to produce negative conductance. When both MOS transistors are biased in cut-off (class-B or class-C) they don't produce any negative conductance as their respective transconductances are equal to 0. Moreover, because the negative conductance oscillator is a closed-loop system, it is impossible to observe how loaded quality factor of the circuit changes with bias conditions, and therefore affects a low phase noise operation of the oscillator.

When negative conductance approach to the oscillator design becomes no longer practical, a feedback analysis can be used instead, even if the original circuit of interest is not normally considered to be a feedback oscillator. This paper presents a new methodology of class-B CMOS cross-coupled oscillator analysis and design based on two techniques known as Alechno's virtual ground circuit transformation [2] and Randall-Hock's open-loop gain correction [3]

II. Open-loop approach to design of a cross-coupled oscillator

The feedback approach to oscillator design allows to analyse two important parameters: open-loop gain and phase response of the loop. Known as Barkhausen's criteria, the circuit is potentially oscillatory if:

$$|G(j\omega_0)| = 1 \rightarrow \text{Amplitude condition} \tag{1}$$

that is the system has unity open-loop gain $G(j\omega)$, and

$$\angle G(j\omega_0) = 2k\pi \quad \text{for} \quad k = 0,1,2,\ldots \rightarrow \text{Phase condition} \tag{2}$$

the total phase shift of open-loop equals zero (or multiple of 2π). Phase response function $\angle G(j\omega)$ of open-loop leads to a loaded quality factor Q_L described by:

$$Q_L = -\frac{\omega_0}{2}\frac{\partial \angle G(j\omega)}{\partial \omega}\bigg|_{\omega=\omega_0} \tag{3}$$

Having (1)-(3) at hand, one is able to analyse the oscillator, providing that the feedback loop around the circuit can be recognised first. In many negative conductance oscillators the loop is usually obscured and circuit transformations have to be employed to define it. One of methods, Alechno's technique [2], allows to rearrange an oscillator circuit by introducing a virtual ground in one of the nodes that under normal operation is not grounded, a signal output for example. This results in circuit rearrangement where a feedback loop

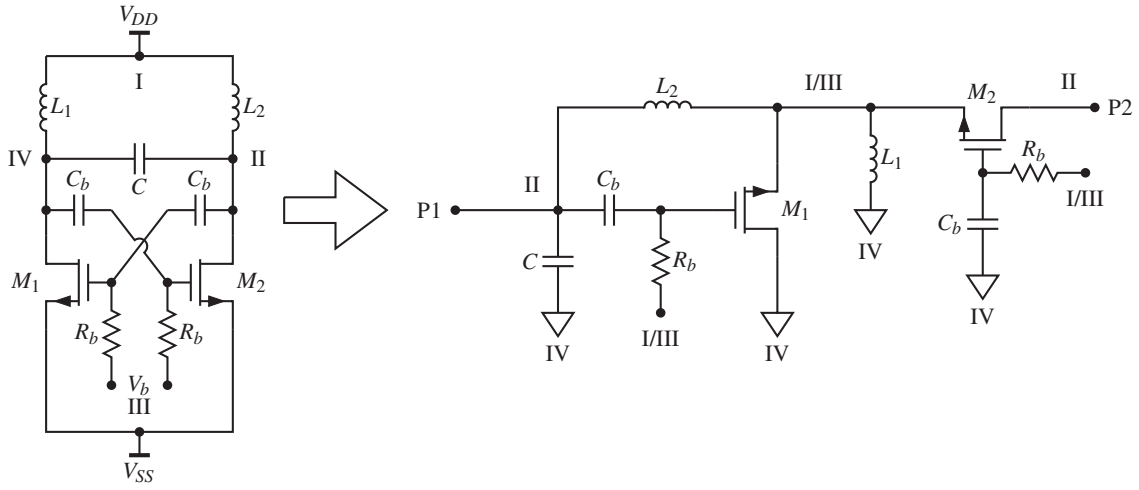

Fig. 1. Proposed cross-coupled class-B oscillator transformation using Alechno's technique.

can be easily recognised and analysed as such. The method has own limitations. As the arrangement of circuit parasitics has been also changed, their influence on resonant frequency of the oscillator may be affected [4]. However, if the parasitics are much smaller than the LC components, the resulting mismatch with practical circuit is small.

Figure 1 presents the proposed transformation of a cross-coupled oscillator with LC tank using differential inductor. Roman numerals on both schematics correspond to the same nodes in both circuits. Note that there are two loops present in the network. The main loop is formed between drain of M_2 and gate of M_1, and the second one, made of LC components around M_1. In general, the LC-M_1 loop can be unstable itself, however only in a presence of M_2 (and the main loop) the proper Barkhausen's criteria can be defined. This is due to the fact that in practical situations, amplitude condition (1) for both loops is different.

The loop has been opened between two transistors, creating an open-loop cascade at node II, with respective ports P1 and P2. The transformation has been conducted in steps. First, all of the points at RF ground have been connected together (V_{DD}, V_{SS} and V_b). Then, the outputs at node IV has been connected to the virtual ground, leading to a single feedback loop between M_1 and M_2 with a single reference to the virtual ground. After transformation, both transistors have to be DC biased through set of blocking capacitors and RF chokes, omitted from Figure 1 for clarity.

Equations (1)-(3) can be calculated using two port network S-parameter analysis in any RF circuit simulator. We have recognised that since an oscillator operates under large signal regime, large signal S-parameters are the most suitable for the characterisation. Small signal behaviour can be still extracted, providing that relatively low magnitudes of test signals are applied.

The last important step of the analysis is a correction of calculated results due to unmatched impedances between the circuit ports and test generators. In theory, during circuit simulation, corresponding reflection coefficients on each port could be found and then used to calculate proper test generator impedances. This process however is tedious, especially if bias conditions change (as in the case of class-B oscillator). It is then more practical is to use Randall-Hock's correction of open-loop gain accounting for unmatched port impedances [3].

$$G_{corr}(j\omega) = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{4}$$

The corrected gain formula (4) allows to estimate (1)-(3), capturing small and large signal behavior of an open-loop cascade depicted in Figure 1.

III. Oscillator design

Using the circuit presented on Figure 1 together with UMC 130 nm RF process libraries, 10 GHz, low power CMOS oscillator has been designed. The differential inductance of 0.5 nH, MOM capacitor of 440 fF and parasitics of cross-coupled pair (approx. 60 fF) form the resonator. The unloaded quality factor is equal to 14.75 at resonant frequency. Gates of both transistors are biased through RC networks consisting of 2 pF MOM capacitor (forming DC block) and 7 kΩ high resistance RF resistor (forming RF block to ground). Cross-coupled pair is formed using two RF NMOS transistors with drawn gate length L of 120 nm, and a total width W of 1200 nm×5 fingers×4 devices (for matching purposes). As circuit is intended to operate at sub-1 V voltage, no current source was used, resulting in relatively large output signal amplitudes, in the range close to V_{DD}. Oscillator produces two out-of-phase sinusoidal signals at nodes II and IV respectively. Note that in the practical circuit, these outputs are connected to the buffer amplifiers whose input parasitics have to be included in the design.

IV. Calculation and simulated results

Figures 2 and 3 present the results of gain and phase calculations of open-loop transfer function, based on

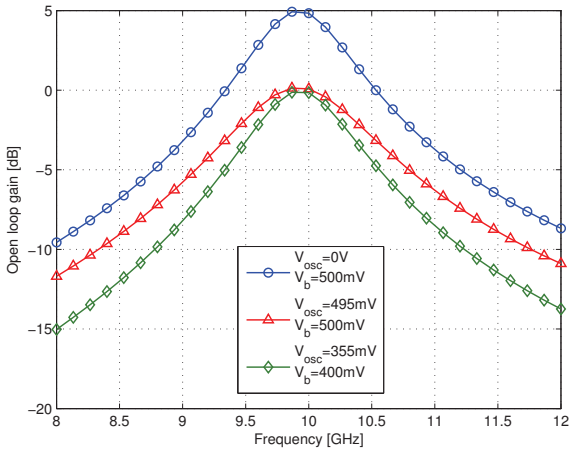

Fig. 2. Open-loop gain of the proposed oscillator.

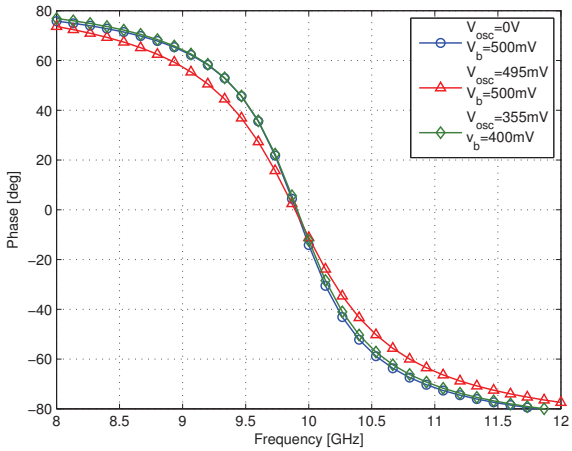

Fig. 3. Phase characteristics of the proposed oscillator.

large signal S-parameters extraction from Eldo RF, using 50 Ω test sources with 11 harmonics. The gates of both transistors in cross-coupled pair are initially biased such $V_{GS} = V_{DD} = 0.5V$. When the signal amplitude of the test sources is small ($P_{in} = -80$ dBm), the circuit provides a gain margin of approximately 4.76 dB at frequency of 9.92 GHz where phase shift around the loop equals 0, refer to curves marked with ◯ on Figures 2 and 3. This bias point provides typical values of power gain in a the range of 3 (in linear scale), enough for oscillations to build-up. When amplitude rises, the non-linearities of both transistors cause compression of gain, until it's margin drops to 0 dB (curves marked with △). This is the moment when oscillator reaches it's steady state. To observe this behavior, the amplitude on both ports of open-loop cascade has to increase from initial small signal value to 0.495 V. Note, that under large signal conditions, a loaded quality factor of the oscillator, as depicted on Figure 4, drops by more than 25% from its initial value of 11.83 down

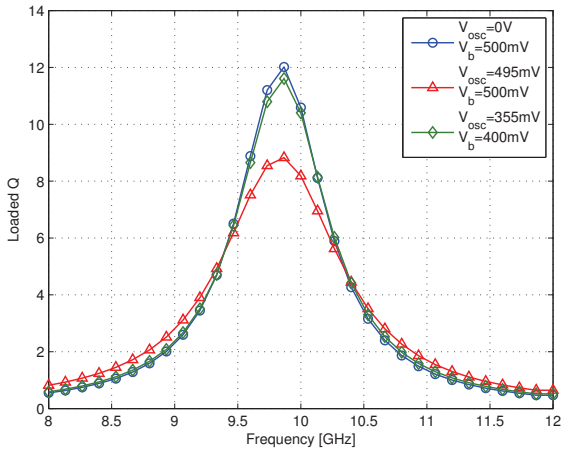

Fig. 4. Loaded Q factor of the proposed oscillator.

to 8.73. This can be explained by instantaneous drain current increase during switching, effectively increasing drain to source conductances in both transistors and present higher load to the resonator.

In the last case, curves marked with ♢ on Figures 2-4, bias conditions has been changed such both transistors are now biased as class-B devices in steady state, $V_{GS} = V_{th} = 0.4V$. It can be seen that signal amplitudes for which open-loop gain drops to 0 dB is now smaller, in the range of 0.355 V, however loaded quality factor is increased to 11.41. In this case, transistors stay "on" for shorter period than during start-up, effectively reducing a loading presented to the resonator.

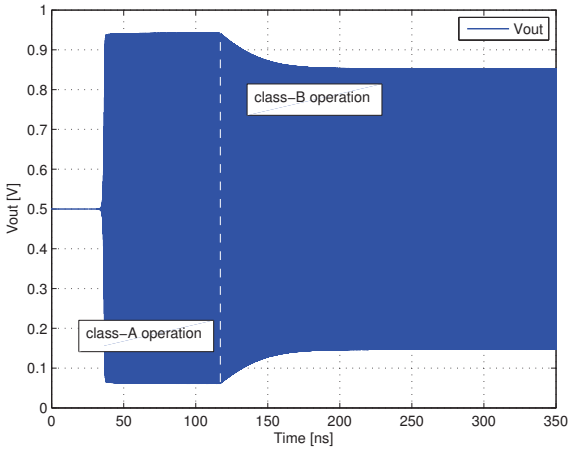

Fig. 5. Simulated single-ended output signal of class-B oscillator.

To confirm usability of the proposed method, the complete oscillator circuit have been simulated in time domain. Figure 5 depicts the simulated response using transient simulation. At time of $T \approx 120$ ns, the bias voltage has been decreased to

400 mV and oscillation amplitude drops, as following the behavior predicted by the open-loop technique. The signal amplitude in steady state class-B oscillator found by transient simulation is equal to 0.352 V versus 0.355 V resulting from open-loop methodology presented in this paper. Using the same transient simulation, it can be confirmed that class-B structure allows to reduce power consumption by approx 30% from initial 1.53 mW RMS at start-up down to 1.09 mW RMS at steady-state, under new bias conditions. Simulated SSB phase noise level of -113 dBc/Hz at 1 MHz offset from 10 GHz carrier has been obtained, as illustrated on Figure 6.

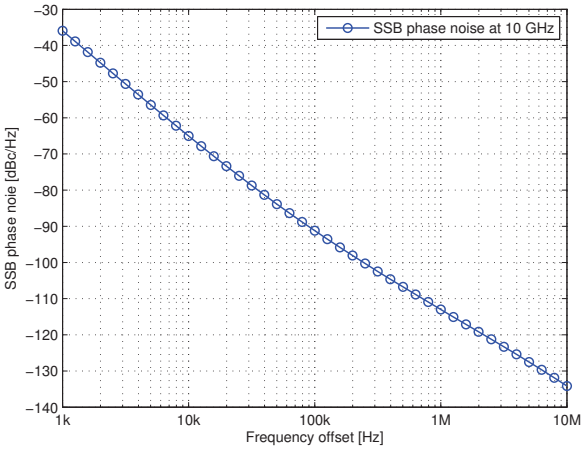

Fig. 6. Simulated SSB phase noise at 10 GHz output frequency.

V. Conclusion

In this paper we have presented a new analysis and design methodology of class-B cross-coupled CMOS oscillators. The use of open-loop approach and large signal S-parameter simulations allow to estimate oscillation amplitude and load quality factor of the circuit, and subsequently optimise it if necessary for low phase noise and low power operation. The obtained results match these of transient simulations, confirming that the proposed open-loop technique provides simple and intuitive yet effective tool improving the design of high performance, low voltage CMOS oscillators.

Acknowledgments

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