Open Loop Approach to Design Low Voltage, 400 mV, 1.3 mW, 10 GHz CMOS Class-B VCO

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***Abstract*— The paper presents a method for design of LC cross-coupled oscillators based on an open loop technique and its practical application leading to a high frequency CMOS oscillator prototype. Thanks to the proposed approach, the main circuit parameters such as loaded quality factor (responsible for phase noise performance of LC oscillator) and steady-state oscillation amplitude, can be extracted without the necessity of time consuming transient simulations. The presented method is not technology specific and allows fast calculations under changing bias conditions. The proposed 130 nm CMOS prototype operates at 10 GHz from a 400m V power supply achieving an average SSB phase noise of -110 dBc/Hz at 1 MHz offset from the carrier and a fractional bandwidth of more than 7.5%. Low average power consumption of 1.3 mW RMS, has been obtained by biasing the oscillator devices to operate in class-B i.e. $V_{GS} = V_{DD} = V_{th}$.**

I. Introduction

The design of LC oscillators at RF frequencies using deep submicron technologies becomes a challenge taking into account the stringent performance of modern communication standards. The trend for battery operated, hand held devices, is to promote low power solutions, leading to improved energy consumption of the whole RF systems. This forces designers to find ways to implement circuits with reduced voltage headroom and lower current amplitudes - clearly a demanding task if the expected performance has to remain high. In the case of oscillators, the performance metrics include: low phase noise to avoid the destructive effects of reciprocal mixing; large signal swing to provide enough drive for mixers or frequency dividers; and small footprint for low cost integration. These requirements become even more stringent when deep submicron technologies are taken into account due to an unique set of additional phenomena related to a very high degree of scaling.

The power consumption of an RF oscillator can be improved by recognising that the circuit requires less energy to sustain the oscillations than to start them. Once the signal is generated and its amplitude is stable, the bias conditions of the circuit can change, thus the amount of current drawn from the power supply is decreased, resulting in smaller RMS power. One solution proposes changing the bias of the transistors in the oscillator close to (class-B) or below (class-C) a threshold voltage. As a result, while in steady-state, active devices in the oscillator core stay "on" for shorter time during each period than during start-up [1], and the RMS power necessary to operate the oscillator decreases.

As the conditions to sustain the oscillations differ from the ones during the start-up period, it makes the design procedure more complicated in practice. Firstly for a successful start-up, a cross-coupled oscillator requires both transistors in the core to be biased with DC current to produce negative conductance. When both MOS transistors are biased in cut-off (class-B or class-C) they don't produce any negative conductance as their respective transconductances are equal to zero. In this case the transistors can be switched on only by the signal generated in the oscillator. Moreover, because the negative conductance oscillator is a closed-loop system, it is impossible to observe how the loaded quality factor of the circuit changes with bias conditions, and how it affects the phase noise performance of the oscillator.

When the negative conductance approach to the oscillator design becomes no longer practical, a feedback analysis can be used instead, even if the original circuit of interest is not normally considered to be a feedback oscillator [2].

This paper presents a new methodology of cross-coupled oscillator analysis and design based on two techniques known as Alechno's virtual ground circuit transformation [3] and Randall-Hock's open loop gain correction [4].

II. Open loop approach to design of a cross-coupled oscillator

A. Oscillation criteria

The feedback approach to oscillator design relies on two important parameters: open loop gain and phase response of the loop. As depicted in Figure 1, a feedback oscillator consists of generic transconductance block, which output is sampled back to the input. Under certain conditions, this circuit has the potential to become unstable if for zero input excitation $X(j\omega)$

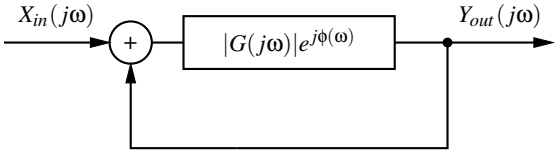

Fig. 1. Generic positive feedback oscillatory circuit.

the output response $Y(j\omega)$ is non-zero. These conditions are widely known as Barkhausen's criteria and can be derived by analysis of the closed-loop gain of circuit from Figure 1:

$$\frac{Y_{out}(j\omega)}{X_{in}(j\omega)} = \frac{G(j\omega)}{1-G(j\omega)} \tag{1}$$

$$|G(j\omega)| = 1 \rightarrow \text{Amplitude condition} \tag{2}$$

$$\phi(\omega) = 2k\pi \;\text{ for }\; k = 0,1,2,\ldots \rightarrow \text{Phase condition} \tag{3}$$

that is the system has unity open loop gain $G(j\omega)$ and the total phase shift of the open loop equals zero (or multiple of 2π). The phase $\phi(\omega)$ of open loop leads to a loaded quality factor Q_L is described by:

$$Q_L = -\frac{\omega_0}{2}\frac{\partial\phi(\omega)}{\partial\omega}\bigg|_{\omega=\omega_0} \tag{4}$$

It is worth noting that amplitude and phase conditions (2) and (3) should not be treated as criteria defining instability of the circuit *per se*. When the open loop gain is larger than one (during oscillator start-up), a non-zero output requires finite input stimulus $X_{in}(j\omega)$ typically provide by thermal noise and power supply transients in the circuit. Periodic signal can subsequently build up if the transfer function (1) has a pair of complex conjugate poles placed in the right hand side of the complex plane. Thus, the presented Barkhausen criteria indicate only a boundary for which the amplitude and frequency of the oscillations become constant. For these reasons, in this paper we assume *a priori* that the circuit is potentially unstable when its open loop gain is larger than one and the transfer function has a pair of complex poles.

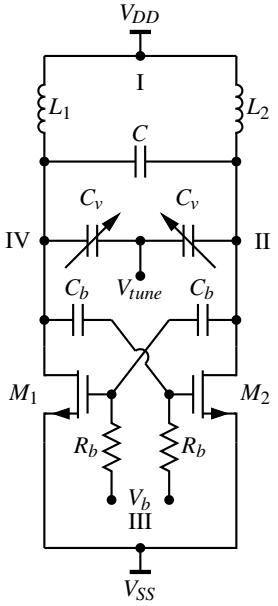

Fig. 2. Low voltage cross-couple CMOS oscillator with separate gate bias.

B. Loop identification

Having (2)-(4) at hand, one is able to analyse the oscillator, providing that the feedback loop around the circuit can be recognised. In many negative conductance oscillators the loop is usually obscured and circuit transformations have to be employed to define it. One of methods, Alechno's technique [3], allows one to rearrange an oscillator circuit by introducing a virtual ground in one of the nodes that under normal operation is not grounded, a signal output for example. In cross-coupled oscillator, this transformation becomes essential as its amplifier operates in a differential mode. When circuit parameters are thus extracted using single ended ports, the ports have to be referenced to a different potential than electrical ground of the circuit to capture the behaviour of the differential phenomena.

Alechno's transformation results in a circuit rearrangement where the feedback loop can be easily recognised and analysed as such. The method has limitations. As the arrangement of circuit parasitics has been changed, their influence on the resonant frequency of the oscillator may be affected [2]. However, if the parasitics are much smaller than the LC components, the resulting mismatch with practical circuit is acceptable. Figure 2 depicts a classical low voltage cross-coupled VCO architecture, with a single differential planar inductor (formed by L_1, L_2), the tank capacitance being a combination of MIM capacitor and MOS varactors, and NMOS pair forming a differential amplifier for the compensation of energy losses in the resonator. Applying Alechno's transformation to this circuit, yields an open loop equivalent presented in Figure 3. Roman numerals on both figures correspond to the same nodes in both circuits. Note that there are two loops present in the network. The main loop is formed between drain of M_2 and gate of M_1, and the second one, made of the inductors around M_1 and its parasitic capacitances. In general, the LC-M_1 loop can also become unstable, however normally at much higher frequency. Thus only in a presence of M_2 the proper Barkhausen's criteria for the main loop can be defined. This is due to the fact that in practical situations, the oscillation conditions (2) for both loops are much different.

The loop has been opened between the two transistors, creating an open loop cascade at node II, with respective ports P1 and P2. The transformation has been conducted in steps. First, all of the points at RF ground have been connected together (V_{DD}, V_{SS} and V_b). Then, the outputs at node IV has been connected to the virtual ground, leading to a single feedback loop between M_1 and M_2 with a single reference to the virtual ground. After transformation, both transistors have to be DC biased through set of blocking capacitors and RF chokes, omitted from Figure 3 for clarity.

Equations (2)-(4) can be calculated using two port network S-parameter analysis in any RF circuit simulator. We have recognised that since an oscillator operates under large signal regime, large signal S-parameters are the most suitable for the characterisation. Small signal behaviour can be still extracted,

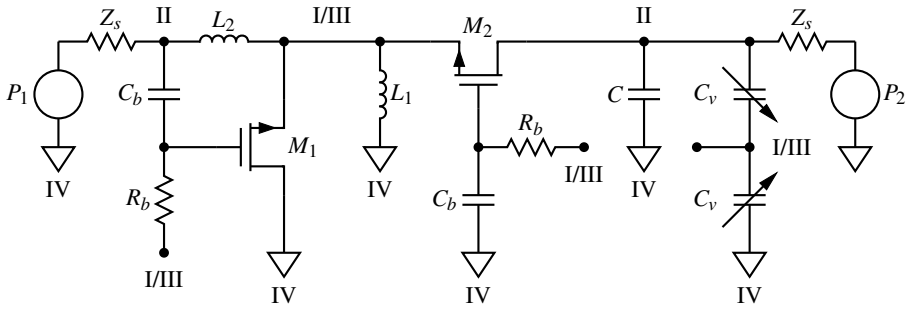

Fig. 3. Proposed cross-coupled class-B oscillator transformation using Alechno's technique.

provided that relatively low magnitudes of test signals are applied.

C. Gain correction

The last important step of the analysis is a correction of calculated results due to unmatched impedances between the circuit ports Z_s and the test generators. In theory, during circuit simulation, the corresponding reflection coefficients on each port could be found and then used to calculate the proper test generator impedances. However this process is tedious, especially if the bias conditions change (as in the case of a class-B oscillator). It is then more practical to use Randall-Hock's correction of open loop gain accounting for unmatched port impedances [2], [4].

$$G_{corr}(j\omega) = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{5}$$

where S_{ij} represent large signal S-parameters defined for two ports respectively.

The corrected gain formula (5) allows to estimate (2)-(4), at the same time capturing small and large signal behavior of an open loop cascade depicted in Figure 3.

III. Oscillator design

Using the circuit presented on Figure 2 together with UMC 130 nm RF process libraries, 10 GHz, low power CMOS oscillator has been designed. The most important circuit parameters are presented in Table I.

The unloaded quality factor of the resonator averages on 10 around the resonant frequency of 10 GHz. The gates of both transistors are biased through the DC block capacitor C_b and the high resistance RF resistor, forming an RF block to ground. The cross-coupled pair is formed using minimum length devices. As the circuit is intended to operate well under 1 V and with limited headroom, no current source was used, allowing for relatively large output signal swing, close to V_{DD}. The oscillator produces two out-of-phase sinusoidal signals at nodes II and IV respectively, that in the practical circuit have to be extracted through the buffer amplifier. In the presented circuit we used capacitively compensated fast differential buffer presented on Figure 4, published previously by Heydari [5]. This type of amplifier uses positive feedback through C_c capacitors which results in superior bandwidth response and the care has to be taken to ensure its stability over frequency of interest. Note, that the amplifier is biased directly by a common mode voltage taken from the oscillator, which results in smaller output amplitudes for the reduced V_{DD} of the VCO operating in the class-B regime. The buffer is powered by 1 V, yet consuming only the fraction of oscillator power as driving the capacitive loads is of a voltage not power type. The load of 0.1 pF is in line with typical loads presented by fast frequency dividers on a chip. To provide a fair approximation

TABLE I

Circuit parameters of the proposed VCO.

Part	Dimensions	Value@10 GHz	Comments
$L_1 + L_2$	OD=116.5 µm, W=9.7 µm, S=1.6 µm, NT=2	0.5 nH Q=22	Diff.
C	W=0.2 µm, L=20 µm, NF=10, M=4, nm=5	220 fF Q=47	MOM RF
C_v	W=2.54 µm, L=0.25 µm, NF=6, M=5	210 fF Q=30-100	MIS RF
M_1, M_2	W=1.2 µm, L=0.12 µm, NF=7, M=4	–	RF
C_b	W=0.2 µm, L=20 µm, NF=40, M=5, nm=5	2 pF Q=47	MOM RF
R_b	W=1 µm, L=7 µm, M=1	7 kΩ	RF

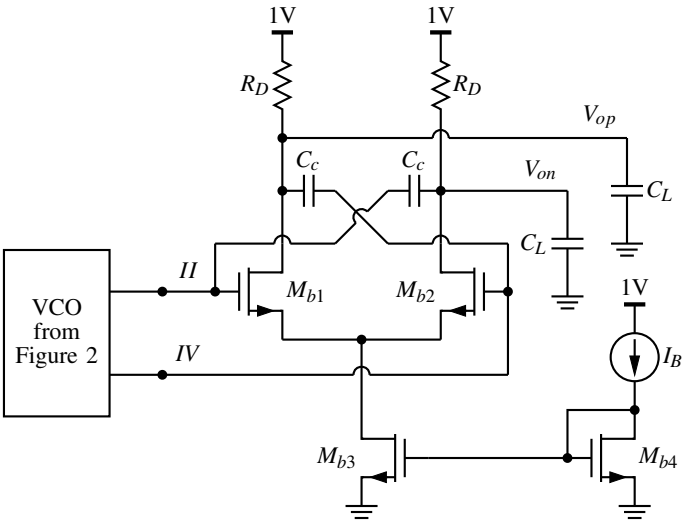

Fig. 4. Capacitively compensated differential output buffer with 0.1 pF loads.

of layout effects, two lumped capacitances of 0.15 pF were connected between oscillator outputs and electrical grounds in both circuits: the open loop cascade and complete VCO.

IV. Calculation and Simulated Results

The circuit from Figure 3 has been co-simulated in Eldo RF and MATLAB. Large signal steady state (SST) simulation allows us to extract the scattering parameters matrix of interest as a function of frequency and port amplitude. When the correction algorithm (5) is employed, a real source impedance of 50 Ω can be used directly. To achieve good accuracy, SST has been set to 11 harmonics.

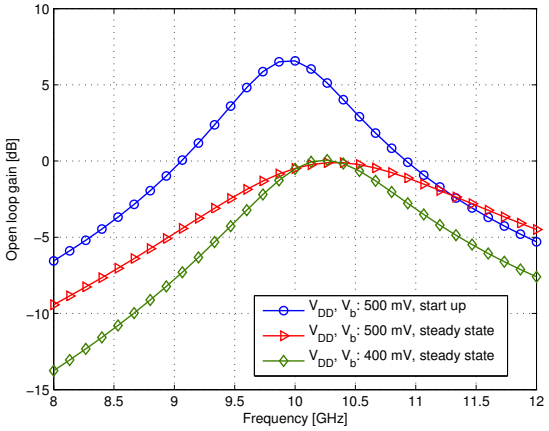

Fig. 5. Open loop gain of the proposed oscillator.

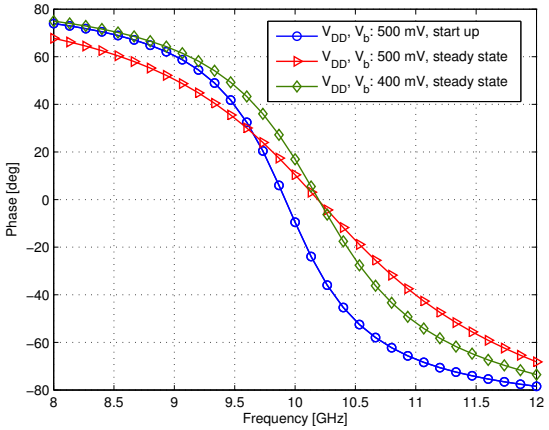

Fig. 6. Phase characteristics of the proposed oscillator.

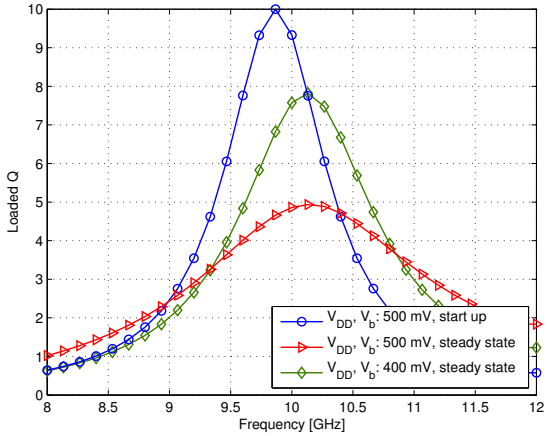

Fig. 7. Loaded Q factor of the proposed oscillator.

A. Open loop transfer function analysis

Figures 5 and 6 present the results of gain and phase calculations of the open loop transfer function. Initially oscillator has been biased for start up. The gates of both transistors in cross-coupled pair were biased such $V_b = 0.5V$. When the signal amplitude of the test sources is small ($P_{in} = -80$ dBm, $V_{in} = 30$ μV), the circuit provides gain margin of approximately 7 dB at frequency of 9.9 GHz where phase shift around the loop equals 0, refer to the curves marked with ◯ on Figures 5 and 6. The tuning voltage V_{tune} is set to 500 mV, which represents the mid point of VCO tuning range. The rather excessive gain margin during start-up is due to the size of transistors used. When operating in class-B, the same devices deliver narrow current pulses to the resonator, but with enough amplitude to compensate the total resonator losses and finite output conductances of the cross-coupled pair. Thus, when biased for start up, the resulting DC current introduces high gain margins.

When the signal amplitude rises, the non-linearities of both transistors cause compression of gain, until the margin drops to 0 dB (curves marked with △). This is the moment when oscillator reaches its steady state. Note that the frequency of oscillations increased to 10.2 GHz as a result of large voltage swing through non-linear LC resonator. As quality factor of the tank is low, drain current pulses delivered by both transistors can not be translated into a pure sinusoidal voltage by such LC resonator. This introduces a non-zero mean (DC shift) voltage in the output signal, reducing a varactor capacitance and results in higher oscillation frequency.

Under large signal conditions, a loaded quality factor of the oscillator, as depicted on Figure 7, drops by 50% from its initial value of 10 down to less than 5. This can be explained by instantaneous drain current increase during switching, effectively increasing drain to source conductances in both transistors and presents higher load to the resonator.

In the last case, curves marked with ♢ on Figures 5-7 represent steady state response of the same oscillator where the bias conditions have been changed. Both transistors are now biased as class-B devices and $V_b = V_{DD} = V_{th} = 400$ mV. Less power is drawn from the source and this reduces the amount of current in the circuit, resulting in smaller oscillation amplitude. When the oscillator operates in class-B, the voltage amplitude on both ports necessary to decrease the open loop gain to 0 dB is close to 450 mV. The transient simulation of to complete oscillator circuit conducted to compare these results showed the signal with amplitude of 370 mV. The main source of this error comes from the placement of varactors at port P2 and introduction of additional set of amplitude dependant parasitics, distributed differently between the closed and open loop circuits. In our previous publication on 5 GHz class-C

oscillator [6], varactors were placed at port P1, resulting in much closer results between SST and transient simulations, in the range of few percent. This shortcoming of high non-linearity placement along the cascade has not been indicated previously by Randall and Hock [4].

In the case of class-B bias scheme the transistors stay "on" for shorter period than during start-up, effectively reducing a loading presented to the resonator. This manifests itself in a improvement of loaded quality factor, that as depicted in Figure 7, now closer to the value of original Q_L during start up. One can think that the Q_L increase should immediately translate into smaller phase noise, however in the case of class-B oscillators this mechanism is not straightforward. Firstly, relatively short current pulses consist of larger number of spectral components that are responsible for noise folding in the oscillators [7]. Secondly, the proposed class-B VCO operates under smaller RMS power and generates smaller amplitudes that may not necessarily translate into an improved phase noise performance.

B. Power consumption, tuning range and figure of merit simulations of complete VCO circuit

To compare the performance of various oscillators, a normalized parameter known as figure of merit with tuning range (FOMT) can be used. This function allows a fair benchmark of phase noise of oscillators working at different frequencies, tuning ranges, fractional bandwidths and power consumption. One generally accepted $FOMT$ has the following form:

$$FOMT = \mathcal{L}(\omega_m) - 20log\left(\frac{\omega_0}{\omega_m}\frac{FBW}{10}\right) + 10log(P) \qquad (6)$$

where $\mathcal{L}(\omega_m)$ is the phase noise at a frequency offset of ω_m, ω_0 is the resonant frequency, FBW is the fractional bandwidth of carrier frequency given in % and P is the DC power consumption of the core expressed in mW. Since in the presented paper class-B oscillator does not consume power in a static sense, the $FOMT$ (6) is modified such that RMS power is taken into account instead. Figure 8 shows a comparison

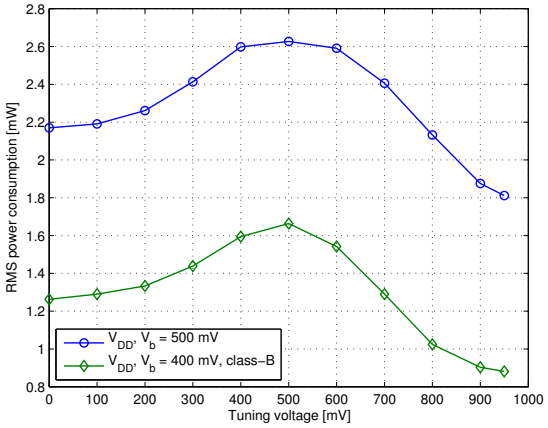

Fig. 8. Power consumption of proposed oscillator as a function of bias conditions.

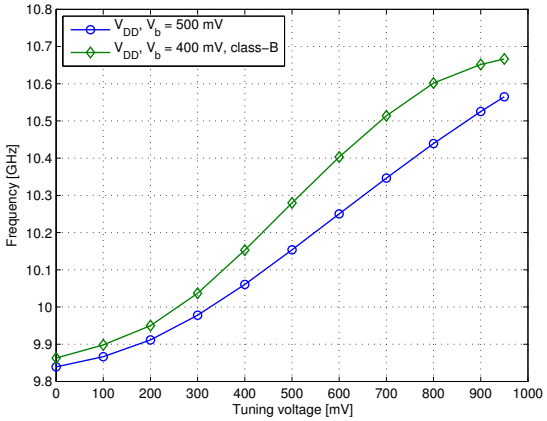

Fig. 9. Tuning curves of the proposed oscillator a function of bias conditions.

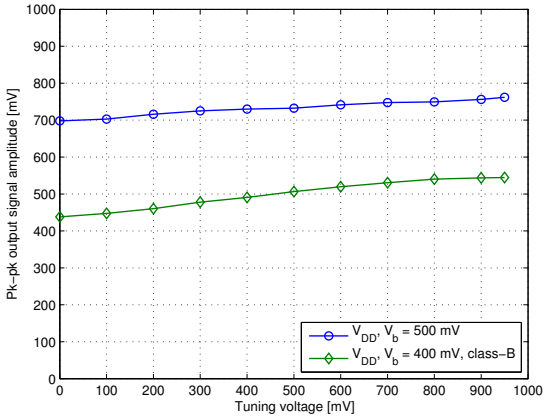

Fig. 10. Pk-pk signal amplitude on the output of loaded differential buffer.

of RMS power consumption of the proposed oscillator, for the considered bias conditions. In the case of class-B regime, the power required to sustain oscillations is reduced by 40% from the start up. Figure 9 shows that the proposed oscillator can be tuned over 0.8 GHz around the centre frequency of 10.27 GHz, which translates to more than 7.5% of fractional bandwidth. Note, that as power supply voltage drops, so does the common mode voltage biasing the varactors, resulting in shift of the VCO frequency up. At these frequencies, DC separation of varactor branches would require impractically high fixed capacitances in order to preserve wide tuning range. For this reason, the proposed circuit relies on the common mode voltage of VCO power supply. In comparison with the open loop results, it can be seen that frequency prediction in Figure 6 (in the range of 10.2 GHz) corresponds closely to the results of simulations of the complete VCO circuit from Figure 9.

Figure 10 presents the peak to peak amplitude of the output voltage for 0.1 pF load. The drop in amplitude in the class-B regime is caused by the smaller common mode voltage biasing the buffer and lower current levels delivered to the resonator. Note, that the gain of the buffer improves slightly with frequency as a result of capacitive positive feedback in the circuit from Figure 4. The differential amplitude levels

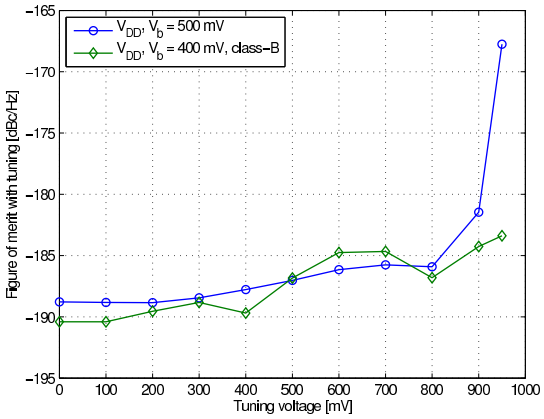

Fig. 11. FOMT comparison between start-up and class-B modes of operation.

are large enough to drive subsequent stages as rail to rail RF output buffers or frequency dividers.

As predicted, the phase noise of the class-B oscillator is higher than of the same circuit operating with constant DC bias. The average SSB phase noise at 1 MHz offset from the carrier of -110.2 dBc/Hz has been extracted. Due to higher non-linearity levels and reduced voltage swing, this value is 3 dB smaller than the phase noise of the same circuit when higher bias voltages are used. However, when combining the consumed power, tuning range and phase noise levels for various tuning voltages, the same FOMT can be maintained, under reduced bias conditions. Figure 11 depicts the results of this comparison. The values in the range of better than -185 dBc/Hz are in line with $FOMT$ levels for sub-1 V power supply CMOS VCO circuits reported in the literature [6], [8]–[12].

V. Conclusion

In this paper we have presented a new analysis and design methodology of class-B cross-coupled CMOS oscillators. The use of open loop approach and large signal S-parameter simulations allow to estimate oscillation amplitude and load quality factor of the circuit, and subsequently optimise it if necessary for low phase noise and low power operation. The obtained results match simulations of complete VCO circuit, confirming that the proposed open loop technique provides a simple and intuitive yet effective tool improving the design of high performance, low voltage CMOS oscillators as the one presented in this paper.

Acknowledgments

This material is based upon works supported by the Science Foundation Ireland under Grant No. 10/CE/I1853. The authors gratefully acknowledge this support.

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