# A Fully Differential Phase-Locked Loop With Reduced Loop Bandwidth Variation

Diarmuid Collins
MASTERS BY RESEARCH

NUI MAYNOOTH
Ollscoil na hÉireann Má Nuad

Callan Institute
National University of Ireland, Maynooth
Co. Kildare
Ireland

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Supervisor: Dr. Ronan Farrell
Head of Department: Dr. Seán McLoone

*Dedicated to my parents Séan and Grace for affording me the education and encouragement to achieve my goal of becoming an IC designer.*

# Abstract

Phase-Locked Loops (PLLs) are essential building blocks to wireless communications as they are responsible for implementing the frequency synthesizer within a wireless transceiver. In order to maintain the rapid pace of development thus far seen in wireless technology, the PLL must develop accordingly to meet the increasingly demanding requirements imposed on it by today's (and tomorrows) wireless devices. Specifically this entails meeting stringent noise specifications imposed by modern wireless standards, meeting low power consumption budgets to prolong battery lifetimes, operating under reduced supply voltages imposed by modern technology nodes and within the noisy environments of complex system-on-chip (SOC) designs, all in addition to consuming as little silicon area as possible. The ability of the PLL to achieve the above is thus key to its continual progress in enabling wireless technology achieve increasingly powerful products which increasingly benefit our daily lives.

This thesis furthers the development of PLLs with respect to meeting the challenges imposed upon it by modern wireless technology, in two ways. Firstly, the thesis describes in detail the advantages to be gained through employing a fully differential PLL. Specifically, such PLLs are shown to achieve low noise performance, consume less silicon area than their conventional counterparts whilst consuming similar power, and being better suited to the low supply voltages imposed by continual technology downsizing.

Secondly, the thesis proposes a sub-banded VCO architecture which, in addition to satisfying simultaneous requirements for large tuning ranges and low phase noise, achieves significant reductions in PLL loop bandwidth variation. First and foremost, this improves on the stability of the PLL in addition to improving its dynamic locking behaviour whilst offering further improvements in overall noise performance. Since the proposed sub-banded architecture requires no additional power over a conventional sub-banded architecture, the solution thus remains attractive to the realm of low power design.

These two developments combine to form a fully differential PLL with reduced loop bandwidth variation. As such, the resulting PLL is well suited to meeting the increasingly demanding requirements imposed on it by today's (and tomorrows) wireless devices, and thus applicable to the continual development of wireless technology in benefitting our daily lives.

# Acknowledgements

The writing up of this thesis was the most gruelling and time consuming task I have ever undertaken, which can only be compared to cutting down a giant oak tree ... with a butter knife! Nevertheless, five months after I first started, and some 10 billion cups of tea later, 200+ pages have resulted to constitute my masters by research thesis. However, the fruitful content contained herein could not have resulted in the slightest without the help of various people.

First and foremost I would like to express my deepest gratitude to my thesis supervisor - Dr. Ronan Farrell. Firstly, for giving me the opportunity to pursue a two year research scholarship in the field of PLLs thereby enabling me achieve my long term goal of becoming an analog IC designer. For this I am infinitely grateful. Next, for allowing me the creative freedom to pursue PLL research topics of interest to me and proving a constant source of solid supervision throughout. Lastly, I would like to thank him for undertaking the unenviable task of correcting the various chapters of this thesis as they were compiled.

Next my gratitude goes to two guys who, from my first day at NUIM, proved an immeasurable source of help for me pertaining to all topics ranging from basic analog design, to VCO complexities, right through to CAD related issues. As much for their patience (regarding my, at times, rather basic questions) as for their in depth knowledge and experience pertaining to IC design, my deepest gratitude goes to Dr. Aidan Keady and "General G", aka. Dr. Grzegorz Szczepkowski. Two guys who, in addition to enabling me get so much out of my research here at NUIM, also made it great fun by being such a good laugh throughout.

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Following on from this, my gratitude is extended to my brother Rory, sister Niamh and close cousin Stephen Gallagher for encouragement and help over the past 29 years in addition to providing uncountable laughs and great times along the way.

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*Diarmuid Collins, October 2011*

# List of Published Contributions

- D. Collins, A. Keady, G. Szczepkowski and R. Farrell, "A 90nm, Low Power VCO with Reduced KVCO and Sub-band Spacing Variation," in *New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International*, June 2011, pp. 141-144.
- D. Collins, A. Keady , G. Szczepkowski and R. Farrell, "Fast Digital Calibration of Static Phase Offset in Charge-Pump Phase-Locked Loops," in *Signals and Systems Conference (ISSC 2011), IET Irish*, June 2011, pp. tbd.
- D. Collins, A. Keady and R. Farrell, "Fast Frequency Calibration of VCO's in Phase-Locked Loops," in *Signals and Systems Conference (ISSC 2010), IET Irish*, June 2010, pp. 147-151.

# Contents

# List of Figures

# List of Tables

CHAPTER 1

# Introduction

## 1.1 Motivation

You don't need to be an electronic engineer to realise that our everyday lives are becoming increasingly dependant on wireless communications. Advances in wireless technology have made the transfer or sharing of information between people simple and efficient thereby maximising its impact to society around the globe.

Central to wireless technology is the wireless transceiver, since it is its task to enable any information be transferred (or received) from (or to) a wireless device. Viewing the basic block diagram for a wireless transceiver in Fig. 1.1 enables us to qualitatively describe its basic operation, in addition to identifying the blocks most fundamental to it, and hence wireless communication itself.

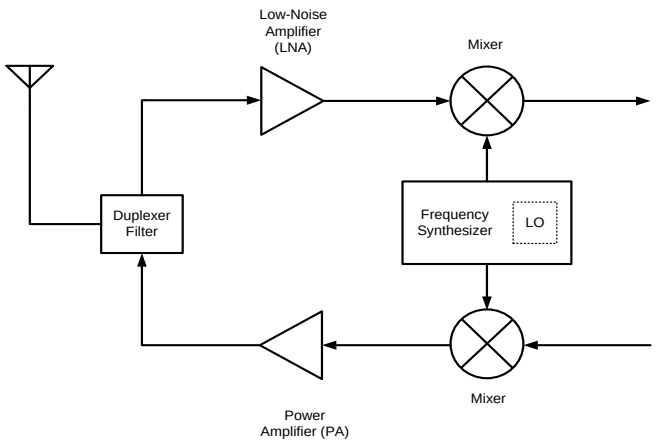



**Fig. 1.1:** Basic block diagram of a wireless transceiver

From Fig. 1.1 we can see the wireless transceiver to consist of two parallel paths. The top path is responsible for receiving the incoming (weak) RF signal which it then amplifies (with the low noise amplifier) before mixing it down (with the mixer and frequency synthesizer) to a lower frequency baseband signal for data manipulation elsewhere within the wireless device. The bottom path is then responsible for transmitting the outgoing signal which it does by first mixing the original baseband signal up to an RF frequency (with the mixer and frequency synthesizer) prior to amplifying the RF signals power (with the power amplifier) and transmitting it. As such, each of the illustrated blocks are fundamental to a wireless transceiver and hence the wireless revolution which has impacted so significantly the last decade or so of innovation. Although the low noise amplifier (LNA) and power amplifier (PA) are extremely important, their further description is beyond the scope of this thesis which focuses solely on the most popular realisation of a frequency synthesizer.

The frequency synthesizer is responsible for generating a stable output frequency with which to mix the received (or transmitted) signal down to lower (or up to higher) frequencies. Stand alone on-chip local oscillators (LO) cannot be used to replace the synthesizer block as their output frequency will not be stable i.e. it will drift from its nominal value. Off-chip stable crystal oscillators can also not be used on their own as they provide no tuning mechanism thereby requiring impractical numbers to be used for modern day wireless specifications (*for example*: GSM1800 would require 374 such oscillators). Therefore, the most popular means of realising a frequency synthesizer which generates a stable output frequency is with a Phase-Locked Loop (PLL). Therefore the PLL, first proposed in 1932 [1], becomes the cornerstone of wireless technology.

Even though literature on PLLs dates back to 1919 [2], [3], it wasn't until their introduction in integrated circuit (IC) form that their popularity really took off. This occurred in the 1970's with the introduction of the 4046 CMOS Micropower PLL from RCA [4], which allowed designers to implement a frequency synthesizer ranging from tens of kilohertz to 1MHz using an external loop filter and feedback divider.[1] Since then the significance of the PLL, along with improvements in fabrication technology, have greatly improved on the 4046 model, with modern day PLLs typically being approx. 2000 times smaller with output frequencies approx. 2000 times larger for a given power consumption [5]. As such, it is common nowadays to find complete transceiver systems embedded on a single IC or as part of a complex system-on-chip (SOC) design.

However, with such high integration comes new design challenges. Firstly, wireless transceivers must operate to various specifications which typically place demanding requirements on the overall noise performance of the PLL. Given that increased integration typically increases common-mode noise (discussed in chapters 3 and 4), low noise

[1] A complete description of the PLL and its various blocks is provided in chapter 2.

performance becomes particularly challenging for PLLs embedded on complex SOCs. In order to ensure the specified output frequency range is reliably covered over process, voltage and temperature (PVT) variation, and to enable multi-band (or standard) operation, modern day PLLs must typically operate over large frequency ranges. However, as will be shown in chapters 2 and 3, this directly conflicts with low noise performance. In addition, circuits intended for wireless applications should consume as little power as possible so as to maximise the battery life of the end wireless product. This places emphasis on the overall power consumption of the PLL which, as will be seen in chapter 2, can also directly conflict with low noise requirements. High integration is then made possible with technology downsizing whereby device dimensions are scaled down by a constant factor. However, hand in hand with this comes a downsizing of supply voltages which, as will be shown throughout chapters 2 and 3, can place severe limitations on overall PLL operation/performance. Further increases in device integration then require the overall silicon area consumption of the PLL to be reduced, requiring new circuit techniques to be achieved without degrading the performance of the end system.

Despite these challenges, in order to maintain the rapid progress we have seen up to this point in wireless technology, it is the task of the design engineer to meet the required specifications in realising PLLs which consume less silicon area and power whilst offering improved performance. The end result of such efforts is thus the realisation of more powerful wireless products which operate faster, perform better and consume less battery power, thereby impacting our everyday lives to an even greater extent than has been seen.

## 1.2 Objective of this Thesis

The objective of this thesis is to realise a PLL architecture suitable for implementation in modern day wireless transceivers. Such a PLL would therefore be extremely applicable in furthering the impact wireless technology has on modern day society.

## 1.3 Contributions of this Thesis

This thesis achieves the following two contributions:

1. Firstly, the thesis shows a fully differential PLL to achieve low noise operation (even in the presence of large scale common-mode noise) whilst consuming less silicon area over conventional PLLs and being applicable to low technology nodes with reduced voltage supplies. As these achievements come at the cost of no significant increases in power consumption, the resulting PLL is thereby deemed well suited for implementation as the frequency synthesizer within wireless transceivers embedded on complex SOCs, fabricated in low technology nodes.

2. Secondly, this thesis presents a VCO architecture which achieves low noise operation over wide frequency ranges, whilst also reducing variations in loop bandwidth which would otherwise result using conventional VCO architectures. As this comes at the cost of no increase in power consumption, it is deemed highly applicable for use in PLLs used in modern day wireless products.

## 1.4 Structure of this Thesis

This thesis is divided into the following parts:

- Chapter 2 presents a system overview of a PLL. Through this, the basic operation of a PLL is explained (both qualitatively and quantitatively), its key components described and most important design criteria/parameters identified. Following from this, the choice of PLL architecture, upon which the final PLL of this thesis is based, is justified with its main weaknesses (which will be addressed in forthcoming chapters) being identified.

- Chapter 3 explains in detail the primary RF block of a PLL - the VCO.[2] Through this, the operating principles and design criteria for the VCO are detailed, its various components described in addition to modelling its noise behaviour. Following from this, the choice of VCO architecture, upon which the VCO used in the final PLL of this thesis is based, is justified with its main weaknesses (which will be addressed in forthcoming chapters) being identified.

- Chapter 4 presents the fully differential PLL as an excellent solution to issues such as low noise operation and operation with reduced supply voltages. Furthermore, this is shown to be achievable using less silicon area over conventional PLL architectures without significantly adding to the overall power budget of the circuit. Following from this, the fully differential PLL, upon which the final PLL of this thesis is based, is justified.

- Chapter 5 addresses variation of the most important PLL design parameter (loop bandwidth) from its nominal, designed for value. Specifically, this issue is addressed by dramatically reducing a prominent source of loop bandwidth variation arising from VCO architectures seeking to achieve low noise operation over wide frequency ranges. Following from this, the VCO architecture for the final PLL of this thesis is justified.

- Chapter 6 presents the final PLL of this thesis - a fully differential PLL with reduced loop bandwidth variation. Schematics of the PLL and specifications which it was

[2] The VCO can be viewed as the LO in Fig. 1.1.

designed to meet are presented. All necessary simulations required to verify the functionality and performance of the PLL are also included to completely justify its choice for meeting the design challenges encountered in modern day PLL design.

- Chapter 7 concludes the thesis in addition to presenting possibilities for future work.

# CHAPTER 2

# Phase-Locked Loop Overview

At the heart of a Phase-Locked Loop (PLL) is a negative feedback system seeking to counteract any changes in the output signal which would otherwise force it to deviate from a multiple of the input signal. This is achieved by matching the phase and frequency of the input signal thereby enabling it to be locked onto, and tracked, by the PLL.

Fundamental to PLL understanding is thus a solid grounding in its associated system theory. As such, it is the core function of this chapter to provide that foundation by describing and introducing the PLL predominantly at system level, upon which the lower level detailed discussions of proceeding chapters will be based. It is therefore imperative the reader be well versed on all the fundamentals discussed in this chapter.

## 2.1 Basic PLL Operation

The PLL is a negative feedback system whose primary function is to generate an output signal with phase locked onto that of the input reference signal. In order to achieve this, its output frequency must be equal to that of the input reference frequency, or equal to a multiple ($N$) times the reference frequency. The core block diagram of a PLL is shown in Fig. 2.1 which consists of a Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO) and feedback divider (/N). As can be seen from this block diagram, both the input reference ($\phi_{ref}$) and feedback ($\phi_{fb}$) signals are applied to the PD. The feedback signal can be seen to be generated from the output of the VCO ($\phi_{out}$) from which it can be divided down by a factor of $N$, depending on end application requirements. The role of the PD is then to generate an output signal whose mean is proportional to the phase variation (phase error) existing between the two input signals. This mean is extracted by

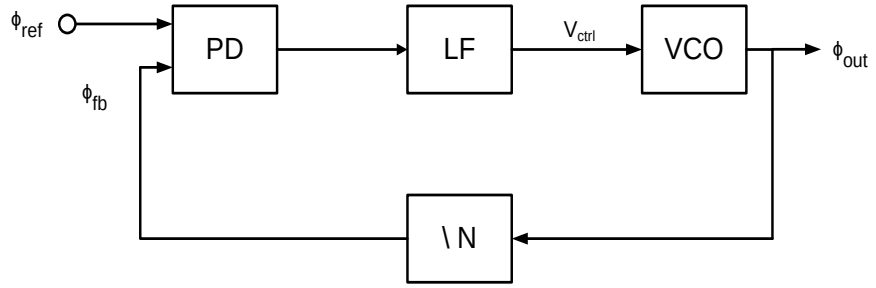



**Fig. 2.1:** Basic block diagram of a PLL

the LF to be sensed by the VCO control line ($V_{ctrl}$) which forces the VCO to adjust its output frequency until (ideally) zero phase error is present at the input to the PD. At this point, the PLL is said to have locked onto the phase and frequency of the input reference signal.

PLL operation can be divided into the following two regions:

- *Pull-in range ($\Delta\omega_P$)*: This represents the input frequency error range ($\omega_e$) within which the PLL will always lock. Frequency error ranges outside of this pull-in range will never attain lock which is defined in section 2.2.2.
- *Lock-in range ($\Delta\omega_L$)*: This represents the input frequency error range ($\omega_e$) within which the PLL will lock within one loop iteration. PLL operation is generally restricted to within this region which is approximated in section 2.7.1.

These concepts are illustrated in Fig. 2.2.

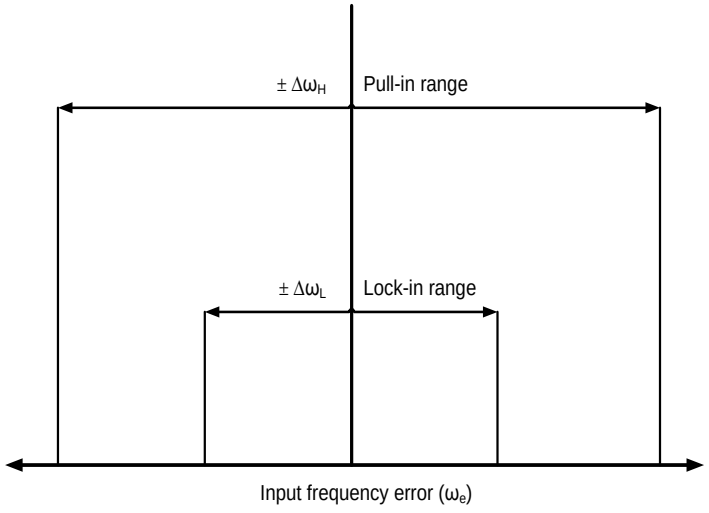



**Fig. 2.2:** Operation ranges of a PLL

## 2.2 PLL Categories

The PLL can be divided into 3 categories: The analog PLL (APLL), digital PLL (DPLL) and the all-digital PLL (ADPLL). The APLL and DPLL comprise very similar architectures which only differ in phase detector architecture. The ADPLL comprises an all digital architecture and will not be discussed in this thesis.

### 2.2.1 Analog PLL

Both input reference and feedback signals are applied to the inputs of a multiplier whose mean output signal (extracted by the LF) varies in proportion to the input phase error. This architecture dominated the earliest PLLs but is rarely used nowadays due to the following disadvantages:

- Maximum phase error detectable is $\pm\pi/2$ rads. This results in small lock-in ranges in comparison to those achievable for a DPLL.
- Pull-in range is dependent on LF architecture.
- Frequency detection is not possible. This leads to prolonged pull-in times.
- Gain of the PD is dependent on input signal amplitudes [6]. Where amplitudes are not well controlled this may result in large variations of the PD gain which, as will be shown in chapter 5, gives rise to undesirable loop characteristics.

### 2.2.2 Digital PLL

A DPLL employs a PD consisting of logic gates with all other blocks remaining similar to the APLL. Various choices of PD exist for this type of PLL.

*EXOR PD*: Applying both the input reference and feedback signals to the input of an XOR gate constitutes the simplest type of DPLL. This type of PD is an improvement over a multiplier PD as its gain is independent on input signal amplitudes. However, it can only detect phase errors between $\pm\pi/2$ rads resulting in small lock-in ranges where frequency detection is not possible leading to prolonged pull-in times. Pull-in ranges are also dependent on LF architecture.

*JK-flipflop (Edge-triggered) PD*: By applying both the input reference and feedback signals to the edge-triggered inputs of a JK-flipflop a second type of PD can be realised. Like the EXOR PD, the gain of the JK-flipflop is independent on input signal amplitudes, although unlike the EXOR PD it can detect phase errors between $\pm\pi$ rads leading to increased lock-in ranges. Frequency detection is however once again not possible with

pull-in ranges being dependant on LF architecture.

*Phase-frequency-detector (PFD)*: The PFD is fundamentally different to the previous PDs as, in addition to phase detection, it also provides frequency detection. The block diagram of a basic PFD is illustrated in Fig. 2.3.

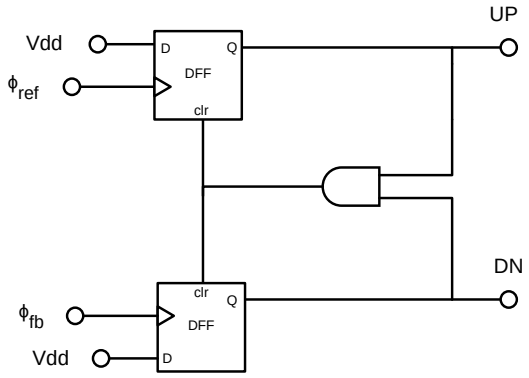



**Fig. 2.3:** Block diagram of a basic PFD

Fig. 2.3 shows the PFD to consist of 2 D-type flipflops (DFFs) and an AND logic gate. Both inputs of the DFFs are tied high with the input reference and feedback signals applied to their clocking inputs. The outputs of the DFFs are denoted as "UP" and "DN" (down) and are connected via the AND gate back to the reset inputs of the DFFs. This enables the following truth table of operation:

| UP | DN | state |
|---|---|---|
| 0 | 0 | Z |
| 0 | 1 | -1 |
| 1 | 0 | +1 |
| 1 | 1 | X |

**Table 2.1:** Truth table of operation for a PFD

As seen in Table 2.1, the resetting operation inhibits the final state to occur thereby enabling the PFD to behave as a tri-state device. It is this tri-state behaviour which is fundamental to the PFDs attractiveness over the EXOR or JK PDs as when UP = DN = 0 (which as will be shown in section 2.3 corresponds to the PLL being locked) the output of the PFD is in a high impedance state. Since this output is connected to the LF (see Fig. 2.1), the LF can thus have a finite output when its input is 0, causing it to behave as an ideal integrator. Ideal integrators exhibit infinite DC gain and so given that pull-

in range is directly proportional to the LF DC gain [7], this achieves the following ideal pull-in range irrespective of LF architecture:

$$\Delta\omega_P \to \infty \tag{2.1}$$

In addition, the tristate behaviour also achieves frequency detection. To see how, suppose that the input reference frequency is greater than the feedback frequency i.e. $\omega_{ref} > \omega_{fb}$. This forces the PFD to toggle between the states 0 and +1, spending increasingly more time in the +1 state for $\omega_{ref} >> \omega_{fb}$ and never entering the -1 state. Suppose now that the input reference frequency is less than the feedback frequency i.e. $\omega_{ref} < \omega_{fb}$. This forces the PFD to toggle between the states 0 and -1, spending increasingly more time in the -1 state for $\omega_{ref} << \omega_{fb}$ and never entering the +1 state. As the output varies monotonically with frequency error it is therefore capable of frequency detection. This is an attractive feature as it greatly reduces pull-in time (shown in section 6.6).

Plotting the mean value of PFD output ($U_{PFD}$) against input phase error ($\phi_e$) reveals its transfer characteristic, as shown in Fig. 2.4.

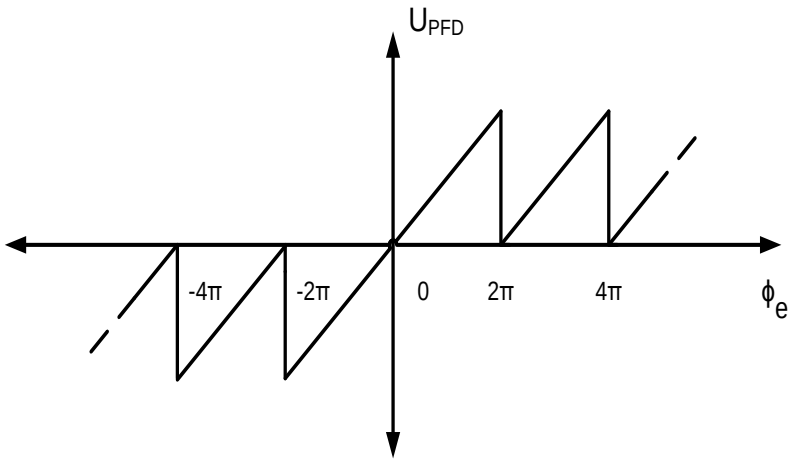



**Fig. 2.4:** Transfer characteristics of a PFD

The transfer characteristic of the PFD in Fig. 2.4 is seen to be highly non-linear. As phase errors increase from 0 to $\pm 2\pi$, the characteristic wraps around itself thereby creating a periodic waveform of period $2\pi$. As a result the PFD is capable of detecting input phase errors within the range:

$$-2\pi < \phi_e > 2\pi \tag{2.2}$$

This leads to increased lock-in ranges over the previous PDs (an approximate definition is provided in section 2.7.1).

## 2.3 Charge-Pump PLL (CP-PLL)

We know from the preceding section that the PFD proves the optimal choice for PD as it provides (ideally) infinite pull-in ranges irrespective of LF architecture, reduced pull-in times and extended lock ranges. When placed in a PLL, its output logic states must be converted into analog signals to control the VCO. This is the function of the charge-pump (CP) which always accompanies the PFD in a PLL to form a PFD-CP, as shown in Fig. 2.5.

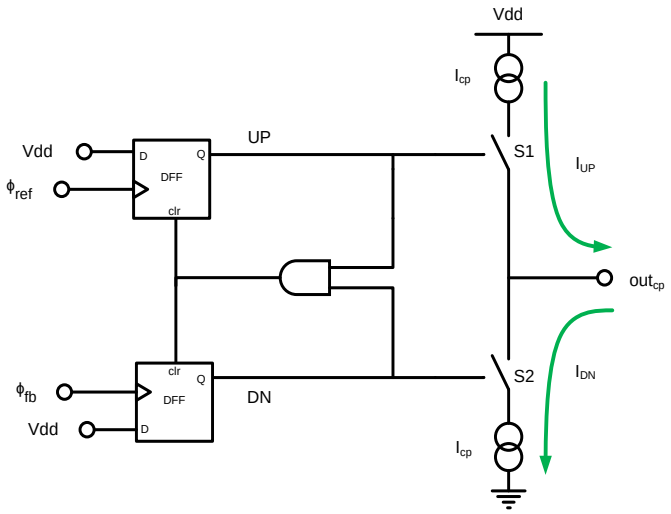



**Fig. 2.5:** Block digram of a basic PFD-CP

The CP shown in Fig. 2.5 has only one output thereby terming it a "single-ended CP". It consists of a current source, current sink and two switches with inputs directly connected to the outputs of the PFD. The switches control the current from the CP ($I_{cp}$) where it is sourced or sinked in proportion to the input phase error. Current is sourced through $S1$ which is controlled by the "UP" output of the PFD. This source current is thereby termed the "UP current" ($I_{UP}$) with $S1$ termed the "UP switch". Current is sinked through $S2$ which is controlled by the "DN" output of the PFD. This sink current is thereby termed the "DN current" ($I_{DN}$) with $S2$ termed the "DN switch". The UP and DN currents must be respectively defined by a current source and current sink to maintain them constant so as to achieve desirable loop performance (shown in section 2.7.4 and Chapter 5). The combination of $S1$ and its current source is therefore termed the "UP network" with $S2$ and its current sink termed the "DN network".

In Fig. 2.5, $S1$ and $S2$ are shown as ideal devices. However, in practice these are realised as complimentary MOSFET devices whose behaviour is not so ideal. The resulting single-ended CP is shown in Fig. 2.6 where the $UP$ ($S1$) and $DN$ ($S2$) switches are realised with PMOS ($M1$) and NMOS ($M2$) devices respectively.

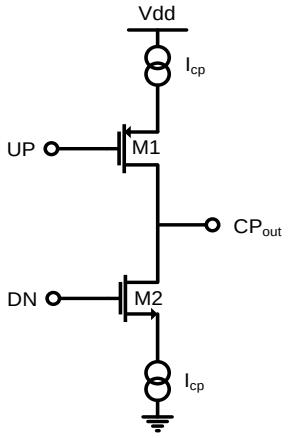



**Fig. 2.6:** Single-ended CP with practical switches

The non-ideal behaviour of these practical switches arises due to the capacitance now seen at the PFD outputs. This is dominated by the input gate capacitances of $M1$ and $M2$ which must be charged up prior to an inversion layer forming and the MOSFETs turning on. This renders a finite turn-on time for the switches which can create problems for the detection of small input phase errors. Small input phase errors render narrow pulses on the PFD outputs, whose pulse durations may be insufficient for turning on the switches and sourcing or sinking the required proportional current. Such small input phase errors thus go undetected leading to a deadzone of operation defined as:

$$-\phi_{dz} \leq \phi_e \geq +\phi_{dz} \tag{2.3}$$

where the maximum undetected input phase error is represented as $\phi_{dz}$.

Fortunately, due to finite propagation times within the PFD it outputs narrow pulses at a frequency $\omega_{ref}$ when the PLL is in lock (i.e. in steady state). Provided the duration of these steady state pulses are longer than the turn-on times of the switches, the switches will be on for any input phase error present. Therefore, this undesirable deadzone can be eliminated if the following is adhered to:

$$t_{pfd} > t_{on} \tag{2.4}$$

where the duration of PFD steady state pulse widths and the turn-on time of the CP switches are represented by $t_{pfd}$ and $t_{on}$ respectively. This is achieved in practice by inserting a delay (chain of inverters) with propagation time equal to $t_{on}$, in the reset path of the PFD. This therefore modifies the PFD-CP block diagram of Fig. 2.5 to its more realistic implementation in Fig. 2.7, where the delay block is depicted as $t_{on}$.

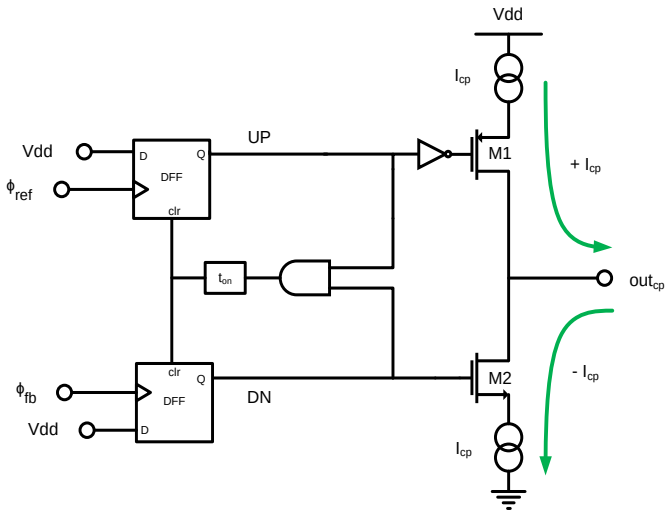



**Fig. 2.7:** Practical PFD-CP which eliminates deadzone

As can be seen in Fig. 2.7, an inverter is inserted after the input to the AND gate and connected to the gate of M1. This inverter can be inserted on either of the CP input lines and is simply required to achieve equivalent behaviour between both switches.

When placed in a PLL, the PFD-CP realises a charge-pump PLL (CP-PLL) whose block diagram is shown in Fig. 2.8.

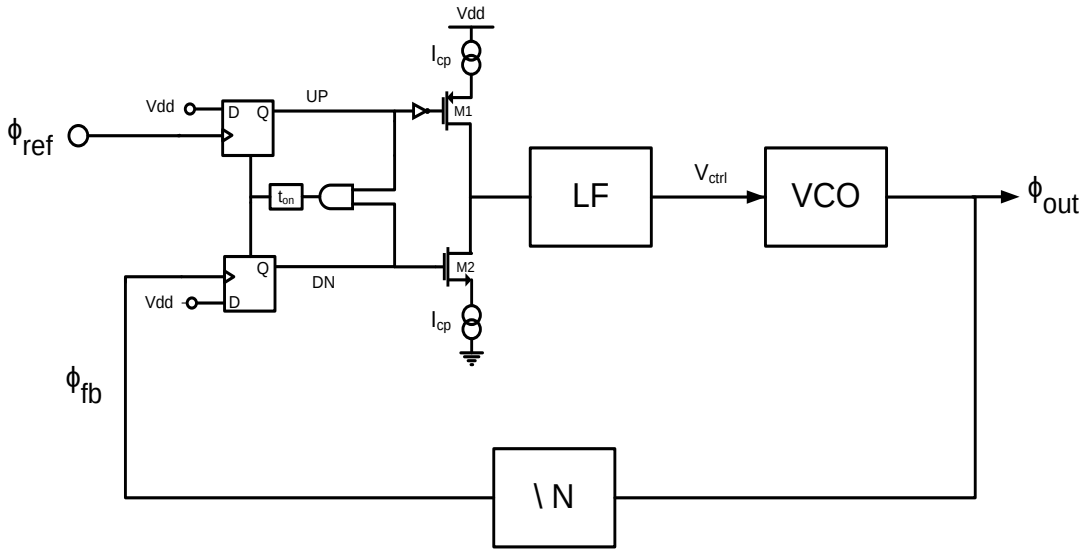



**Fig. 2.8:** Block diagram of a basic CP-PLL

Referring to Fig. 2.8, the operation of a CP-PLL can now be qualitatively described (a quantitative description follows in section 2.4). As shown in section 2.2.2, when the PFD detects a phase (and frequency) error between the input reference ($\phi_{ref}$) and feedback

signals ($\phi_{fb}$), it outputs UP/DN pulses (+1/-1 states) in proportion to the initial error, forcing the CP to source or sink current ($I_{cp}$) accordingly. As the mean of this output contains information on the input error it needs to be extracted by the LF which, in doing so, also converts it into a voltage to be directly sensed by the VCO control line ($V_{ctrl}$). This then forces the VCO to alter its output frequency until the PLL output signal ($\phi_{out}$) equals an integer multiple ($N$) times the input reference frequency, in other words - until the PLL locks. This operation is summarised in the following table:

| | UP | DN | $M1$ | $M2$ | $I_{cp}$ | $V_{ctrl}$ | $\phi_{out}$ | $\phi_{fb}$ |
|---|---|---|---|---|---|---|---|---|
| $\phi_{ref} > \phi_{fb}$ | 1 | 0 | ON | OFF | +ive | increase | increase | |
| $\phi_{ref} < \phi_{fb}$ | 0 | 1 | OFF | ON | -ive | decrease | decrease | |

**Table 2.2:** Operation table for a CP-PLL

Assuming the LF behaves as an ideal integrator (i.e. exhibits infinite DC gain), the pull-in range for the CP-PLL is as defined in (2.1). In reality however, leakage currents within the LF force it to behave less ideally hence exhibiting a finite DC gain. This reduces the pull-in range to [8]:

$$\Delta\omega_P \approx \sqrt{K_{DC}K} \tag{2.5}$$

where DC gain of the PLL and PLL loop bandwidth (defined in section 2.7) are represented by $K_{DC}$ and $K$ respectively. Although a reduction from the ideal, the pull-in range defined in (2.5) is still very large, where practical pull-in ranges are more commonly limited by the output frequency range of the VCO.

Due to its superior performance over other DPLLs, the CP-PLL is the most commonly implemented PLL architecture in industry today. Nevertheless, it does exhibit various issues, the most dominant of which will be addressed in this thesis. The first of these are due to CP non-idealities.

### 2.3.1 Issues with the CP Addressed in this Thesis

When in lock no changes to the overall PLL state should occur. This reduces to constraining the VCO control line ($V_{ctrl}$) to remain at its nominal voltage such that the PLL output frequency remains an integer multiple of the input reference frequency. However, due to non-idealities within the CP, $V_{ctrl}$ can vary during steady state thereby inducing frequency variations in the VCO and PLL outputs. This is extremely concerning as these variations appear as spurious frequencies (spurs) in the PLL output frequency spectrum which can severely degrade its spectral purity, and hence overall noise performance. The resulting phase error produced by these spurs at the input to the PFD

is termed the steady state phase error or more commonly - static phase error.

Static phase error ($\phi_v$) is defined as [9]:

$$\phi_v = \frac{2\pi\Delta\omega}{K_{VCO}I_{cp}F(0)} \tag{2.6}$$

where VCO gain and LF DC gain are represented as $K_{VCO}$ and $F(0)$ respectively. The parameter $\Delta\omega$ then represents the difference between the feedback and reference frequencies when in lock. This non-zero frequency difference may at first be surprising as when in lock, the input and feedback frequencies should equal each other. However, in practice these frequencies almost never exactly equal each other [8], hence giving rise to $\Delta\omega$.

Immediately obvious from (2.6) is yet another benefit of using a PFD since, as discussed in section 2.2.2 it forces the LF to ideally exhibit infinite DC gain which, from (2.6) reduces $\phi_v$ to 0. However as discussed in section 2.3, in practice $F(0)$ is never infinite (although it is larger than with other PDs) and thus static phase error always exists in a CP-PLL. It sources are shown in Fig. 2.9.

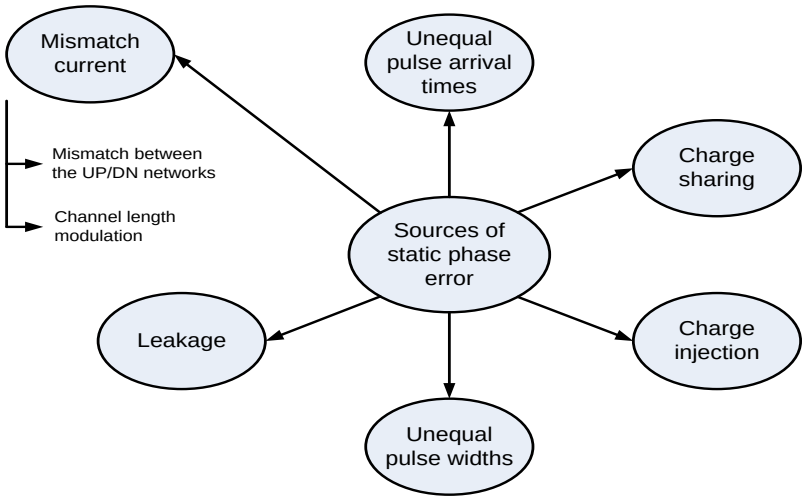



**Fig. 2.9:** Sources of static phase error

Mismatch current is the most dominant source of static phase error [10] and occurs due to mismatches between the UP and DN networks of the CP and channel length modulation effects. This gives rise to unequal UP and DN currents flowing during the steady state pulse duration which violates Kirchoffs current law at the output node. As a result, a net flow of charge to or from the LF ensues such that its voltage is altered to equalise the UP and DN currents (shown in section 4.3.2). This will however alter $V_{ctrl}$ hence generating spurs at an offset of $\pm\omega_{ref}$ (thereby termed "reference spurs") from the PLL nominal output frequency. Provided this mismatch current flows only for the steady state pulse duration, the resulting static phase error is defined as [11]:

$$|\phi_v| = 2\pi \frac{t_{pfd}}{T_{ref}} \frac{\Delta i_{cp}}{I_{cp}} \tag{2.7}$$

where mismatch current and reference period are represented by $\Delta i_{cp}$ and $T_{ref}$ respectively.

Assuming mismatch current only flows for the duration of the steady state pulses,[1] an effective approach to reducing $\phi_v$ is by reducing $t_{pfd}$ in (2.7). However, to avoid deadzone this approach is limited by (2.4). Another approach to reducing $\phi_v$ is through increasing $I_{cp}$. However, as this results in increased power consumption it is unattractive for low power applications. A more attractive approach is thus by reducing the mismatch current itself, which in practice corresponds to improving matching between the UP/DN networks and making them more robust against channel length modulation effects.

Matching between the UP/DN networks can be improved by reducing device mismatch. This occurs due to mismatches between the aspect ratios and threshold voltages ($V_T$) of devices. Provided non-minimum dimensions are employed, mismatch between the aspect ratios of devices is small, becoming increasingly negligible (for non-minimum dimensioned devices) as technologies shrink. Although the same is true for threshold voltage variation ($\Delta V_T$), it still remains significant making it the dominant source of device mismatch. In [12], $\Delta V_T$ was shown to exhibit the following well known proportionality:

$$\Delta V_T \propto \frac{1}{\sqrt{WL}} \tag{2.8}$$

where the transistor widths and lengths (aspect ratio) are represented by $W$ and $L$ respectively.

Therefore, it is clear from (2.8) that increasing device dimensions decreases $\Delta V_T$ by the square root of that increase. This is an especially attractive approach as it results in long channel devices whose increased output conductances make them more robust against channel length modulation effects. Nevertheless, for a single-ended CP (see Fig. 2.6), such matching efforts inevitably result in trying to match PMOS with NMOS devices. The inherent physical differences between these devices (for example the difference between the mobilities of their majority carriers) presents a severe limitation to the degree of matching obtainable. As such, this represents a serious issue with single-ended CPs which is addressed in chapter 4 where another CP architecture is introduced and shown to practically eliminate the net effect of mismatch current.

Another dominant source of error is due to unequal pulse arrival times which results from the difference in arrival times of the steady state pulses at the CP switches. This occurs due to the inverter shown in Fig. 2.7 which forces the pulse arrival times to be out of sync by $t_{inv}$ s, where $t_{inv}$ represents the propagation time of the inverter. As a result, a current will flow in one network (the DN network in Fig. 2.7) and not the other

[1] This assumption does not hold for all CP architectures, see section 6.4.2.

for $t_{inv}$ s, hence contributing to the reference spurs and giving rise to the following static phase error:

$$\phi_v = t_{inv}\ \omega_{ref} \tag{2.9}$$

Although the impact of this source reduces with downsizing technologies ($t_{inv}$ reduces), it is inherent in single-ended CPs, raising more concerns over this CP architecture. These concerns are addressed in chapter 4 which introduces a CP architecture which eliminates this source of error.

The remaining sources of error are negligible or can be addressed with clever design and so will not be focused on in this thesis. For example, charge sharing occurs due to the mismatch in peak currents at the turn-on instances of the switches. Although this reduces with improved matching, it can be further reducing using a voltage follower [11] or current steering [13] technique. The current steering approach however is favoured as it is more applicable to lower technology nodes and reduces turn-on times of the switches, hence reducing $t_{pfd}$ (see (2.4)) and $\phi_v$ in (2.7). Charge injection then occurs due to the injection of charge from the switches onto the LF when they turn-off. It is not a significant source of static phase error but can be reduced using smaller switches which simply inject less charge. This approach also has the benefit of reducing the input gate capacitances of the switches, leading to reductions in $t_{on}$, $t_{pfd}$ and $\phi_v$ as previously discussed. Nevertheless, care should be taken not to make the switches so small as to dramitically increase their threshold voltage mismatch ($\Delta V_T$) in (2.8), where in practice the optimum dimensions will be found through simulation. Unequal pulse widths then occur due to mismatches in the PFD leading to unequal widths of the steady state pulses. For modern technologies, mismatches in digital circuitry are negligible and so this source can be neglected. Finally, for technology nodes of 90nm and below, leakage currents within devices severely increases. This is especially true for gate leakage whose mismatch cannot be addressed using classical techniques which can actually worsen its effect [14]. Therefore to address this issue, new techniques are currently being developed such as mismatch reduction through digital calibration [10],[15],[16].

Despite the issues arising as a result of the CP (and other issues discussed in sections 2.7.4 and 2.8.3), the performance of the CP-PLL is still far superior to other DPLLs. As such, this thesis focuses solely on the CP-PLL, which from here on in the text is what is referred to when the term "PLL" is used.

## 2.4 PLL Transfer Characteristics

To quantify the behaviour of a PLL its transfer characteristics need to be derived. As seen in Fig. 2.4, the transfer characteristics of the PFD are highly non-linear hence causing

the pull-in process to be highly non-linear. In addition, the PFD essentially performs a sampling operation causing the pull-in process to also be non-continuous in time. Therefore due to the nature of the PFD, the pull-in process is a discrete, non-linear process requiring cumbersome mathematics to describe it which does not lend itself easily to practical PLL design. Fortunately however, under a few simplifying assumptions the PLL can be viewed as a linear time-invariant (LTI) system to which powerful transfer function theory, already existing for APLLs, can be applied. To do this however, we must define the conditions under which each block of the PLL exhibits linearity and time-invariance, define their respective transfer functions before combining them to give the overall transfer function of the PLL in describing its transfer characteristics.

### 2.4.1 PFD-CP

This is the most non-linear block of the PLL due to the non-linear transfer characteristics of the PFD. As can be seen in Fig. 2.4, if input phase errors are restricted to within the ranges defined by (2.2), the PFD-CP can be viewed as a linear block.

Due to its switching nature, the PFD-CP is also time-varying. If however the input signals are periodic (or close to periodicity), and the state of the PLL only changes after a number of input cycles of the reference signal, then the PFD-CP can be viewed as time-invariant over the duration of these cycles [9].

This first constraint for time-invariance basically requires the PLL to be locked or close to lock such that the input signals are periodic or close to periodicity. The second constraint requires the update rate of the loop to be less than the input reference frequency such that the PLL is updated only after every number of input reference cycles. In section 2.7.1, the update rate of a PLL is shown to be represented by the PLL loop bandwidth ($K$) which allows the second constraint to be more succinctly stated to hold when:

$$K \ll \omega_{ref} \tag{2.10}$$

Therefore, although the PFD-CP is a non-linear, time-varying block, under the above assumptions it can be viewed as an LTI block. Following from this, its transfer function can be defined (see Appendix A.1 for derivation) as:

$$H_{PFD-CP}(s) = \frac{I_{cp}}{2\pi} \tag{2.11}$$

### 2.4.2 LF

In its most basic form, the LF presents an equivalent impedance to the loop ($Z_{LF}$) as shown in Fig. 2.10.

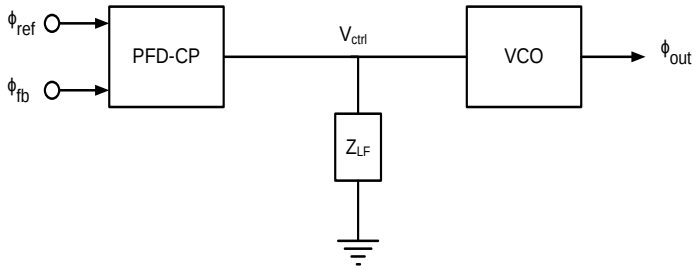



**Fig. 2.10:** Equivalent impedance presented to the loop by the LF

Its transfer characteristic is therefore inherently linear and time-invariant, which for the moment is defined to be:

$$H_{LF}(s) = F(s) \tag{2.12}$$

This definition is sufficient for deriving the transfer characteristics of a PLL. As F(s) depends on LF architecture its exact definition is left to section 2.6.4 where the various LF architectures are discussed.

### 2.4.3 VCO

The VCO is the primary RF block of a PLL and hence one of the most challenging to design, whose thorough description is left to chapter 3. However, for the purposes of deriving its overall transfer characteristics its basic role is sufficient to be understood. This is to produce a frequency variation ($\omega_{out}(t)$) in response to an applied control voltage ($V_{ctrl}$ in Fig. 2.8). Assuming this response to be linear, its transfer characteristics can be illustrated as shown in Fig. 2.11.

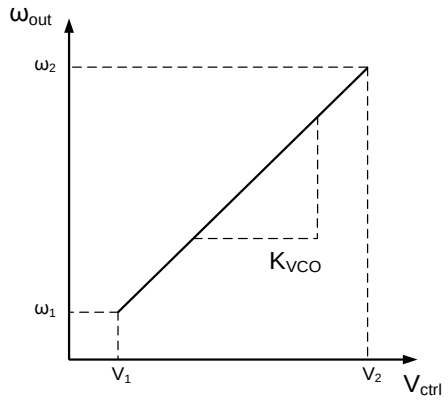



**Fig. 2.11:** Ideal transfer characteristics of a VCO

The slope of this graph ($K_{VCO}$) quantifies the gain of the VCO i.e. the frequency

change per volt, which from Fig. 2.11 is defined as:

$$K_{VCO} = \frac{\omega_2 - \omega_1}{V_2 - V_1} \tag{2.13}$$

Using this, the output of the VCO is defined as:

$$\omega_{vco}(t) = \omega_a + K_{VCO}\ V_{ctrl}(t) \tag{2.14}$$

where $\omega_a$ is the frequency the VCO oscillates at when no control voltage is present i.e. when $V_{ctrl} = 0$V.

As will be shown in section 3.4.3, $K_{VCO}$ is non-linear in practice. If however for the purposes of deriving the VCO transfer characteristics we assume $K_{VCO}$ to be linear, then the VCO can be viewed as a linear block. Since the output of the VCO from (2.14) does not explicitly depend on time, the VCO is also inherently time-invariant.

Therefore, under the assumption of a linear $K_{VCO}$, the VCO can be viewed as an LTI block with transfer function defined (see Appendix A.2 for derivation) as:

$$H_{VCO}(s) = \frac{K_{VCO}}{s} \tag{2.15}$$

From (2.15) it is immediately obvious that the VCO exhibits infinite DC gain, hence behaving as an ideal integrator with one pole occurring at 0 rads/s.

### 2.4.4 Feedback Divider

The Feedback Divider is inherently linear and time-invariant with transfer function simply defined as:

$$H_{FB}(s) = \frac{1}{N} \tag{2.16}$$

### 2.4.5 Overall Transfer Characteristics

As noted in section 2.1, the PLL is a negative feedback system which, under the previously described assumptions, can be viewed as an LTI system. The graphical illustration of such a system in terms of its individual transfer blocks is shown in Fig. 2.12. Following from this, the open-loop transfer characteristics of such a system are defined (see Appendix A.3 for derivation) as:

$$H_{ol}(s) = H_{PFD-CP}(s)\ H_{LF}(s)\ H_{VCO}(s)\ H_{FB}(s) \tag{2.17}$$

Substituting in (2.11), (2.12), (2.15) and (2.16) gives:

$$H_{ol}(s) = \frac{I_{cp}}{2\pi}\ F(s)\ \frac{K_{VCO}}{s}\ \frac{1}{N} \tag{2.18}$$

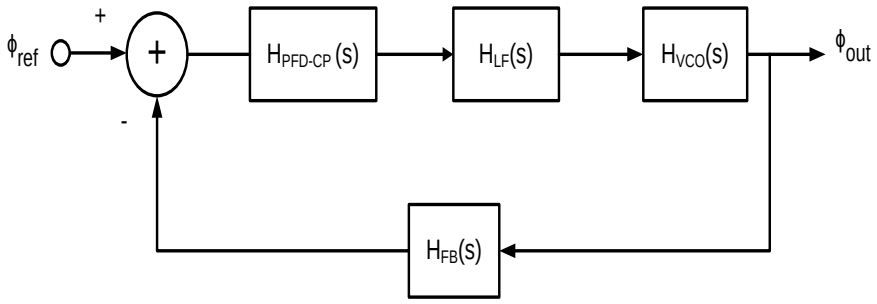



**Fig. 2.12:** LTI model of a PLL

Simplifying then gives:

$$H_{ol}(s) = \frac{K_{VCO} I_{cp} F(s)}{2\pi N s} \tag{2.19}$$

Similarly, the closed-loop transfer characteristics of such a system are defined (see Appendix A.4 for derivation) as:

$$H_{cl}(s) = \frac{H_{PFD-CP}(s)\ H_{LF}(s)\ H_{VCO}(s)}{1 + H_{ol}(s)} \tag{2.20}$$

Substituting in (2.11), (2.12), (2.15) and (2.19) gives:

$$H_{cl}(s) = \frac{(I_{cp}/2\pi)F(s)(KVCO/s)}{1 + K_{VCO} I_{cp} F(s)/2\pi N s} \tag{2.21}$$

Simplifying then gives:

$$H_{cl}(s) = \frac{K_{VCO} I_{cp} F(s)}{2\pi s + K_{VCO} I_{cp} F(s)/N} \tag{2.22}$$

Equations (2.19) and (2.22) are the two most fundamental equations of PLLs as together they describe the general behaviour of a PLL. As they are intuitive and easy to use they lend themselves very easily to practical PLL design where they equip the designer with all the tools necessary to assess and design for the primary criteria and parameters of a PLL. The open-loop transfer characteristics are given by (2.19) which, as will be shown in section 2.6 describe the open-loop response of a PLL through which its stability can be assessed. The closed-loop transfer characteristics of the loop are then given by (2.22) which, as will be shown in section 2.7 describe the closed-loop response of a PLL through which its loop bandwidth can be assessed.

### 2.4.6 Applicability of the LTI Model

One could argue over the exact usefulness of the LTI model used to describe the behaviour of a PLL, as it only does so under a strict set of operating conditions. Non-linear models do exist which describe PLL behaviour over a wider range of operating conditions [17, 18, 19]. However, as the resulting mathematics from these models is cumbersome, they do not lend themselves easily to practical PLL design. Given that a PLL will spend most of its time operating within the ranges required for linearity and time-invariance of the PFD, and that the assumption of a linear $K_{VCO}$ does provide a good general description of VCO behaviour, the LTI model does suffice in describing the general behaviour of a PLL. Furthermore, the LTI model is versatile and intuitive hence lending itself much more easily to practical PLL design. From it we can assess the stability of the PLL, describe its loop bandwidth and perform an insightful analysis into the noise characteristics of the loop (see section 2.8.2). It is for these reasons that the LTI model has become the de-facto model used to describe general PLL behaviour and as such, it is the sole model used to describe general PLL behaviour in this thesis.

## 2.5 PLL Type and Order

With the PLL architecture described and quantitatively defined, it is informative at this stage to define the type and order of a PLL.

### 2.5.1 Type

The type of a PLL is a term borrowed from control theory and refers to the number of integrators within the loop. We know from (2.15) that the VCO contributes one integrator to the loop and so all PLLs will be at least type 1. As shown in section 2.2.2, the tri-state behaviour of a PFD enables the LF to exhibit (ideally) infinite DC gain (irrespective of LF architecture). This contributes a second integrator to the loop thereby raising its type to 2. As this second integrator leads to (ideally) infinite pull-in range, it is desirable to have it, and so high performance PLLs are generally type 2. Although type 3 PLLs do exist, they are much less common with type 4 PLLs being an extreme rarity. The focus of this thesis is on type 2 PLLs.

### 2.5.2 Order

The order of a PLL refers to the number of poles within the loop,[2] i.e. the order of the denominator polynomial (characteristic polynomial) of its closed-loop (or open-loop)

[2]It is informative to note that, as each integrator contributes a pole to the PLL, the order of a PLL can never be less than the type.

transfer function. We know from (2.15) that the VCO contributes one pole to the loop and so all PLLs will be at least first-order. As shown in section 2.2.2, the tri-state behaviour of a PFD forces the LF to behave as an integrator thereby contributing a second pole to the loop and raising its order to 2. Therefore, for reasons previously discussed, all high performance PLLs are at least second-order. For reasons discussed in section 2.6.4, the focus of this report is on third-order PLLs.

## 2.6 Stability

Stability is the most important design criterion for a PLL and is largely determined by the LF. Therefore, in order to design the LF, stability must be accurately defined and the criteria for controlling it fully understood. Following this, an informed decision on the optimum LF architecture can be made, where its resulting transfer function can be inserted into the open and closed-loop PLL transfer characteristics (defined in section 2.4.5) to completely determine the general behaviour of the PLL.

### 2.6.1 Stability Criteria

In (2.20) the closed-loop transfer characteristic of a PLL was to exhibit the following relationship:

$$H_{cl}(s) \propto \frac{1}{1 + H_{ol}(s)} \tag{2.23}$$

Therefore if $H_{ol}(s)$ equals $-1$, the closed-loop response goes to infinity resulting in an unbounded output and rendering the system as unstable. As such, we can define a system as being unstable if its open-loop response $H_{ol}(s = j\omega)$, adheres to the following:

$$|H_{ol}(j\omega_1)| = 1 \tag{2.24}$$

$$\angle H_{ol}(j\omega_1) = -\pi \tag{2.25}$$

If (2.24) and (2.25) are satisfied then any components at $\omega_1$ (most commonly noise) regenerate themselves around the loop, thus leading to an unbounded output or an unstable PLL.

### 2.6.2 Bode Plots

The stability of a system under certain constraints can be examined using a Bode plot. This plots the log of the magnitude and phase response of a system across a wide range

of frequencies according to the frequencies of its poles and zeros. The rules for creating Bode plots are as follows:

- The slope of the magnitude response changes by +20dB/dec (decade) for each zero frequency and -20dB/dec for each pole frequency.
- For a pole/zero frequency of $\omega_1$, the phase response begins to fall/rise at a frequency of approximately 0.1 $\omega_1$, reaching at $\omega_1$, 45° below/above its phase at $\omega < 0.1\ \omega_1$, and approaching 90° below/above that initial phase at approximately 10 $\omega_1$.

The Bode plot for a 2nd-order system with no zeros is illustrated in Fig. 2.13.

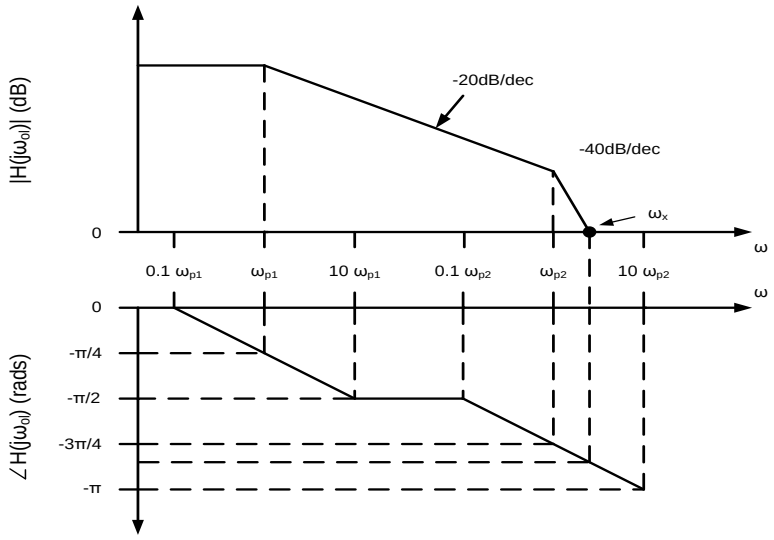



**Fig. 2.13:** Bode plot of the open-loop response of a second-order system

As stated, a Bode plot can be used to assess the stability of a system under certain constraints. These are the following:

- The magnitude response of the system must only cross the 0dB point at one frequency.
- The system must be open-loop stable i.e. all open-loop poles must occur on the left hand side of the $s$-plane.

Since the vast majority of PLLs meet these constraints, Bode plots are widely used to assess if a PLL is stable or unstable. In addition, Bode plots can give information on exactly how stable a PLL is, in other words how close its open-loop response is to satisfying (2.24) and (2.25). This can be achieved using the parameter of phase margin ($PM$), defined as follows:

$$PM = 180^\circ + \angle H_{ol}(j\omega_x) \tag{2.26}$$

where $\omega_x$ in (2.26) represents the gain crossover frequency i.e. the frequency for which $20 \cdot \log(|H_{ol}(j\omega)|) = 0\text{dB}$, shown in Fig. 2.13. Following from this, the phase response at the gain crossover frequency is represented by $\angle H_{ol}(j\omega_x)$.

As can be seen from (2.26), a system is unstable if $PM \leq 0^\circ$ and stable if $PM > 0^\circ$, becoming more stable as $PM$ grows. The effects of large and small $PM$ on a system [3] are shown in Figs. 2.14 to 2.19.

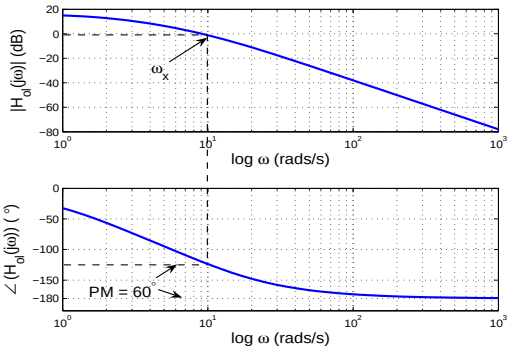



**Fig. 2.14:** $H_{ol}$ for $PM = 60^\circ$

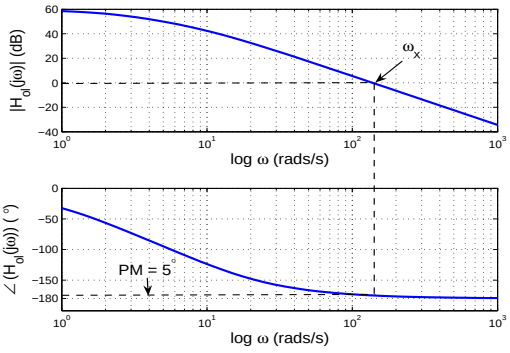



**Fig. 2.15:** $H_{ol}$ for $PM = 5^\circ$

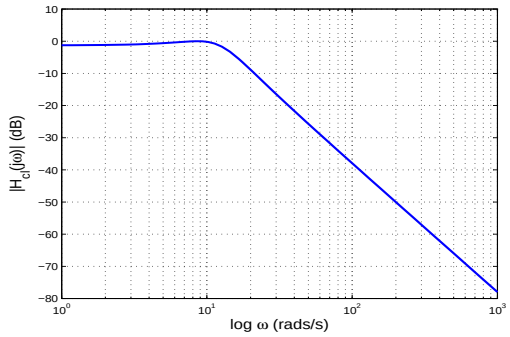



**Fig. 2.16:** $H_{cl}$ for $PM = 60^\circ$

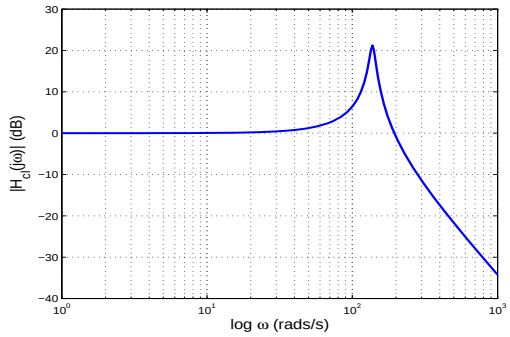



**Fig. 2.17:** $H_{cl}$ for $PM = 5^\circ$

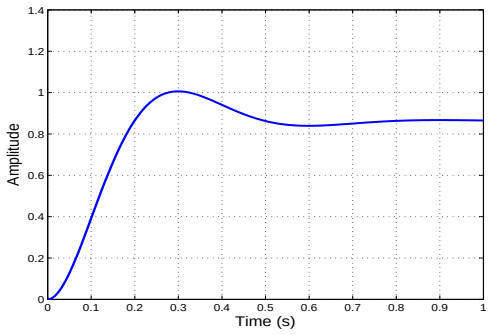



**Fig. 2.18:** Step response for $PM = 60^\circ$

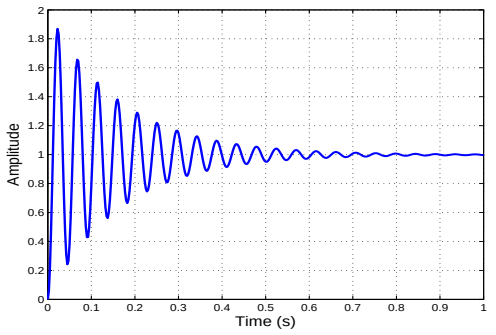



**Fig. 2.19:** Step response for $PM = 5^\circ$

[3] The transfer function for the applied system is H(s) = K/s(s + 2)(s + 10) and so contains no zeros and three ploes at s = 0, s = -2 and s = -10. $K$ is then varied to get the required $PM$.

In Figs. 2.14 and 2.15 the open-loop response of the system is plotted for $PM = 60°$ and $PM = 5°$ respectively. The corresponding closed-loop responses for both $PM$s are then plotted in Figs. 2.16 and 2.17 respectively, which show a dramatic increase in peaking of the closed-loop response as $PM$ decreases. The effect of this in the time domain is then shown in Figs. 2.18 and 2.19 which plots the step responses for $PM = 60°$ and $PM = 5°$ respectively. From these the step response can be seen to become increasingly oscillatory (and hence increasingly unstable) as $PM$ decreases.

### 2.6.3 Beware False Stability Criteria

Fig. 2.19 shows that as a system becomes less stable its time domain response becomes increasingly oscillatory. This has led many literatures to incorrectly state the Barkhausen criteria for oscillation as a general criteria for stability. Barkhausen developed these criteria as the necessary (but not sufficient) conditions for oscillation and never intended them as criteria for stability. It was later authors that mistakenly made this assumption which unfortunately has remained in some texts. Barkhausen's criteria for oscillation can only be applied to a Bode plot to assess for stability if, in addition to the constraints given in section 2.6.2, both the magnitude and phase response of the system are monotonically decreasing. As such, it does not suffice as a general criteria for stability and moreover does not apply to PLLs since their phase response is never monotonically decreasing (shown in section 2.6.4). The general criteria for stability is given by the Nyquist stability criteria from which (2.24) and (2.25) are derived.

### 2.6.4 LF Architectures

LFs can be passive or active, with the latter consuming more power and so being less commonly found in practice. As such, this thesis focuses solely on passive LFs. The most intuitive realisation of a passive LF is that of a single capacitor ($C_1$) placed in parallel to the CP output, as shown in Fig. 2.20.

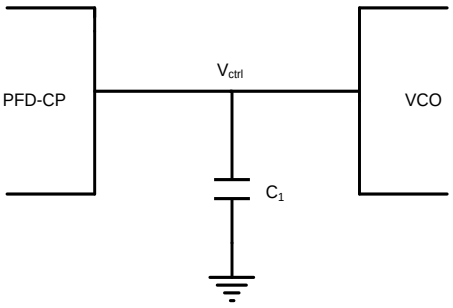



**Fig. 2.20:** First-order passive lag LF

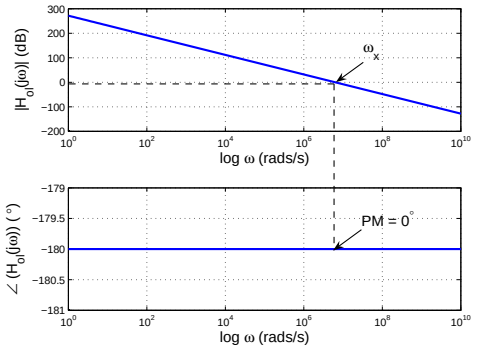



**Fig. 2.21:** Open-loop response

The capacitor ($C_1$) contributes a pole ($p_1$) at 0 rads/s and so given that no zero occurs, the filter is termed a first-order passive lag filter. Placing such a filter in a PLL realises a two pole system (i.e. a second-order PLL) since the VCO already contributes one pole, with both poles occurring at 0 rads/s to realise a type 2 PLL. As no zero occurs this means that $\angle H(j\omega) = -\pi$ when $|H(j\omega)| = 1$. In other words, $\angle H(j\omega) = -\pi$ at the gain crossover frequency or more succinctly stated, $\angle H(j\omega_x) = -\pi$. In accordance with (2.24) and (2.25), this architecture is therefore unstable which can be easily seen in the open-loop response of Fig. 2.21 where $PM = 0°$. Phase margin can be increased by adding a zero ($z_1$) to induce a phase shift such that $\angle H(j\omega_x) \neq -\pi$ rads. The resulting $PM$ is thus defined as:

$$PM = 180° + tan^{-1}\left(\frac{\omega_x}{\omega_{z_1}}\right) \tag{2.27}$$

where $\omega_{z_1}$ represents the frequency which $z_1$ occurs at.

The introduction of $z_1$ is achieved in practice by placing a resistor ($R_1$) in series with $C_1$, as shown in Fig. 2.22.[4]

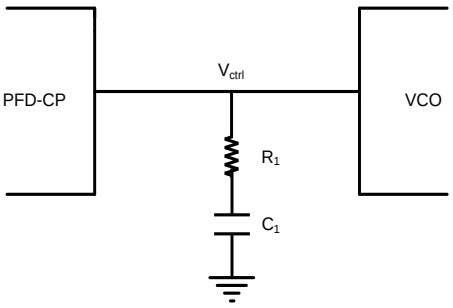



**Fig. 2.22:** First-order passive lag-lead LF

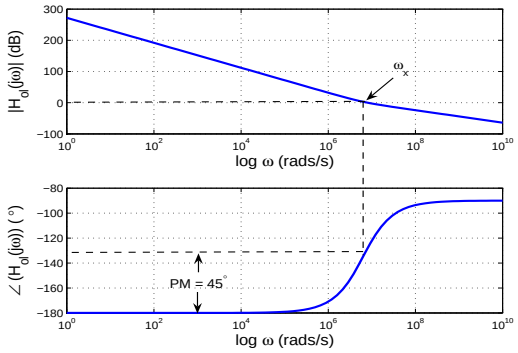



**Fig. 2.23:** Open-loop response

As $z_1$ induces a phase shift, the resulting LF is termed a first-order passive lag-lead filter. Analysis of its transfer function shows $z_1$ to occur at a frequency defined by:

$$\omega_{z_1} = \frac{1}{R_1 C_1} \tag{2.28}$$

Component values for $R_1$ and $C_1$ must be carefully chosen to ensure $\omega_{z_1}$ occurs at a frequency which ensures $\angle H(j\omega_x) \neq -\pi$ whilst achieving low PLL settling times. Setting $s_{z_1}$ at too low a frequency ($\ll K$) should be avoided as the resulting large $PM$s ($> 60°$) will increase settling times. As will be seen in section 2.7.2, $\omega_x$ equals loop bandwidth ($K$) and so a good starting point is to set $\omega_{z_1} = K$, which from (2.27) achieves a PM of 45°. This can be seen in the open-loop response of Fig. 2.23.

[4] $R_1$ can be placed at either side of $C_1$ with no change to the LF transfer characteristics.

The resistor ($R_1$) will however induce voltage spikes of magnitude $I_{cp}R_1$ on the VCO control line leading to spurious frequencies (spurs) at the VCO output. These can be dampened down by placing a second capacitor ($C_2$) in parallel to $C_1$, shown in Fig. 2.24.

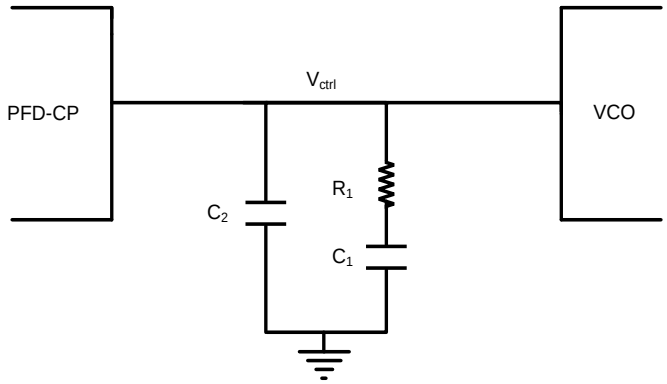



**Fig. 2.24:** Second-order passive lag-lead LF

The capacitor ($C_2$) adds a second pole ($p_2$) to the LF thereby rendering it as second-order with transfer function defined by (see Appendix A.5 for derivation):

$$H_{LF}(s) = \frac{(C_1R_1)s + 1}{(C_2C_1R_1)s^2 + (C_1 + C_2)s} \tag{2.29}$$

The DC gain of this LF ($H_{LF}(0)$) goes to infinity in agreement with section 2.2.2. Placing such a LF in a PLL thus realises a third-order type 2 system whose open and closed-loop transfer characteristics are found through substitution of (2.29) for $F(s)$ into (2.19) and (2.22) respectively. Analysis of the resulting transfer functions (or (2.29)) reveals $z_1$ to occur at the frequency defined in (2.28) and $p_2$ to occur at a frequency defined by:

$$\omega_{p_2} = \frac{C_1 + C_2}{C_1C_2R_1} \tag{2.30}$$

This additional pole then reduces the $PM$ as follows:

$$PM = 180^\circ + tan^{-1}\left(\frac{\omega_x}{\omega_{z_1}}\right) - tan^{-1}\left(\frac{\omega_x}{\omega_{p_2}}\right) \tag{2.31}$$

The components of the LF must therefore be chosen carefully so as to place $p_2$ and $z_1$ at frequencies which result in a $PM$ large enough to ensure reliable stability, whilst at the same time achieving low PLL settling times. As such, the required $PM$ completely determines the positions of $p_2$ and $z_1$ by virtue of the following equations:

$$\omega_{p_2} = k\ \omega_x \tag{2.32}$$

$$\omega_{z_1} = \frac{\omega_x}{k} \tag{2.33}$$

where $k$ is defined as:

$$k = \sqrt{\frac{1 + sin(PM)}{1 - sin(PM)}} \tag{2.34}$$

for $PM < 90°$.

In [20] it was shown that, for a third-order type 2 PLL with passive lag-lead LF, minimum settling times occur for $PM$s of $\approx 50°$, which also achieves robust stability. Equations (2.32) and (2.33) show that to achieve $PM = 50°$, $p_2$ and $z_1$ must occur at frequencies of 2.75 and 0.36 times $\omega_x$ respectively. Given that $\omega_x$ can be approximated by loop bandwidth (see section 2.7.2), this corresponds to placing $p_2$ and $z_1$ at approximately 2.75 and 0.36 times K respectively.

It should be noted that the required capacitances to achieved the desired $PM$ are typically large, consuming significant silicon area if placed on-chip (discussed in further detail in section 4.4) and are thus often placed off-chip. However, where small capacitances permit on-chip implementation, $C_2$ should always be placed at the output of the PFD as shown in Fig. 2.24. Although placing $C_2$ at the input to the VCO causes no change in LF transfer characteristics (see section 2.4.2), it will increase its effective capacitance as follows:

$$C_2(effective) = C_2 + C_{VCO_{input}} \tag{2.35}$$

where the input capacitance of the VCO is represented by $C_{VCO_{input}}$.

Achieving $PM = 50°$ in practice results in $C_2 < C_1$ (see (2.43)) and so a small $C_2$ placed at the input to the VCO could have its effective capacitance significantly increased by $C_{VCO_{input}}$. This is extremely concerning as it forces $p_2$ to occur at a frequency less than designed for in (2.30) hence reducing the $PM$. Therefore to avoid this, for on-chip LF implementation $C_1$ should always be placed at the input to the VCO (as seen in Fig. 2.24) whose large capacitance ($>> C_{VCO_{input}}$) will not be affected by $C_{VCO_{input}}$, hence maintaining the desired $PM$.

To graphically show the effect of pole/zero positioning on $PM$, Fig. 2.25 plots the open-loop transfer characteristics for a third-order, type 2 PLL with passive lag-lead LF for various pole/zero positions, where $K = 6.3$ x $10^6$ rads/s ($\approx 1$ MHz)). In this plot the pole/zero positions are varied by varying the value of $k$, as per (2.32). As $k$ grows, so does the distance between $p_2$ and $z_1$, forcing $p_2$ to become increasingly less dominant over $z_1$. This reduces the attenuation of the positive phase shift due to $z_1$, hence giving rise to larger $PM$s. As $k$ reduces so does the $PM$, reaching 0° for $k = 1$ where $\omega_{z_1} = \omega_{p_2}$. For

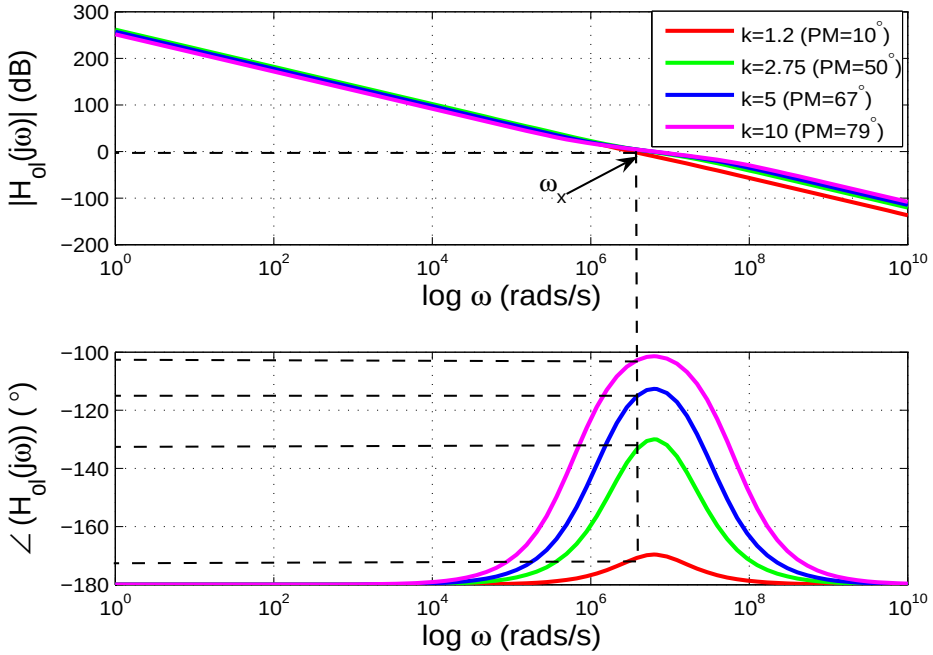



**Fig. 2.25:** Open-loop response of a third-order type 2 PLL with passive lag-lead LF, for various values of $k$

this value of $k$, $p_2$ lies on top of $z_1$ thereby completely cancelling it and in effect, bringing us back to the unstable first-order lag LF of Figs. 2.20 and 2.21.

### 2.6.5 Higher-Order LFs

Due to their simplicity, reliable stability and capability to suppress voltage spikes on the VCO control line, the final PLL of this thesis will employ a second-order passive lag-lead LF. However, it should be noted that in theory the LF can be any order with each additional order contributing another pole, hence compromising stability. For example, further attenuation of voltage spikes occurring on the VCO control line can be achieved with the addition of an RC filter onto the end of a second-order LF. The additional pole realises a third-order LF which, when placed in a PLL, realises a fourth-order type 2 system. Although this type of LF has found use in many industrial applications [21], [22], with a fourth-order LF being shown in [23], only second-order LFs will be discussed in this thesis.

## 2.7 Loop Bandwidth

Loop bandwidth is the most important design parameter of a PLL. It is indeed one of the two central themes of this thesis which up to this point has only been briefly introduced.

### 2.7.1 Loop Bandwidth for Second-Order PLLs

Under the assumptions defined in section 2.4, the generalised closed-loop transfer function of a second-order, type 2 PLL with passive lag-lead LF is defined as:

$$H(s) = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.36}$$

where dampening factor and natural frequency of the system are represented as $\zeta$ and $\omega_n$ respectively.[5] The closed-loop response of such a system is plotted in Fig. 2.26 for various values of $\zeta$. Specifically Fig. 2.26 plots the closed-loop response of the concerned system, normalised to its dc gain ($H(0) = N$) since, as will be shown, this enables loop bandwidth to be precisely defined.

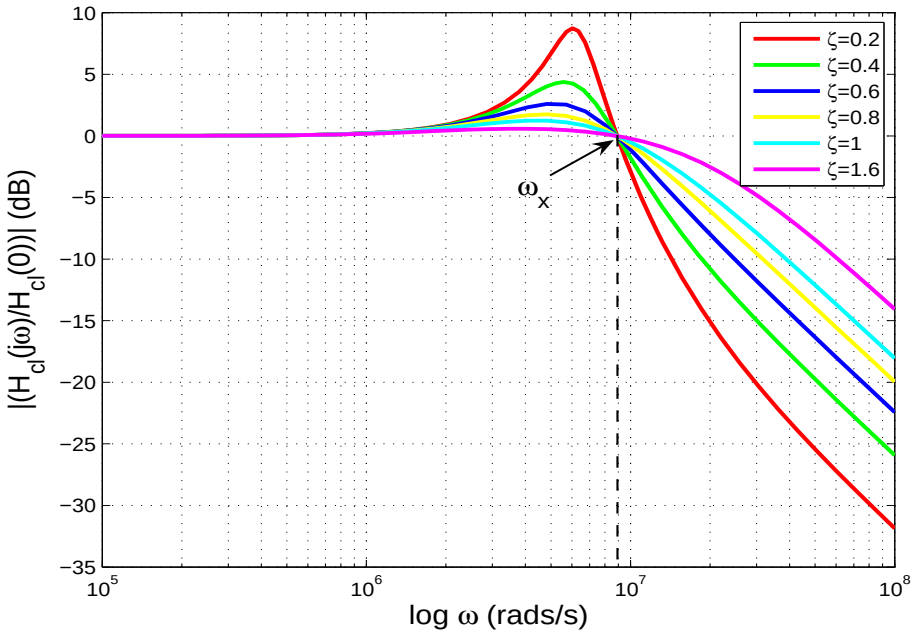



**Fig. 2.26:** Closed-loop response of a second-order, type 2 PLL with passive lag-lead LF, for various values of $\zeta$

Immediately obvious from Fig. 2.26 is the low-pass filtering characteristic displayed. This behaviour is common to all PLLs and comes about because the PLL has limited bandwidth. Any frequency error at the input to the PLL within this bandwidth gets tracked by the loop and passes to the output. Those outside it do not get tracked and thus become attenuated at the output. The corner frequency of this low-pass characteristic is described by the loop bandwidth ($K$). Through normalising to its dc gain then, we can see this corner frequency to be described by the gain crossover frequency ($\omega_x$) (i.e. the frequency where $|H(s)/H(0)| = 0\ dB$) and so can percisely define loop bandwidth ($K$) as:

[5] Equation (2.36) can be got in terms of the various PLL components through substitution of the first-order lag-lead LF transfer function for $F(s)$ in (2.22).

$$K = \omega_x \tag{2.37}$$

thereby leading to the various deductions regarding pole/zero placements made in section 2.6.4.

As can be seen in Fig. 2.26, $\omega_x$ occurs at the same point irrespective of the value of $\zeta$, indicating loop bandwidth to be independent on dampening for the concerned PLL. This behaviour is common only to second-order PLLs where it can be precisely defined (see Appendix A.6 for derivation) as:

$$K = \sqrt{2}\ \omega_n \tag{2.38}$$

Noting that the closed-loop transfer characteristics are defined under the assumption of (2.2), Fig. 2.26 can be approximated as the closed-loop response of one loop iteration of the PLL. Using this approximation it is reasonable to state that the PLL is not able to track any frequency variations outside of $K$ within one loop iteration, leading to the following useful (though crude) approximation [8] for lock-in range:

$$\Delta\omega_L \approx K \tag{2.39}$$

Plotting the transient response of the input phase error for small phase errors (as done in [7]) shows the error to converge to 0 within at most one damped oscillation (for $\zeta < 1$). As the frequency of this oscillation is approximated by $\omega_n$, it is therefore reasonable to approximate lock-in time as:

$$T_L \approx \frac{2\pi}{\omega_n} = \frac{2\sqrt{2}\pi}{K} \tag{2.40}$$

Following from (2.40), $K$ can also be loosely interpreted as the update rate of the PLL or put simply - the speed of the loop.

Equation (2.38) is very attractive as it provides a precise definition for $K$. Unfortunately, such a precise definition for loop bandwidth does not carry over to higher-order systems. This is because $\omega_n$ loses physical meaning for systems of order greater than 2 where loop bandwidth itself starts to exhibit a dependence on $\zeta$. Therefore, a more general definition for loop bandwidth applicable to all PLLs is required.

One interesting point to note about Fig. 2.26 is the gain peaking exhibited close to the corner frequency. This occurs due to the presence of the zero ($z_1$) (defined in section 2.6.4) which forces $|H(j\omega)|$ to rise with frequency. This rise is attenuated by the rolloff of the poles and so is reduced by moving $z_1$ closer to the poles through increasing $R_1$ or $C_1$ (i.e. by increasing $\zeta$). However, as $z_1$ can never be moved on top of the poles for any finite values of $R_1$ or $C_1$, peaking will always occur. Therefore, any PLL employing a LF

exhibiting a phase-leading action (i.e. containing a zero) will always experience peaking to some extent. This is however a small price to pay since (as shown in section 2.6.4) the zero is necessary to maintain stability of the PLL, where in general $n$ - 1 zeros are required for a type $n$ PLL to be stable [8].

### 2.7.2 General Loop Bandwidth Definition

In [8], loop gain is shown to be a good indicator of loop bandwidth for all PLLs. In its most general form loop gain ($G_K$) is defined to be:

$$G_K = K_{FB}\ K_{PFD-CP}\ K_{VCO}\ F_{p+i}(s)\ F_{hf}(0) \tag{2.41}$$

where gains of the feedback, PFD-CP and VCO blocks are represented by $K_{FB}$, $K_{PFD-CP}$ and $K_{VCO}$ respectively, with $F_{p+i}(s)$ representing the proportional and integral components of the LF and $F_{hf}(0)$, the high frequency LF components.

### 2.7.3 Loop Bandwidth for Third-Order PLLs

The closed-loop response of a third-order, type 2 PLL with passive lag-lead LF for various values of dampening,[6] designed for $K = 6.3 \text{ x } 10^6$ rads/s ($\approx$ 1 MHz), is plotted in Fig. 2.27.

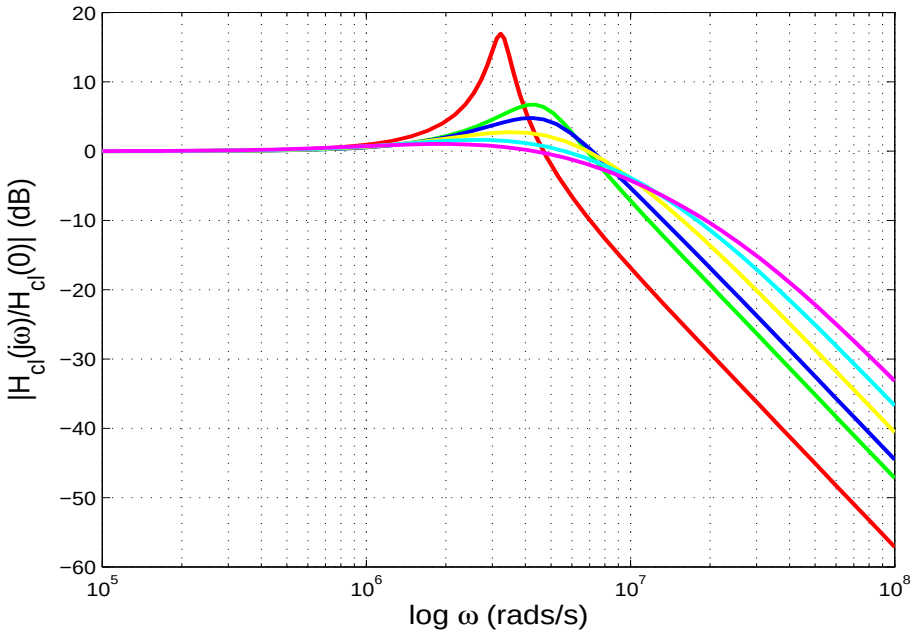



**Fig. 2.27:** Closed-loop response of a third-order, type 2 PLL with passive lag-lead LF, for various values of dampening

[6] As $\zeta$ does not directly follow over to third-order systems, it is approximated in this plot as $PM/100$. As shown in [24], this approximation holds for the concerned PLL where $35° \leq PM \geq 70°$.

Once again Fig. 2.27 plots the closed-loop response of the concerned system normalised to its dc gain ($H(0) = N$). This clearly shows the gain crossover not to always occur at the same frequency hence indicating loop bandwidth to be dependent on dampening for this PLL. Table 2.2 shows the resulting gain crossover frequencies ($\omega_x$) for various dampening factors, revealing loop gain ($G_K$) to approximate it (and hence loop bandwidth) reasonably well for mid to low values of dampening, with the approximation loosing accuracy as dampening increases.

| Dampening | $\omega_x$ (rads/s) | $\omega_x/G_K$ |
|---|---|---|
| 0.1 | 4.8 x $10^6$ | 0.76 |
| 0.29 | 6.75 x $10^6$ | 1.07 |
| 0.37 | 6.85 x $10^6$ | 1.09 |
| 0.5 | 6.75 x $10^6$ | 1.07 |
| 0.62 | 5.4 x $10^6$ | 0.9 |
| 0.71 | 4 x $10^6$ | 0.63 |

**Table 2.3:** Accuracy of loop bandwidth approximation for different dampening values

For reasons discussed in sections 2.2.2, 2.3 and 2.6.4, this thesis focuses solely on third-order type 2 PLLs whose optimum phase margins ($PM$) were shown in [20] to be 50°. Given that dampening for a third-order system, where $35° \leq PM \geq 70°$, can be approximated as $PM/100$ [24], this optimum $PM$ corresponds to a dampening factor of $\approx 0.5$. Since Table 2.3 shows loop gain ($G_K$) to approximate loop bandwidth ($K$) reasonably well for this dampening factor, its use as an approximation to $K$ is thus justified for the concerned PLL.

For a third-order, type 2 PLL with passive lag-lead LF, $G_K$ in (2.41) simplifies to:

$$G_K = \frac{I_{cp} K_{VCO} R_1}{2\pi N} \frac{C_1/C_2}{C_1/C_2 + 1} \tag{2.42}$$

where the factor $C_1/C_2$ is completely determined by the required $PM$ (see Appendix A.7 for derivation) as follows:

$$\frac{C_1}{C_2} = \frac{2sin(PM)}{1 - sin(PM)} \tag{2.43}$$

for $PM < 90°$.

We know from section 2.6.4 that 50° is the optimum $PM$ for the concerned PLL, which from (2.43) yields a $C_1/C_2$ factor of $\approx 6.5$. Using this, (2.42), and hence loop bandwidth ($K$) for the concerned PLL can be approximated as:[7]

$$K \approx \frac{I_{cp} K_{VCO} R_1}{2\pi N} \tag{2.44}$$

[7]It should be noted that (2.44) equals the precise definition for loop bandwidth of a second-order, type 2 PLL with passive lag-lead LF defined in (2.38), when $\zeta = 1/\sqrt{2}$.

### 2.7.4 Issues with Loop Bandwidth Addressed in this Thesis

As shown by (2.41), loop bandwidth is dependent on various parameters. Since these parameters exhibit the potential to vary from their nominal values in practice they give rise to loop bandwidth variation ($\Delta K$). This is extremely concerning in terms of overall PLL performance and in fact represents one of the main challenges faced by PLL designers today. The aspects of PLL performance affected by $\Delta K$ are as follows:

- *Stability*: Phase margin ($PM$) for second and third order PLLs was defined in (2.27) and (2.31) respectively. These showed $PM$ to be directly proportional to the gain crossover frequency ($\omega_x$) which, from section 2.7.2 can be approximated by $K$. Therefore if $K$ reduces from its nominal value, resulting $PM$s will be degraded hence comprising the stability of the PLL. As will be shown in section 2.8.3, stability is also compromised if $K$ increases from its nominal value to within $\pm\ \omega_{ref}/10$. As such, one of the major causes for concern over $\Delta K$ is that it degrades the stability of a PLL.

- *Acquisition ranges*: The concerns over $\Delta K$ increase when we recall the expressions for pull-in and lock-in ranges defined in (2.5) and (2.39) respectively. These showed both $\Delta\omega_P$ and $\Delta\omega_L$ to be directly proportional to $K$ and so any reductions in $K$ from its nominal value will reduce these ranges also. As $\Delta\omega_P$ is generally limited by the output frequency range of the VCO in practice, its reduction due to a decreasing $K$ is not of major practical concern. The same cannot be said for $\omega_L$ however since, as shown in (2.39) it is approximately equal to $K$ and so will be directly degraded.

- *Acquisition times*: Hand in hand with the reduction of pull-in and lock-in ranges comes an increase in pull-in and lock-in times. This can be seen from (2.40) which shows $T_L$ to be inversely proportional to $K$, with this inverse proportionality also exhibited by pull-in times [8]. Therefore yet another concern over $\Delta K$ is slower loop performance.

- *Noise*: Finally, as will be shown in section 2.8, the overall noise performance of a PLL is greatly influenced by loop bandwidth. Any variations in $K$ may therefore lead to increases in the noise from various sources within the loop. As a result, $\Delta K$ becomes also a major concern for PLLs operating in low noise applications.

Therefore, as loop bandwidth variation can affect stability, reduce lock-in and pull-in ranges, increase lock-in and pull-in times in addition to degrading the noise performance of a PLL, all efforts to reduce $\Delta K$ become completely justifiable. As such, there has been an increased number of publications dealing with this topic over recent years. These various efforts will be reviewed in chapter 5 which looks at the issue of $\Delta K$ in more detail before proposing a VCO architecture which significantly reduces it.

## 2.8 PLL Noise Performance

Next to stability, noise performance is the most important criterion for PLL design as all PLLs must exhibit minimal noise on their output signals. This however is especially true for a PLL operating in the frequency synthesizer of a wireless transceiver (see chapter 1), where the demanding noise specifications imposed by modern wireless standards force the designer to assess each individual circuit of the PLL in terms of the noise it generates. To make this task even more challenging, modern wireless transceivers often have to operate to extremely low power requirements. Therefore, to achieve low noise performance without relying on extra power, all noise sources of a PLL must be investigated and the various dependencies they exhibit within the loop, fully understood.

### 2.8.1 Phase Noise

The output of a PLL in its most basic form is a sinusoidal wave, described as:

$$V(t) = Asin(\omega t) \tag{2.45}$$

The phase of this output wave can be corrupted by noise. Hence a noisy output from a PLL can be described as:

$$V(t) = Asin(\omega t + \phi(t)) \tag{2.46}$$

The impact of this phase noise corruption is illustrated in both the time and frequency domains in Fig. 2.28.

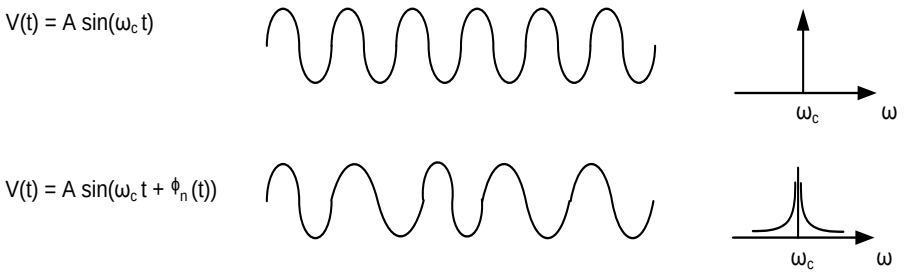



**Fig. 2.28:** Illustration of phase noise in the time and frequency domains

As shown in Fig. 2.28, when the phase is corrupted by noise, the output frequency spectrum exhibits 'skirts' around the carrier frequency ($\omega_c$). For a PLL operating in the frequency synthesizer of a wireless transceiver (see chapter 1), this can corrupt both the transmitted and received signals [25]. Due to the narrow channel spacings employed in modern wireless communications systems (*for example : GSM* standard employs channel

spacings of only 200kHz), these 'skirts' need to be sharply attenuated, leading to the demanding phase noise specifications imposed by modern wireless standards.

### 2.8.2 Noise Transfer Characteristics in a PLL

Noise behaviour in a PLL can be analysed by injecting noise sources at various points in the LTI model derived in section 2.4.5, as shown in Fig. 2.29.

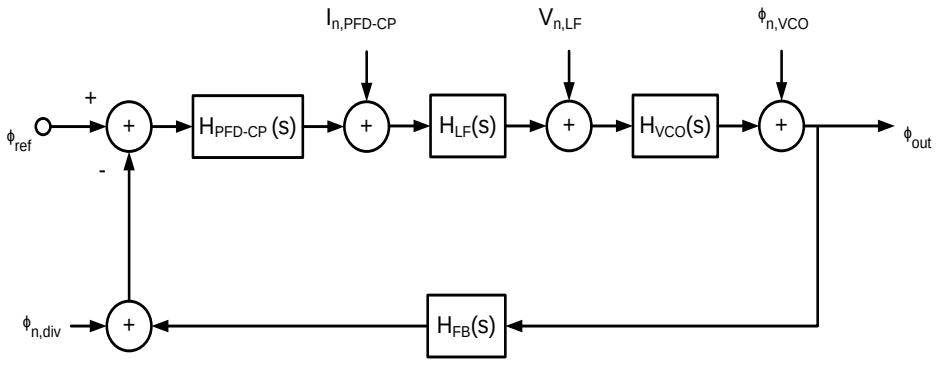



**Fig. 2.29:** LTI model of a PLL with injected noise sources

Each noise source represents noise occurring within the block directly preceding it. Under the assumptions defined in section 2.4, the transfer functions for each of these noise sources with respect to the output can be found and their corresponding transfer characteristics plotted. These are plotted for a second-order, type 2 PLL with passive lag-lead LF in Figs. 2.30 to 2.33, where $K = 6.3$ x $10^6$ rads/s ($\approx 1$ MHz).

From Figs. 2.30 and 2.31, it can be seen that noise from the feedback divider and PFD-CP share the same low-pass characteristic as the closed-loop response of such a system shown in Fig. 2.26.[8] Noise from the LF is shown in Fig. 2.32 to exhibit a band-pass characteristic where Fig. 2.33 shows noise from the VCO to exhibit a high-pass characteristic.

There are many practical causes of these noise sources. In the CP it could be due to thermal or flicker noise from the devices whereas in the LF it could be due to thermal noise from $R_1$. Thermal, flicker and inductor noise are prevalent in the VCO (shown in section 3.6) with thermal noise being a contributor in the feedback divider. In addition to all this, there exists common-mode noise (see section 2.8.3) which affects all noise sources within the loop equally. Therefore, to simplify matters, for the moment we will ignore flicker, inductor and common-mode noise such that the remaining noise sources can be assumed Gaussian and white. Under these assumptions, the power spectral

[8] Figs. 2.30 and 2.31 are normalised to their respective dc gains to maintain consistency with Fig. 2.26, clearly illustrate where $K$ occurs and allow a more direct comparison with VCO noise shown in Fig. 2.33.

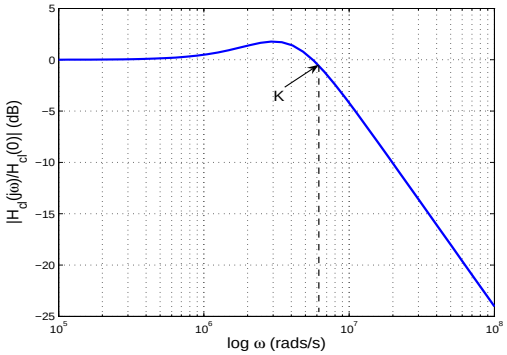



**Fig. 2.30:** Response of PFD-CP noise

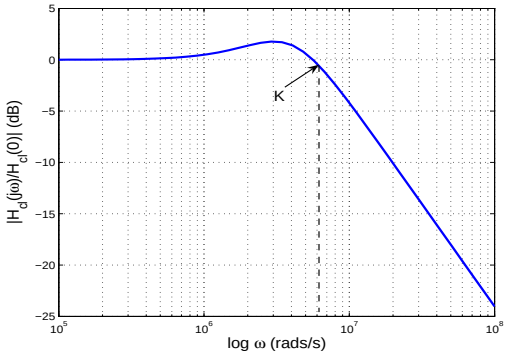



**Fig. 2.31:** Response of divider noise

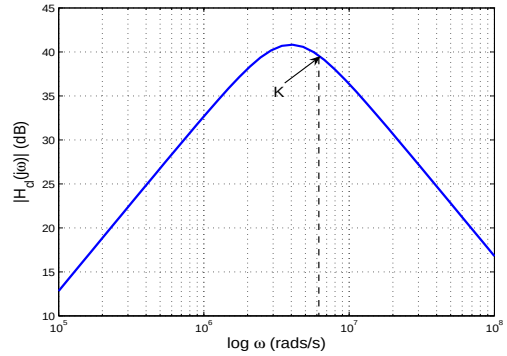



**Fig. 2.32:** Response of LF noise

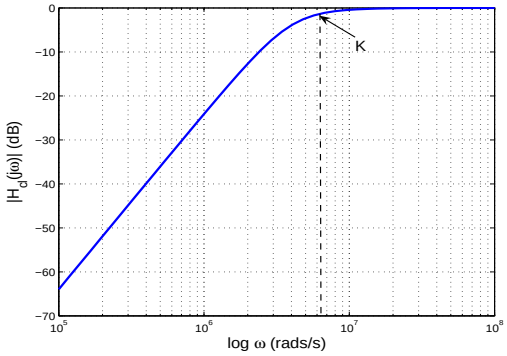



**Fig. 2.33:** Response of VCO noise

densities (PSD) for each of the noise sources can be easily obtained. Given that we are assuming the PLL to behave as an LTI system, each PSD is shaped by its corresponding transfer function to yield the output PSD due to each specific noise source. Integrating then over frequency yields the total output power from each noise source (i.e. the output phase noise due to each block). This analysis was performed in [26] which showed the following useful relationships:

$$\phi^2_{n,PFD-CP} \propto \frac{K}{K^2_{PFD-CP}} \tag{2.47}$$

$$\phi^2_{n,div} \propto K \tag{2.48}$$

$$\phi^2_{n,LF} \propto \frac{K^2_{VCO}}{K} \tag{2.49}$$

$$\phi^2_{n,VCO} \propto \frac{1}{K} \tag{2.50}$$

where output phase noise due to the PFD-CP, feedback divider, LF and VCO are represented by $\phi^2_{n,PFD-CP}$, $\phi^2_{n,div}$, $\phi^2_{n,LF}$, and $\phi^2_{n,VCO}$ respectively.

From (2.47) and (2.48), output phase noise from the PFD-CP and feedback divider are seen to be directly proportional to loop bandwidth ($K$). This is in agreement with the low-pass filter transfer characteristic exhibited by these sources in Fig. 2.30 and Fig. 2.31 respectively. Increasing loop bandwidth pushes out the corner frequency at which noise from these sources start to become attenuated, thereby increasing their respective noise contributions. Conversely, output phase noise from the VCO is shown in (2.50) to be inversely proportional to $K$. Again, this is in agreement with the high-pass filter transfer characteristic exhibited by this source in Fig. 2.33. Increasing loop bandwidth pushes out the corner frequency at which noise from the VCO starts to grow, thereby reducing its noise contribution.

### 2.8.3 Issues with Reducing Phase Noise Addressed in this Thesis

All the noise sources described in section 2.8.2 occur simultaneously in a PLL and so with the apparent conflict in loop bandwidth requirements described previously, it is reasonable to ask if all these sources can be simultaneously reduced. While all the sources cannot be simultaneously reduced, the most dominant ones often can. For example, the classical approach to reducing PLL phase noise is through increasing loop bandwidth ($K$) by increasing $K_{PFD-CP}$ whilst keeping $K_{VCO}$ constant (see (2.44)). As can be seen from (2.47), (2.49) and (2.50), this will reduce noise contributions from the PFD-CP, LF and VCO respectively (assuming it to be white and Gaussian) and so only becomes effective when such noise dominates. This is an especially attractive approach as it increases pull-in and lock-in ranges whilst decreasing pull-in and lock-in times. However, defining $K_{PFD-CP}$ as:

$$K_{PFD-CP} = \frac{I_{cp}}{2\pi} \tag{2.51}$$

we can see its increase to correspond to an increase in $I_{cp}$. This reveals the first major issue with this approach - it increases power consumption and so is unsuitable to low power applications.

Another issue arising with increasing loop bandwidth ($K$) is that it can compromise the stability of the loop. In section 2.4, it was shown that the closer $K$ comes to the input reference frequency ($\omega_{ref}$), the more time-varying the PLL becomes hence causing our LTI model to break down. Furthermore, the closer $K$ comes to $\omega_{ref}$ the greater the risk of the loop over-compensating for any input errors thereby rendering it unstable. It should be noted that this instability cannot be examined through pole zero analysis due to the deviation from LTI theory on which such analysis is based. It therefore represents more of a "large signal instability" which presents an upper limit for $K$. In practice the following upper limit for $K$ [9] has been shown to work reliably in practice:

$$K \leq \frac{\omega_{ref}}{10} \tag{2.52}$$

Another issue with increasing loop bandwidth is that it does not reduce noise contributions from the feedback divider (2.48), or that from a source outside of the loop - noise on the input reference signal. Since these noise sources exhibit the same low-pass filter transfer characteristic as the closed-loop response, their contributions cannot be decreased by increasing loop bandwidth. For frequency synthesizers however, noise on the input reference signal can often be neglected as the reference signal itself is generated by a quartz crystal oscillator with high spectral purity, and only passes through a digital prescaler prior to entering the loop. The same can be said for noise from the feedback divider which only becomes significant at high frequencies not practically encountered by a PLL. For PLLs not operating in a frequency synthesizer however, $K$ needs to be optimised as opposed to being simply increased.

Finally, increasing $K$ does not address the reduction of common-mode noise. Common-mode noise (also known as environmental noise) is defined as the noise which corrupts all (or a subset of) nodes in a system equally. Such noise on an integrated circuit (IC) is often generated by the high frequency switching of digital circuitry which can ac-couple onto nearby lines. All nodes common to these corrupted lines thus become equally affected hence experiencing a common-mode perturbation defined as common-mode noise. For modern low technology nodes where device dimensions decrease, the integration of digital devices increases. Hand in hand with this increase comes an increase in common-mode noise. Such high integration is typical to that of system-on-chip (SOC) designs onto which wireless transceivers are commonly embedded. Therefore, in order to meet the demanding noise specifications imposed by modern wireless standards, it is imperative that the PLLs in the frequency synthesizers of these transceivers be robust against common-mode noise.

Therefore, although the classical approach of increasing loop bandwidth through increasing $I_{cp}$ reduces contributions from some of the most dominant noise sources within a PLL, it does so at the cost of increased power consumption and does not address common-mode noise. In addition, it can compromise stability making this approach questionable, especially concerning low noise, low power PLLs operation on densely populated SOCs. Therefore, an alternative PLL architecture is presented in chapter 4 which dramatically reduces common-mode noise in addition to other noise soures, withtout the need for large increases in $I_{cp}$.

## 2.9 Summary

This chapter was written with four goals in mind. The first was to simply introduce the PLL and explain it basic operation. This was achieved in section 2.1.

The second goal was to justify the chosen PLL architecture on which the proceeding chapters will be based. Starting with section 2.2, we justified the choice for using a digital PLL (DPLL) which employed a PFD as its phase detector (PD). This then rendered the charge-pump PLL (CP-PLL) described in section 2.3. Due to its versatility and applicability to practical PLL design, the LTI model already existing for the analog PLL (APLL), was adapted to describe the general behaviour of the DPLL. This was introduced and justified in section 2.4. Reasons for employing a second-order passive lag-lead LF were then given in section 2.6, to render the overall PLL as third-order and type 2.

At this point we could focus on the third goal of this chapter - to introduce the primary design parameters and criteria for a PLL. Stability was introduced in section 2.6 as the most important design criterion for a PLL which must be robustly designed for. Loop bandwidth ($K$) was then introduced in section 2.7 as the most important design parameter for a PLL, which led to the introduction of low noise performance in section 2.8 as the second most important design criterion for a PLL.

The fourth and probably most important goal of this chapter was to recognise the limitations of the CP-PLL and introduce the most dominant issues arising with it. These were introduced throughout the chapter starting in section 2.3.1 where issues arising due to the inclusion of a CP (static phase error) were discussed. Issues with loop bandwidth (loop bandwidth variation) were then discussed in section 2.7.4 where those pertaining to the reduction of output phase noise in a CP-PLL were discussed in section 2.8.3.

Upon reading this chapter, the reader will be fully equipped with the basic principles of a PLL, be confident about the choice of PLL architecture made in this thesis, how to describe its general behaviour and design for its most important criteria and parameters. Most importantly the reader will be fully aware of the issues pertaining to the chosen architecture (CP-PLL) which will be addressed in the forthcoming chapters.

# CHAPTER 3

# VCO Overview

In section 2.1 the VCO was shown to be responsible for generating the output frequency of a PLL. As such, it is the primary RF block of a PLL, the next being the input stages of the feedback divider. Although its design architecture appears quite simple, the high frequency operation of a VCO often complicates its behaviour making it the most challenging block of a PLL to design in terms of meeting specifications. This is especially true for wireless applications where the demanding noise requirements imposed by modern wireless standards require very careful VCO design and in-depth knowledge of its operating principles and noise mechanisms. As such, there has been a large number of publications on various aspects of VCO design in recent years which, in addition to the various textbooks on the subject, have made VCO design a very specialised field.

It is for the above reasons, coupled with the fact that the VCO is strongly influenced by both central themes of this thesis, that an entire chapter is devoted to explaining its basic operating and design principles, high frequency behaviour and the various issues pertaining to achieving low phase noise VCO operation.

## 3.1 Basic Architectures

The exact role of a VCO was stated in section 2.4.3 to produce a frequency variation in response to an applied control voltage. Therefore when choosing the basic architecture with which to implement this function, the decision simplifies to the choice of waveform oscillators or resonant oscillators. Waveform oscillators are realised as a ring oscillator which simply consist of a cascade of inverting amplifiers whose basic implementation is shown in Fig. 3.1.

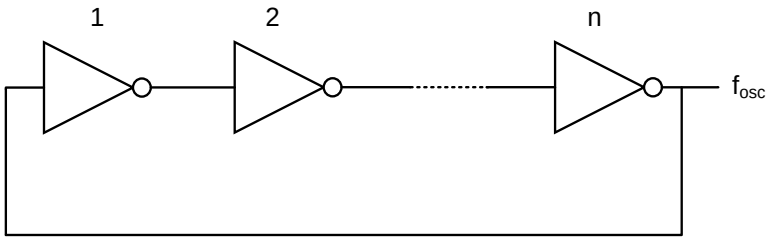



**Fig. 3.1:** Basic $n$-stage ring oscillator

In Fig. 3.1 an $n$-stage ring oscillator is depicted with each inverting amplifier comprising one stage. For single ended topologies there must always exist an odd number of stages[1] to avoid the circuit latching up, with three or five stages being commonly found in practice. The propagation delay from one stage to the next, and the total number of stages thus determines the frequency of oscillation ($f_{osc}$).

Resonant oscillators on the other hand are realised as LC-tank oscillators which simply consist of a series combination of an inductor and capacitor (operating principles will be detailed later).

Both oscillator types are quite different and as such exhibit various performance advantages and disadvantages over each other, which are summarised in Table 3.1.

| Oscillator type | Waveform oscillator | Resonant oscillator |
|---|---|---|
| Architecture | Ring | LC-tank |
| Power | Low | High |
| Area | Small | Large |
| Tuning range [a] | Large | Small |
| Phase noise performance | Poor | Excellent |

[a] The tuning range represents the frequency range covered by the VCO.

**Table 3.1:** Performance comparison between ring and LC-tank oscillators

Clearly evident from Table 3.1 is that in terms of power, area and tuning range, a ring oscillator is far more advantageous than an LC-tank oscillator. In fact the only disadvantage of a ring oscillator is its poor phase noise performance. However, due to the priority given to low noise performance for modern wireless applications (see chapter 1), this disadvantage proves to be the downfall of ring oscillators for such applications.

[1] Differential ring oscillators can be realised with an even number of stages by configuring appropriate stages such that they do not invert.

Although power and area hungry with a small tuning range, it is the superior phase noise performance of LC-tank oscillators which make them the optimum VCO architecture for wireless applications. Given that this thesis primarily focuses on the design of PLLs for wireless applications, LC-tank oscillators will be solely employed and hence discussed.

## 3.2 LC-Tank Basics

The basic operating principles of an LC-tank oscillator stem from the universal concept of a system continually seeking to exist in its lowest energy state. This can be seen with reference to the basic LC-tank circuit of Fig. 3.2.

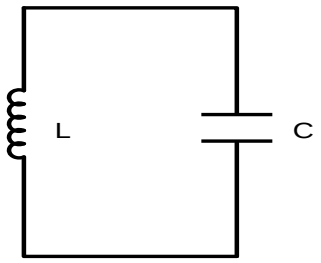



**Fig. 3.2:** Basic LC-tank

Suppose capacitor ($C$) in Fig. 3.2 is initially charged up to a voltage +V at time t = $t_1$. More specifically stated, suppose the top plate of $C$ is charged up to a voltage +V greater than the bottom plate at t = $t_1$. This is a high energy state which the system seeks to relieve by discharging the top plate of $C$ until its voltage equals that of the bottom plate, in other words until both plates hold the same amount of charge. If the inductor ($L$) were not present, this discharge would occur through the wires connecting the two plates after which the circuit would exist in its lowest energy state causing no further behaviour in the absence of external stimulation.[2] However as $L$ is present, $C$ discharges through the inductor hence generating a magnetic field around it. This magnetic field generates a voltage across the inductor which opposes the direction of current flow through it resulting in an increase in discharge time for $C$. When $C$ has discharged such that its voltage is the same on both plates, the magnetic field around $L$ now prevents the circuit from existing in its lowest energy state and so starts to collapse. This induces a voltage across the inductor such that the bottom plate of $C$ now charges up (this time to -V), thereby once again realising a high energy state. As before, the circuit seeks to relieve this high energy state by discharging $C$ through $L$ hence generating a magnetic field around $L$ whose collapse will charge up the top plate of $C$ to +V again and so forth. Assuming this circuit incurs

[2] Assumes the wires between both plates exhibit negligible inductance, a reasonable assumption for the concerned application.

zero loss, this "to and fro" process will continue forever resulting in the generation of an undampened sinusoidal waveform as shown in Fig. 3.3.

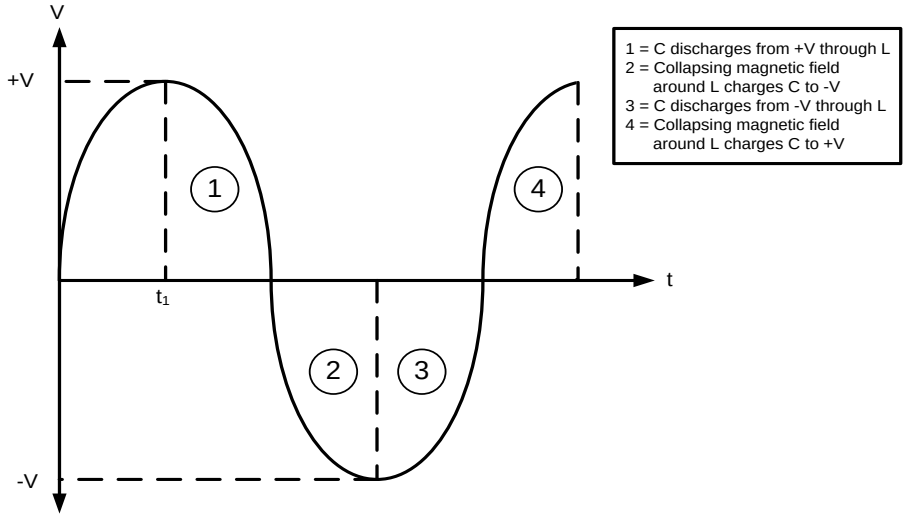



**Fig. 3.3:** Sine wave generated from the basic LC-tank

From Fig. 3.3, an obvious question to ask is at what frequency will the resulting sinusoid oscillate. The answer to this is that it will oscillate at such a frequency that results in zero net internal impedance. As both the inductor and capacitor consist of purely reactive components, this can be more succinctly stated as:

$$X_L + X_C = 0 \tag{3.1}$$

$$X_L = -X_C \tag{3.2}$$

where the inductor and capacitor reactance's are represented by $X_L$ and $X_C$ respectively.

Inserting the well known expressions for $X_L$ and $X_C$ into (3.2) and solving for $\omega$ gives the following expression for the oscillation frequency of a basic LC-tank:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.3}$$

where $\omega_o$ is termed the resonant frequency of the tank.

For a VCO, (3.3) represents an linear time-invariant (LTI) approximation of the output signal oscillation frequency. As such, it ignores the non-linearity of the VCO transfer characteristic (shown in section 3.4.3) and its time-dependant capacitive behaviour over the output signal swing [27]. It also ignores small-signal effects and as such typically yields values on the higher side of what is seen in practical VCOs. Nevertheless, due to

its simplicity it forms an excellent basis for VCO design and can be used providing the various shortcomings of it are consistently acknowledged.

Valuable understanding can be gained from examining the transfer function of the circuit in Fig. 3.2 which is defined (see Appendix A.8 for derivation) as:

$$H(s) = \frac{Ls}{LCs^2 + 1} \tag{3.4}$$

Analysis of (3.4) reveals the basic LC-tank to have one zero at 0 rads/s and two poles at the following frequencies:

$$\omega_{1,2} = \pm\frac{1}{\sqrt{LC}} \tag{3.5}$$

Both poles lie on the imaginary axis and exist as complex conjugate pairs, as expected for a purely oscillatory system. This gives rise to the magnitude response plotted in Fig. 3.4 for a basic LC-tank designed with $\omega_o \approx 3$ x $10^{10}$ rads/s (4.8 GHz).

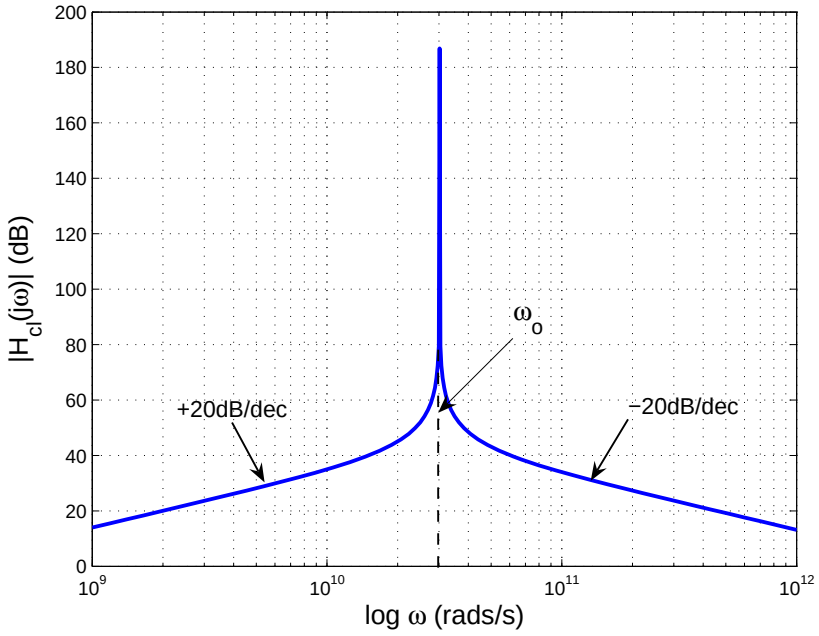



**Fig. 3.4:** Frequency response for a basic LC-tank

Fig. 3.4 shows the response to initially increase at a rate of +20dB/dec due to the zero at 0 rads/s. This increase continues up to $\omega_o$ after which the response decays at a rate of -20dB/dec due to the two poles at $\pm\omega_o$. Immediately obvious from Fig. 3.4 is the gain peak at $\omega = \omega_o$. This gain peak should go to infinity[3] and occurs because at resonance, zero internal impedance occurs (i.e. zero loss occurs) thereby enabling the

[3]Inserting (3.3) into (3.4) equals $\infty$, implying infinite gain at $\omega_o$. The version of Matlab used to create this plot (Ver. 7.2.0.294 (R2006a)) seems incapable of displaying an infinite peak and reaches a limit at $\approx$ 187 dB, indicating an input/output power ratio of $\approx 2.2$ x $10^9$.

system to oscillate forever. Typically such a peak would be very concerning as it indicates an unstable system (see Figs. 2.14 to 2.19). However as we require the VCO to oscillate (i.e. be "unstable") the opposite applies where such a sharp peak is highly desirable. In addition, the magnitude response of Fig. 3.4 shows the basic LC-tank to exhibit a band-pass characteristic behaviour. As will be shown in section 3.6.2, this characteristic greatly influences the phase noise behaviour of a VCO.

The behaviour of Fig. 3.4 can be neatly expressed using the quality factor of the LC-tank ($Q_{tank}$). This quantifies the energy loss of the tank, which in its most fundamental form is expressed [28]:

$$Q_{tank} = \frac{\omega W_{max}}{P_{diss}} \tag{3.6}$$

where $\omega$ is the radian frequency, $W_{max}$ is the maximum total electrical and magnetic energies stored in the tank and $P_{diss}$ is the total power dissipation of the tank. The most important observation from (3.6) is that $Q_{tank}$ is inversely proportional to $P_{diss}$ (i.e. energy loss). In other words, as the energy loss of the tank increases, its quality factor ($Q_{tank}$) decreases, thereby qualifying $Q_{tank}$ as a suitable parameter for quantifying total energy loss of the tank. In addition to this, as will be shown in section 3.6.2, $Q_{tank}$ greatly influences the phase noise performance of a VCO thereby making it one of the most important design parameters for an oscillator.

Assuming for the moment that zero loss occurs within the tank, then at resonance $P_{diss} = 0$, which from (3.6) results in an ideal infinite $Q_{tank}$. In practice however, losses do occur in the tank which reduce $Q_{tank}$ from this ideal infinite value. These losses are primarily dominated by losses within the inductor which severely degrade the quality factor of the inductor ($Q_L$). As $Q_L$ is typically much less than the quality factor of the capacitor ($Q_C$), it dominates (and hence severely degrades) $Q_{tank}$, as follows:

$$\begin{aligned} \frac{1}{Q_{tank}} &= \frac{1}{Q_L} + \frac{1}{Q_C} \\ &= \frac{Q_L}{1 + Q_L/Q_C} \\ &\approx Q_L \quad ..... \quad for\ Q_L << Q_C \end{aligned} \tag{3.7}$$

Therefore since $Q_L$ dominates $Q_{tank}$, it then becomes one of the most important design parameters for an oscillator.

The losses from the inductor can be represented by placing a resistor ($R_s$) in series with $L$ in Fig. 3.2. This gives the more practical representation of an LC-tank shown in Fig. 3.5.

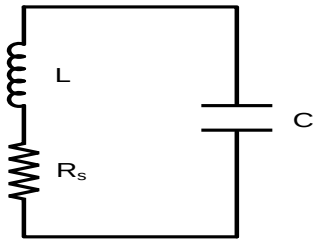



**Fig. 3.5:** Practical LC-tank

The transfer function describing the circuit of Fig. 3.5 (see Appendix A.9 for derivation) is defined as:

$$H(s) = \frac{Ls + R_s}{LCs^2 + +sR_sC + 1} \tag{3.8}$$

The poles of (3.8) now contain a real part due to the dampening ($\zeta$) introduced by $R_s$. Therefore, increases in $R_s$ will increase $\zeta$ forcing oscillations to decay and die out after some time.[4] As a result, the magnitude of the peak at $\omega_o$ in the frequency response decreases with increasing $R_s$. This can be seen in Fig. 3.6 which plots the frequency response of a practical LC-tank designed with $\omega_o \approx 3$ x $10^{10}$ rads/s (4.8 GHz) for various values of $R_s$.

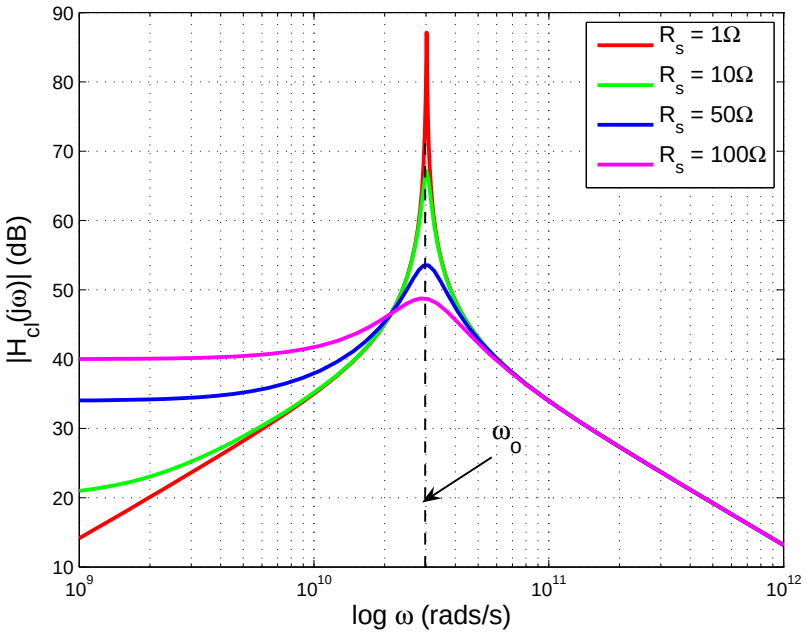



**Fig. 3.6:** Frequency response of a practical LC-tank for various values of $R_s$

The total impedance for the circuit of Fig. 3.5 at resonance ($Z_o$) can found by substituting (3.3) into (3.8) for $s = j\omega_o$ to be:

[4] If $R_s$ is increased such that $\zeta > 1$, no oscillations will occur at all.

$$Z_o = \frac{R_s + j\sqrt{L/C}}{jR_s\sqrt{C/L}} \tag{3.9}$$

Equation (3.9) is difficult to work with and so one seeks to describe it more succinctly which lends itself more easily to VCO design. This can be achieved through a parallel transformation of Fig. 3.5 to that shown in Fig. 3.7:

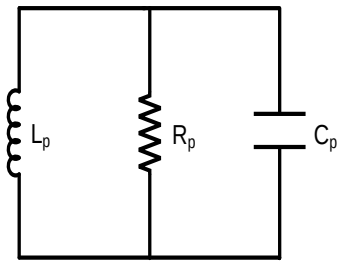



**Fig. 3.7:** Parallel representation of an LC-tank

In Fig. 3.7, $L_p$, $R_p$ and $C_p$ represent the parallel transformations of $L$, $R_s$ and $C$ in Fig. 3.5. These display the following relationships at (or close to) resonance [29]:

$$L_p \approx L_s \quad ..... \quad for\ Q_L\ >\ 3 \tag{3.10}$$

$$R_p \approx Q_{tank}^2\ R_s \tag{3.11}$$

$$C_p = C_s \tag{3.12}$$

The transfer function describing the circuit of Fig. 3.7 (see Appendix A.10 for derivation) is defined as:

$$H(s) = \frac{LR_p s}{LR_p Cs^2 + Ls + 1} \tag{3.13}$$

Substituting (3.3) into (3.13) for $s = j\omega_o$, reveals the total impedance of this circuit at resonance to be:

$$Z_o = R_p \tag{3.14}$$

Comparing (3.14) with (3.9) show it to represent the total impedance of the tank at resonance much more succinctly. As will be shown in the following section, this expression lends itself much easier to VCO design hence making $R_p$, in addition to $Q_L$, one of the most important VCO design parameters.

## 3.3 Design for Oscillation

Given that $R_s$ dampens down oscillations, the next obvious question to ask is how do we modify the LC-tank of Fig. 3.7 such that it sustains oscillation. This can be achieved by adhering to the Barkhausen Criteria which are the necessary (but not sufficient [30]) criteria for oscillation. These state that a system $H(s = j\omega)$ will oscillate if the following are adhered to:

$$|H(j\omega_o)| \geq 1 \tag{3.15}$$

$$\angle H(j\omega_o) = 2n\pi \quad ..... \quad for\ n = 0, 1, 2, ... \tag{3.16}$$

Provided the above are adhered to, the system will oscillate at $\omega_o$ rads/s. It is worth re-stressing that the above only serve as a criteria for oscillation and should not be used to assess the stability of a system as explained in section 2.6.3.

It is known from basic circuit theory that a common-source amplifier with resistive load $R$ exhibits the following voltage gain ($A_v$):

$$A_v = -g_m R \tag{3.17}$$

where $g_m$ represents the transconductance of the driving transistor and the negative sign denotes the $\pi$ rads phase shift inherent to the amplifier. Therefore, loading a common-source amplifier with an LC-tank provides a path to replenish the losses of the tank ($R_p$) and sustain oscillation. This is shown in Fig. 3.8 for a common-source amplifier with NMOS driving transistor ($M1$).

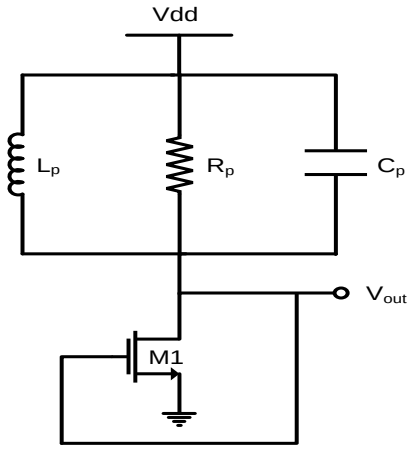



**Fig. 3.8:** Common-source amplifier with LC-tank load

The gain of the amplifier (from (3.17)) is $A_v = -g_m R_p$ and so $M1$ can be sized such that it contributes sufficient $g_m$ to satisfy (3.15). However, as the amplifier only exhibits a

total phase shift of $\pi$ rads it does not satisfy (3.16) and therefore achieves zero oscillation. Nevertheless, the common-source amplifier of Fig. 3.8 can be modified such that it satisfies (3.16) through the following configuration.

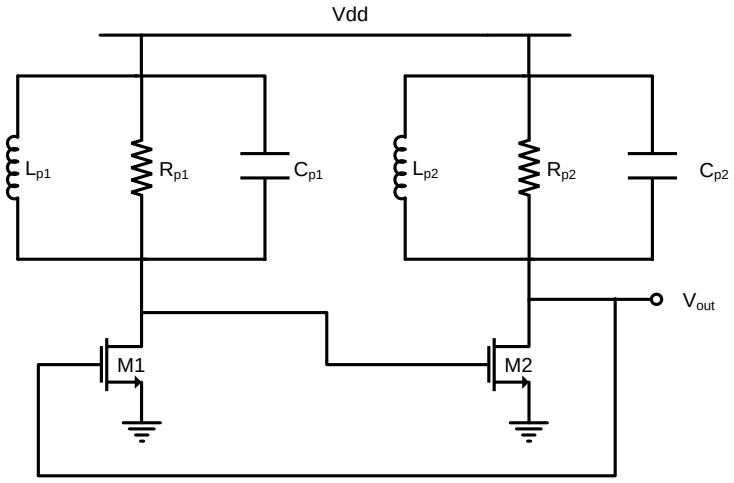



**Fig. 3.9:** Basic LC oscillator

The circuit of Fig. 3.9 is a basic LC oscillator and consists of two series connected common-source amplifiers with NMOS driving transistors ($M1$, $M2$), typically termed the cross-coupled differential pair. As each amplifier contributes a phase shift of $\pi$ rads, a total phase shift of $2\pi$ rads is achieved to satisfy (3.16). The total voltage gain ($A_{V_T}$) of the circuit is then:

$$\begin{aligned} A_{V_T} &= (-g_{m1}R_{p1})(-g_{m2}R_{p2}) \\ &= g_m^2 R_p^2 \quad ..... \quad M_1 = M_2 \; and \; R_{p1} = R_{p2} \\ &= (g_m R_p)^2 \end{aligned} \tag{3.18}$$

We know from (3.14) that $A_{V_T} \geq 1$ to sustain oscillation, which from (3.18) basically means $g_m R_p \geq 1$. From this it follows:

$$g_m \geq \frac{1}{R_p} \tag{3.19}$$

In practice a factor of safety of two is included to ensure oscillations are sustained giving the following well known formula for oscillation:

$$g_m \geq \frac{2}{R_p} \tag{3.20}$$

Inserting (3.11) into (3.20) reveals the importance of achieving a large $Q_{tank}$ since it

reduces the $g_m$ requirements to sustain oscillation hence leading to a reduction in power consumption. This makes intuitive sense as the higher the $Q_{tank}$, the lower the tanks energy loss and hence the lower the power required to replenish this loss. More specifically stated - increasing $Q_{tank}$ by a factor of $x$ increases $R_p$ by a factor of $x^2$ thereby reducing $g_m$ and hence overall power consumption also by a factor of $x^2$.

In practice the $g_m$ requirements of (3.20) are achieved by sizing one cross-coupled transistor accordingly for a specified drain-source voltage ($V_{ds}$). This drain-source voltage is determined by the DC bias level ($V_{DC}$) of the VCO which is typically set to Vdd/2 to maximise output signal swings (output signals will oscillate around $V_{DC}$). The resulting current required from this sizing is then multiplied by two (two cross-coupled transistors exist) to yield the total bias current ($I_{bias}$) for the oscillator. It is imperative that $I_{bias}$ be accurately defined and remain constant over process, voltage and temperature (PVT) variation in order to sustain constant oscillation around a fixed DC bias point. Therefore, it must be defined using a current source or sink. This is achieved in Fig. 3.10 which shows a conventional LC oscillator where $I_{bias}$ is defined using a current sink. The oscillator has NMOS cross-coupled transistors ($M_1$ and $M_2$) and is shown to exhibit differential outputs ($V_{out^+}$ and $V_{out^-}$) thereby terming it a differential oscillator. In addition, it shows the two LC-tanks of Fig. 3.9 to now be combined into one LC-tank whose inductor and capacitor will be sized to give the required $L$ and $C$ values necessary to achieved the specified resonant frequency as per (3.3).

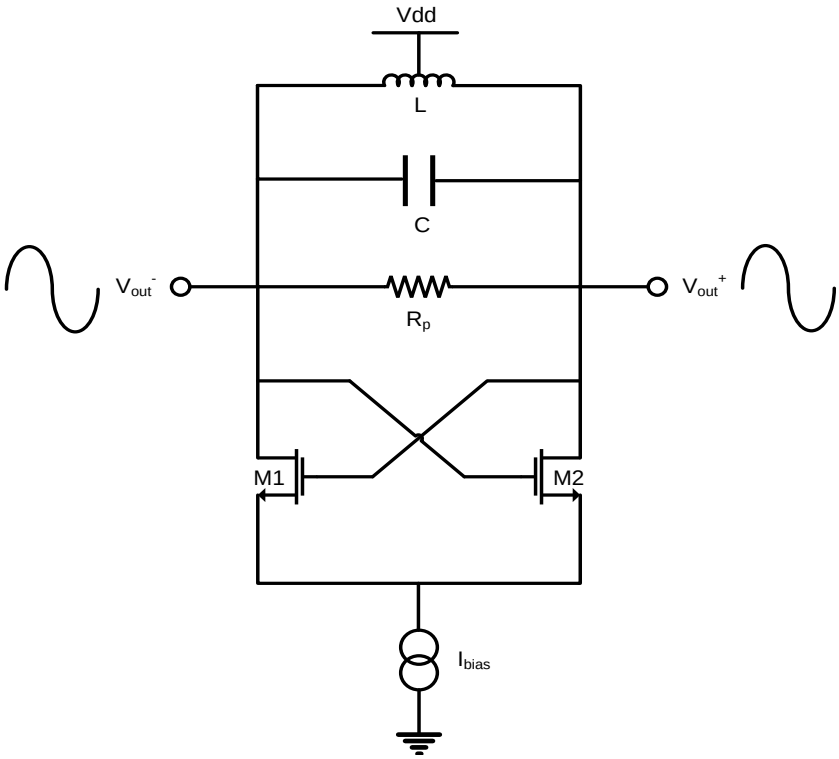



**Fig. 3.10:** Differential LC oscillator

## 3.4 Tuning in LC Oscillators

The oscillators up to this point are only capable of oscillating at one frequency ($\omega_o$). However, to function in a PLL they must be modified such that they are capable of operating over a number of frequencies. This is achieved in practice by incorporating a tuning mechanism into the oscillator which enables it to oscillate over the required frequency range, most commonly specified as the tuning range ($TR$) of the oscillator. This is defined as follows:

$$TR(\%) = \frac{2(f_{max} - f_{min})}{f_{max} + f_{min}} \cdot 100 \tag{3.21}$$

where the maximum and minimum oscillation frequencies are represented by $f_{max}$ and $f_{min}$ respectively. As can be seen from (3.21), $TR$ is normalised to the frequency range of the oscillator where it is generally represented as a percentage.

Equation (3.3) showed oscillation frequency ($\omega_o$) to be proportional to the total inductance ($L$) and capacitance ($C$) of the tank. Therefore variation of $\omega_o$ is simply achieved through variation of either $L$ or $C$. Since in practice it is difficult to vary the value of $L$, $C$ is typically the varied parameter. This is achieved by replacing the fixed capacitor in the tank with a variable capacitor whose capacitance varies with changing voltage across it. Such a capacitor is termed a voltage controlled capacitor, or more commonly a varactor, which when inserted for the fixed capacitance in a standard oscillator realises a voltage controlled oscillator (VCO). This voltage variation is stimulated by an applied control voltage, which for VCOs placed in a PLL (as in Fig. 2.1) corresponds to $V_{ctrl}$.

Care must be taken with $V_{ctrl}$ so as it does not disturb the DC bias of the tank ($V_{DC}$). This is achieved in practice by ac-coupling $V_{ctrl}$ and $V_{DC}$ through splitting the total varactor capacitance into two equal capacitance's ($C_{var}$), as shown in Fig. 3.11.

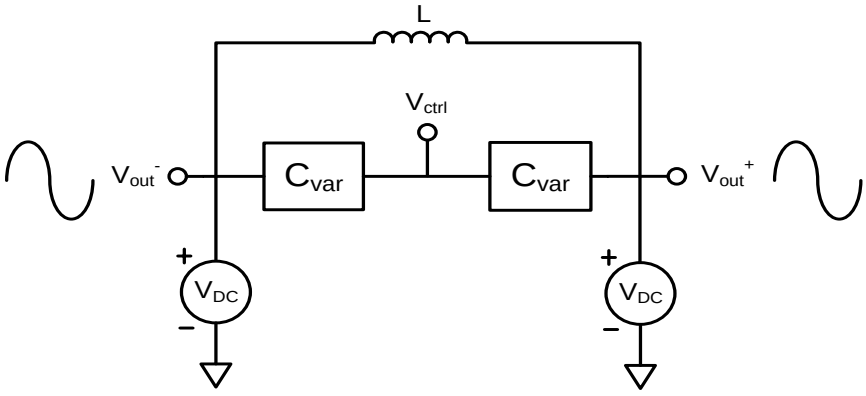



**Fig. 3.11:** Typical varactor configuration for single-ended VCO tuning

The ideal transfer characteristics produced by the circuit of Fig. 3.11 were shown in

Fig. 2.11, where the frequency range as a function of control voltage was shown to be neatly represented by the gain of the VCO ($K_{VCO}$ defined in (2.13)). In practice this behaviour is determined by the capacitance to voltage characteristics of the varactor, shown by its corresponding C(V) characterisation curve. These curves are used extensively in practice to determine the behaviour of a particular varactor or varactor configuration. From them, the maximum and minimum capacitances of the varactor (or varactor configuration) for the allowable $V_{ctrl}$ limits can be extracted and the ratio of the two computed. This gives the $C_{max}/C_{min}$ ratio which can be shown (see Appendix A.11 for derivation) to loosely approximate $TR$ as follows:

$$TR(\%) = 2\sqrt{\frac{C_{max}/C_{min} + 1 - 2\sqrt{C_{max}/C_{min}}}{C_{max}/C_{min} + 1 + 2\sqrt{C_{max}/C_{min}}}} \cdot 100 \tag{3.22}$$

It is important to note that (3.22) ignores non-LTI and small-signl effects in addition to parasitic capacitances introduced during layout (see Appendix B3). As such, it typically yields values on the higher side of what are seen in practice and so should only be used as an approximate guide. Nevertheless, it does suffice to show the dominance of the $C_{max}/C_{min}$ ratio on the $TR$ which when plotted, gives an idea of the ratios required to yield a specified $TR$. This is shown in Fig. 3.12 which plots $TR(\%)$ for $C_{max}/C_{min}$ ratios ranging from $1 \rightarrow 5$.

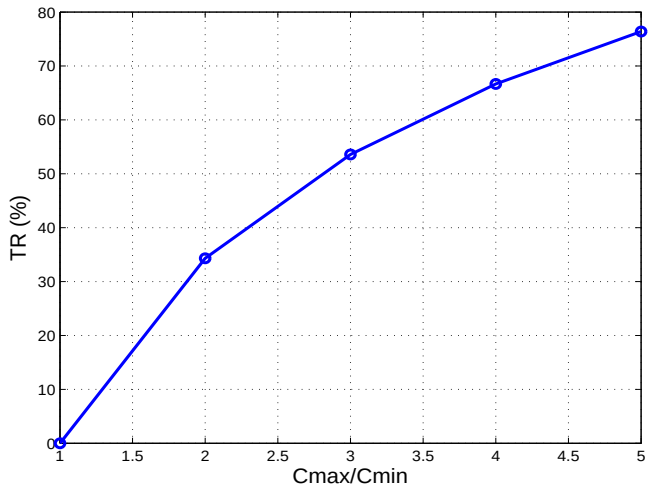



**Fig. 3.12:** $TR$ versus $C_{max}/C_{min}$ ratio

Looking purely at Fig. 3.12 one could assume that the maximum possible $C_{max}/C_{min}$ ratio should always be designed for in order to increase the tuning range of the VCO. However as large $C_{max}/C_{min}$ ratios result in large $K_{VCO}$ values, this will increase the phase noise of the VCO (shown in sections 4.2.2 and 4.5.4). As a result, achieving low noise performance whilst maintaining a large tuning range is a major challenge in VCO design.

Varactors in practice can be realised using MOSFET devices (MOS varactors) or diodes (diode varactors).

### 3.4.1 MOS Varactors

We know from basic MOSFET theory that the gate terminal of a MOSFET, its gate oxide and underlying channel exhibit a capacitive behaviour which varies with applied gate bias. Therefore, by suitably configuring a MOSFET and varying its gate bias, a voltage dependant capacitive behaviour can be achieved thereby realising a MOS varactor.

PMOS devices sitting in an $n$-well are generally preferred to implement MOS varactors as this allows the substrate to be biased at a variable voltage. Various configurations to realise such MOS varactors exist in practice, two of which are shown in Figs. 3.13 and 3.14.

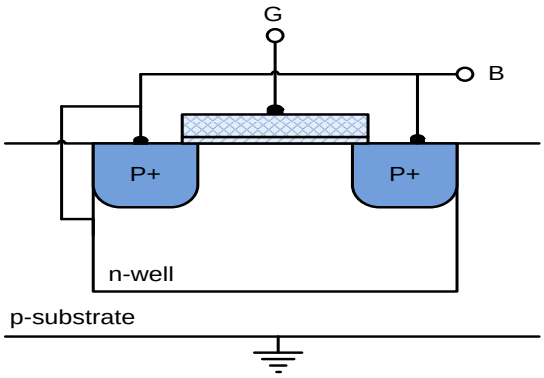



**Fig. 3.13:** Drain/source/bulk shorted

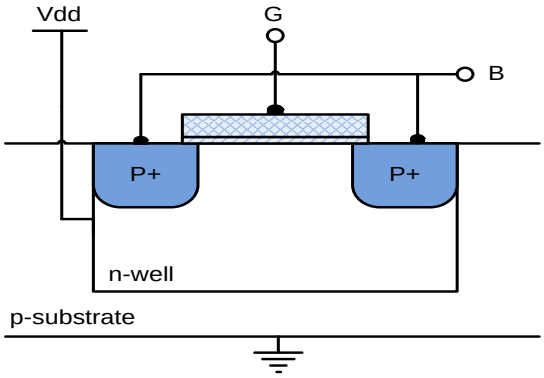



**Fig. 3.14:** Drain/source shorted

In Fig. 3.13, the drain, source and bulk terminals of a PMOS are shorted together to form one terminal of the varactor (B) with the gate node forming the second terminal (G). However, as this configuration can operate in the inversion, depletion and accumulation regions, it exhibits a non-monotonic C(V) characteristic [31] unsuitable for VCO tuning. A similar configuration is then shown in Fig. 3.14 where the drain and source terminals are shorted together to form one terminal (B) with the gate node once again forming the second terminal (G). As the bulk terminal for this configuration is connected to Vdd, operation in the accumulation region can no longer occur thereby realising a monotonic C(V) curve suitable for VCO tuning. Nevertheless, the C(V) characteristic is very abrupt [32] and therefore when placed in a VCO realises large $K_{VCO}$ values unsuitable for low phase noise operation (see section 4.2.2).

A more practical MOS varactor can be obtained by replacing the $P+$ source and drain wells of the previous varactors with $N+$ wells [33] and applying the same configuration as shown in Fig. 3.13.[5] This suppresses the injection of minority carriers (holes) into

[5] A similar MOS varactor can be fabricated by implanting $P+$ source and drain wells into a $p$-well. This structure however requires a triple well process (leading to increased manufacturing costs) and exhibits poor quality factors due to the increased resistance of the $p$-well [33].

the channel thereby eliminating the inversion region of operation. As operation can now only occur in the depletion and accumulation regions, a monotonic C(V) characteristic results with the resulting varactor typically termed an accumulation mode MOS varactor (AMOS). An additional advantage of the $N+$ regions is they eliminate the parasitic pn-junction capacitance associated with the source and drains of the varactors (see Figs. 3.13 and 3.14) which would otherwise reduce the tuning range ($TR$) [33]. A cross-section of an AMOS, along with its corresponding C(V) characterisation curve are shown in Figs. 3.15 and 3.16 respectively.

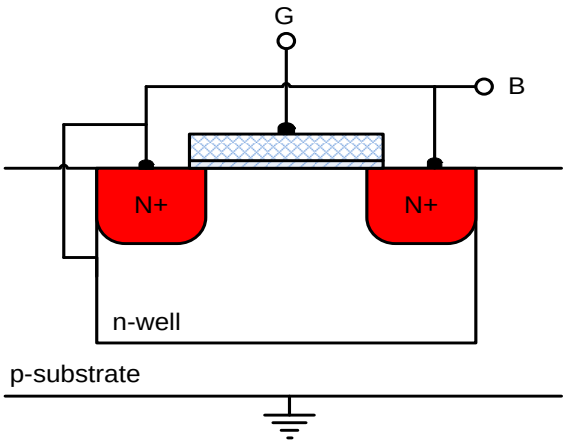



**Fig. 3.15:** Cross-section of an AMOS

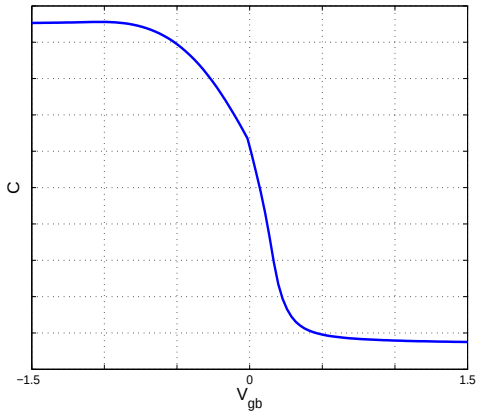



**Fig. 3.16:** C(V) curve for an AMOS

The AMOS characterised by the C(V) curve of Fig. 3.16 was taken from UMCs 90nm CMOS process with its exact device dimensions being of no major significance to this discussion. For the characterisation, a fixed DC bias of 0.5V was applied to the bulk terminal ($V_b = 0.5V$) with a tuning bias ($V_{ctrl}$) varying from -1 $\rightarrow$ 2V applied to the gate terminal ($V_g = -1V \rightarrow 2V$), such that $V_{gb} = -1.5V \rightarrow 1.5V$. Applying a 4.8GHz sine wave to the AMOS and plotting the resulting capacitance for each value of $V_{gb}$ then yielded the corresponding C(V) characterisation curve. Immediately obvious from the curve is how non-linear it is which, as will be seen in section 3.4.3, causes severe problems for the VCO and PLL itself. Since the slope of the curve varies over $V_{gb}$, it can be seen to be maximal at the centre of the curve (i.e. where $V_{gb} = 0V$) entering flatter regions as it moves either side of this. As such, it is desired to operate AMOS varactors between these flatter regions since it provides the most significant capacitance variation and hence tuning capability, often referred to as the dynamic region of the varactor.

There are the two possible implementations of an AMOS in a VCO with single-ended tuning. These are shown in Figs. 3.17 and 3.18 using the standard circuit symbols for a MOS varactor. In Fig. 3.17 the gates are tuned whereas in Fig. 3.18 the bulks are tuned. The tuning of Fig. 3.17 is similar to that used to obtain the C(V) characterisation curve in Fig. 3.16 and so exhibits a similar C(V) characteristic. As the tuning in Fig. 3.18 is

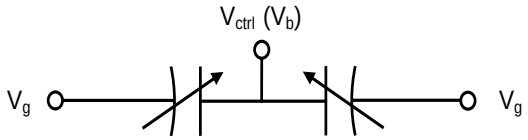



**Fig. 3.17:** Gate tuning

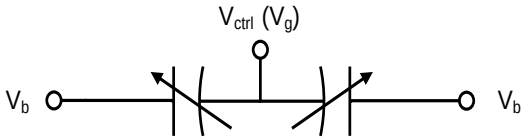



**Fig. 3.18:** Bulk tuning

opposite to Fig. 3.17, its C(V) characterisation curve moves in the opposite direction to that shown in Fig. 3.16 (i.e. C monotonically increases with increasing $V_{ctrl}$). Nevertheless, from a functionality point of view both configurations can be used in a VCO as they provide the same net behaviour. However, from a performance point of view the configuration of Fig. 3.17 was seen through simulation using UMCs 90nm CMOS process to be more advantageous as it always resulted in higher quality factors. The exact physical reasons for this, and their consistency over all processes and frequency, is a subject left to in depth device physics and as such is beyond the scope of this thesis. However, it is suspected that the increased losses seen for bulk tuning are highly influenced by the behaviour of the depletion region existing between the $n$-well and $p$-substrate (see Fig. 3.15).

### 3.4.2 Diode Varactors

A second type of varactor can be realised using a simple pn-junction diode illustrated in Figs. 3.19 and 3.20.

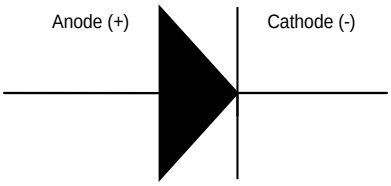



**Fig. 3.19:** Diode symbol

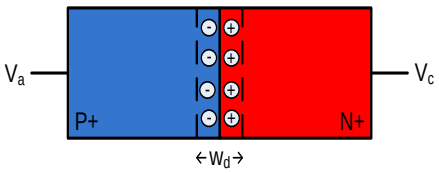



**Fig. 3.20:** PN-junction diode

We know from basic semiconductor theory that an intrinsic depletion region always forms at the junction of the $p^+$-type and $n^+$-type regions (shown in Fig. 3.20) whose width ($w_d$) increases as the reverse bias voltage across it increases (i.e. as the cathode voltage ($V_c$) exceeds the anode voltage ($V_a$)). Recall that the capacitance ($C$) of a parallel plate capacitor exhibits the following proportionality:

$$C \propto \frac{A}{d} \tag{3.23}$$

where the area of the plates and their separation distance are represented by $A$ and $d$

respectively. Viewing the depletion region of a pn-junction diode in terms of a parallel plate capacitor, we can see its increase in width to correspond to an increase in $d$ in (3.23) and hence a reduction in $C$. Therefore, by varying the reverse bias voltage across a diode we can achieve a voltage dependant capacitive behaviour, thereby realising a diode varactor.

The most important aspect of a diode varactor, and often the most limiting, is that it must never be forward biased. Should this occur, the voltage dependent capacitive behaviour will no longer be significantly realised as the width of the depletion region can no longer be significantly varied. This can be seen in Fig. 3.21 which plots both the capacitance of a diode varactor ($C_{var}$) and the current through it ($I_d$) against the voltage across it from anode to cathode ($V_{ac}$).

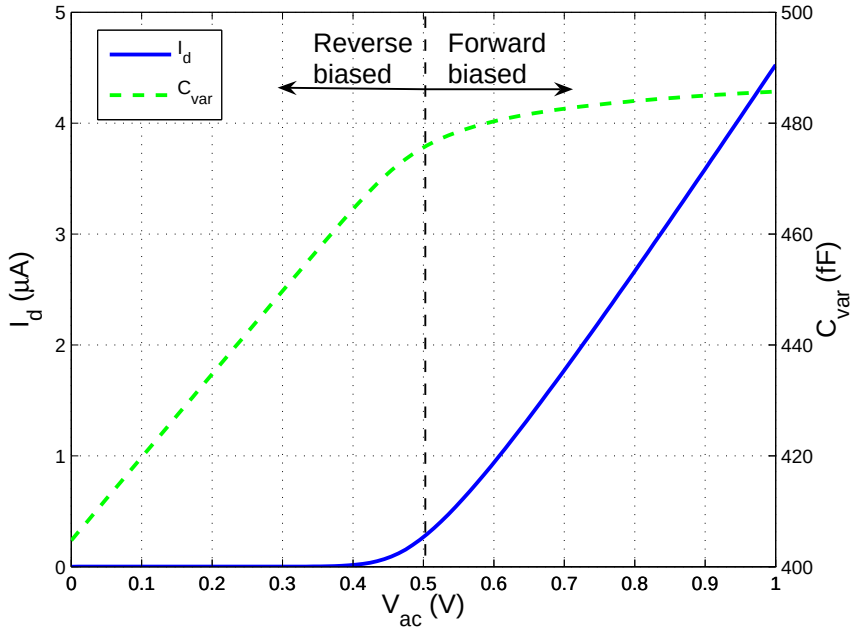
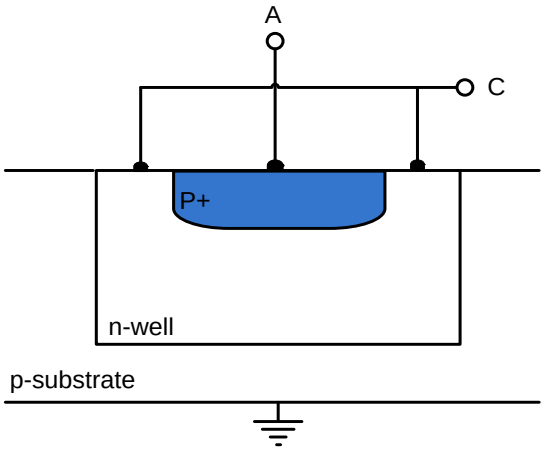



**Fig. 3.21:** $I_d$ and $C_{var}$ versus $V_{ac}$

In Fig. 3.21 the current through the varactor ($I_d$) is plotted by the solid blue line whose corresponding values are shown on the left y-axis. This shows little or no current to flow for $V_{ac} < 0.5$V (i.e when the diode is reverse biased). However at $V_{ac} \approx 0.5$V, the diode starts to conduct and become forward biased with any further increases in $V_{ac}$ resulting in an exponential rise in $I_d$ (as per agreement with basic semiconductor theory). The capacitance of the varactor ($C_{var}$) is then plotted by the green trace with its corresponding values shown on the right y-axis. This shows $C_{var}$ to significantly increase with $V_{ac}$ up to $\approx 0.5$V above which it only experiences a slight increase. The reason for this is because when the varactor is reverse biased, the width of its depletion region significantly decreases with increases in $V_{ac}$ up to $\approx 0.5$V. However at $V_{ac} \approx 0.5$V, the

diode varactor turns on and becomes forward biased where the width of its depletion region can no longer significantly reduce due to further increase $V_{ac}$. As a result only very slight increases in $C_{var}$ occur above $V_{ac} \approx 0.5$V.

In practice, a varactor diode is typically realised by implanting a $p^+$ region (to realise the cathode) inside an $n$-well (to realise the anode) on a $p$-substrate. The cross-section of such a realisation is shown in Fig. 3.22 where its corresponding C(V) characteristic is shown in Fig. 3.23.



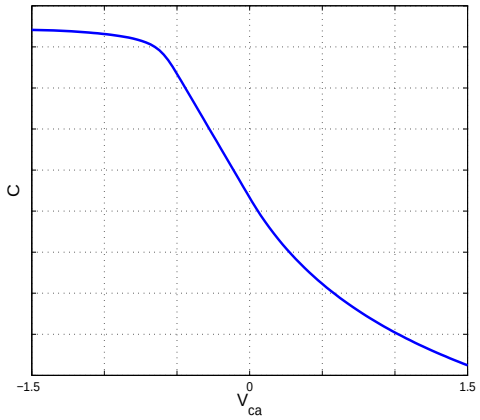




**Fig. 3.22:** Cross-section of diode varactor **Fig. 3.23:** C(V) curve for a diode varactor

The diode varactor characterised by the C(V) curve of Fig. 3.23 was taken from UMCs 90nm CMOS process with its exact device dimensions being of no major significance to this discussion. For the characterisation a fixed DC bias of 0.5V was applied to the anode (i.e. $V_a = 0.5V$), with a tuning bias ($V_{ctrl}$) varying from -1V $\rightarrow$ 2V applied to the cathode (i.e. $V_c = 0 \rightarrow 1V$) such that $V_{ca} = -1.5V \rightarrow 1.5V$. Applying a 4.8GHz sine wave to the diode varactor and plotting the resulting capacitance for each value of $V_{ca}$ then yielded the corresponding C(V) characterisation curve. As was the case for the C(V) curve of the AMOS in Fig. 3.16, the curve in Fig. 3.23 is also seen to be very non-linear resulting in the same problems for VCO and end PLL operation discussed in section 3.4.3. Since the slope of the curve varies over $V_{ca}$, it can be seen to be maximal at the centre of the curve (i.e. where $V_{ca} = 0V$) entering flatter regions as it moves either side of this. As is the case with AMOS varactors, it is desired to operate diode varactors between these flatter regions to realise the full potential of their dynamic region.

Like with the AMOS, two configurations can be used to implement diode varactors in a VCO with single-ended tuning. These are shown in Figs. 3.24 and 3.25 using the standard circuit symbols for a diode varactor. In Fig. 3.24 the cathodes are tuned (i.e. $V_c = V_{ctrl}$) with the anodes biased so as not to forward bias the varactor. In Fig. 3.25 the anodes are tuned (i.e. $V_a = V_{ctrl}$) with the cathodes biased so as not to forward bias the varactor. The tuning of Fig. 3.24 is similar to that used to obtain the C(V) characterisation curve

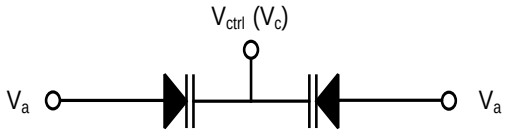



**Fig. 3.24:** Cathode tuning

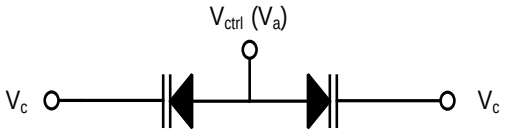



**Fig. 3.25:** Anode tuning

in Fig. 3.23 and so exhibits a similar C(V) characteristic. As the tuning in Fig. 3.25 is opposite to Fig. 3.24, its C(V) characterisation curve moves in the opposite direction to that shown in Fig. 3.23 (i.e. C monotonically increases with increasing $V_{ctrl}$). Nevertheless as was seen with MOS varactors, both configurations can be employed in a VCO as they result in the same net functionality. However from a performance point of view, the configuration of Fig. 3.24 is more advantageous as it typically results in higher quality factors over the configuration of Fig. 3.25. This is due to signal losses to the substrate and is heavily influenced by the depletion region existing between the $n$-well and $p$-substrate of the diode varactor [34] (see Fig. 3.22). For anode tuning, this depletion region is directly modulated by the signal swing across the varactor, hence becoming periodically forward biased and contributing to signal loss to the substrate. Since for cathode tuning this depletion region is somewhat shielded from the signal swing across the varactor (signal enters at the anode), it is not modulated to such a great extent hence resulting in reduced signal loss to the substrate and correspondingly higher quality factors. As a result, where possible cathode tuning should be employed when using diode varactors.

The configurations of Figs. 3.24 and 3.25 can not however be directly implemented in a VCO as this will result in them becoming periodically forward biased by the output signal swings of the VCO, unless $V_{ctrl}$ is severely restricted [35]. To avoid this, a biasing scheme such as that described in [36] should be adopted to ensure the varactors remain reverse biased over the entire output signal swing of the VCO. This will result in the configurations shown in Figs. 3.26 and 3.27.

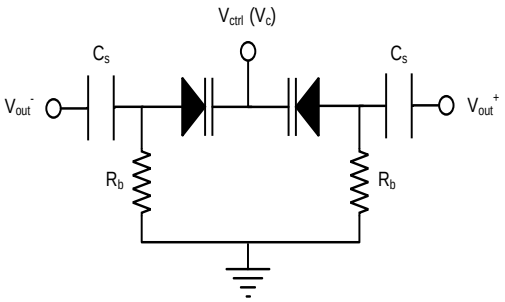



**Fig. 3.26:** Modified cathode tuning

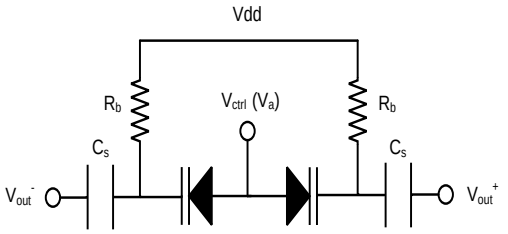



**Fig. 3.27:** Modified anode tuning

In Figs. 3.26 and 3.27 the output signals of the VCO are represented by $V_{out}^{+}$ and $V_{out}^{-}$ which can be seen to be ac-coupled to the diode varactors through the ac-coupling capacitor $C_s$. This enables the applied biasing scheme which ensures the anode voltages of the varactors in both configurations never exceed their cathode voltages (i.e. $V_a \not> V_c$), thereby ensuring the varactors always remain reverse biased without restricting $V_{ctrl}$. The resistors ($R_b$) in both configurations are required to prevent signal loss, with simulation showing the following rule to prevent significant loss:

$$R_b \geq 10 \cdot (2(X_{C_{var}} + X_{C_s})) \tag{3.24}$$

where the impedance's of the diode varactors and ac-coupling capacitors are represented by $X_{C_{var}}$ and $X_{C_s}$ respectively. The expression $2(X_{C_{var}} + X_{C_s})$ thus represents the total impedance of the ideal path in the LC-tank with the resulting values for $R_b$ to satisfy (3.24), being typically large in practice. The ac-coupling capacitors ($C_s$) are then sized according to the specified tuning range (typically achieved through simulation).

Although this biasing scheme prevents the varactors forward biasing, it does so at the cost of reduced tuning range (due to the additional capacitance from $C_s$), increased phase noise (due to thermal noise contributions from $R_b$) and increased silicon area consumption (due to the additional area requirements of both $C_s$ and $R_b$). Nevertheless, it is a biasing scheme found in most papers pertaining to VCOs employing diode varactor tuning and thus is adapted in this thesis for all such VCOs.

### 3.4.3 Performance Comparison of MOS Varactors and Diode Varactors

Comparing the C(V) characterisation curves for MOS and diode varactors in Figs. 3.16 and 3.23 respectively reveals both varactor types to exhibit different C(V) characteristics. The advantages and disadvantages of both types are discussed below leading to various conclusions regarding the optimal varactor type. It should be noted however that these conclusions are purely based on simulations performed on varactors using UMCs 90nm CMOS process and thus may not be consistent over all processes. Nevertheless they do suffice to give a good overview of the performance for both varactor types and clearly show why one type was chosen over the other for the final VCO of this thesis.

*Varactor quality factor ($Q_{var}$)*: For UMCs 90nm CMOS process, simulations showed diode varactors in general to yield far superior quality factors than MOS varactors. Therefore, from the perspective of low power and low phase noise operation (see sections 3.3 and 3.6) their high quality factors make diode varactors (in UMCs 90nm CMOS process) more preferable.

*Linearity*: The non-linearity of the C(V) curves in Figs. 3.16 and 3.23 results in a non-linear $K_{VCO}$. This represents a major issue with both varactor types in general. In section 2.4.3, $K_{VCO}$ was assumed linear to enable a linear representation of the VCO (and PLL). The non-linear C(V) characteristics therefore reduce the accuracy of the resulting linear models used to describe the VCO and PLL. In section 2.7.2, loop bandwidth ($K$) was shown to be directly proportional to $K_{VCO}$. As a non-linear $K_{VCO}$ varies over the $V_{ctrl}$ swing it gives rise to loop bandwidth variation ($\Delta K$) and all the associated issues discussed in section 2.7.4 (discussed in greater detail in chapter 5.) Lastly, as will be shown in section 3.6.3, varactor non-linearity degrades the close-in phase noise performance of a VCO. As such, it is clear that varactors exhibiting good linearity are highly desirable. For UMCs 90nm CMOS process, analysis of both C(V) characteristics in Figs. 3.16 and 3.23 reveals diode varactors to achieve improved linearity over MOS varactors, hence making diode varactors (in UMCs 90nm CMOS process) more preferable.

$C_{max}/C_{min}$ *ratio*: In section 3.4 the $C_{max}/C_{min}$ ratio was shown to dominate the resulting tuning range ($TR$) of the VCO with Fig. 3.12 plotting the growth in $TR$ for increasing ratios. In general, MOS varactors achieve significantly larger $C_{max}/C_{min}$ ratios than diode varactors hence enabling larger $TR$s to be realised. To exemplify this using UMCs 90nm CMOS process, the MOS and diode varactor configurations, characterised by Figs. 3.16 and 3.23 respectively, were each sized so as to achieve identical $C_{max}$ values thereby allowing a fair comparison between their respective $C_{max}/C_{min}$ ratios. The resulting comparisons are shown in Table 3.2 which show the MOS varactor to achieve a $C_{max}/C_{min}$ ratio almost 4 times greater than that for the diode varactor. Cross referencing with Fig. 3.12 then shows this to realise significantly larger tuning ranges ($TR$) and so from the perspective of satisfying large $TR$ specifications,[6] MOS varactors are preferred (this fact is further emphasised by the biasing scheme of Figs. 3.26 and 3.27 where $C_s$ further reduces the diode varactors realisable $TR$).

| | MOS varactor | Diode varactor |
|---|---|---|
| $C_{max}$ (fF) | 100 | 100 |
| $C_{min}$ (fF) | 20 | 75 |
| $C_{max}/C_{min}$ | 5 | 1.3 |
| $TR$ [a] (%) | $\approx 76$ | $\approx 12$ |

[a] $TR$ values were extracted from Fig. 3.12

**Table 3.2:** MOS and diode varactor $C_{max}/C_{min}$ ratio comparison

Nevertheless with high $C_{max}/C_{min}$ ratios comes large $K_{VCO}$ values which, as will be

[6] Large $TR$s are required from wideband VCOs/PLLs necessary to enable multi-band (or standard) operation in wireless communication systems.

shown in sections 4.2.2 and 4.5.4, degrades VCO phase noise performance. As such, the lower $C_{max}/C_{min}$ ratios of diode varactors favours low noise performance.

*Symmetry*: This is a point which will be fully explored in chapter 4. However for now it should be noted that for differentially tuned VCOs, the symmetrical C(V) characterisation curves are extremely important to obtaining as high a common-mode rejection ratio (CMRR) as possible. Simulations for UMCs 90nm CMOS process have shown diode varactors to exhibit improved symmetry over MOS varactors thereby (shown in section 4.5) making them preferable (in UMCs 90nm CMOS process) to differentially tuned VCOs with high CMRRs.

Given that this thesis is primarily focused on wireless applications, we strongly prioritise noise (as discussed in chapter 1). As such, the high $Q_{var}$, low $C_{max}/C_{min}$ ratios and good symmetry of diode varactors becomes very attractive to our application needs. In addition, this thesis is focussed on reducing loop bandwidth variation ($\Delta K$) hence making the improved linearity of diode varactors extremely attractive. This leads us to the conclusion that, for our application needs using UMCs 90nm CMOS process, diode varactors prove a far superior choice and thus were employed in the final VCO of this thesis.

## 3.5 Inductors

The inductor is a critical component of the VCO which dominates VCO performance and greatly influences overall PLL design. In section 3.2 its losses were seen to dominate that of the tank resulting in $Q_{tank} \approx Q_L$ and thereby dramatically reducing $Q_{tank}$. In addition to increasing VCO power consumption (see (3.20) and the paragraph directly proceeding it), as will be shown in section 3.6, a low $Q_{tank}$ (i.e. low $Q_L$) also severely degrades the phase noise performance of a VCO. Therefore, the primary criterion for inductor choice is to make $Q_L$ as high as possible. This is achieved in practice by reducing the inductor losses ($R_s$).

In [37], $Q_{tank}$ in (3.6) was shown to be simplified to:

$$Q_{tank} = \frac{1}{R_s}\sqrt{\frac{L}{C}} \tag{3.25}$$

This shows that in addition to reducing $R_s$, $Q_{tank}$ can be increased by maximising the $L/C$ ratio in (3.25). In practice this corresponds to choosing an inductor with large L thereby requiring small values for C from (3.3) to achieve the specified output frequency range. Therefore, another criterion for inductor choice is to make $L$ as large as possible. In practice however, $L$ cannot be made indefinitely large as this may result in impractically

small values for C being required.

It has been proposed in [38] to realise inductors using the inherent inductance characteristics of a bond-wire. The advantage of such an approach is that due to the low series resistance of gold bond wires, they can achieve large $Q_L$'s, with $Q_L > 30$ being reported in [39]. However, this approach is far from practical as the precise inductance of a bond wire is very difficult to guarantee from manufacturing and as such is not applicable to industry.

A more practical alternative is realised using spiral inductors. As these can be fabricated more easily (since the early 1990's [40], [41]) they are more applicable to industry, with their main downfall being lower quality factors (typically less than 20) as a result of their various loss mechanisms. These loss mechanisms can be divided into two groups consisting of metal losses and substrate losses, as shown in Fig. 3.28.

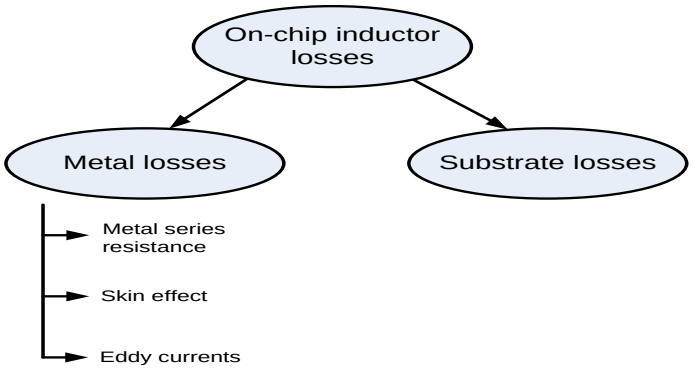



**Fig. 3.28:** Loss mechanisms in an on-chip inductor

Fig. 3.28 shows three different phenomenons to give rise to metal losses. The first of these is due to the series resistance of the inductor coil material (Aluminium or Copper) and dominates at low frequencies. However at high frequencies (where the VCO is commonly operated) losses due to the skin effect become more influential. The skin effect is a high frequency effect which causes current density to be highest at the surface of the conducting material thereby increasing the effective resistance seen by the current. Conventional wisdom suggests making the metal conductors (which constitute the inductor coils) wide so as to reduce their series resistance. However, as shown in [42] this increases the skin effect, and so for high frequency VCOs the width of the metal conductors should be limited. Eddy currents are another high frequency effect occurring due to the large magnetic fields passing through the inner coils [42]. This results in the generation of eddy currents within the innermost coils which force current to flow at the outer edges of the coils thereby increasing the effective resistance seen by the current. However, due to their small area the inner coils do not contribute much to the overall inductance and so can be omitted to dramatically reduce the effect of eddy currents [43].

Substrate losses are a significant source of loss and occur due to the generation of currents within the substrate from the magnetic field of the inductor. According to Lenz's law, this induced current flows in such a direction to oppose the original change in magnetic field hence resisting the original current flow of the inductor and lowering $Q_L$. In addition, this induced current also reduces the total magnetic field resulting in lower values of $L$. As this effect decreases with increased substrate resistivity (less induced current flows) it can be decreased by fabricating the VCO on a substrate with high resistivity [40]. However, this approach does not apply to CMOS technologies which require a substrate with low resistivity to eliminate various non-ideal effects. A more general approach is therefore to shield the inductors magnetic field from the substrate using ground shields [44]. Due to process restrictions however, this approach could not be pursued for the final VCO of this thesis.

The above discussions show the loss mechanisms within an inductor to be mainly dependant on frequency. As such, its quality factor ($Q_L$) varies over frequency leading to the obvious question of what frequency will $Q_L$ be maximum. There is no set rule to this as inductors in a standard process are generally optimised for operation around a specific frequency range.[7] Therefore, this optimum frequency range must first be found by characterising $Q_L$ over a wide range of frequencies (frequency sweep). This is shown in Fig. 3.29 where the quality factor of a standard hollow spiral inductor, (to reduce the high frequency effects from eddy currents) taken from UMCs 90nm CMOS process, is characterised over a frequency sweep from 1GHz $\rightarrow$ 10GHz (i.e. an applied sine wave oscillates across the inductor at frequencies ranging from 1GHz $\rightarrow$ 10GHz).

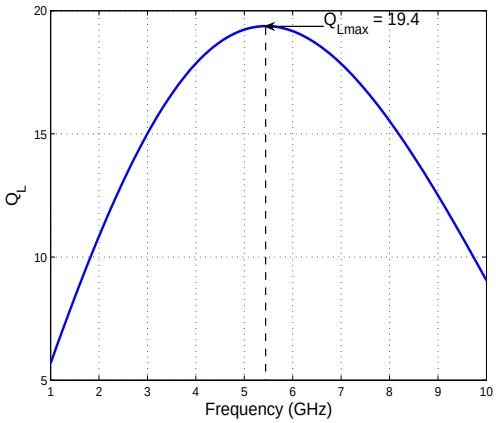



**Fig. 3.29:** $Q_L$ across frequency

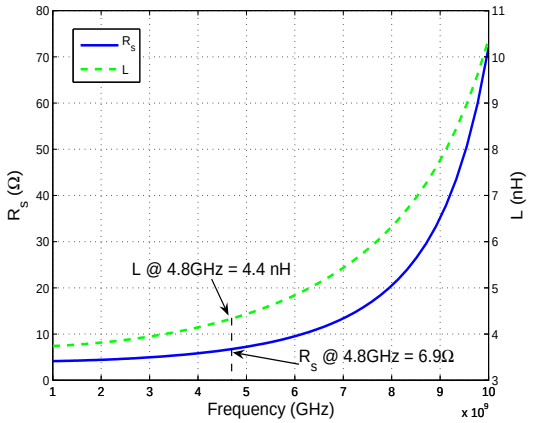



**Fig. 3.30:** $R_s$ and $L$ across frequency

Fig. 3.30 plots the values for $R_s$ (shown on the left y-axis) and $L$ (shown on the right y-axis) obtained for the characterised inductor over the applied frequency sweep, to give

[7] Of course an inductor can be customised to exhibit maximum $Q_L$ at a specified frequency. However this is a highly specialised task generally not offered by standard processes and so can only be pursued where project budget and resources permit.

an idea of the values encountered for these parameters in practice. Values for $R_s$ are plotted by the blue solid line where values for $L$ are plotted by the green trace.

The dimensions of the inductor characterised in Fig. 3.29 were initially chosen at random as the purpose of the characterisation was to find the frequency where $Q_{var}$ is maximum. Fig. 3.29 shows $Q_{var}$ to reach a maximum value of 19.4 for a frequency of $\approx$ 5.5GHz. As this particular inductor was used in the final VCO of this thesis, Fig. 3.29 led to the decision to operate it (and hence the final PLL) at a centre frequency of 4.8GHz. This frequency achieves a high $Q_L$ of 19 and can be divided by 2 to make the final PLL applicable to the highly popular 2.4GHz - 2.5GHz unlicensed industrial, scientific and medical (ISM) frequency bands occupied by standards such as Wi-Fi (IEEE 802.11b/g/n) and Bluetooth. The corresponding values for $R_s$ and $L$ at this frequency are shown in Fig. 3.30 to be 6.9$\Omega$ and 4.4nH respectively.

Once the optimum centre frequency of the VCO has been selected, the dimensions of it can then be optimised according to the previous discussions to further improve $Q_L$ (i.e. limit the widths of the metal conductors to reduce skin effect and optimise $L$ to achieve a large (but practical) $L/C$ ratio).[8] In practice, such optimisation was achieved by simulating a spiral hollow inductor in UMCs 90nm CMOS process at 4.8GHz. By sweeping the widths of the metal conductors (w), spacing between the metal conductors (s), number of metal turns (nt) and outer diameter (od) between their maximum and minimum values, a maximum $Q_L$ of 19.4 was found to be obtainable with the following dimensions:

| w ($\mu$m) | s ($\mu$m) | id ($\mu$m) | nt |
|---|---|---|---|
| 3.5 | 2.9 | 136 | 5 |

**Table 3.3:** Optimum dimensions for spiral inductor in UMCs 90nm process

## 3.6 VCO Phase Noise

The importance of low noise PLL output signals (particularly for wireless communications systems) was discussed in chapter 1 and section 2.8. As the VCO is directly responsible for generating the PLL output signal, this places extreme significance on the design of VCOs with low phase noise performance. In section 2.8.2 phase noise from the VCO was shown to be attenuated by increasing the PLL loop bandwidth ($K$). However, as this approach comes at the cost of the various issues discussed in section 2.8.3, a more attractive approach is to reduce phase noise from the VCO itself. To do this however, phase noise must be defined and its behaviour in a VCO accurately modelled so as to provide meaningful insights into how it can be reduced.

[8] The reader interested in a more graphical approach to the selection of $L$ is referred to [45].

### 3.6.1 Definition of Phase Noise

In Fig. 2.28, phase noise was shown to produce 'skirts' in the frequency spectrum centred around the carrier frequency ($\omega_c$). As such, phase noise is generally defined at a frequency offset ($\Delta\omega$) from $\omega_c$ as follows:

$$L(\Delta\omega) = 10 \cdot \log \left[ \frac{S(\omega_c + \Delta\ \omega)}{\int_{-\infty}^{+\infty} S(\omega) d\omega} \right] \tag{3.26}$$

where $L(\Delta\omega)$ represents the phase noise at an offset $\Delta\omega$ from $\omega_c$ and $S(\omega)$ represents the power spectral density (PSD) of the output signal i.e. the power of the output signal at frequency $\omega$. The factor $10 \cdot \log$ is included as phase noise is generally specified in decibels, specifically decibels from the carrier frequency ($\omega_c$) per hertz (dBc/Hz). As the 'skirts' are symmetrical around $\omega_c$ they are generally quoted with respect to one side of the frequency spectrum, commonly termed the single-sideband (SSB) phase noise.

### 3.6.2 Modelling of VCO Phase Noise

With phase noise mathematically defined in general, we now seek to describe its behaviour in a VCO. In addition to describing phase noise behaviour in a VCO, the resulting model should be practical and intuitive so as to provide meaningful insights into how phase noise in a VCO can be reduced.

A comprehensive model for phase noise in a VCO was developed by Hajimiri and Lee in [46]. However as the resulting model has practical limitations and is not as intuitive as other models, it was not adopted by this thesis. A second model describing phase noise behaviour in a ring VCO was developed by Razavi in [25]. However, as such oscillators are not employed in this thesis (see section 3.1), this model was also not adopted. A third model was proposed by Leeson in [47] where he heuristically derived an LTI model describing VCO phase noise behaviour. Although derived without formal proof, this model has maintained reasonable accuracy up to and including present day VCO designs. The most attractive feature of this model is that it is intuitive and provides meaningful insights into how phase noise in a VCO can be reduced. As such it is the model adopted by this thesis which predicts the following SSB behaviour for $L(\Delta\omega)$:

$$L(\Delta\omega) = 10 \cdot \log \left\{ \frac{2FkT}{P_s} \left[ 1 + \left( \frac{\omega_o}{2Q_{tank}\Delta\omega} \right)^2 \right] \cdot \left( 1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega} \right) \right\} \tag{3.27}$$

In (3.27), $P_s$ represents the power of output signal and $\omega_o$ represents the oscillation frequency of the VCO defined in (3.3). Temperature is then represented by $T$, $k = 1.38$ x $10^{-23} J/K$ is the Boltzmann constant and $\Delta\omega_{1/f^3}$ is a specific frequency explained later. The parameter $F$ in (3.27) is the "effective noise figure" which lumps all the excess noise in and around the VCO into one factor.

Splitting up the terms of (3.27) show it to predict VCO phase noise behaviour to occur in three distinct regions shown in Fig. 3.31.

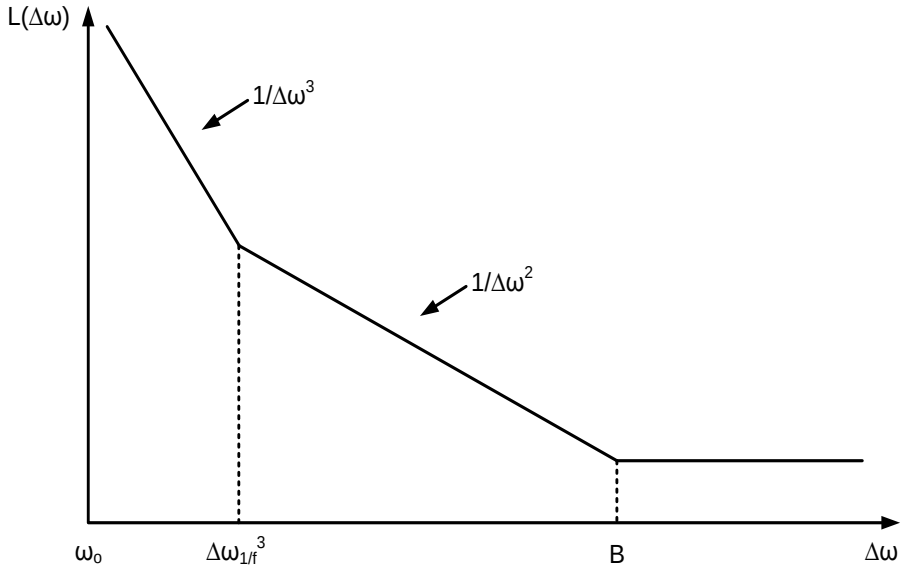



**Fig. 3.31:** SSB phase noise behaviour for a VCO predicted by Leeson's model

As shown in Figs. 3.4 and 3.6, the LC-tank exhibits a bandpass characteristic.[9] The cut-off frequency for this characteristic is shown as B in Fig. 3.31, defined as follows:

$$B = \frac{\omega_o}{2Q_{tank}} \tag{3.28}$$

Moving from right to left in Fig. 3.31, we see a flat region to occur for $\Delta\omega > B$ which is predicted by the following term in (3.27):

$$L(\Delta\omega) = 10 \cdot \log\left\{\frac{2F_1kT}{P_s}\right\} \tag{3.29}$$

This region occurs due to noise at offset frequencies outside the bandwidth of the tank which, due to its frequency selective nature, strongly suppresses any frequency modulation from occurring. As such, the phase noise in this region follows the flat white spectrum of thermal noise whose sources are due to various background noise sources such as that from measurement systems, output buffers, surrounding circuitry, general atmospheric noise or even possibly echoes of the Big Bang [24]! This flat spectrum is commonly termed the noise floor where its excess noise is accounted for by the excess noise factor specific to the region, $F_1$ in (3.29).

Moving closer in towards $\omega_o$ for $1/\Delta\omega_{1/f^3} \leq \Delta\omega \leq B$, we encounter a second region

[9] All VCOs exhibits this band-pass characteristic and so the proceeding discussions do not pertain only to LC-tank VCOs.

where $L(\Delta\omega)$ is dependant on frequency and rolls-off at a rate $1/\Delta\omega^2$ above the noise floor. As such, this region is commonly termed the $1/f^2$ region of phase noise whose behaviour above the noise floor is predicted by the following term in (3.27):

$$L(\Delta\omega) = 10 \cdot \log \left\{ \frac{2F_2kT}{P_s} \left( \frac{\omega_o}{2Q_{tank}\Delta\omega} \right)^2 \right\} \tag{3.30}$$

Since the noise predicted by (3.30) occurs at offset frequencies below the cut-off frequency of the tanks bandwidth, its effect on output frequency is no longer strongly attenuated by the bandwidth of the tank. This leads to phase noise on the output signal which rolls off at a rate of $1/\Delta\omega^2$ as predicted by (3.30). The noise factor describing excess thermal noise in a VCO is then denoted as $F_2$ in (3.30). In [48], $F_2$ was shown for a VCO employing MOSFET biasing and cross-coupled differential transistors to be:

$$F_2 = 1 + \frac{4\gamma I_{VCO} R_p}{\pi V_o} + \gamma \frac{4}{9} g_m R_p \tag{3.31}$$

Equation (3.31) shows $F_2$ to account for thermal noise contributions from the active elements (i.e. the MOSFETs) of a VCO. Omitting it would result in thermal noise contributions only from the tank being accounted for (as indicated by setting the first term in the expression to 1). The second term in (3.31) describes thermal noise contributions from the differential cross-coupled MOSFET pair where the VCO biasing current and output signal amplitude are represented by $I_{VCO}$ and $V_o$ respectively. The third term in (3.31) then describes thermal noise contributions from the biasing MOSFETs. The co-efficient $\gamma$, found in both the second and third terms, is the noise factor for a single MOSFET which is approximately equal to 2/3 for long-channel MOSFETs.[10] As will be seen in section 3.7 valuable insight into the different regions of operation for a VCO can be explained by (3.31).

Moving closer in again towards $\omega_o$ for $\Delta\omega \leq 1/\Delta\omega_{1/f^3}$, we encounter a third and final region where $L(\Delta\omega)$ is once again seen to be dependant on frequency, but this time with a roll-off rate of $1/\Delta\omega^3$ above the noise floor. As such, this region is commonly termed the $1/f^3$ region of phase noise whose behaviour above the noise floor is predicted by the following term in (3.27):

$$L(\Delta\omega) = 10 \cdot \log \left\{ \frac{2F_2kT}{P_s} \left[ \left( \frac{\omega_o}{2Q_{tank}\Delta\omega} \right)^2 \right] \cdot \left( \frac{\Delta\omega_{1/f^3}}{\Delta\omega} \right) \right\} \tag{3.32}$$

The increased roll-off rate in the third region is due to flicker noise within the active components (i.e. the transistors) of the VCO. Flicker noise is a strange phenomenon[11]

[10] $\gamma$ may need to be increased for short-channel MOSFETs [49].

[11] There exists various models seeking to described the origin of flicker noise in electronic devices ([50], [51]) where at present no unified theory has been agreed on.

which occurs most predominantly at low frequencies. As such it exhibits a noise spectrum which rolls-off at a rate of $1/f$ leading to it being commonly termed $1/f$ noise. Therefore at low frequencies, flicker noise forces the slope of the close-in phase noise behaviour of a VCO (in the third region above the noise floor) to increase by a factor of $1/f$, resulting in the increased roll-off rate of $1/\Delta\omega^3$ as predicted by (3.32). The boundary frequency between the $1/f^3$ and $1/f^2$ regions is then represented by $\Delta\omega_{1/f^3}$ where it is commonly termed the flicker noise corner frequency.

Leeson's model in (3.27) can thus be viewed as a composite expression of the terms in (3.29), (3.30) and (3.32) with the individual noise excess factors ($F_1$ and $F_2$) being lumped into one factor ($F$). In practice it is generally quite difficult to calculate $F$ (and $\Delta\omega_{1/f^3}$) a priori, and so Leeson's model is rarely used to compute values for phase noise under specific conditions (this task is left up to simulation). However as previously mentioned, the most attractive feature of the model (and the reason for its popularity) is that it intuitively describes phase noise behaviour in a VCO in a way which provides meaningful insights into how it can be reduced. The main insights can be taken from (3.30) by replacing $P_s$ with its equivalent expression $V_o^2/R_s$ to give the following:

$$L(\Delta\omega) = 10 \cdot \log \left\{ \frac{2F_2 kTR_s}{V_o^2} \left( \frac{\omega_o}{2Q_{tank}\Delta\omega} \right)^2 \right\} \tag{3.33}$$

Analysis of (3.33) thus reveals the following:

1. $L(\Delta\omega) \propto 1/Q_{tank}^2$: Increasing $Q_{tank}$ significantly reduces phase noise in a VCO. From (3.7) and section 3.5 this corresponds to optimising the inductor such that it achieves as high a quality factor ($Q_L$) as possible.

2. $L(\Delta\omega) \propto 1/V_o^2$: Increasing the amplitude of the output signal significantly reduces phase noise in a VCO. This however only applies up to a certain point after which phase noise starts to degrade (discussed further in section 3.7).

3. $L(\Delta\omega) \propto F_2$: Decreasing the thermal noise contributions from the active VCO components themselves reduces phase noise in a VCO. In [52] it was shown that the third term in (3.31) can be significantly reduced by decreasing the widths of the cross-coupled differential MOSFETs.

4. $L(\Delta\omega) \propto R_s$: Decreasing $R_s$ increases $Q_L$ and so it only holds to reason that a reduction in phase noise will also be achieved.

5. $L(\Delta\omega) \propto \omega_o^2$: This may or may not provide a means of reducing VCO phase noise but it is worth noting that the larger $\omega_o$, the lower the phase noise. As a result, achieving low phase noise operation for high frequency applications becomes very challenging.

### 3.6.3 Limitations of Leeson's Model and the Reduction of Flicker Noise

The primary limitation of Leeson's model is that it does not provide any meaningful insights into flicker noise behaviour in a VCO and how it can be reduced. This is quite concerning since flicker noise is a major issue for modern wireless applications employing narrow channel spacings (*for example:* GSM standard employs channel spacings of only 200kHz). Since it degrades the close-in phase noise performance of a VCO, flicker noise can lead to cross-channel interference between closely separated channels and so should be strongly suppressed for such applications. To alleviate this, the time-varying model developed in [46] offers some insight into flicker noise dependencies within a VCO. In particular it shows flicker noise to be dependant on the symmetry of the output waveform and so can be reduced by improving this symmetry. One interesting result following from this is that the flicker noise corner frequency in a VCO ($\Delta\omega_{1/f^3}$) is not equal to the device corner frequency where it is shown to be less by a specific factor. The design implications of this are that by improving output waveform symmetry, device flicker noise can be compensated for. Since LC-tank VCOs generally offer more symmetrical output waveforms than ring VCOs, this contributes to their superior phase noise performance.

Further insight into flicker noise behaviour in a VCO was reported in [27] which showed the biasing transistors to be a significant contributor to the overall flicker noise of a VCO. In particular it showed such bias flicker noise to upconvert to phase noise via CMM-FM and AM-FM mechanisms stimulated by the varactor non-linearity. Therefore, a direct method to reduce such flicker noise effects in a VCO is by reducing varactor non-linearity, which for the UMCs 90nm CMOS process was seen in section 3.4 to be achievable by employing diode varactors over MOS varactors. As this upconversion mechanism is particularly sensitive to VCO gain ($K_{VCO}$), the low resulting $K_{VCO}$ values from diode varactors further reduces its end effect.

There are many more publications claiming various techniques to reduce flicker noise, some of which can be found to contradict each other. As such the subject of flicker noise reduction in a VCO is a vast topic still very much under active research whose in-depth treatment is beyond the scope of this thesis. Nevertheless, some simple guidelines were followed to reduce the effect of flicker noise in the final VCO of this thesis, as will be seen in section 3.8.

## 3.7 Current Flow in a VCO

Excellent insight can be gained into the different regions of VCO operation by analysing its current flow during steady state. This is illustrated in Fig. 3.32 for a single-ended tuned VCO architecture with PMOS current sink ($M_1$, $M_2$) and NMOS cross-coupled differential pair ($M_3$, $M_4$).

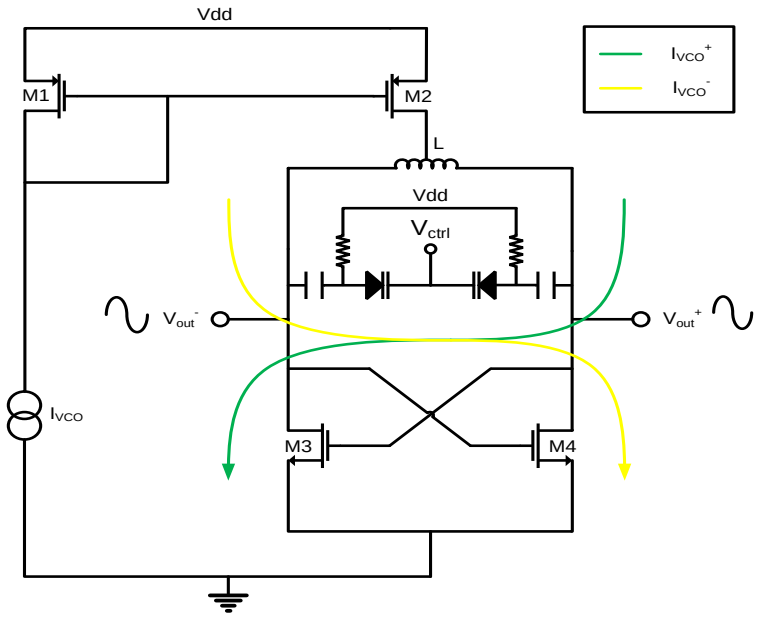



**Fig. 3.32:** Current flow in a VCO during steady state

From Fig. 3.32, the VCO current ($I_{VCO}$) can be assumed to be periodically commutated between the left ($I^{-}_{VCO}$) and right ($I^{+}_{VCO}$) sides of the tank. This occurs due to the switching nature of the cross-coupled differential pair as summarised by Table. 4.8.

| $V^{+}_{out}$ | $V^{-}_{out}$ | M3 | M4 | $I_{VCO}$ |
|---|---|---|---|---|
| $> V_{DC}$ | $< V_{DC}$ | ON | $\approx$ OFF | $I^{+}_{VCO}$ |
| $< V_{DC}$ | $> V_{DC}$ | $\approx$ OFF | ON | $I^{-}_{VCO}$ |

**Table 3.4:** Operation table for steady state current flow in a VCO

At low frequencies where switching times of $M_3$ and $M_4$ are negligible, the current waveform injected into each side of the tank can be assumed a square wave [48] of frequency $\omega_o$. As all the odd harmonics (3rd, 5th, etc) of this square wave will be strongly attenuated by the tanks band-pass characteristic (see section 3.2 and (3.28)), it is sufficiently described by the fundamental component of its Fourier representation. Assuming for the moment that the voltage across the tank (which equals the output signal amplitude $V_o$) is not limited by the available headroom from the supply voltage, it can at low frequencies be approximated as follows [48]:

$$V_o \approx \frac{4}{\pi} I_{VCO} R_p \tag{3.34}$$

However at high frequencies, where the finite switching times of $M_3$ and $M_4$ do not become negligible, the injected current into each side of the tank can be better

approximated by a sine wave [53]. Once again, assuming for the moment that $V_o$ is not limited by the available headroom from the supply voltage, it can at high frequencies be approximated as follows [53]:

$$V_o \approx I_{VCO} R_p \tag{3.35}$$

Both (3.34) and (3.35) assumed $V_o$ was not limited by the available headroom from the supply voltage. These showed it to increase linearly with $I_{VCO}$ and hence become limited only by $I_{VCO}$. Operation within this region is thus defined as the current-limited ($I$-limited) region where any increases in $I_{VCO}$ result in direct increases in $V_o$. This increase cannot continue indefinitely however as eventually $V_o$ will become limited by the available headroom from the supply voltage. Once this occurs, (3.34) and (3.35) no longer apply as $V_o$ is now pegged at some maximum value. Operation within this region is thus defined as the voltage-limited ($V$-limited) region where any further increases in $I_{VCO}$ render no change in $V_o$.

These two regions are extremely important in terms of low phase noise and low power operation of a VCO. In (3.33), phase noise within a VCO was shown to be inversely proportional to the square of the output signal amplitude (i.e. $L(\Delta\omega) \propto 1/V_o^2$) suggesting that $V_o$ should be made as large as possible to minimise phase noise. From (3.34) and (3.35), this suggests that $I_{VCO}$ should be increased until $V_o$ reaches its maximum value, in other words until it becomes limited by the available headroom from the supply voltage. This statement alone suggests that in the interest of minimising phase noise, $I_{VCO}$ should be increased until the VCO is operating in the $V$-limited region. Whilst it is true to state that increasing $V_o$ through increasing $I_{VCO}$ in the $I$-limited region reduces phase noise, this reduction does not continue into the $V$-limited region. In fact as shown in [54], phase noise will be at its minimum at the boundary between the $I$- and $V$-limited regions and then start to degrade as $I_{VCO}$ is increased further. The reason for this can be seen through close analysis of the expression for the excess noise factor due to thermal noise contributions from the active elements (i.e. MOSFETs) of a VCO ($F_2$) in (3.31) [48]. In the $I$-limited region, any increases in $I_{VCO}$ cause $V_o$ to grow according to (3.34) and (3.35). Substituting these equations separately into (3.31) show the second term of $F_2$ to reduce to $\gamma$ and $4\gamma/\pi$ for low and high frequency operation respectively. Therefore, assuming $g_m R_p$ is held constant, $F_2$ remains constant in the $I$-limited region and so by virtue of (3.33), allows phase noise to reduce by $1/V_o^2$. In the $V$-limited region however, where $V_o$ becomes pegged at some maximum value, the second term of $F_2$ starts to increase linearly with $I_{VCO}$. In other words, in the $V$-limited region thermal noise contributions from the cross-coupled differential pair starts to increase. Since $V_o$ no longer increases with increasing $I_{VCO}$, with this increase in $F_2$ comes a hand in hand increase in phase noise.

The effects of the previous discussion can be clearly seen in Fig. 3.33 which plots the

phase noise of a VCO for different values of $I_{VCO}$. The VCO used for the measurements in Fig. 3.33 was designed using UMCs 90nm CMOS process where its architecture was based on that shown in Fig. 3.32. For the plot to achieve a fair representation of phase noise behaviour due to operation in the $I$- and $V$-limited regions, various efforts were required to reduce insignificant dependencies pertaining to the current discussion. Firstly, all phase noise measurements were carried out at the same offset frequency ($\Delta\omega = 100$kHz) to eliminate the dependency on $\Delta\omega$ in (3.33). As such, phase noise on the plot is denoted as $PN$ instead of $L(\Delta\omega)$ since for this plot, it no longer depends on $\Delta\omega$. Secondly, all $PN$ measurements were made at the same frequency (4.8GHz) to eliminate the dependency on $\omega_o$, $Q_{tank}$ and $R_s$ in (3.33). This was achieved in practice by slightly adjusting the capacitance within the tank for each bias current setting, thereby maintaining a constant oscillation frequency. Lastly, the DC bias level ($V_{DC}$) for each measurement was held constant to reduce any dependencies due to small signal effects.

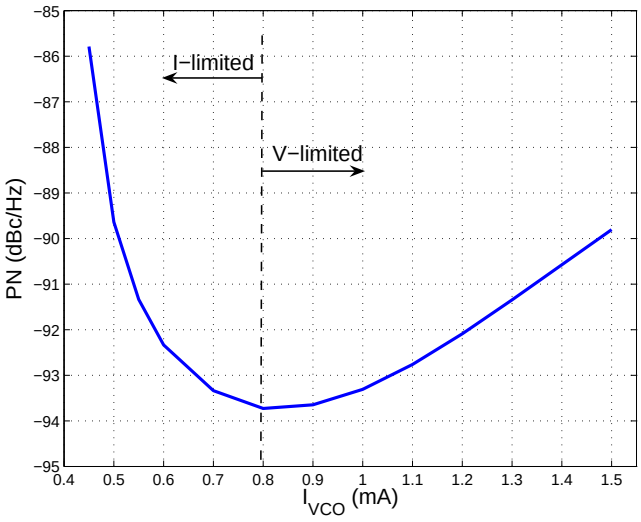



**Fig. 3.33:** VCO PN behaviour in the $I$- and $V$-limited regions of operation

The plot of Fig. 3.33 clearly shows the VCO to operate in the $I$-limited region for $I_{VCO} < 800\mu A$ with its phase noise decreasing as $I_{VCO}$ reaches $800\mu A$, at which point $PN$ is at its minimum value. For $I_{VCO} > 800\mu A$ then, the VCO enters the $V$-limited region where thermal noise contributions from the differential cross-coupled pair cause phase noise to increase again. Therefore in Fig. 3.33, it is obvious to see the boundary between the $I$- and $V$-limited regions occurs for $I_{VCO} = 800\mu A$ which, from the perspective of low phase noise operation, becomes the optimal bias current setting for the simulated VCO.

It should be noted that setting $I_{VCO}$ at the boundary point between the $I$- and $V$-limited regions is also in the interest of low power operation since increasing $I_{VCO}$ beyond the boundary point constitutes a waste in power with no beneficial return.

## 3.8 VCO Architectures

There are various architectures to implement a VCO, all of which differentiate by the configuration of the active elements around the LC-tank. Four of the main choices are shown in Figs. 3.34 → 3.37.

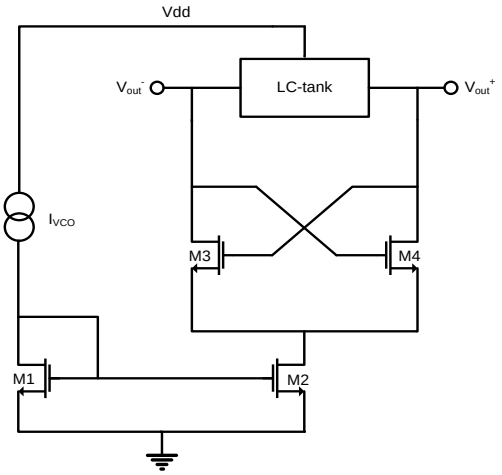



**Fig. 3.34:** All NMOS topology

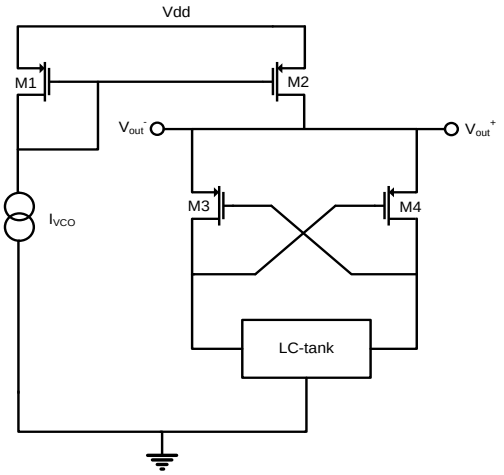



**Fig. 3.35:** All PMOS topology

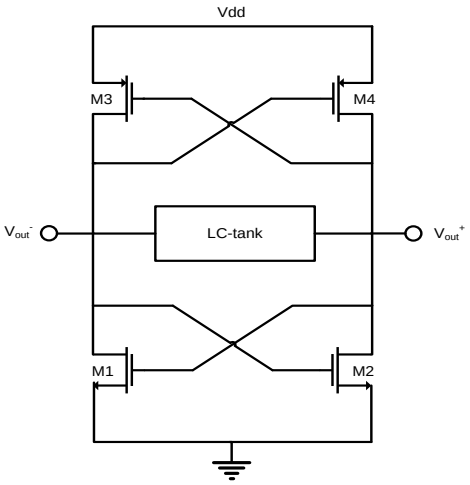



**Fig. 3.36:** Double cross-couple topology

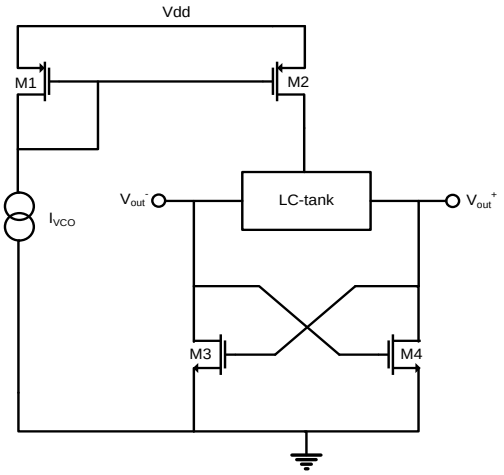



**Fig. 3.37:** Hybrid topology

In Fig. 3.34 all the active elements are realised with NMOS devices [55]. This architecture enables output voltage swings to grow to twice the power supply voltage, which from (3.33) dramatically improves phase noise performance of the VCO. However, from a reliability point of view such large output voltage swings are highly undesirable as they are directly seen at the gates of the cross-coupled differential MOSFET pair ($M_1$, $M_2$). Large voltages experienced at the gates of a MOSFET will overtime degrade its gate oxide material (break molecular bonds within the oxide leading to trapped charges and hence

hot-electron tunnelling) leading to reduced performance or in extreme cases, all out device failure (oxide breakdown [56]). In addition, the all NMOS topology results in the LC-tank being placed at the Vdd line thereby offering no isolation from noise on the Vdd line.

Such issues are not encountered by switching to an all PMOS architecture (shown in Fig. 3.35) which results in the tank being placed at Vss [57]. This provides excellent isolation from supply noise where [52] claims a 20dB improvement in output phase noise over the architecture of Fig. 3.34. Output voltage swings are then limited by this architecture to $<$ Vdd, for which gate oxide reliability over a specified time will always be guaranteed by the process reliability engineer. In addition, the use of PMOS devices may result in reduced flicker noise over NMOS devices, attributed to their buried channel behaviour [58].[12]

The bias sink and source of Figs. 3.34 and 3.35 are implemented as NMOS and PMOS devices respectively. In order to make them robust against channel length modulation effects, these devices will typically employ large dimensions (to increase output conductance's) which will somewhat reduce their flicker noise [29]. Nevertheless their flicker noise will still be prevalent with [27] claiming it to be a dominant source of phase noise degradation. This can be addressed with filtering [60], however at the cost of an additional inductor thereby dramatically increasing silicon area requirements. It can also be addressed by operating the bias source or sink in the triode-region [61], however at the cost of requiring a voltage regulator and amplitude control scheme thereby increasing design complexity, time, cost, resources and overall power consumption of the end circuit. Such noise can be most effectively eliminated by simply eliminating the bias source or sink altogether [62]. This gives the doubled cross-coupled architecture of Fig. 3.36 which employs both PMOS and NMOS differential cross-coupled pairs. Another advantage of this architecture is that it halves the required current necessary to sustain oscillation as per (3.20), leading to a reduction in power consumption over the other architectures by a factor of two. However, the primary disadvantage of this architecture is that by removing the biasing element of a VCO we can thus no longer guarantee its DC bias level ($V_{DC}$) over PVT variation. This issue could be addressed by adding a bias source or sink onto the circuit [53], but at the cost of re-introducing the problem of bias flicker noise. In addition, the resulting architecture would actually consume more voltage headroom (by one overdrive voltage $V_{ov}$, see see section 4.2.2) than the previous architectures thus making it unsuited to modern technologies with limited supply voltages.

The final architecture shown in Fig. 3.37 is simply a hybrid of the architectures of Figs. 3.34 and 3.35 [35] and so exhibits a mixture of their various advantages and disadvantages.

[12] It should be noted that superior flicker noise performance of PMOS over NMOS has not been consistently observed over all processes [59].

From the point of view of low phase noise and power operation, the architecture of Fig. 3.36 is highly desirable. However, as it is not PVT robust it is simply not practical. From the point of view of reliability the architecture of Fig. 3.34 is non-optimal. This leaves the architectures of Fig. 3.35 and 3.37, which for the final VCO of this thesis, the architecture of Fig. 3.37 was chosen.

One interesting modification to the chosen architecture is to place a capacitor ($C$) at the drain of $M_2$ as shown in Fig. 3.38. The effect of this seems to slightly suppress flicker noise upconverting to phase noise via the mechanisms described in [27]. This is shown in Fig. 3.39 which plots the simulated phase noise of a VCO oscillating at 4.8GHz for the cases with and without the additional capacitor. The VCO was designed using the chosen architecture in UMCs 90nm CMOS process, where a metal-insulator-metal (MIM) capacitor was inserted for $C$. The widths and lengths for this capacitor were set to 20$\mu$m (larger dimensions resulted in insignificant improvements) to achieve a total capacitance of $\approx$ 0.8pF. Phase noise ($PN$) measurements were taken at 10kHz offset from the carrier frequency for $V_{ctrl} = 0.5$V. This ensured the varactors were biased at the centre of their tuning curves, which from Fig. 3.23 achieves the largest slope and hence upconversion of flicker noise [35]. Fig. 3.39 shows this simple step to reduce close-in phase noise by 1dB representing a phase noise improvement of $\approx 20\%$ over the case without $C$.

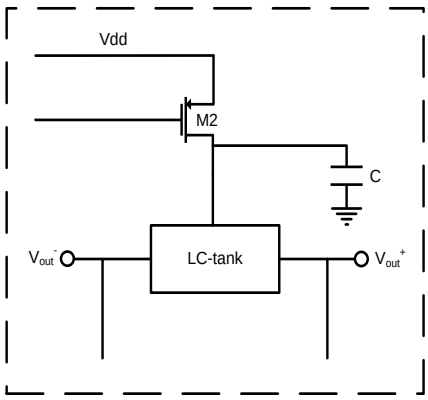



**Fig. 3.38:** Placement of additional capacitor

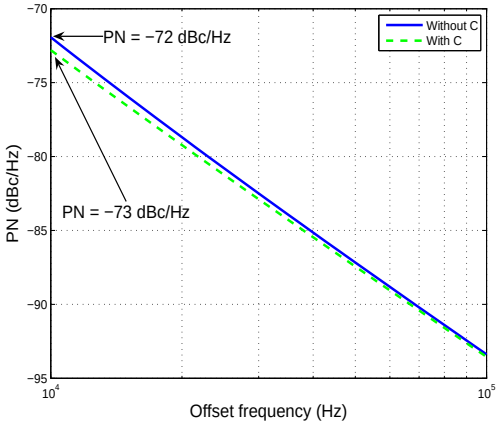



**Fig. 3.39:** Simulated phase noise

## 3.9 VCO Issues Addressed in this Thesis

In order to ensure the specified output frequency range is reliably covered over PVT variation, and to enable multi-band (or standard) operation in wireless communication systems, modern day VCOs are required to have a sufficiently large tuning range (typically termed wideband VCOs). This, together with the reduced supply voltages that accompany low technology nodes, imply a high VCO gain, $K_{VCO}$ defined in (2.13). This is concerning

as the larger the $K_{VCO}$ value, the more degraded the VCO (and hence PLL) phase noise performance (shown in sections 4.2.2 and 4.5.4). As a result, achieving low noise performance whilst maintaining large tuning ranges is a major issue for modern day VCO designs. This is addressed by the architectures introduced in chapters 4 and 5 which together simultaneously achieve requirements for low phase noise and large tuning ranges.

In section 3.4, varactors were shown to exhibit a non-linear C(V) characteristic which results in a non-linear $K_{VCO}$ that varies across $V_{ctrl}$. It should be clear from the discussions in sections 2.7.4, 3.4.3 and 3.6.3 that $K_{VCO}$ variation is a major issue for VCOs and in fact represents one of the primary challenges facing VCO design today. Furthermore, with the architecture introduced in chapter 5 to simultaneously achieve low phase noise with large tuning ranges, comes a new source of $K_{VCO}$ variation. As this new source severely increases $K_{VCO}$ variation it must be addressed, with the novel architecture presented in chapter 5 effectively eliminating its occurrence.

Finally, all the VCOs thus far discussed exhibited single-ended tuning. As will be shown in chapter 4, differential CPs together with differential LFs offer superior performance over their single-ended counterparts. However, in order to control a VCO with single-ended tuning, the differential outputs of such a CP/LF combination must first be converted to single-ended form via a differential to single-ended converter (i.e. a differential amplifier) [13], [21]. However, as this approach requires additional components it increases design complexity, cost, time and resources. More importantly, it increases power consumption and may degrade noise performance of the PLL. This issue is elegantly addressed in chapter 4 which introduces a VCO architecture directly compatible with a differential CP/LF.

## 3.10 Summary

This chapter was written with three goals in mind. The first goal was to explain the fundamentals of oscillation, the design of a VCO and most importantly, various justifications to choices made for the final VCO of this thesis. The physical causes for oscillation in an LC-tank were explained in section 3.1 where energy transfer between the passive components was shown to be responsible for the generation of an output signal oscillating at a specified frequency. The dampening of this output signal was then attributed to losses primarily within the inductor of the tank, which introduced one of the most important design parameters pertaining to VCO design - the quality factor of the tank ($Q_{tank}$). The design of an oscillator to overcome these losses such that constant oscillation is sustained was then shown in section 3.3, which introduced another extremely important design parameter to VCO design (inextricably linked to $Q_{tank}$) - parallel resistance of the tank ($R_p$). Tuning in a VCO was shown in section 3.4 to be achievable through two

physically different devices. Both devices were described and analysed which led to the justification of one device over the other for the final VCO of this thesis. The importance of the inductor and its primary loss mechanisms were then described in section 3.5 which justified the inductor choice and operation frequency of the final PLL for this thesis. In section 3.8, various VCO architectures were discussed where the final architecture for the VCO of this thesis was justified.

The second goal of this chapter was then to describe the general behaviour of a VCO and in particular the behaviour of one of the most influential design criterion for a VCO - low phase noise operation. Phase noise in a VCO was modelled in section 3.6 which showed its various dependencies, thereby providing insights pertaining to its reduction. In particular, this showed the importance of $Q_{tank}$ and the output signal swing to low phase noise operation, with the limitations of the output signal swing being explained in section 3.7.

Finally the third goal of this chapter was to recognise the limitations of the VCO. This was achieved through the various discussions throughout this chapter (and some from the proceeding chapter) which were cumulated in section 3.9 where the issues dealt with in forthcoming chapters of this thesis were explained.

Upon reading this chapter, the reader should be aware of the fundamentals of VCO operation, its primary design parameters and most importantly its limitations which will be addressed in the coming chapters. In addition, the reader should be confident of various choices made for the final VCO of the thesis.

# CHAPTER 4

# Fully Differential PLLs

The core block diagram for a PLL was given in Fig. 2.1 where it was shown to consist of five main blocks: PD, CP, LF, VCO and feedback divider. Of these, the CP, LF and VCO are generally considered the analog blocks of a PLL with the PD and feedback divider being considered the digital blocks. The conversion of a PLL to fully differential operation centers around the analog blocks. For example, in the earliest PLLs both the CP and LF strictly employed single-ended operation (i.e. exhibited a single output line) where the VCO employed single-ended tuning (i.e. exhibited one control line $V_{ctrl}$). However, by converting the CP and LF to differential operation and the VCO to being differentially tuned, a fully differential PLL can be realised which exhibits numerous advantages over its single-ended counterpart.

The advantages of a fully differential PLL will be shown throughout this chapter where they will be seen to make them an increasingly attractive alternative over single-ended PLLs for shrinking technologies and low noise operation.

## 4.1 Differential Operation

Single-ended circuit blocks exhibit one output whereas differential circuit blocks exhibit two which (ideally) are equal and opposite in magnitude. This is illustrated in Fig. 4.1:

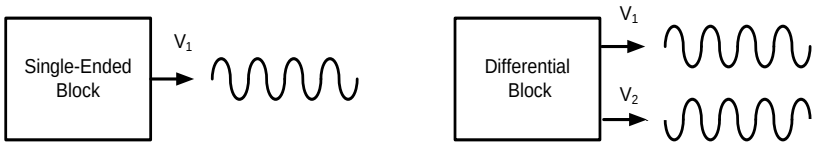



**Fig. 4.1:** Illustration of single-ended and differential-ended outputs

The voltage output of a circuit block is always measured with respect to a reference potential and so can be rigorously defined as:

$$V_{out} = V_{measured} - V_{ref} \tag{4.1}$$

where output, measured and reference voltages are represented by $V_{out}$, $V_{measured}$ and $V_{ref}$ respectively.

The output of a single-ended block ($V_1$ in Fig. 4.1) is usually measured with respect to ground (0V), and so from (4.1) can be defined as:

$$\begin{aligned} V_{out} &= V_1 - 0 \\ &= V_1 \end{aligned} \tag{4.2}$$

The outputs of a differential block ($V_1$ and $V_2$ in Fig. 4.1), however are measured with reference to a common-mode voltage ($V_{cm}$), defined as:

$$V_{cm} = \frac{V_{DC_1} + V_{DC_2}}{2} \tag{4.3}$$

where the DC bias levels for $V_1$ and $V_2$ are represented as $V_{DC_1}$ and $V_{DC_2}$ respectively.

The output of a differential block (i.e. the differential output) is thus defined as the difference between the two individual outputs, which from (4.1) can be defined as:

$$\begin{aligned} V_{out} &= (V_1 - V_{cm}) - (V_2 - V_{cm}) \\ &= V_1 - V_2 \end{aligned} \tag{4.4}$$

## 4.2 Advantages of Differential Operation

### 4.2.1 Common-Mode Noise Reduction

Common-mode noise was defined in section 2.8.3 as noise which affects all (or a subset of) nodes in a system equally. As this noise source becomes increasingly significant with continual technology downsizing where device integration increases, the reduction of it (or its effects) becomes increasingly necessary to realising low noise performance. For example, wireless transceivers (see chapter 1) are commonly embedded on densely populated system-on-chip (SOC) integrated circuits (ICs) which are often fabricated using low technology nodes to enable a high integration of digital circuit blocks. Given that the standards which the wireless transceivers must typically comply with often impose demanding low noise specifications, the reduction of their common-mode noise (or its effects) becomes

absolutely necessary to meeting such specifications.

As stated in section 2.8.3, common-mode noise is often generated by the high frequency switching of digital circuitry which can ac-couple onto nearby lines. On an IC, lines particularly vulnerable to such behaviour are the Vdd and Vss lines common to all devices. Therefore in such cases, one approach to reducing the effects of common mode noise is simply to isolate any noise sensitive circuitry (such as PLLs) from the noisy Vdd and Vss lines. Isolation from the Vdd line is achieved in practice by supplying the noise sensitive circuitry with its own unique supply potential. This however requires a voltage regulator to be implemented thereby increasing design complexity, cost, time, resources and overall power consumption of the end circuit. Isolation from the Vss line is then achieved by embedding the noise sensitive circuitry in its own unique $n$-well using a triple-well process. Disadvantages with this approach arise due to the high manufacturing costs associated with triple-well processes thereby dramatically increasing overall project cost.

One very attractive property of differential operation is that it dramatically reduces the effects of common-mode noise on the Vdd and Vss lines (amongst other lines), without the need for expensive triple well processes or voltage regulators. To see why this is so, suppose the differential block of Fig. 4.1 incurs common-mode noise which affects both outputs equally, hence perturbing them from their nominal values by a voltage $|\Delta v_{cm}|$. Since the differential output is simply the difference between these two outputs (see (4.4)), this common-mode perturbation cancels out as follows:

$$\begin{aligned} V_{out} &= (V_1 + |\Delta v_{cm}|) - (V_2 + |\Delta v_{cm}|) \\ &= V_1 - V_2 \end{aligned} \tag{4.5}$$

The reduction of common-mode noise through differential operation will be shown repeatedly throughout this chapter.

### 4.2.2 Doubled Output Voltage Swing

The output voltage swing of a single-ended block is defined as:

$$V_{swing} = V_{max} - V_{min} \tag{4.6}$$

Following from (4.6) and recalling (4.4), the output voltage swing of a differential block is:

$$\begin{aligned} V_{swing} &= (V_{1_{max}} - V_{2_{min}}) - (V_{1_{min}} - V_{2_{max}}) \\ &= V_{1_{max}} - V_{2_{min}} - V_{1_{min}} + V_{2_{max}} \end{aligned} \tag{4.7}$$

Provided the differential architecture exhibits perfect symmetry, its outputs will be equal in magnitude (i.e. $V_{1_{max}} = V_{2_{max}} = V_{max}$ and $V_{1_{min}} = V_{2_{min}} = V_{min}$). From this it follows that:

$$V_{swing} = 2(V_{max} - V_{min}) \tag{4.8}$$

This is an attractive property for low noise operation as it reduces the effect of noise by increasing signal to noise ratios (SNR). It is an especially attractive property for low technology nodes where the reduction of supply voltages (in order to maintain constant scaling with decreasing device dimensions) severely limits output voltage swings. This can be seen for the single-ended CP illustrated in Fig. 2.6 whose output voltage swing can be shown to be:

$$V_{swing_{cp}} = V_{dd} - 2V_{ov} \tag{4.9}$$

where $V_{ov}$ represents the overdrive voltage of the current source and sink i.e. the minimum drain-source voltage required to maintain the current defining transistors in saturation.

Evident from (4.9) is that the output voltage swing of a single-ended CP scales linearly with Vdd. This reduction is however reduced by halve for a differential CP whose output voltage swing (from (4.8) and (4.9)) follows as:

$$V_{swing_{cp}} = 2(V_{dd} - 2V_{ov}) \tag{4.10}$$

The effect of this doubled output voltage swing is reduced phase noise from the VCO. To see why this is, recalling (2.14) and noting that the CP output voltage swing ($V_{swing_{cp}}$) completely determines the control voltage range for a VCO ($\Delta V_{ctrl}$), the frequency range covered by a VCO can be defined as follows:

$$\begin{aligned} \Delta\omega_{vco} &= K_{VCO}\ \Delta V_{ctrl} \\ &= K_{VCO}\ V_{swing_{cp}} \end{aligned} \tag{4.11}$$

From (4.11) we can see that for a specified tuning range, a doubled output voltage swing from the CP (as per (4.10)) reduces $K_{VCO}$ requirements by half.[1] As $K_{VCO}$ quantifies the gain of a VCO, by its very nature it will translate noise on the VCO control line ($V_{ctrl}$) to phase noise at its output. Therefore a reduction in $K_{VCO}$ by half reduces noise contributions from the $V_{ctrl}$ line by 3dB. As flicker noise effects are sensitive to $K_{VCO}$ (see

[1] Maintaining the same $K_{VCO}$, a doubled output voltage swing from the CP doubles $\Delta\omega_{vco}$, making differential operation also very suitable to wideband VCOs/PLLs necessary to enable multi-band (or standard) operation in wireless communication systems.

section 3.6.3), a reduction in $K_{VCO}$ will also reduce their contributions to output phase noise. This reduction in VCO phase noise will be shown in section 4.5.4.

### 4.2.3 Additional Advantages

In addition to the above advantages, differential operation for a CP achieves a dramatic reduction in static phase error (shown in section 4.3.2), where for LFs implemented on-chip (i.e. fabricated onto silicon), differential operation reduces silicon area requirements of the LF by approximately a factor of two (shown in section 4.4.2).

All these advantages of differential operation and their relevance to PLLs and IC design in general, are thus summarised in Fig. 4.2.

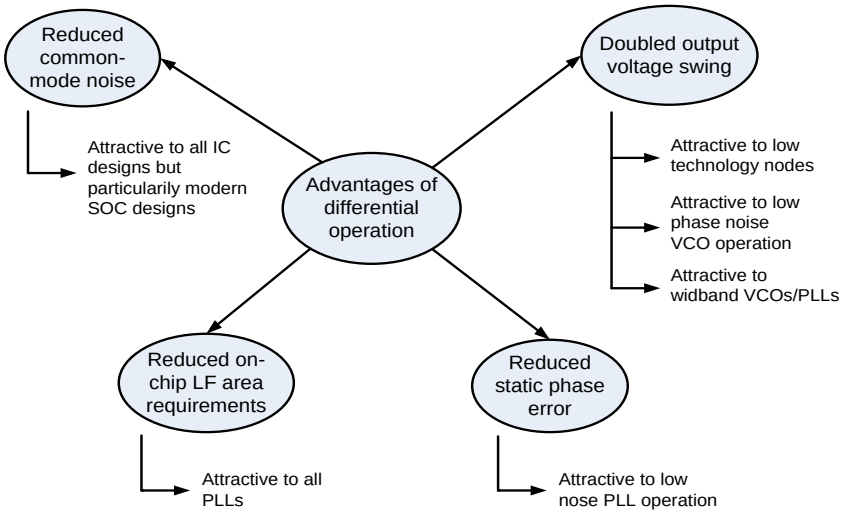



**Fig. 4.2:** Advantages of differential operation

It should be noted however that the advantages of Fig. 4.2 do come at a small cost. This is more complex circuitry and the need for common-mode feedback circuitry (see section 4.3.4). However, these costs are often acceptable in comparison to the benefits gained, where it is the primary goal of this chapter to completely justify the conversion of a conventional PLL to fully differential operation.

## 4.3 Differential Charge-Pump (CP)

The first block of a PLL which will be converted to differential operation in this chapter, is the CP.

### 4.3.1 Basic operation

The differential CP exhibits two outputs which (assuming perfect matching) are always equal and opposite in magnitude (i.e. as one output voltage increases, the other decreases).

An ideal differential CP is illustrated in Fig. 4.3 which shows it to be basically a parallel connection of the two single-ended CPs shown in Fig. 2.6 with differential outputs denoted by $CP^-$ and $CP^+$. As such, it consists of two "UP switches" and associated current sources giving rise to two "UP" networks, and two "DN switches" and associated current sinks giving rise to two "DN networks". The overall operation of the differential CP can thus be summarised in Table 4.1 which is given with reference to the PLL input conditions and CP outputs.

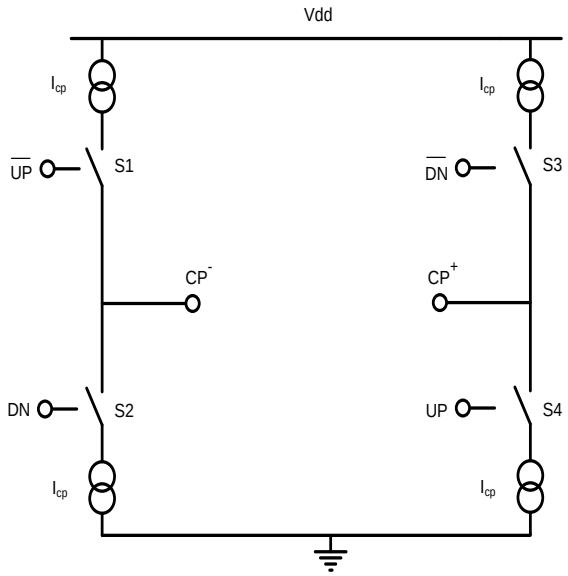



**Fig. 4.3:** Ideal differential CP

| | $UP$ | $DN$ | $\overline{UP}$ | $\overline{DN}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $CP^-$ | $CP^+$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $\phi_{ref} > \phi_{fb}$ | 1 | 0 | 0 | 1 | ON | OFF | OFF | ON | increase | decrease |
| $\phi_{ref} < \phi_{fb}$ | 0 | 1 | 1 | 0 | OFF | ON | ON | OFF | decrease | increase |

**Table 4.1:** Operation table for a differential CP

Table 4.1 shows that when the input reference signal ($\phi_{ref}$) has frequency greater than the feedback signal ($\phi_{fb}$) or phase which leads that of $\phi_{fb}$, the PFD outputs an UP pulse to turn on switches $S1$ and $S4$ and turn off switches $S2$ and $S3$. As a result $CP^-$ and $CP^+$ proportionally increase and decrease respectively. Then for the case where $\phi_{ref} < \phi_{fb}$, $S2$ and $S3$ turn on while $S1$ and $S4$ turn off hence causing $CP^-$ and $CP^+$ to proportionally decrease and increase respectively. The resulting current flow for both these cases is illustrated in Fig. 4.4, where that for $\phi_{ref} > \phi_{fb}$ is shown by the green arrows and that for $\phi_{ref} < \phi_{fb}$ is shown by the yellow arrows.

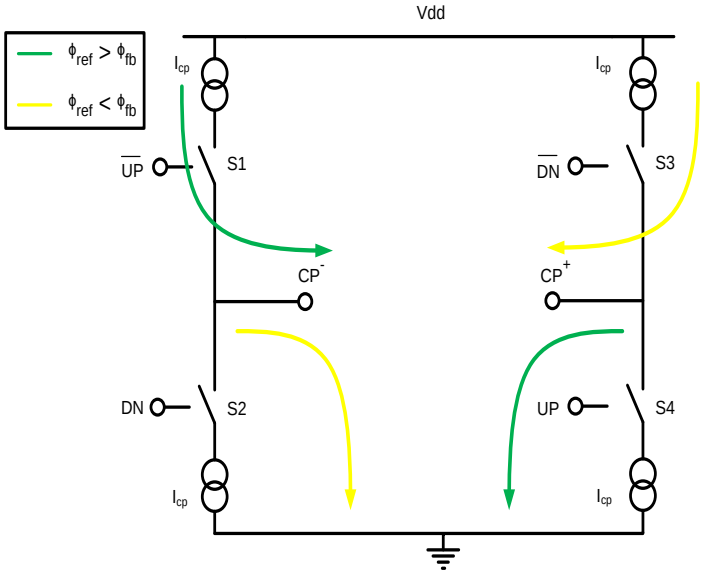



**Fig. 4.4:** Current flow in a differential CP

To realise this behaviour in practice, the ideal switches shown in Figs. 4.3 and 4.4 must be realised using complementary devices as shown in Fig. 4.5. This shows the UP switches to be realised with PMOS devices ($M1$ and $M3$) and the DN switches with NMOS devices ($M2$ and $M4$). Similar to the single-ended CP illustrated in Fig. 2.7, the gate inputs of $M1$ and $M3$ are connected to an inverter to realise the CP operation. These inverters are typically left out in differential CP diagrams where the inputs to $M1$ and $M3$ are typically denoted as $\overline{M1}$ and $\overline{M3}$, as will be adopted from this point on in the thesis.

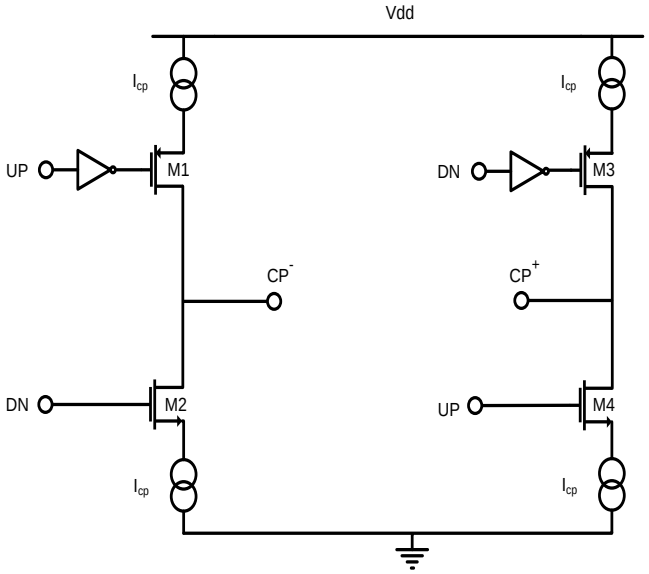



**Fig. 4.5:** Practical differential CP

### 4.3.2 Performance Analysis

To analyse the performance advantages offered, the differential CP of Fig. 4.5 was designed using UMCs 90nm CMOS process. The performance was then compared with the single-ended CP of Fig. 2.6, designed using the same process.

*Output voltage swing*: First the output voltage swings for both CPs ($V_{swing_{cp}}$) were examined. Given that the concerned process is a low technology node, its voltage supply was limited to 1V. This, in addition to $V_{ov}$ for the current sources and sinks severely limited $V_{swing_{cp}}$ for both CPs (see (4.9) and (4.10)). For the single-ended CP, $V_{swing_{cp}}$ was limited to 0.5V, where for the differential CP it was double that at 1V (as per (4.10)). This increased output voltage swing thus results in the advantages discussed in section 4.2.2.

*Common-mode noise*: Next the effect of common-mode noise was examined. First, to gain an intuitive view of its effects, noise was superimposed onto the Vdd lines of both CPs and its effect on the output signals during steady state in the time domain examined. This noise was modelled by placing a signal source in series with the Vdd line which injected a sine wave of specified frequency and amplitude into the circuits. A sine wave was used for the analysis as it enables the effects of common-mode noise at specific frequencies (namely low and high frequencies) to be examined (a pulse wave has a large frequency content and thus would not enable such analysis). Figs. 4.6 and 4.7 plot the outputs from the single-ended and differential CPs respectively, for a sine wave oscillating at 1MHz with amplitude of 10mV (i.e. 0.001% of Vdd) superimposed on the Vdd lines.

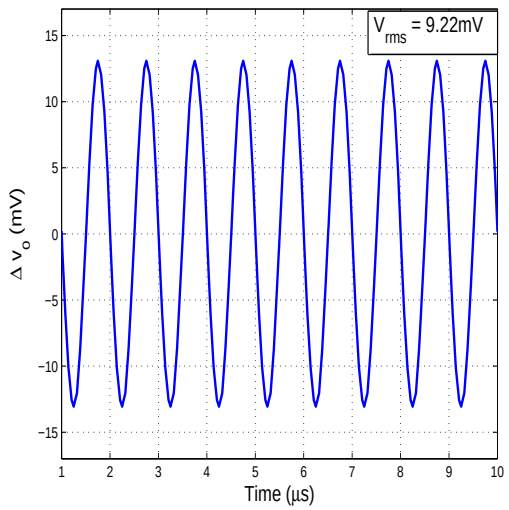



**Fig. 4.6:** $\Delta v_o$ for the single-ended CP

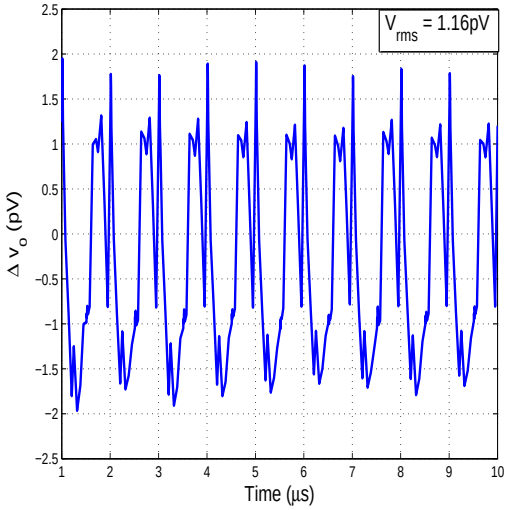



**Fig. 4.7:** $\Delta v_o$ for the differential CP

Immediately obvious from Figs. 4.6 and 4.7 is the dramatic reduction in common-mode

noise effects achieved by the differential CP. For the single-ended CP, Fig. 4.6 (whose y-axis is in units of mV) shows noise on the Vdd line to pass almost unaffected thereby greatly perturbing the outputs from their steady state nominal value. However for the differential CP, Fig. 4.7 (whose y-axis is in units of pV) shows the effect of such noise on the output signal to be significantly smaller. This is best summed up by taking the rms values for both signals which were calculated for the single-ended and differential CPs to be 9.22mV and 1.16pV respectively. Comparing the two values thus shows the differential CP to achieve a reduction in the described common-mode noise over the single-ended CP of almost 200dB.

Next the effect of common-mode noise at different frequencies was examined. To achieve this, the signal source previously described injected sine waves oscillating over a wide range of frequencies, where the maximum perturbation of the output signal from its nominal steady state value ($\Delta v_{o_{max}}$) for each frequency was recorded. In order to make the analysis complete, and to give a good general overview of the effects of common-mode noise in both circuits, the signal sources were placed at all the nodes susceptible to common-mode noise for both circuits and their effect on the output signals each individually examined. For both CPs this entailed placing the signal sources in series with the Vdd lines (as previously described), Vss lines and at the inputs to all the switches. The sine waves injected at each of these nodes all had amplitude of 10mV and oscillated over a frequency range of 100kHz $\rightarrow$ 100MHz.[2] The effect of this on the output signals for both the single-ended and differential CPs is thus shown in Figs. 4.8 and 4.9 respectively.

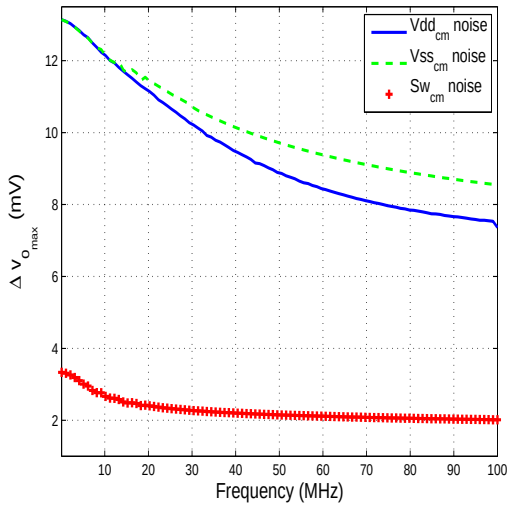



**Fig. 4.8:** $\Delta v_{o_{max}}$ for the single-ended CP

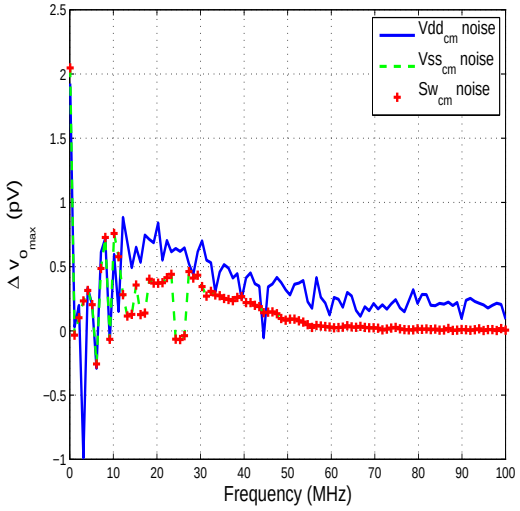



**Fig. 4.9:** $\Delta v_{o_{max}}$ for the differential CP

[2]Noise from the CP occurring at frequencies above the loop bandwidth ($K$) will be attenuated by the loops low pass filter characteristic (see Fig. 2.30 and (2.47)). As 100MHz is far greater than any practical values for $K$, it was set as the maximum noise frequency to be analysed.

In general, Figs. 4.8 and 4.9 show the effects of common-mode noise on the outputs of both CPs to decrease as frequency increases. For the single-ended CP, Fig. 4.8 shows noise superimposed on the Vss line ("$Vss_{cm}$ noise") to become increasingly dominant at higher frequencies with noise superimposed on the inputs to the switches ("$Sw_{cm}$ noise") being the least dominant. For the differential CP, Fig. 4.9 shows all the noise sources to affect the output signal more or less equally with noise superimposed on the Vdd line ("$Vdd_{cm}$ noise") shown to marginally dominate. Nevertheless, the effect of such noise on the output signal is in the low pV range and so can be assumed negligible. This is in sharp contrast to the single-ended CP where noise effects are shown to be in the mV range, hence significantly perturbing the output signal from its nominal steady state value. In addition, this dramatic reduction of common-mode noise effects achieved by the differential CP is also seen to be maintained at high frequency.

It should be noted that the above analysis was specific to the CP and thus ignores common-mode rejection capabilities of proceeding blocks in addition to any effects the LF will have on the CP outputs.[3] Nevertheless, the above analysis does suffice to show the potential significant reduction in common-mode noise effects of a CP achieved by adopting a differential CP architecture over a single-ended one, with this reduction being maintained at high frequency.

*Static phase error*: Static phase error was introduced in section 2.3.1 where its dominant cause was stated to be due to mismatch current. Differential CPs dramatically reduce mismatch current thereby achieving significantly lower static phase errors. This can be explained with reference to Figs. 4.10 and 4.11.

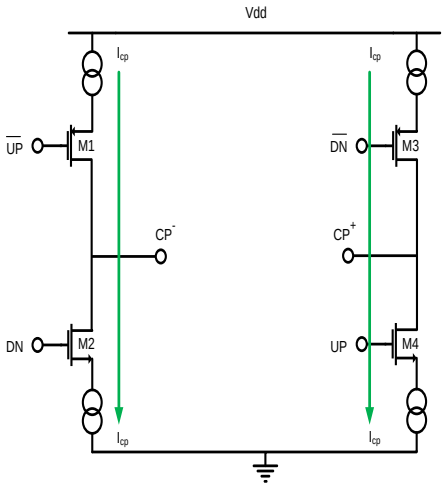



**Fig. 4.10:** Perfect matching

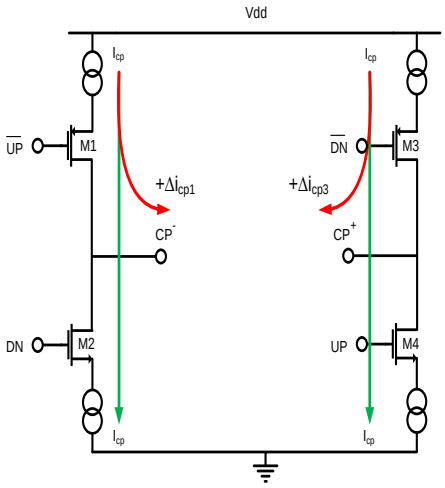



**Fig. 4.11:** Mismatch in UP network

[3] In practice the LF capacitors significantly dampen any perturbations on the CP outputs and so when placed in a PLL, common-mode noise will not perturb the CP outputs to the same extent seen in Fig. 4.6.

In steady state, UP = DN = 1 which turns on all switches. Assuming perfect matching between all UP and DN networks, zero mismatch current exists and the CP current ($I_{cp}$) does not affect the outputs (no net flow of charge exits through $CP^-$ or $CP^+$), as indicated by the green arrows in Fig. 4.10. Assuming now that mismatches exist within both UP networks, mismatch currents will appear at both CP outputs. This is shown in Fig. 4.11 where mismatches within the UP networks are shown to generate positive mismatch currents ($+\Delta i_{cp_1}$ and $+\Delta i_{cp_3}$) indicated by the red arrows. If both UP networks are perfectly matched such that they exhibit identical mismatches, then the degree of mismatch between them will be zero. As a result, $+\Delta i_{cp_1} = +\Delta i_{cp_3}$ causing both CP outputs to be equally affected. In other words the mismatch currents will appear as a common-mode offset on the differential CP outputs which, by virtue of (4.5) will have negligible effect on the PLL. The exact same applies for mismatches within the DN networks with resulting mismatch currents appearing as a common-mode offset on the CP outputs as long as the DN networks are perfectly matched.

Mismatch current in a differential CP behaves as a common-mode offset only if the UP networks perfectly match each other and the DN networks perfectly match each other. In practice this reduces to the constraint of matching PMOS with PMOS and NMOS with NMOS thereby avoiding the matching of physically different devices (PMOS with NMOS) which results with single-ended CPs. As this new matching constraint is much more effectively dealt with by increasing device dimensions as per (2.8), mismatch current in a differential CP is typically orders of magnitude less than in a single-ended CP. To verify this, the UP ($I_{UP}$) and DN ($I_{DN}$) currents for both the single-ended and differential CPs were analysed under steady state conditions and their respective percentage mismatches calculated. The resulting $I_{UP}$ and $I_{DN}$ currents for the single-ended CP are plotted over an output voltage swing ($V_{cp}$) ranging from 0 → Vdd (0 → 1V) in Fig. 4.12.

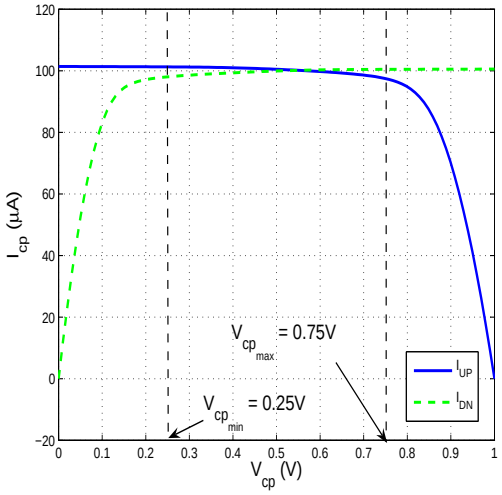



**Fig. 4.12:** $I_{UP}$ vs $I_{DN}$

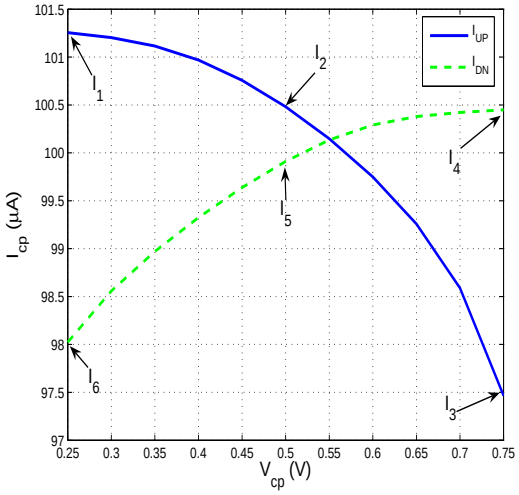



**Fig. 4.13:** $I_{UP}$ vs $I_{DN}$ close-up

Given that the single-ended CP was designed for a steady state output of 0.5V and nominal CP current ($I_{cp}$) of 100$\mu A$, Fig. 4.12 shows $I_{UP}$ and $I_{DN}$ to be $\approx I_{cp}$ only over a limited voltage range ($I_{DN} \approx I_{cp}$ for $V_{cp} > V_{cp_{min}}$ and $I_{UP} \approx I_{cp}$ for $V_{cp} < V_{cp_{max}}$). This is due to the overdrive voltages ($V_{ov}$) of the current sink and source, which for the single-ended CP were both $\approx$ 0.2V, hence resulting in the following allowable CP output voltage swing (with some tolerance):

$$V_{cp_{min}}(0.25V) \leq V_{cp} \leq V_{cp_{max}}(0.75V) \tag{4.12}$$

As we are only interested in this region of operation, Fig. 4.13 focuses in on it to clearly show the mismatch between $I_{UP}$ and $I_{DN}$. The resulting mismatches can then be calculated using currents $I_1 \rightarrow I_6$ shown on Fig. 4.13 [23], whose precise values are given in Table 4.2.

| Fig. 4.13 | Definition | Simulated value ($\mu A$) |
|---|---|---|
| $I_1$ | $I_{UP_{max}}$ | 101.26 |
| $I_2$ | $I_{UP_{mid}}(V_{cp} = 0.5V)$ | 100.48 |
| $I_3$ | $I_{UP_{min}}$ | 97.47 |
| $I_4$ | $I_{DN_{max}}$ | 100.45 |
| $I_5$ | $I_{DN_{mid}}(V_{cp} = 0.5V)$ | 99.91 |
| $I_6$ | $I_{DN_{min}}$ | 98.02 |

All quoted values are typical case i.e. taken from a standard process corner simulation

**Table 4.2:** Simulated values for $I_{UP}$ and $I_{DN}$ for the single-ended CP

Using the values in Table 4.2, the mismatch between $I_{UP}$ and $I_{DN}$ ($\Delta_{i_{cp}}$) and the worst case $I_{cp}$ mismatch over $V_{swing_{cp}}$ ($\Delta_{i_{cp},V_{cp}}$) can be calculated as follows [23]:

$$\Delta_{i_{cp}}(\%) = \frac{(2(I_2 - I_5))}{I_2 + I_5} \cdot 100 \tag{4.13}$$

$$\Delta_{i_{cp},V_{cp}}(\%) = \frac{(I_1 - I_3)}{I_1 + I_3} \cdot 100 \tag{4.14}$$

$$= \frac{(I_4 - I_6)}{I_4 + I_6} \cdot 100 \tag{4.15}$$

Inserting the relevant values from Table 4.2 into (4.14) and (4.15) yields $I_{cp}$ mismatches over $V_{swing_{cp}}$ of 1.9% and 1.2% respectively. This worst case variation of 1.9% is not a specific concern for static phase offset however as it quantifies output current variation as opposed to current mismatch per say. Nevertheless, from the perspective of loop

bandwidth variation ($\Delta K$) this variation is an issue (discussed in detail in chapter 5).

From the perspective of static phase offset, equation (4.13) is the most relevant which, inserting the relevant values from Table 4.2 yields a typical mismatch between $I_{UP}$ and $I_{DN}$ ($\Delta_{i_{cp}}$) of 0.6%. Although this may seem small, Fig 4.13 shows its effect to increase the steady state output voltage from 0.5V $\rightarrow$ 0.55V (i.e. a 10% increase), seen where $I_{UP}$ and $I_{DN}$ intersect such that Kirchoffs current law at the output node can be satisfied.

To gain a perspective of these numbers, Table 4.3 compares them with specified values (typical case) taken from two frequency synthesizer ICs available on the market today.

| Manufacturer | National Semiconductor | Analog Devices | - |
|---|---|---|---|
| Model | LMX2541 [23] | ADF4351 [22] | Single-ended CP |
| $\Delta_{i_{cp}}(\%)$ | 3 | 2 | 0.6 |
| $\Delta_{i_{cp},V_{cp}}(\%)$ | 4 | 1.5 | 1.9 |

**Table 4.3:** Performance comparison for the single-ended CP

It is somewhat surprising to see from Table 4.3 that the single-ended CP analysed in this section offers improved matching in $\Delta_{i_{cp}}$ over the two industry ICs. It should be stressed that this was not intentional (no clever or novel design techniques were employed in the single-ended CP) and is most probably due to the matching of the process technologies involved. As stated in section 2.3.1, provided non-minimum dimensions are used, device mismatch improves as technologies shrink.[4] Although the exact technology nodes used for the two industry ICs were not specified, the required Vdd supplies suggest technology nodes around the $0.35\mu m$ node were used. Considering that our single-ended CP was designed using a 90nm process, it would seem reasonable to assume the improved matching in $\Delta_{i_{cp}}$ is due to superior matching between devices employing non-minimum dimensions (such as those used in the current sources and sinks) for our process.

Nevertheless, mismatch between $I_{UP}$ and $I_{DN}$ is still prevalent in the single-ended CP whose effect can be effectively eliminated in the differential CP which fully exploits the excellent matching seen for this 90nm process. As already explained, differential operation in a CP reduces matching constraints to how well the UP networks match each other and how well the DN networks match each other. This matching can be examined by analysing the respective currents in each network under steady state conditions, that is the two UP currents ($I_{UP_1}$ and $I_{UP_3}$, see Fig. 4.4) and the two DN currents ($I_{DN_2}$ and $I_{DN_4}$, see Fig. 4.4). These are plotted in Fig. 4.14 over the allowable CP output voltage swing.

[4]The realisation of minimum dimensions in low technology nodes requires the processing equipment to realise extremely small dimensions hence making their realisation of larger dimensions much more accurate. As such, the matching of devices employing non-minimum dimensions greatly improves.

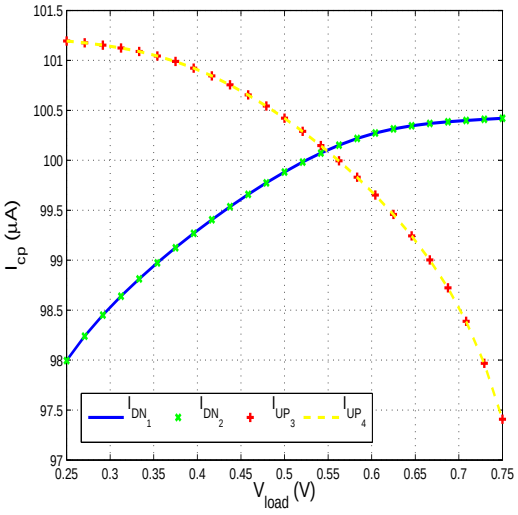



**Fig. 4.14:** $I_{UP}$ vs $I_{DN}$

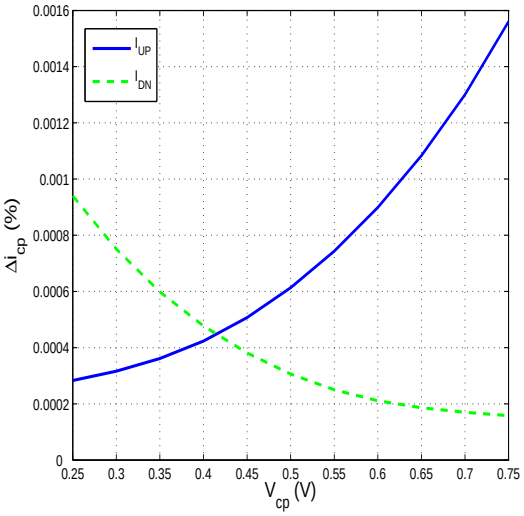



**Fig. 4.15:** $\Delta i_{cp}$

As expected (and given that the differential CP was also designed for a nominal CP current ($I_{cp}$) of $100\mu A$), all currents exhibit a similar behaviour to that seen in Fig. 4.13 for the single-ended CP. Given the excellent matching for the concerned process, the UP currents are seen to match each other excellently as is also the case for the DN currents. To illustrate the mismatch $\Delta_{i_{cp}}$, it was calculated using (4.13) over the allowable CP output voltage swing and plotted in Fig. 4.15. This shows the resulting mismatches to be negligible with the UP network exhibiting slightly worse mismatch over the DN network.[5] To allow a comparison with the single-ended CP, $\Delta_{i_{cp},V_{cp}}$ and the worst case value for $\Delta_{i_{cp}}$ at $V_{cp} = 0.5$V were calculated. These are shown in Table 4.4 which compares them with corresponding values from the single-ended CP analysed in this section and a frequency synthesizer IC employing a differential CP, available on the market today.

| Manufacturer | Analog Devices | - | - |
|---|---|---|---|
| Model | ADF4193 [21] | Single-ended CP | Differential CP |
| $\Delta_{i_{cp}}(\%)$ | 0.1 | 0.6 | 0.0006 |
| $\Delta_{i_{cp},V_{cp}}(\%)$ | 1 | 1.9 | 1.9 |

**Table 4.4:** Performance comparison for the differential CP

Table 4.4 shows the differential CP to achieve a reduction in $\Delta_{i_{cp}}$ by three orders of magnitude over the single-ended CP. In addition, it shows a reduction in $\Delta_{i_{cp}}$ by over two orders of magnitude over the differential CP used in Analog Devices ADF4193 frequency

[5]This occurs due to the additional $n$-well for PMOS devices introducing additional variability over NMOS devices and thereby increasing device mismatch

synthesizer (attributed mainly to the excellent matching of the 90nm process as previously discussed). Interestingly it shows no difference in $\Delta_{i_{cp},V_{cp}}$ suggesting differential CPs not to address the issue of mismatch current over CP output voltage swing. As such mismatch is due to channel length modulation effects, it can be addressed by cascoding (where voltage headroom allows) and (or) increasing output conductances using increased channel lengths. Given that a voltage supply of 5V is specified for the CP of the ADF4193, cascoding could be (and most probably was) used in the CP thereby contributing to its superior $\Delta_{i_{cp},V_{cp}}$ value over our single-ended and differential CPs, which operated from a supply of 1V. In addition to this, since short channel effects increase with shrinking dimensions, they will be more prevalent in the 90nm process used to simulate our differential CP than for the ADF4193 which, as mentioned previously, was fabricated using a technology node around the $0.35\mu m$ node. The reduced occurrence of these effects would thus further contribute to the superior $\Delta_{i_{cp},V_{cp}}$ of the ADF4193. However, as only $\Delta_{i_{cp}}$ directly contributes to static phase error we can thus conclude differential CPs to achieve significant reductions in static phase error over their single-ended counterparts.

Section 2.3.1 stated unequal pulse arrival times to be another dominant source of static phase error which results from having to place an inverter at the input of one of the switches (see Fig. 2.7). Since for a differential CP, such inverters are required on both the switching inputs for either the UP or DN networks (see Fig. 4.5), the pulse arrival times on both inputs will be delayed by similar amounts (any mismatches will be negligible in comparison to the turn-on times for the switches). As a result, a common-mode offset similar to that illustrated by the red arrows in Fig. 4.11 ensues which, through the same mechanism as for mismatch current, will be effectively eliminated.

Overall, the analysis performed in this section shows differential CPs to exhibit far superior performance over their single-ended counterparts. They exhibit twice the output voltage swing, reduce common-mode noise effects (at both high and low frequencies) to negligible amounts and significantly reduce static phase error through reducing the effects of mismatch current to negligible amounts, and practically eliminating those due to unequal pulse arrival times. In light of these advantages it is very surprising that, from an extensive search of frequency synthesizer ICs available on the market today, only one was found to employ a differential CP (the ADF4193). The exact reasons for this are not obvious as differential CPs present no significant overheads whilst realising significant gains in terms of noise performance. Nevertheless, due to these gains, a differential CP was employed in the final PLL of this thesis.

### 4.3.3 Differential CP Architectures

Fig. 4.5 illustrated the simplest architecture [63] for a differential CP. This is in fact an extremely effective architecture whose main modification is that it can be extended to reduce static phase error due to charge sharing (see section 2.3.1) using a voltage follower [62] or current steering [13] technique. For reasons discussed in section 2.3.1, the current steering technique is preferred where the architecture presented in [13] is used in the ADF4193 frequency synthesizer IC analysed in Table 4.4. A variation of this architecture is presented in [16] where all the switches are realised using NMOS devices. As this eliminates the need for inverters on the "UP switches" it was decided to employ this architecture in the final PLL of this thesis, whose complete schematic is presented in Fig. 4.16.[6] This shows the differential CP to consist of 12 NMOS and 3 PMOS transistors. It's biasing current ($I_{cp}$) is assumed to be generated from an on-chip bandgap voltage ($V_{bg}$) to give a "bandgap over R" current defined as:

$$I_{cp} = \frac{V_{bg}}{R_{I_{cp}}} \tag{4.16}$$

where the current defining resistor is represented by $R_{I_{cp}}$.

The NMOS pairs $(M1, M3)$ and $(M1, M4)$ mirror this reference current to the DN networks where $M2$ and PMOS pairs $(M13, M14)$ and $(M13, M15)$ mirror it to the UP networks. All the switches are realised as NMOS devices ($M5 \rightarrow M8$) where $M9 \rightarrow M12$ are required to accurately set and maintain the common-mode voltage ($V_{cm}$), defined in (4.3) and explained in section 4.3.4.

The CP output voltages are limited by the constraint of maintaining $M1 \rightarrow M4$ and $M13 \rightarrow M15$ in saturation. These are defined as:

$$V_{cp_{max}} = Vdd + V_{ov_{13\rightarrow15}} \tag{4.17}$$

$$V_{cp_{min}} = V_{ov_{1\rightarrow4}} + V_{ds_{5\rightarrow8}}(on) + V_{ds_{9\rightarrow12}} \tag{4.18}$$

where the drain-source voltage of $M5 \rightarrow M8$ when switched on is represented by $V_{ds_{5\rightarrow8}}(on)$. The overdrive voltages for $M1 \rightarrow M4$ and $M13 \rightarrow M15$, and the drain-source voltage of $M9 \rightarrow M12$ are then represented as $V_{ov_{1\rightarrow4}}$, $V_{ov_{13\rightarrow15}}$ and $V_{ds_{9\rightarrow12}}$ respectively. Applying (4.17) and (4.18) to (4.8) defines the CP output voltage swing ($V_{swing_{cp}}$) as:

$$V_{swing_{cp}} = 2((Vdd - V_{ov_{13\rightarrow15}}) - (V_{ov_{1\rightarrow4}} + V_{ds_{5\rightarrow8}}(on) + V_{ds_{9\rightarrow12}})) \tag{4.19}$$

The CP inputs are the inputs to the switches which come directly from the PFD and so can be defined as $V_{PFD_{ON}} = 1V$ and $V_{PFD_{OFF}} = 0V$.

[6] W/L ratios and operating points for each transistor of Fig. 4.16 are detailed in section 6.2.

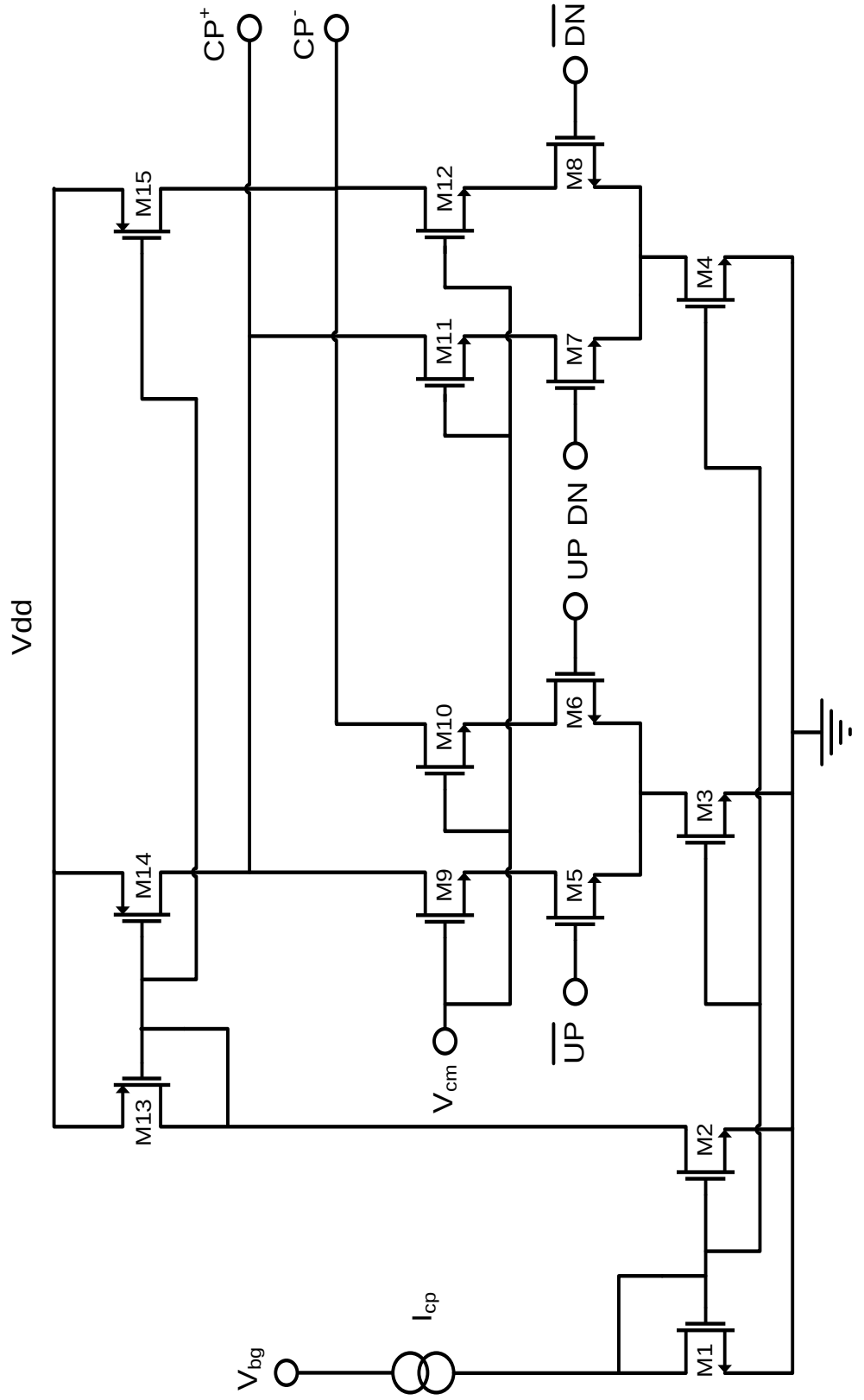



**Fig. 4.16:** Schematic of the chosen differential CP architecture

Although the differential CP of Fig. 4.16 appears vastly different from that shown in Fig. 4.5, it is important to see that its differential operation is identical. This can be seen in Table 4.5 where the overall operation of the CP is summarised.

| | $UP$ | $DN$ | $\overline{UP}$ | $\overline{DN}$ | $M5$ | $M6$ | $M7$ | $M8$ | $CP^+$ | $CP^-$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $\phi_{ref} > \phi_{fb}$ | 1 | 0 | 0 | 1 | OFF | ON | OFF | ON | increase | decrease |
| $\phi_{ref} < \phi_{fb}$ | 0 | 1 | 1 | 0 | ON | OFF | ON | OFF | decrease | increase |

**Table 4.5:** Operation table for the chosen differential CP

Comparing the first and last two columns of Table 4.5 with those of Table 4.1 show them to be the same verifying the differential operation of both CPs to be identical. The only difference is how the differential operation is obtained. Comparing once again Tables 4.1 and 4.5, and noting that $S1 = M5 = \overline{UP}$, $S2 = M7 = DN$, $S3 = M8 = \overline{DN}$ and $S4 = M6 = UP$, it can be seen that the operation of the $UP$ and $DN$ switches are identical for both structures. However, the operation of the $\overline{UP}$ and $\overline{DN}$ switches are the inverse of each other. This is the main difference between the two architectures and results because the $\overline{UP}$ and $\overline{DN}$ switches are realised as NMOS devices in Fig. 4.16, whereas in Fig. 4.5 they were realised as PMOS devices.

The advantage of this architecture is that due to the inverse operation of the NMOS switches, it intrinsically reduces charge sharing effects through current steering. It also eliminates the need for inverters at the PFD outputs in addition to enabling a simple mechanism for common-mode feedback (CMFB) control.

### 4.3.4 CMFB Control

As shown in section 4.1, differential outputs are measured with reference to a common-mode voltage ($V_{cm}$) defined in (4.3). Therefore, it is imperative that $V_{cm}$ be accurately defined and remain constant over process, voltage, temperature (PVT) variation. In order to achieve this, a CMFB control loop is required.

The CMFB control loop is a negative feedback loop, typically divided into three networks: The sensing network, the comparison network and the compensation network. The sensing network simply extracts $V_{cm}$ from the differential outputs. This is then fed to the comparison network which compares it to a reference voltage ($V_{ref}$) (set to some nominal value for $V_{cm}$). The output from the comparison network is then fed to the compensation network such that it counteracts any changes in bias levels to restore $V_{cm}$ back to its nominal value, hence giving the loop its negative feedback behaviour.

*Sensing network*: For the sensing network, a simple resistor divider was used, as shown in Fig. 4.17.

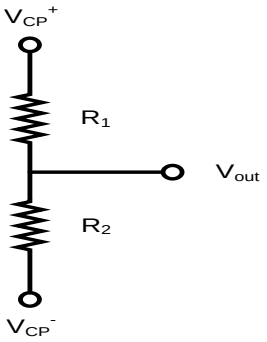



**Fig. 4.17:** Sensing network

Provided $R_1 = R_2$ in Fig. 4.17, the output voltage ($V_{out}$) is defined as (see Appendix A.12):

$$\begin{aligned} V_{out} &= \frac{V_{CP+} + V_{CP-}}{2} \\ &= V_{cm} \end{aligned} \tag{4.20}$$

It is very important to minimise mismatch between $R_1$ and $R_2$. As such, they should be realised with polysilicon ("poly resistors") as these exhibit reduced PVT variations over resistors fabricated using an $n$-well. In addition, the should be laid out very close to each other such that any mismatches are localised (i.e. affect both resistors equally). In addition to this, it is extremely important to set $R_1$ and $R_2$ large ($\geq$ 1M$\Omega$) so as not to interfere with the loop dynamics of the PLL.

*Comparison network*: For the comparison network, a simple differential amplifier was used, whose block diagram is shown in Fig. 4.18.

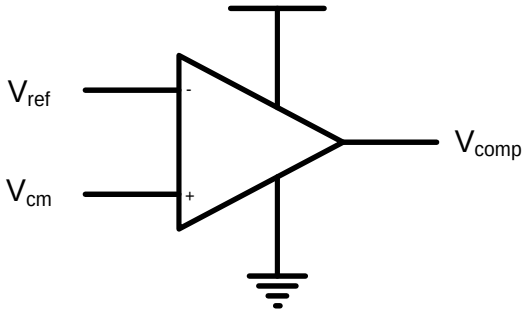



**Fig. 4.18:** Block diagram of the comparison network

As can be seen from Fig. 4.18, the output from the sensing network ($V_{cm}$) is applied to the

positive terminal, with the nominal value for $V_{cm}$ ($V_{ref}$) applied to the negative terminal. The advantages of a large CP output voltage swing were detailed in section 4.2.2, and so to maximise this, $V_{ref}$ is typically set to Vdd/2. Any deviation of $V_{cm}$ from this nominal value ($V_{ref}$) will thus cause the output of the differential amplifier ($V_{comp}$) to vary in proportion as follows:

$$V_{comp} = A_v(V_{cm} - V_{ref}) \tag{4.21}$$

where $A_v$ represents the overall voltage gain of the differential amplifier. The schematic for the differential amplifier is then shown in Fig. 4.19.

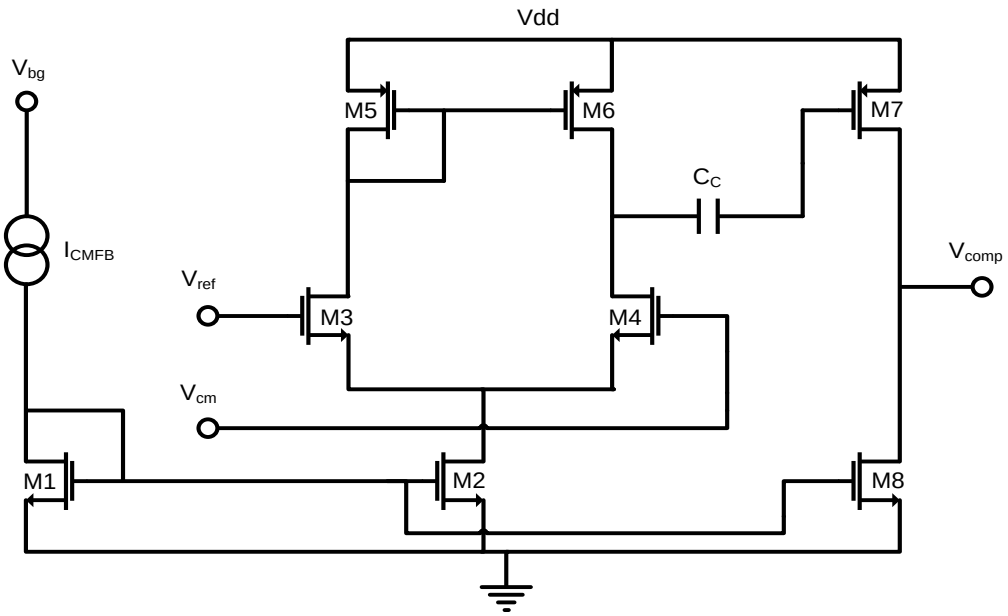



**Fig. 4.19:** Schematic of the differential amplifier used in the comparison network

Fig. 4.19 shows the differential amplifier to be a basic two-stage operational amplifier (op-amp) with both stages biased with a bandgap over R current ($I_{CMFB}$) as per (4.16). The first stage comprises transistors $M2 \rightarrow M6$ with $I_{CMFB}$ mirrored to it by the $(M1, M2)$ NMOS pair. The role of this stage is to amplify any differences between the two input signals, done primarily through $M3$ and $M4$, with $M5$ and $M6$ acting as a current load. Its output voltage ($V_{out_1}$) is therefore defined as:

$$V_{out_1} = A_{v1}(V_{cm} - V_{ref}) \tag{4.22}$$

where $A_{v1}$ represents the voltage gain of the first stage, defined as:

$$A_{v1} = g_{m_{3,4}} \ (r_{o_4} || r_{o_6}) \tag{4.23}$$

where the output resistances of $M4$ and $M6$ are represented by $r_{o_4}$ and $r_{o_6}$ respectively, and the transconductance of $M3$ or $M4$ is represented by $g_{m_{3,4}}$.

It is important for the differential amplifier to exhibit a large voltage gain as this forces the compensation network to react quicker. This could be achieved by increasing $A_{v1}$ either through increasing $g_{m_{3,4}}$ or increasing the total output resistance ($r_{out}$) of the stage. Increasing $g_{m_{3,4}}$ corresponds to increasing $I_{CMFB}$ and hence is unattractive to low power applications. Increasing $r_{out}$ then corresponds to cascoding which is not an option for low technology nodes due to limited voltage headroom. Therefore, a more attractive approach is to simply add on a second stage thereby increasing the overall voltage gain ($A_v$) of the differential amplifier as follows:

$$A_v = A_{v1}\ A_{v2} \tag{4.24}$$

where $A_{v2}$ represents the voltage gain of the second stage.

The second stage comprises transistors $M7$ and $M8$ and can be seen to be a basic common-source amplifier. The biasing current ($I_{CMFB}$) is mirrored to this stage by the NMOS pair ($M1, M8$) with $M7$ acting as the driving transistor. The voltage gain of the stage is thus defined as:

$$A_v 2 = g_{m_7}\ (r_{o_7} || r_{o_8}) \tag{4.25}$$

where the transconductance of $M7$ and the output resistances of $M7$ and $M8$, are represented by $g_{m_7}$, $r_{o_7}$ and $r_{o_8}$ respectively.

All the transistors within the differential amplifier must be maintained in saturation which limits the input and output voltages as follows:

$$V_{in_{min}} = V_{ov_2} + V_{t_{3,4}} \tag{4.26}$$

$$V_{in_{max}} = Vdd - V_{t_{5,6}} + V_{t_{3,4}} \tag{4.27}$$

$$V_{comp_{min}} = V_{ov_8} \tag{4.28}$$

$$V_{comp_{max}} = Vdd - V_{ov_{5,6}} - V_{t_7} \tag{4.29}$$

where the overdrive voltages of $M2$, $M5$, $M6$ and $M8$ are represented by $V_{ov_2}$, $V_{ov_5}$, $V_{ov_6}$ and $V_{ov_8}$ respectively, and the threshold voltages of $M3 \rightarrow M7$ are represented by $V_{t_3}$, $V_{t_4}$, $V_{t_5}$, $V_{t_6}$ and $V_{t_7}$ respectively.

Applying (4.28) and (4.29) to (4.8) then enable the output voltage swing ($V_{swing_{comp}}$)

to be defined as:

$$V_{swing_{comp}} = Vdd - V_{ov_{5,6}} - V_{t_7} - V_{ov_8} \tag{4.30}$$

Although the differential amplifier contains no local feedback connection, it is connected within the CMFB loop and so care must be taken to ensure its stablity (see section 2.6.1). To achieve this, a compensation capacitor (denoted as $C_c$ in Fig. 4.19) is connected between the first and second stages and sized to achieve the required $PM$ (Miller compensation). In practice, a $PM$ of 60° has shown to work reliably, which requires the following value for $C_c$ [64]:

$$C_c \approx 2.2\ C_L \tag{4.31}$$

where $C_L$ represents the loading capacitance on the output node of the amplifier. This $C_L$ is dominated by the compensation network which, as will be seen is simply the sum of the gates oxide capacitance's for $M9 \rightarrow M12$ in Fig. 4.16. As this capacitance is small, it does not interfere with the frequency response of the CMFB loop hence eliminating the need for additional compensation. Also, as the amplifier is driving a purely capacitive load no output buffer is required.

*Compensation network*: The compensation network is simply transistors $M9 \rightarrow M12$ in Fig. 4.16 whose gates are directly connected to the output of the comparison network. As a result, the comparison network will proportionally adjust the gate-source voltages ($V_{gs}$) of $M9 \rightarrow M12$ such that their corresponding drain-source voltages ($V_{ds}$) are proportionally increased or decreased to restore $V_{cm}$ back to its nominal value ($V_{ref}$). This can be seen in Table 4.6 which summarises the behaviour of the entire CMFB control loop.

| | Sensing Network | Comparison Network | Compensation Network |
|---|---|---|---|
| $V_{cm} > Vdd/2$ | $V_{cm}$ too high | Increase $V_{comp}$ | $V_{ds}$ and $V_{cm}$ decreases |
| $V_{cm} < Vdd/2$ | $V_{cm}$ too low | Decrease $V_{comp}$ | $V_{ds}$ and $V_{cm}$ increases |

**Table 4.6:** Operation table for the CMFB control

As shown in Table 4.6, if $V_{cm}$ is greater than its nominal value (> Vdd/2), the difference is sensed by the comparison network which increases $V_{comp}$ in proportion. As this proportionally increases the $V_{gs}$ of transistors $M9 \rightarrow M12$, it results in a proportional decrease in their $V_{ds}$ values hence reducing $V_{cm}$ back to its nominal value. The inverse of this then occurs for the case where $V_{cm}$ is less that its nominal value (< Vdd/2).

The block diagram for the complete differential CP architecture is shown in Fig. 4.20.[7]

[7] W/L ratios and operating points pertaining to Fig. 4.20 are detailed in section 6.2.

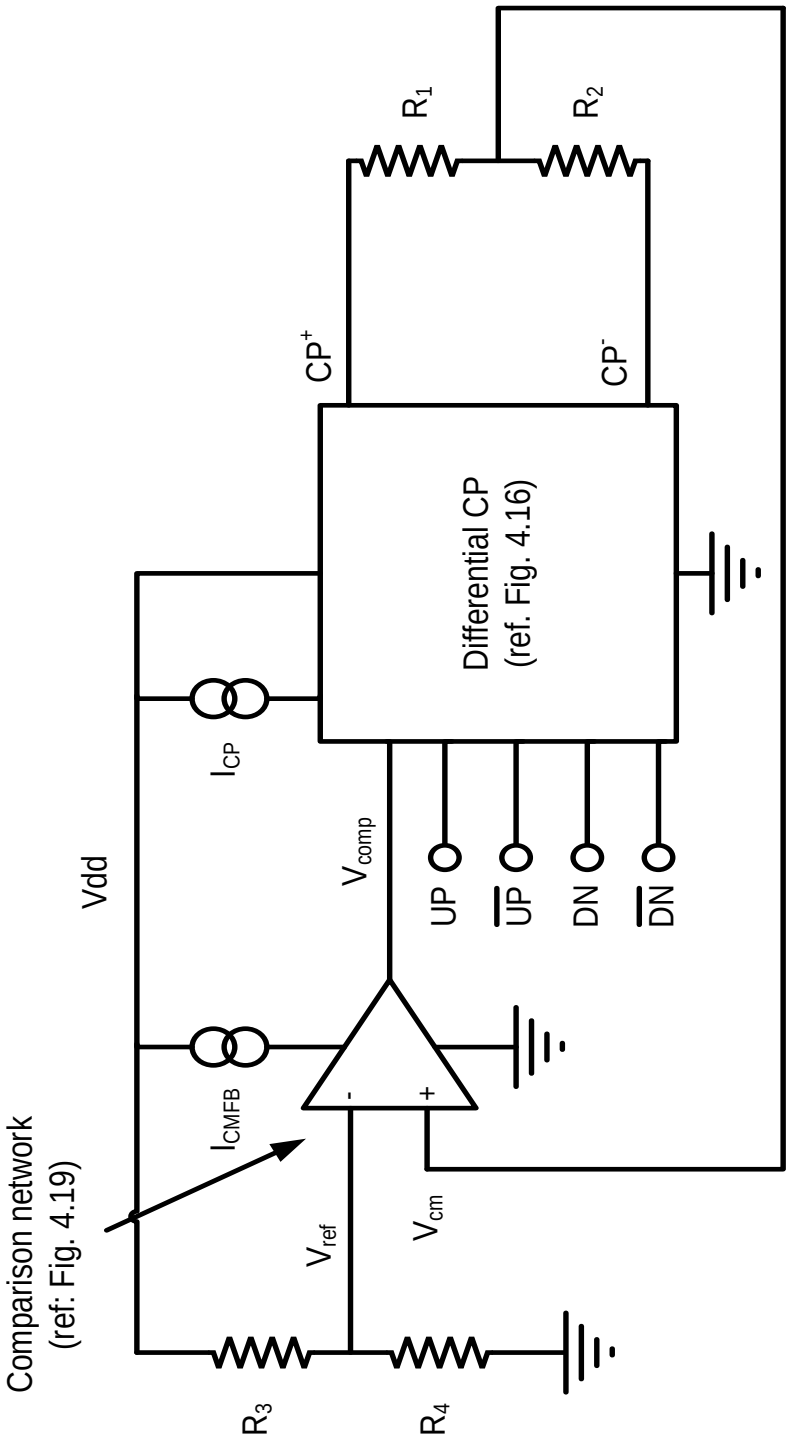



**Fig. 4.20:** Block diagram for the differential CP with CMFB control

The only addition to the schematic of Fig. 4.20 is the simple resistor divider network ($R_3$ and $R_4$) used to extract $V_{ref}$ from Vdd for the compensation network. Otherwise, all the building blocks which comprise Fig. 4.20 have been fully explained in the preceding discussions. The design procedure used for this schematic is outlined in Appendix B1.

## 4.4 Differential Loop Filter (LF)

The use of a differential CP requires a differential LF and so the next block of a PLL to be converted to differential operation in this chapter will be the LF. As noted in section 2.6.4, due to their low power consumption and noise, passive filters are more commonly found in practice with active filters not being discussed in this thesis. As such, the second-order passive lag-lead architecture of Fig. 2.24, shown in section 2.6.4 to provide optimal performance, will be used as the benchmark for this section.

### 4.4.1 Basic Architecture

As seen in Fig. 4.5, the differential CP exhibits two outputs and so at first glance, one would assume this to require two single-ended LFs, as shown in Fig. 4.21.

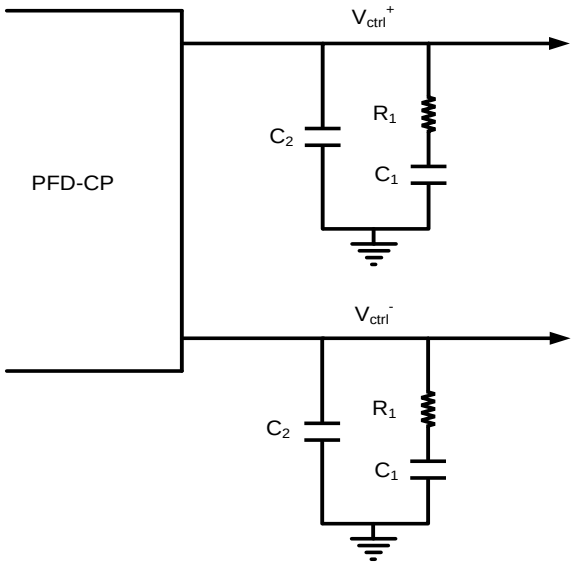



**Fig. 4.21:** Conventional differential LF

The architecture of Fig. 4.21 now contains two VCO control lines ($V_{ctrl+}$ and $V_{ctrl-}$), whose control will be discussed in section 4.5. Whilst it enables a differential CP to be used, this architecture exhibits two disadvantages. The first disadvantage is due to increases in thermal noise. Thermal noise occurs due to the random motion of electrons in an conductor which induce fluctuations in the voltage across the conductor from its

nominal value. For a resistor ($R$), its one-sided power spectral density due to thermal noise ($S_{tn}(f)$) can be modelled by [29]:

$$S_{tn}(f) = 4kTR \tag{4.32}$$

where the product of the Boltzmann constant $k$ (1.38 x $10^{-23}$J/K) and temperature ($T$) represents thermal energy. As can be seen from (4.32), $S_{tn}(f)$ is independent of frequency and directly proportional to $R$, hence increasing linearly with $R$ irrespective of frequency. As a result, the additional resistor required by the differential LF of Fig. 4.21 effectively increases its thermal noise contributions over that of the single-ended LF in Fig. 2.24 by a factor of two.

The second disadvantage of the differential LF is that it increases area requirements, resulting primarily from the additional capacitors. This is particularly alarming when we consider the large areas occupied by the capacitors of a LF, if fabricated on-chip. Silicon dioxide is generally used as the dielectric to realise on-chip capacitors which exhibits capacitance to area ratios of a few fFs per $\mu m^2$. Given that LF capacitor values are regularly in the pF range, the on-chip realisation of them typically consumes silicon area in the fractions of $mm^2$. As will be shown in section 4.4.3, this dominates the overall silicon area requirements of an on-chip LF and is the main disadvantage with passive LFs in general, with them often being simply too large in practice to implement on-chip. Given that the differential LF of Fig. 4.21 doubles the capacitance requirements over its single-ended counterpart, it effectively doubles silicon area requirements, almost certainly mandating it to be implemented off-chip.

In general off-chip LFs are costly as they consume additional IC pins and require additional external components. This increases printed circuit board (PCB) design complexity leading to extended project time, resources and cost. In addition, it also increases the number of potential failure nodes on the PCB. In spite of these disadvantages however, off-chip LFs are often unavoidable due to area and low noise requirements. Bad as these disadvantages are for a single-ended LF, they are increased for the differential LF architecture of Fig. 4.21 since it requires twice as many external components.

At this point differential LFs seem a costly and unattractive option. One might at first try to eliminate them by converting the differential CP outputs to single-ended form for use with a conventional single-ended LF. However, as this would require a differential to single-ended amplifier (similar to that shown in Fig. 4.19) at the CP outputs, current flow from the CP would be restricted hence inhibiting the practical realisation of the CP operation described in section 2.3.

Therefore, presented in the next section is a simplified differential LF architecture which achieves reductions in silicon area requirements by approximately a factor of two.

### 4.4.2 Impedance Transformation Method

The impedance transformation method, taken directly from [65], is applicable only to passive LFs where it exploits the differential control of the VCO (explained in detail in section 4.5). In section 4.4.1, the use of a differential CP was shown to result in two VCO control lines ($V_{ctrl+}$ and $V_{ctrl-}$). As such, the frequency variation of the VCO now becomes a function of the differential voltage across it ($V_d$), defined in this thesis as follows:

$$V_d = V_{ctrl+} - V_{ctrl-} \tag{4.33}$$

Therefore in terms of VCO control, it is not necessary to reference both LFs in Fig. 4.21 to ground. Re-arranging the LFs of Fig. 4.21 as in Fig. 4.22, shows the nodes A and B to be at virtual ground thereby permitting the transformation shown in Fig. 4.23.

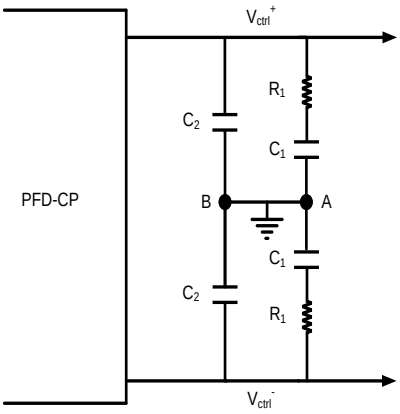



**Fig. 4.22:** Re-arranged differential LF

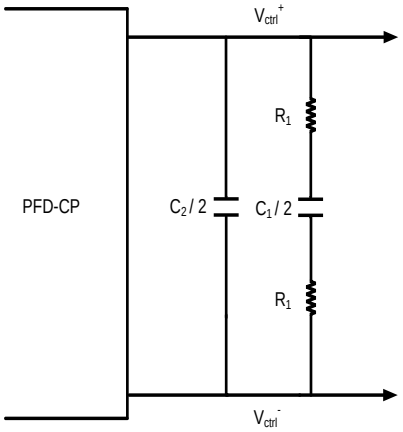



**Fig. 4.23:** Transformed differential LF

As can be seen from Figs. 4.22 and 4.23, viewing the nodes A and B as a virtual ground enables the capacitors ($C_1$ and $C_2$) to be combined in series, thereby permitting them to be reduced as follows:

$$C_1 + C_1 = C_1/2 \tag{4.34}$$

$$C_2 + C_2 = C_2/2 \tag{4.35}$$

This reduction in capacitance requirements is the main advantage of the transformed architecture, which can be seen to achieve reductions in overall capacitance requirements by a factor of four over the conventional differential LF shown in Fig. 4.21. Given that the capacitors dominate the overall silicon area requirements of a LF (shown in section 4.4.3),

this more or less leads to a reduction in LF silicon area requirements also by a factor of four, hence making the transformed differential LF of Fig. 4.23 much more feasible to on-chip implementation. Furthermore, this architecture also achieves reductions in the overall capacitance requirements by a factor of two over its single-ended counterpart, leading to reductions in silicon area requirements by roughly the same factor. As a result, the transformed differential LF becomes more feasible to on-chip implementation even over the single-ended LF shown in Fig. 2.24.

If on-chip implementation is still not possible however, the second advantage of this transformation method can be utilised - it reduces the number of external capacitors required over a conventional differential LF by two (seen through comparison of Figs. 4.22 and 4.23). As such, the PCB design effort to implement the transformed differential LF will be similar to its single-ended counterpart with the exception of the additional resistor.

In fact, this additional resistor represents the only disadvantage with the transformation method as it does not permit a reduction in overall resistance or number of resistors required. As the area requirements for an on-chip LF are dominated by the capacitors (shown in section 4.4.3), this does not raise any justifiable concerns regarding feasibility of on-chip implementation. Nevertheless, it does not alleviate any concerns over thermal noise as discussed in section 4.4.1. This concern can be addressed by increasing $I_{cp}$ such that resulting resistances required by the LF are small (see Table B.2 in Appendix B1), hence reducing $R$ in (4.32) and generating less thermal noise. However, as this results in a hand in hand increase in capacitance (and overall power) requirements (see Table B.2 in Appendix B1), silicon area requirements for the LF significantly rise. As a result, a trade-off between noise performance and area requirement is almost always encountered in passive LF design.

### 4.4.3 Performance Analysis

The main advantage of employing a differential LF is that it enables a differential CP to be used thereby realising the performance advantages of Fig. 4.2. However, to analyse the reduced silicon area requirements achieved by the transformed differential LF of Fig. 4.23, it was designed using UMCs 90nm CMOS process and compared with the single-ended LF of Fig. 2.24, designed using the same process and to meet the same specifications ($PM = 50°$).

*Silicon area requirements*: In order to compare their resulting silicon area requirements, it was important that both LFs employ the same physical devices. As they were intended for on-chip implementation, both LFs employed polysilicon resistors with a resistance to area ratio of $\approx 60\Omega/\mu m^2$ and metal-insulator-metal (MIM) capacitors with a capacitance to area ratio of $2\text{fF}/\mu m^2$. The resulting component values for both LFs and their

corresponding silicon area requirements are summarised in Table 4.7.

| LF architecture | $R_1$ (kΩ) | $A_{R_1}$ ($\mu m^2$) | $C_1$ (pF) | $A_{C_1}$ ($mm^2$) | $C_2$ (pF) | $A_{C_2}$ ($mm^2$) | $A_{LF}$ ($mm^2$) | Component count |
|---|---|---|---|---|---|---|---|---|
| Single-ended | 18.28 | 13.38 | 226.83 | 0.12 | 39.2 | 0.02 | $\approx 0.14$ | 3 |
| Differential | 36.56 | 26.76 | 113.42 | 0.06 | 19.6 | 0.01 | $\approx 0.07$ | 4 |

**Table 4.7:** Single-ended and differential LF requirements

where the total LF silicon area requirements and that for components $R_1$, $C_1$ and $C_2$ are represented by $A_{LF}$, $A_{R_1}$, $A_{C_1}$ and $A_{C_2}$ respectively.

Firstly, Table 4.7 shows the capacitors to dominate overall area requirements of the LF with the resistors occupying only 0.009% and 0.04% of the total area required for the single-ended and transformed differential LFs respectively. Secondly, it shows the transformed differential LF to achieve a reduction in overall area requirements by approximately a factor of two over the single-ended LF. Lastly it shows that if the LFs were to be implemented off-chip, the transformed differential LF would require one additional component over the single-ended LF due to its doubled resistor requirements. Nevertheless, this is still two components less than that required for a conventional differential LF (see Fig. 4.21) if implemented off-chip.

Overall, the analysis performed in this section shows the transformed differential LF of Fig. 4.23 to be more feasible to on-chip implementation over the single-ended LF of Fig. 2.24, in addition to enabling a differential CP to be used. Where on-chip implementation is still not feasible, the transformed differential LF is more attractive to PCB implementation than the conventional differential LF architecture of Fig. 4.21, with the end PCB design effort being similar to that required for the single-ended LF of Fig. 2.24. Since the fully differential PLL of this thesis employs a differential CP, a differential LF was always necessary where due to its advantages, the transformed differential LF of Fig. 4.23 was employed in the final PLL of this thesis. The design procedure used for this LF is outlined in Appendix B2.

## 4.5 Differentially Tuned VCO

Chapter 3 described the design and behaviour of a differential VCO in detail. However, as all the VCOs described contained only one tuning line ($V_{ctrl}$), they are not directly compatible with the differential LF described in the previous section. As mentioned in section 3.9, VCOs with single-ended tuning can be made compatible with differential

CPs (and hence differential LFs) using a differential amplifier (similar to that shown in Fig. 4.19). However as this requires additional components, it increases design complexity, cost, time and resources. More importantly, it consumes additional silicon area, increases power consumption and may even degrade the noise performance of the PLL. A much more elegant approach is thus to convert a VCO with single-ended tuning to one with differential tuning. Such a VCO would be directly compatible with a differential LF thereby eliminating the need for a differential amplifier, and all the associated disadvantages.

Omitting the differential amplifier however means the rejection of common-mode noise from the CP must now take place within the VCO itself. Therefore, it is crucial that the differential tuning inputs of the VCO exhibit good common-mode noise rejection capability which, as will be shown in this section, is achievable with symmetrical differential tuning characteristics.

### 4.5.1 Differential Tuning Characteristics

A basic varactor configuration which realises differential tuning is shown in Fig. 4.24 [66]:

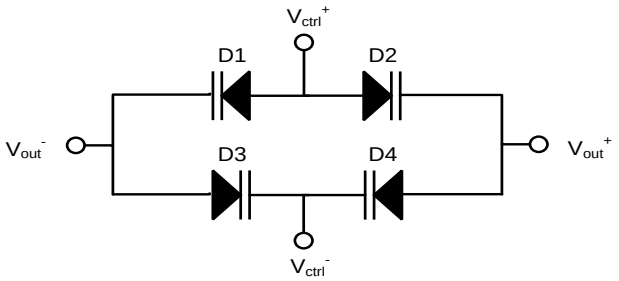



**Fig. 4.24:** Basic varactor configuration for differential tuning

The configuration of Fig 4.21 shows four varactors, comprising two branches connected in an anti-parallel configuration. The first branch consists of the series connection of varactors $D1$ and $D2$ where the second branch consists of the series connection of $D3$ and $D4$. As the two branches are connected in parallel, their capacitances add requiring the sizing of varactors $D1 \rightarrow D4$ to be half that of their single-ended counterparts (assuming differential tuning is employed). All the varactors are shown as diode varactors,[8] where $V_{out^-}$ and $V_{out^+}$ represent the differential outputs as previously shown. The differential tuning inputs are then represented by $V_{ctrl^+}$ and $V_{ctrl^-}$ which in practice are connected to the CP outputs $CP^-$ and $CP^+$ respectively, as shown in Fig. 4.5.

This configuration is however impractical as it renders the diode varactors susceptible to forward biasing unless the CP output voltage swings are severely restricted (see section 3.4.2). In addition, it employs anode tuning which, as discussed in section 3.4.2,

[8] All varactor configurations shown from herein will comprise solely of diode varactors due to the various performance advantages they exhibit over MOS varactors shown for UMCs 90nm process in section 3.4.3.

yields inferior quality factors to cathode tuning. Therefore, similar to Figs. 3.26 and 3.27 a much more attractive and practical realisation for differential tuning is achieved with the modification shown in Fig. 4.25:

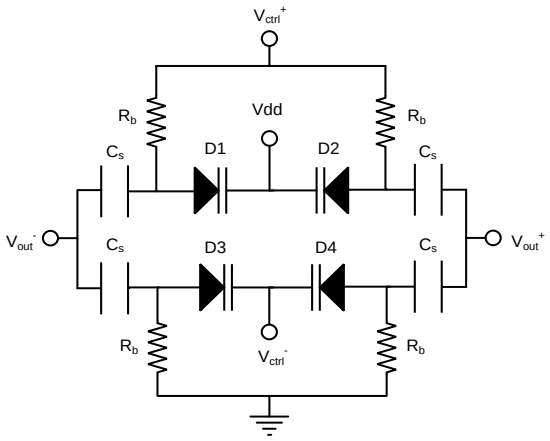



**Fig. 4.25:** Modified varactor configuration for differential tuning

The tuning characteristic of Fig. 4.25 can be found by plotting the C(V) characterisation curves for each of the branches separately and then superimposing them onto each other. The individual C(V) curves for each branch are shown in Figs. 4.26 and 4.27 for varactors in UMCs 90nm CMOS process, with their exact device dimensions being of no major significance to this discussion. For the characterisations, Vdd was 1V with ($V_{ctrl}$) varying from 0.25V $\rightarrow$ 0.75V to replicate the CP output voltage swing shown in section 4.3.2. Applying a 4.8GHz sine wave to both branches individually and plotting the resulting capacitance for each value of $V_{ctrl}$ then yielded the corresponding C(V) curves.

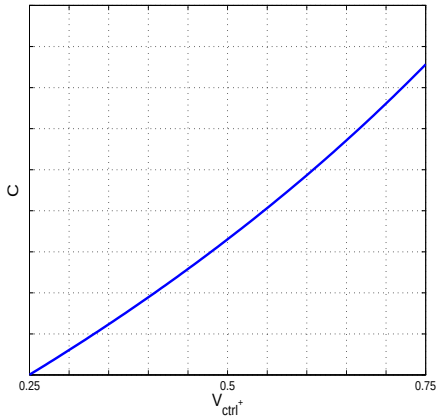



**Fig. 4.26:** C(V) curve for $D1$,$D2$ branch

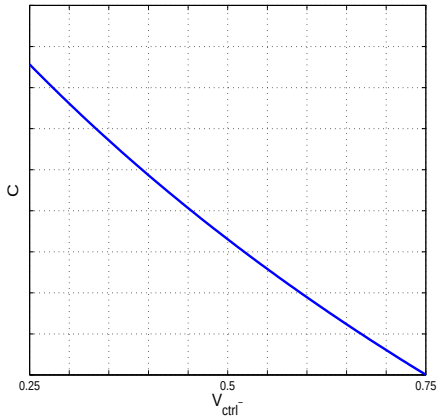



**Fig. 4.27:** C(V) curve for $D3$,$D4$ branch

The tuning characteristic for the differentially tuned varactor configuration of Fig. 4.25 can then be found by simply superimposing both curves on top of each other as shown in Fig. 4.28.

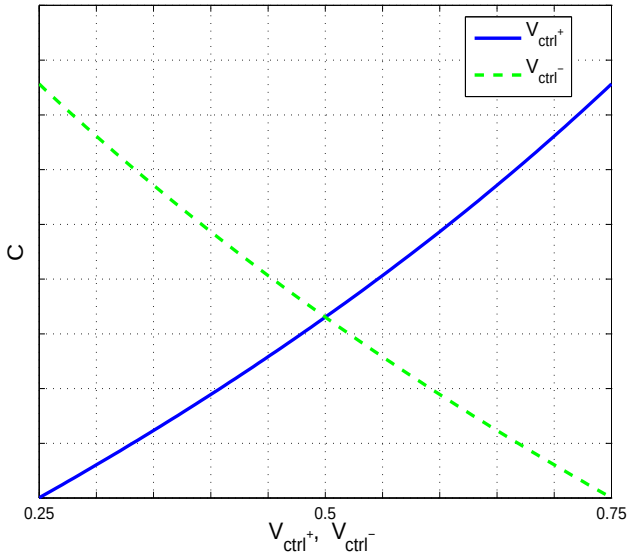



**Fig. 4.28:** Tuning characteristics for the modified differentially tuned varactor configuration

The operation of a differentially tuned VCO can now be explained with reference to Fig. 4.28. Given that $V_{ctrl-}$ and $V_{ctrl+}$ are connected to CP outputs $CP^-$ and $CP^+$ respectively in practice, when $V_{ctrl-}$ increases, $V_{ctrl+}$ proportionally decreases and vice versa. As a result, the capacitances of the LC-tank are altered correspondingly to restore the VCO (and hence PLL) back to its nominal frequency thus realising the standard operation for a CP-PLL, as discussed in section 2.3. This operation for the entire differential PLL is summarised in Table 4.8.

| | $UP$ | $DN$ | $\overline{UP}$ | $\overline{DN}$ | $CP^-$ | $V_{ctrl-}$ | $CP^+$ | $V_{ctrl+}$ | $\phi_{out}$ | $\phi_{fb}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $\phi_{ref} > \phi_{fb}$ | 1 | 0 | 0 | 1 | increase | | decrease | | increase | |
| $\phi_{ref} < \phi_{fb}$ | 0 | 1 | 1 | 0 | decrease | | increase | | decrease | |

**Table 4.8:** Operation table for a differential PLL

From Table 4.8 we can see that when $\phi_{ref} > \phi_{fb}$, the resulting PFD outputs force $CP^-$ and $CP^+$ to proportionally increase and decrease respectively resulting in proportional respective increases and decreases to $V_{ctrl-}$ and $V_{ctrl+}$. From Fig. 4.28 we can see that for $V_{ctrl-}$ and $V_{ctrl+}$ movements in such directions, the overall capacitance of the tank proportionally decreases which, from (3.3) produces a proportional increase in the oscillation frequency of the VCO. This in turn proportionally increases the PLL output frequency ($\phi_{out}$), forcing the feedback signal ($\phi_{fb}$) to increase such that it equals the input reference signal ($\phi_{ref}$), hence causing the PLL to lock. The exact opposite of this then occurs for the situation where $\phi_{ref} < \phi_{fb}$.

### 4.5.2 Common-Mode Biasing

The two curves in Fig. 4.28 are seen to intersect at a particular point. This is an extremely significant point as it represents the common-mode voltage ($V_{cm}$) for that particular varactor configuration. This was defined in (4.3) which showed it to be determined by the DC bias levels ($V_{DC}$) of the differential signals. For differential tuning, these correspond to the DC bias levels of each varactor branch which, for the configuration in Fig. 4.25 are seen to be Vdd and Vss. This therefore results in the following value for $V_{cm}$:

$$\begin{aligned} V_{cm} &= (Vdd + Vss)/2 \\ &= 0.5V \end{aligned}$$

as in agreement with Fig. 4.28.

Probably the most important criteria for differential tuning (and one which cannot be stressed enough) is that $V_{cm}$ must be set equal to the common-mode voltage of the differential tuning inputs ($V_{ctrl_{cm}}$). Given that the tuning inputs are connected to the CP outputs in practice, $V_{ctrl_{cm}}$ is set by the limits of the CP output voltage swing and so can be defined from (4.3) by replacing $V_{DC_1}$ and $V_{DC_2}$ with $V_{cp_{max}}$ and $V_{cp_{min}}$ (shown in Fig. 4.12). If $V_{cm} \neq V_{ctrl_{cm}}$, asymmetrical tuning results which reduces the tuning range of the VCO and, in extreme cases, even result in frequency deadzones for the end PLL. This can be best explained with the following example.

*Example*: Suppose a CP with output signal swings ranging from 0.3V $\rightarrow$ 0.6V was applied to the varactor configuration of Fig. 4.25. Therefore from the previous discussions, $V_{ctrl_{cm}} = ((0.3V + 0.6V)/2) = 0.45V$ and $V_{cm} = 0.5V$. As a result $V_{cm} \neq V_{ctrl_{cm}}$, hence giving rise to the tuning characteristic shown in Fig. 4.29.

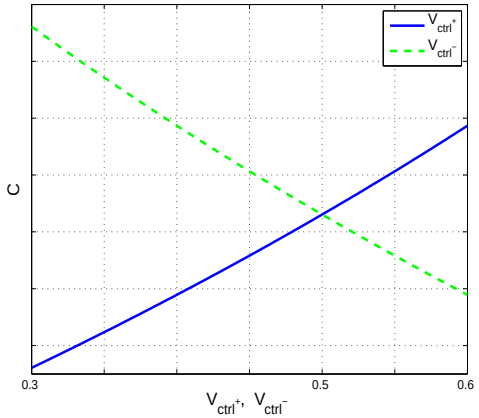



**Fig. 4.29:** Asymmetrical tuning

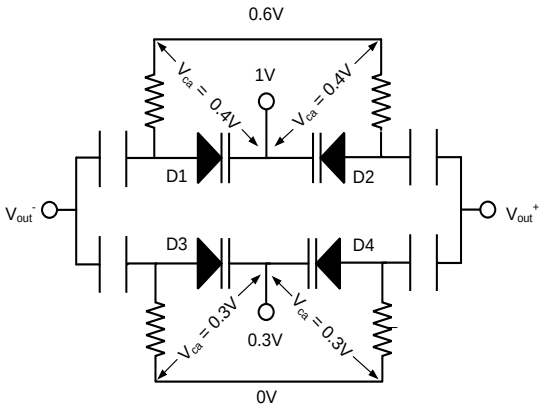



**Fig. 4.30:** Example values

Although the two curves in Fig. 4.29 intersect at 0.5V ($V_{cm} = 0.5V$), they are clearly seen to be asymmetrical over the CP voltage swing. How this reduces the tuning range can be seen by analysing the situation where $V_{ctrl^+} = 0.6V$ and $V_{ctrl^-} = 0.3V$. Such biasing is applied in Fig. 4.30 which show it to result in $V_{ca}$ values across $D1$ and $D2$ of 0.4V each, with those across $D3$ and $D4$ being 0.3V each. As a result, $D1$ and $D2$ become more reverse biased than $D3$ and $D4$ hence exhibiting lower capacitances (see section 3.4.2). This can be seen with reference to Fig. 4.29 where the resulting capacitances of the top and bottom branches for the applied biasing were 63.9fF and 64.5fF respectively. Again from looking at Fig. 4.29, such biasing can be seen to move $V_{ctrl^-}$ closer to its flatter region (see Fig. 3.23) with $V_{ctrl^+}$ remaining well within its dynamic region. As a result, the tuning capability of $V_{ctrl^-}$ is less than that of $V_{ctrl^+}$ thereby reducing the overall dynamic tuning range of the varactor configuration and leading to a reduced tuning range for the VCO. In extreme cases (i.e. when $V_{cm}$ is much different from $V_{ctrl_{cm}}$), the CP output voltage swing may occur over a flat region of one of the curves causing it to contribute negligible capacitance and hence frequency variation to the overall tuning characteristic. As a result, it may not be possible for the CP output voltage swing to enable the VCO realise its specified frequency range, thereby leading to frequency deadzones.

In addition to the above, asymmetrical tuning degrades the VCOs capability to reduce the effects of common-mode noise (generated from the CP as shown in section 4.3.2) on the tuning lines. As such noise ($\Delta v_{cm}$) occurs equally on both tuning lines, it perturbs their voltages as follows:

$$V_{ctrl^+} \rightarrow V_{ctrl^+} + |\Delta v_{cm}| \tag{4.36}$$

$$V_{ctrl^-} \rightarrow V_{ctrl^-} + |\Delta v_{cm}| \tag{4.37}$$

Suppose positive excursions of $\Delta v_{cm}$ occur. From (4.36) and (4.37) these can be seen to perturb $V_{ctrl^+}$ and $V_{ctrl^-}$ such that (from Fig. 4.28) capacitive variations of $+\Delta C^+$ and $-\Delta C^-$ are respectively produced. For such excursions, common-mode noise on the tuning inputs would only be completely rejected if:

$$|+\Delta C^+| = |-\Delta C^-| \tag{4.38}$$

In practice, (4.38) reduces to the requirement that the slopes of the sections traversed on each C(V) curve be identical. Since a varactor's C(V) curve is non-linear, its slope will vary across the CP output voltage swing. Therefore assuming the varactor devices are physically symmetrical (discussed in section 4.5.3), the slopes of the two traversed sections will only be identical (or close to that) if the same sections on each curve have been traversed. As this only occurs for symmetrical tuning, its common-mode noise rejection

capability (for noise on the tuning inputs) is therefore superior to that of asymmetrical tuning. This is verified in Fig. 4.31 which examines the common-mode noise rejection capability of the tuning inputs as $V_{cm}$ deviates from $V_{ctrl_{cm}}$.

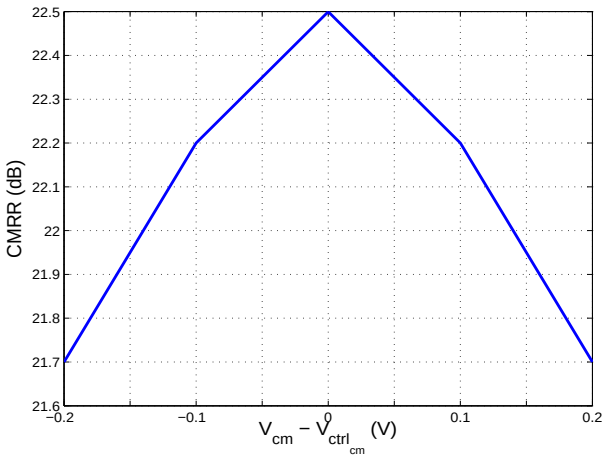



**Fig. 4.31:** Reduction in CMRR as $V_{cm}$ deviates from $V_{ctrl_{cm}}$

For the plot of Fig. 4.31, a VCO was built using the varactor configuration for differential tuning shown in Fig. 4.35, and the common-mode noise rejection capability of its tuning inputs quantified using the common-mode rejection ratio (CMRR) detailed in [67]. Maximum and minimum values for $V_{ctrl+}$ and $V_{ctrl-}$ were 0.75V and 0.25V respectively to set $V_{ctrl_{cm}}$ (and hence the nominal value for $V_{cm}$) equal to 0.5V. The DC bias levels for each varactor branch were then varied such that the resulting $V_{cm}$ values varied between 0.3V and 0.7V to give a variation either side of its nominal value of ± 0.2V (i.e. ±40%). Calculating the CMRR for each value of $V_{cm}$ thus yielded the resulting plot. Analysis of it clearly shows the maximum CMRR to be achieved only when $V_{cm} = V_{ctrl_{cm}}$ becoming increasingly degraded as the difference between $V_{cm}$ and $V_{ctrl_{cm}}$ grows. In other words, common-mode noise rejection capability of the tuning inputs is maximal for symmetrical tuning becoming increasingly less efficient as the tuning characteristic becomes more and more asymmetrical.

At this stage it should be clear that to maximise the dynamic tuning range and optimise common-mode noise rejection capability of a differentially tuned varactor configuration, the following must be strictly adhered to:

$$V_{cm} = V_{ctrl_{cm}} \tag{4.39}$$

Up to this point however, the physical symmetry of the varactor devices and the effects of noise on the Vdd and Vss lines have been ignored. In the following section these will be discussed and shown to greatly differentiate the performance of one varactor configuration for differential tuning over another.

### 4.5.3 Differentially Tuned Varactor Configurations

The four main configurations for differentially tuned varactors reported in literature are shown in Figs. 4.32 → 4.35.

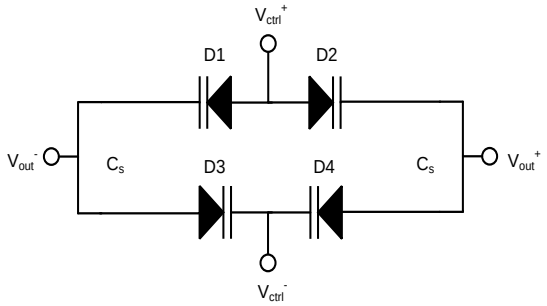



**Fig. 4.32:** Basic configuration

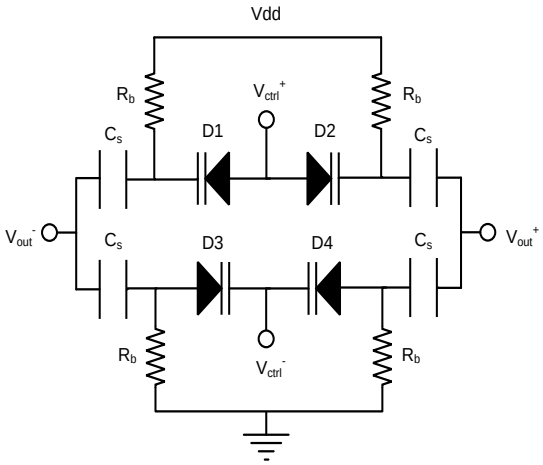



**Fig. 4.33:** Modified basic configuration

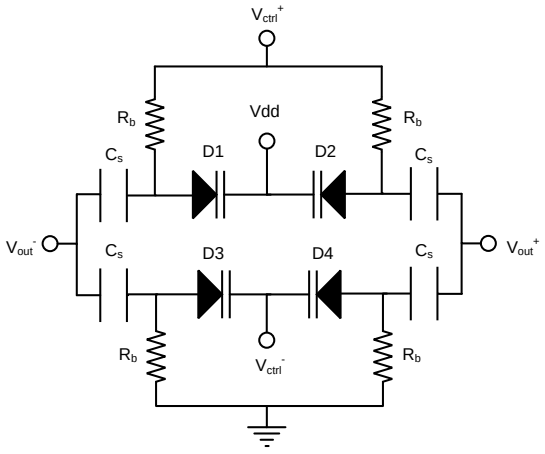



**Fig. 4.34:** Symmetrical tuning

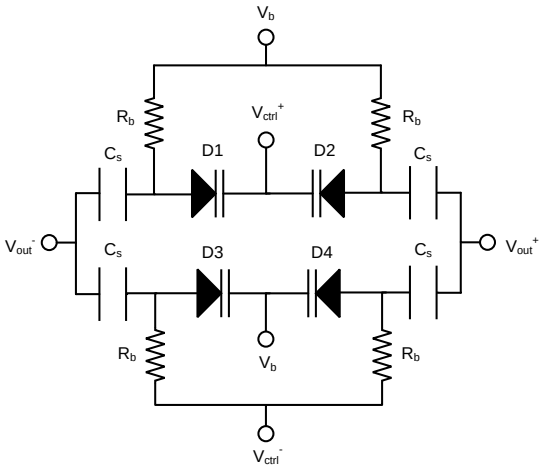



**Fig. 4.35:** Modified symmetrical tuning

The most basic configuration for differentially tuned varactors is shown in Fig. 4.32 [66] (originally shown in Fig. 4.24). Simple as it may be, this configuration exhibits many disadvantages which prohibit its use in practice. The first is that $V_{cm}$ is set by the DC bias level ($V_{DC}$) of the VCO. Therefore, as per (4.39) it is crucial to set $V_{DC}$ equal to $V_{ctrl_{cm}}$ with [68] reporting an elegant method for achieving this. However, as $V_{DC}$ is directly connected to Vdd and Vss, it is susceptible to noise on these lines, in addition to flicker noise from the bias source/sink [35]. This is a major disadvantage since, as $V_{DC} = V_{cm}$ any perturbations on $V_{DC}$ will deviate $V_{cm}$ from its nominal value hence resulting in

asymmetrical tuning and its associated disadvantages (shown in section 4.5.2). Another disadvantage with this configuration is its strong dependence on varactor device symmetry. This is because it employs both anode and cathode tuning resulting in the VCO output signal entering and leaving opposite varactor terminals in each branch. Therefore, only if the varactors exhibit identical C(V) characteristics across symmetry (i.e. C(V) behaviour is independent on input and output terminals) will the resulting C(V) curves be the same for both branches. If this is the case, and provided $V_{cm} = V_{ctrl_{cm}}$, total rejection of common-mode noise on the $V_{ctrl}$ line will be achieved. In practice however, varactor device symmetry is extremely process dependant and thus never perfect thereby further reducing the common-noise rejection capability of this configuration. These disadvantages, coupled with those discussed in section 3.4.2 for such diode varactor connections, make the configuration of Fig. 4.24 highly unattractive for differential tuning.

An improvement to the simple configuration of Fig. 4.32 is shown in Fig. 4.33 [35], [69], which employs a biasing scheme (identical to that discussed in section 3.4.2) to prevent the varactors from forward biasing without restricting the signal swings of their tuning inputs. The DC bias levels for the varactor branches are set by Vdd and Vss and not by the VCOs output bias level ($V_{DC}$). This means that $V_{cm}$ can no longer be affected by flicker noise from the source/sink but is nonetheless still susceptible to noise on the Vdd and Vss lines. In addition, the use of both anode and cathode tuning in this configuration still maintains the strong dependence on varactor device symmetry.

The dependence on varactor device symmetry is addressed by the configuration of Fig. 4.34 (originally shown in Fig. 4.25) which biases the varactors such that their overall tuning characteristic no longer relies on the physical symmetry of the devices. In addition, since the same biasing scheme as Fig. 4.33 is employed, this configuration prevents $V_{cm}$ being affected by flicker noise from the bias/source. However, it is still susceptible to noise on the Vdd and Vss lines.

The susceptibility of $V_{cm}$ to Vdd and Vss is partially addressed with the configuration of Fig. 4.35 [70].[9] This configuration sets the DC bias levels for both varactor branches using one biasing voltage ($V_b$), which from (4.3) equals $V_{cm}$. As such, $V_{cm}$ is no longer directly dependant on Vdd and Vss and hence to an extent, independent on noise from these lines. Nevertheless, $V_{cm}$ is now completely dependent on $V_b$ and so any noise occurring on it will result in asymmetrical tuning. If however we assume $V_b$ to be generated using a voltage regulator which is robustly designed, it would almost certainly exhibit less perturbations due to noise on the Vdd and Vss lines than the Vdd and Vss lines themselves. Therefore, under the assumption of a robustly designed voltage regulator, $V_b$ would prove a more attractive biasing potential, albeit at the cost of additional circuitry and its associated

[9]Note the biasing points of Fig. 4.35 appear opposite to that of Fig. 4.34. This is to maintain consistency with [70] and results in no change to performance or net behaviour of the VCO.

disadvantages.

For the configuration of Fig. 4.35, it is crucial to set $V_b$ so as to prevent the varactors from becoming forward biased over the CP output voltage swing. This is achieved by restricting $V_b$ to within the following range:

$$(V_{ctrl_{max}} - V_{FB}) \leq V_b \leq (V_{ctrl_{min}} + V_{FB}) \tag{4.40}$$

where $V_{FB}$ represents the voltage at which the varactors become forward biased (seen to be $\approx 0.5$ in Fig. 3.21). Given that the differential tuning inputs are connected to the CP outputs in practice, $V_{ctrl_{max}}$ and $V_{ctrl_{min}}$ correspond to $V_{cp_{max}}$ and $V_{cp_{min}}$ respectively in (4.12).

To put some numbers behind the above discussions, three separate VCOs were designed, each employing one of the configurations from Figs. 4.33 $\rightarrow$ 4.35.[10] All three VCOs were designed using UMCs 90nm CMOS process for operation in the same frequency range (around 4.8GHz) and to achieve the same tuning range. The common-mode rejection capability of their tuning inputs was then quantified using the common-mode rejection ratio (CMRR) detailed in [67] and applied in Fig. 4.31. To examine the effect of asymmetries introduced by noise on the Vdd and Vss lines in the tuning characteristics for Figs. 4.33 and 4.34, a DC voltage source of 10mV (i.e. 0.001% of Vdd) was placed in series with each line separately and the CMRRs for each case computed. To examine asymmetries introduced by noise on the $V_b$ line in Fig. 4.35, DC voltage sources of 10mV and 1mV were placed separately in series with it. The value of 1mV was used as it assumes a voltage regulator capable of noise rejection from the Vdd and Vss lines of 20dB is responsible for generating $V_b$. The value of 10mV was then used to account for a poorly designed voltage regulator, and to allow for a direct comparison with the previous configurations. In addition to all this, the CMRRs of each VCO without the additional voltage sources were also computed. The results are summarised in Table 4.9.

Firstly, Table 4.9 shows the CMRRs of all the architectures to degrade as a result of perturbations on the Vdd, Vss and $V_b$ lines, in agreement with the previous discussions. Secondly, it shows an improvement in CMRRs for the configuration of Fig. 4.34 over that of Fig. 4.33 by $\approx$ 3dB. As per the previous discussions, this improvement is attributed to the configuration of Fig. 4.34 being independent on varactor device symmetry. Thirdly, Table 4.9 shows the configuration of Fig. 4.35 to achieve a superior CMRR over that for Fig. 4.34 by $\approx$ 10dB. This is quite surprising since there only exists a small difference in biasing conditions between the two configurations/VCOs, implying that some unaccounted for effect has most likely occurred. Nevertheless, since the CMRR of Fig. 4.35 far outperforms that of the other two, it was employed in the final VCO of this thesis.

[10] The configuration of Fig. 4.32 was not employed due to its many impracticalities.

| Architecture | CMRR (dB) | Conditions |
|---|---|---|
| VCO employing | 8.88 | |
| varactor configuration | 8.78 | 10mV DC source in series with Vdd |
| of Fig. 4.33 | 8.76 | 10mV DC source in series with Vss |
| VCO employing | 11.95 | |
| varactor configuration | 11.4 | 10mV DC source in series with Vdd |
| of Fig. 4.34 | 11.77 | 10mV DC source in series with Vss |
| VCO employing | 22.5 | |
| varactor configuration | 22.4 | 10mV DC source in series with $V_b$ |
| of Fig. 4.35 | 22.49 | 1mV DC source in series with $V_b$ |

**Table 4.9:** CMRRs for differentially tuned varactor configurations

Finally it should be noted that the varactor configurations in Figs. 4.32 → 4.35 can also be implemented using AMOS varactors (see section 3.4.1). The AMOS equivalent configurations of Figs. 4.32 and 4.35 are reported in [71] and [72] respectively, with [67] reporting good symmetrical differential tuning characteristics for AMOS varactors fabricated using SOI technology. However, for UMCs 90nm CMOS process used to simulate the final PLL of this thesis, such symmetry for AMOS varactors was not observed. This is illustrated in Figs. 4.36 and 4.37 which show sample tuning characteristics for the AMOS equivalent configurations of Figs. 4.32 and 4.35 respectively. These clearly show the differential tuning characteristics to be asymmetrical resulting in poor common-mode noise reduction of the tuning inputs and reduced tuning ranges for the VCO. This, coupled with their other inferiority's over diode varactors seen for UMCs 90nm CMOS process in section 3.4.3, rendered AMOS varactors unsuitable for the intended application needs of the final VCO in this thesis.

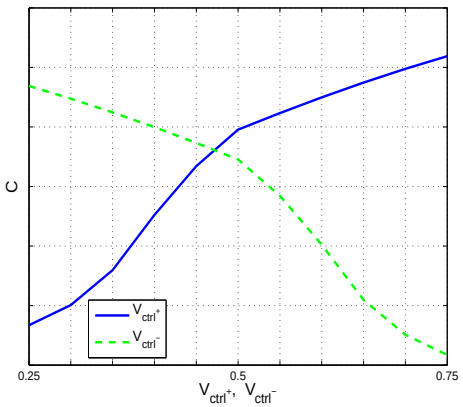



**Fig. 4.36:** Basic AMOS configuration

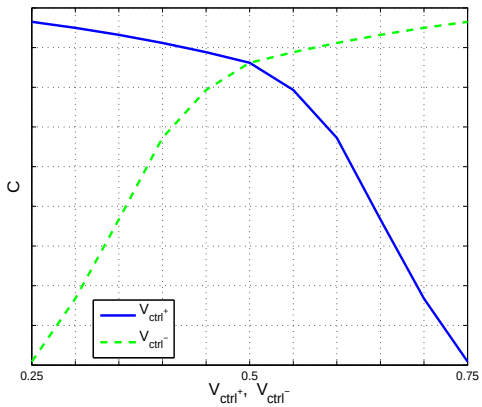



**Fig. 4.37:** Modified gate tuning

### 4.5.4 Performance Analysis

Differentially tuned VCOs exhibit various advantages over their single-ended tuned counterparts when used in either single-ended or differential PLLs. These, together with their disadvantages, are analysed below.

*Ellination of differential amplifier*: As already discussed, the use of a differentially tuned VCO in a differential PLL eliminates the need for a differential amplifier. This is in fact the main advantage with using a differentially tuned VCO in a differential PLL. To gain some perspective on the savings achieved, Fig. 4.38 shows the block diagram of the differential to single-ended conversion circuitry used in Analog Devices ADF4193 frequency synthesizer IC [21], to convert the differential LF outputs to single-ended control. This clearly shows differential to single-ended conversion to not be a straight forward task, requiring a significant amount of additional circuitry. With this comes an increase in design complexity, cost, time and resources which require additional silicon area, increase overall power consumption and may even degrade the noise performance of the PLL. As migrating to a differentially tuned VCO completely eliminates the need for such circuitry, it will avoid all these disadvantages thereby making it a much more preferable solution.

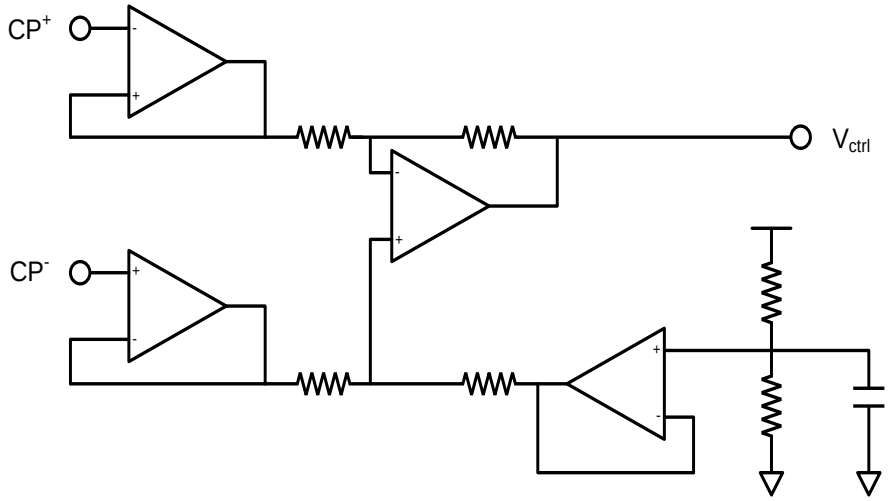



**Fig. 4.38:** Differential to single ended block diagram

*Common-mode noise*: A VCO with single-ended tuning in a single-ended PLL has no capability to reduce the effects of common-mode noise on its tuning input ($V_{ctrl}$). Therefore by definition, such a VCO has a CMRR = 0dB hence making it highly susceptible to common-moe noise from the CP (see section 4.3.2). In section 4.5.3, differentially tuned VCOs were seen in simulation to achieve a CMRR = 22.5dB thereby making them much more capable of reducing such common-mode noise effects. This figure for CMRR is

compared with those reported in previous works on differential tuning, in Table 4.10.

| Reference | [67] | [70] | [72] | This Work |
|---|---|---|---|---|
| CMRR(dB) | 20 | 29.4 | 30.2 | 22.5 |
| Varactor Device | AMOS | Diode | AMOS | Diode |
| Technology | 0.13$\mu$m SOI CMOS | 0.5$\mu$m SiGe BiCMOS | 0.18$\mu$m RFCMOS | 90nm CMOS |

**Table 4.10:** CMRR comparison against previous publications

From Table 4.10, the CMRR we achieved appears to be on the lower side of what has been reported. It is almost 3dB above the CMRR reported in [67] but still inferior to those reported in [70] and [72]. Since the differential tuning configuration we employed was taken from [70], our inferior CMRR to it is thought to be process related attributed to the standard CMOS process used by us and the SiGe BiCMOS process used in [70]. The highest reported CMRR was in [72] which is surprising since it employed an AMOS varactor configuration whose tuning characteristic for UMCs 90nm CMOS process was shown in Fig 4.38 to be very asymmetrical. This proves that such asymmetry is not consistent over all processes, where it appears from [72] that very good symmetry can be achieved using AMOS varactors in an RFCMOS process.

As good as the CMRR reported in [72] is, it (and all the others) is still much less than that obtainable with a differential amplifier. This represents a significant issue with differentially tuned VCOs over their single-ended tuned counterparts. This is because for VCOs employing single-ended tuing, reduction of common-mode noise from the CP will take place within the differential amplifier and not the VCO tank as is the case for VCOs employing differential tuning. Since typical CMRRs for differential amplifiers are $\approx$ 80dB [73],[74], they therefore offer far superior common-mode noise reduction than differentially tuned VCOs. The reason for this huge difference in CMRRs could be due to the fact that differential amplifier design is more mature than that for differentially tuned VCOs. If so, it is hoped that further research (see section 7.2) will enable the CMRRs of differentially tuned VCOs to be comparable with those for differential amplifiers. Nevertheless, at this point in time from the perspective of common-mode noise reduction, the use of a differential amplifier with single-ended tuning is more attractive than differentially tuned VCOs, albeit at the cost of additional circuitry and all the associated disadvantages previously discussed.

*Phase noise*: Although not a direct result of employing a differentially tuned VCO, it is at this point instructive to illustrate the reduction in VCO phase noise due to the larger output voltage swing of a differential CP. As per (4.10), differential operation enables the CP double its output voltage swings over that of a single-ended CP. As discussed in section 4.2.2, this halves the $K_{VCO}$ requirements of the VCO to achieve a specified tuning range, thereby reducing VCO phase noise. To verify this, two VCOs were designed and simulated using UMCs 90nm CMOS process to meet identical tuning ranges. One of the VCOs employed single-ended tuning with the other employing differential tuning. As a result, the average $K_{VCO}$ for the differentially tuned VCO was $\approx$ 50MHz/V with that for the VCO employing singled ended tuning being $\approx$ 100MHz/V. The phase noise ($PN$) performance of both VCOs was simulated with the results shown in Fig. 4.39. This clearly shows a reduction in VCO phase noise due to differential tuning. Measurements taken at 100kHz offset from the carrier frequency show a phase noise reduction of 3dB, attributed to a reduction in noise transfer from the tuning inputs and improvements in the LC-tanks quality factor ($Q_{tank}$). Measurements taken at 10kHz offset from the carrier frequency then show this phase noise improvement to reduce slightly to 2dB, implying the reduction of flicker noise effects to be less than for noise on the tuning inputs.

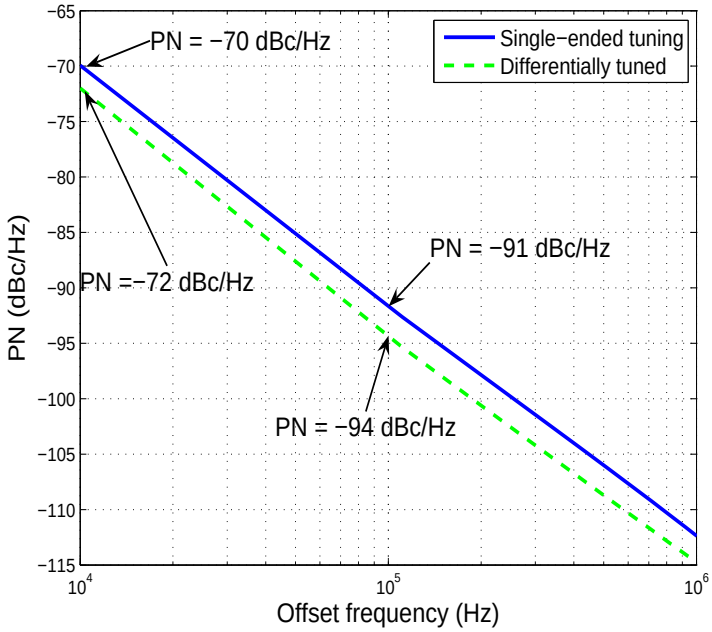



**Fig. 4.39:** Simulated phase noise improvement due to differential operation

Overall, the analysis performed in this section showed the various advantages of differentially tuned VCOs. In comparison to VCOs with single-ended tuning in a single-ended PLL, differentially tuned VCOs offer reduction of common-mode noise effects from

the CP, with the enlarged output voltage swing of the differential CP enabling significant reductions in VCO phase noise. In comparison to VCOs with single-ended tuning in a differential PLL, differentially tuned VCOs eliminate the need for a differential amplifier and all its associated disadvantages, albeit at the cost of reduced common-mode noise reduction. Nevertheless, due to the significance of eliminating the differential amplifier, it was decided to employ a differentially tuned VCO in the final PLL of this thesis, whose core schematic is shown in Fig. 4.40.[11]

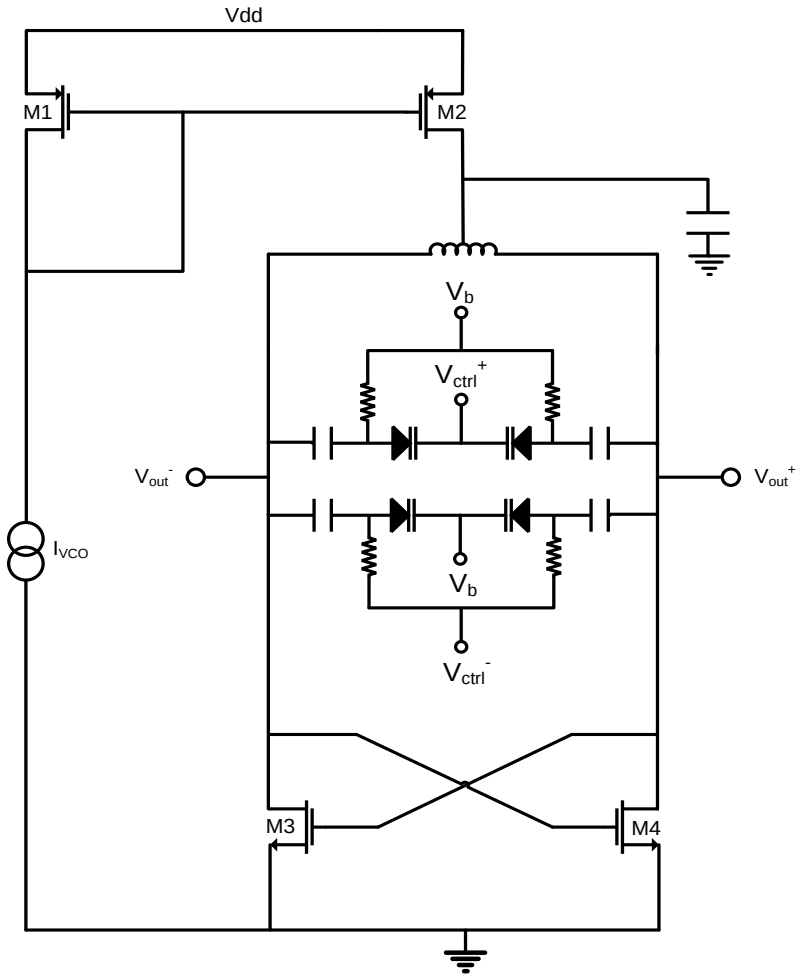



**Fig. 4.40:** Schematic of the differential VCO used in the final PLL of this thesis

The schematic of Fig. 4.40 shows the VCO to be based on the PVT robust hybrid topology of Fig. 3.37, with the additional capacitor included to somewhat suppress flicker noise effects (see section 3.8). It should be noted that for this VCO architecture, a differential inductor was used with its centre tap connected to the drain of $M2$. This is because if symmetrical single-ended inductors are used in the applied architecture, two are

[11] W/L ratios, operating points and component dimensions pertaining to Fig. 4.40 are detailed in section 6.4.

required to be connected in series, with the drain of $M2$ connected between them. This is to ensure symmetrical differential outputs such that capacitance and inductance values will remain consistent with their characterised values, in addition to reducing non-linearities in the varactor C(V) curve. The first problem with such a series configuration is that it consumes more silicon area for a given inductance [75], with simulations using UMCs 90nm CMOS process showing it to consume $\approx 30\%$ more silicon area than a differential inductor for the same inductance. The second problem with such a series configuration is that it exhibits inferior quality factors ($Q_L$) to a differential inductor for a given inductance [76], [77], with simulations using UMCs 90nm CMOS process showing it to exhibit quality factors $\approx 25\%$ less than a differential inductor for the same inductance. Therefore, due to its ability to reduce silicon area requirements and improve quality factors when used in the architecture of Fig. 4.40, a differential inductor was employed.[12] The design procedure used for the schematic of Fig. 4.40 is then outlined in Appendix B3.

## 4.6 Summary and Achievements of this Chapter

This chapter was written with three goals in mind. The first was to introduce differential operation in a general sense and demonstrate its general performance advantages, namely reduction of common-mode noise and doubled output voltage swing. This was achieved in sections 4.1 and 4.2.

The next goal of this chapter was, as stated in section 4.2.3, to completely justify the conversion of a conventional PLL to fully differential operation. Section 4.3 showed how to convert a single-ended CP to differential operation, through which it illustrated a differential CP to exhibit the following performance advantages over its single-ended counterpart:

- Reduction in common-mode noise effects by almost 200dB.
- Reduction in mismatch current by three orders of magnitude.
- Doubled output voltage swing.

These advantages thus justify the conversion of a single-ended CP to differential operation as it is more attractive to low noise PLL operation, wideband VCO/PLL operation and low technology nodes with reduced voltage supplies.

The use of a differential CP then necessitates the use of a differential LF with section 4.4 showing how to convert a single-ended LF to differential operation. Through this, the

[12] Differential inductors are not necessarily optimal for all VCO architectures. For example, the doubled cross-coupled topology of Fig. 3.36 permits the symmetrical single-ended inductors to be combined into a bulk inductance with simulations showing comparable quality factors and reduced area requirements to differential inductors.

resulting differential LF was shown to realise the following advantage over its single-ended counterpart:

- Reduction in silicon area requirements by approximately a factor of two.

This advantage makes the differential LF more feasible to on-chip implementation with its off-chip implementation requiring roughly the same PCB effort as a single-ended LF.

Section 4.5 showed how to convert a VCO with single-ended tuning to one with differential tuning. Although this is not necessitated by the use of a differential LF, section 4.5 showed a differentially tuned VCO to realise the following performance advantages over its single-ended counterpart:

- No differential amplifier required between the differential LF and VCO.
- CMRR of 22.5dB with up to 30dB being reported in literature.

These advantages justify the conversion of a VCO with single-ended tuning to one with differential tuning as it offers potentially lower noise operation whilst reducing design complexity, cost, time, resources, silicon area and power consumption.

The third goal of this chapter followed on from the second in that it further justifies the use of a fully differential PLL, but by showing how such a PLL can effectively address some of the issues with PLLs outlined in chapters 2 and 3. Section 2.3.1 stated static phase offset to be a major issue in PLLs. This was addressed by the capability of a differential CP to significantly reduce CP mismatch current and practically eliminate the effect of unequal pulse arrival times, thereby significantly lowering static phase offset. Section 2.8.3 stated achieving low noise PLL operation without relying on additional power or increasing loop bandwidth to be a major issue. This was addressed by the capability of a fully differential PLL to significantly reduce static phase offset, common-mode noise effects, VCO phase noise and eliminate any noise due to a differential amplifier on the VCO tuning inputs. Furthermore, this was achieved without increasing loop bandwidth or significantly increasing power consumption. Section 3.9 stated the simultaneous requirements for low VCO phase noise and large tuning ranges to be a major issue. This was addressed by the differential CP whose doubled output voltage swing halved $K_{VCO}$ requirements for a specified tuning range, thereby achieving reductions in flicker noise effects and a 3dB reduction in noise from the tuning inputs. A further improvement on this issue is achieved with the architecture introduced in chapter 5. Section 3.9 also stated the requirement of a differential amplifier between a differential LF and VCO with single-ended tuning to be an issue. This was addressed by the differentially tuned VCO which completely eliminates the need for such a differential amplifier. The remaining issues outlined in chapters 2 and 3 not addressed in this chapter, will thus be addressed in chapter 5.

Overall this chapter can be best summed up with the question: *"Why should I use a fully differential PLL?"* The answer to this is summarised in Fig. 4.41.

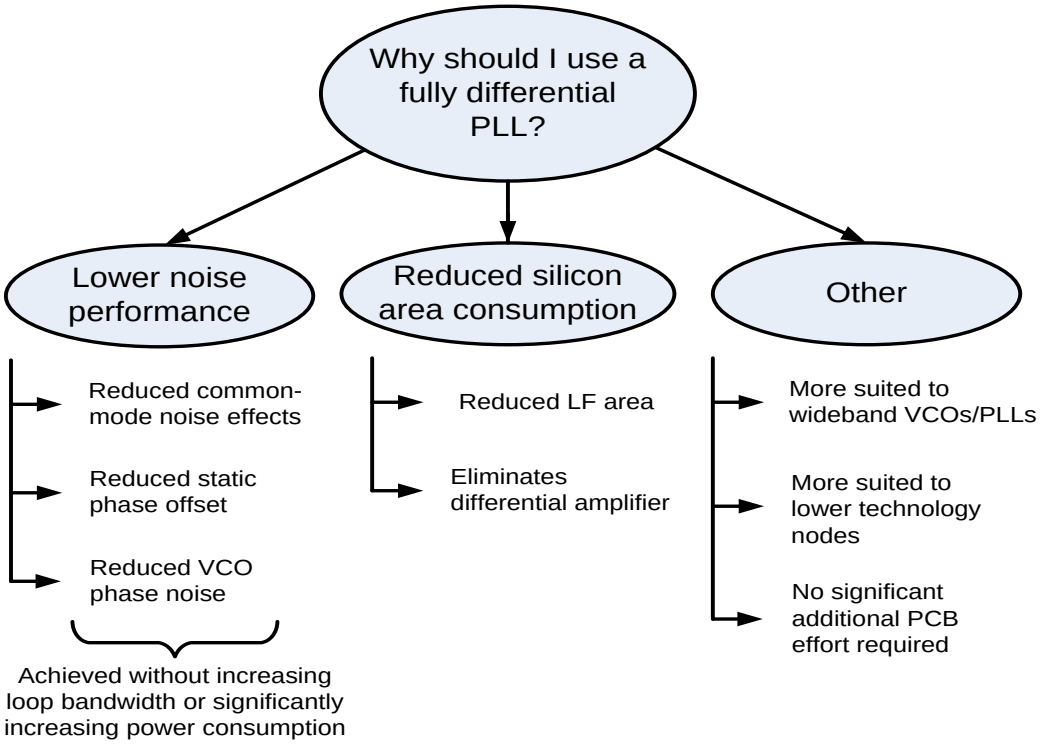



**Fig. 4.41:** Justification for a fully differential PLL

It should however be noted that fully differential PLLs come with some disadvantages. With reference to the differential CP these are more complex circuitry and the need for common-mode feedback circuitry. With reference to the differential LF these are increases in thermal noise by a factor of two. Finally with reference to the differentially tuned VCO, the disadvantage is inferior CMRR's over their differential amplifier alternatives.

To complete this chapter, the block diagram for a fully differential PLL (which the final PLL of this thesis was based on) is shown in Fig. 4.42.[13] This gives a block level view of the differential CP and differentially tuned VCO (underlying schematics are referenced inside the blocks) whilst presenting a component level view of the transformed differential LF. The PFD and feedback divider (/N) are then maintained at block level with no underlying schematics referenced, since these were synthesised using VHDL in the final design. The only additional block included is a buffer placed at the VCO outputs, required to make it independent on loading conditions, in addition to enabling the PLL output signal be used elsewhere on the IC or off-chip.

[13] W/L ratios, operating points, component dimensions and all other relevant design data pertaining to Fig. 4.42 are detailed in chapter 6.

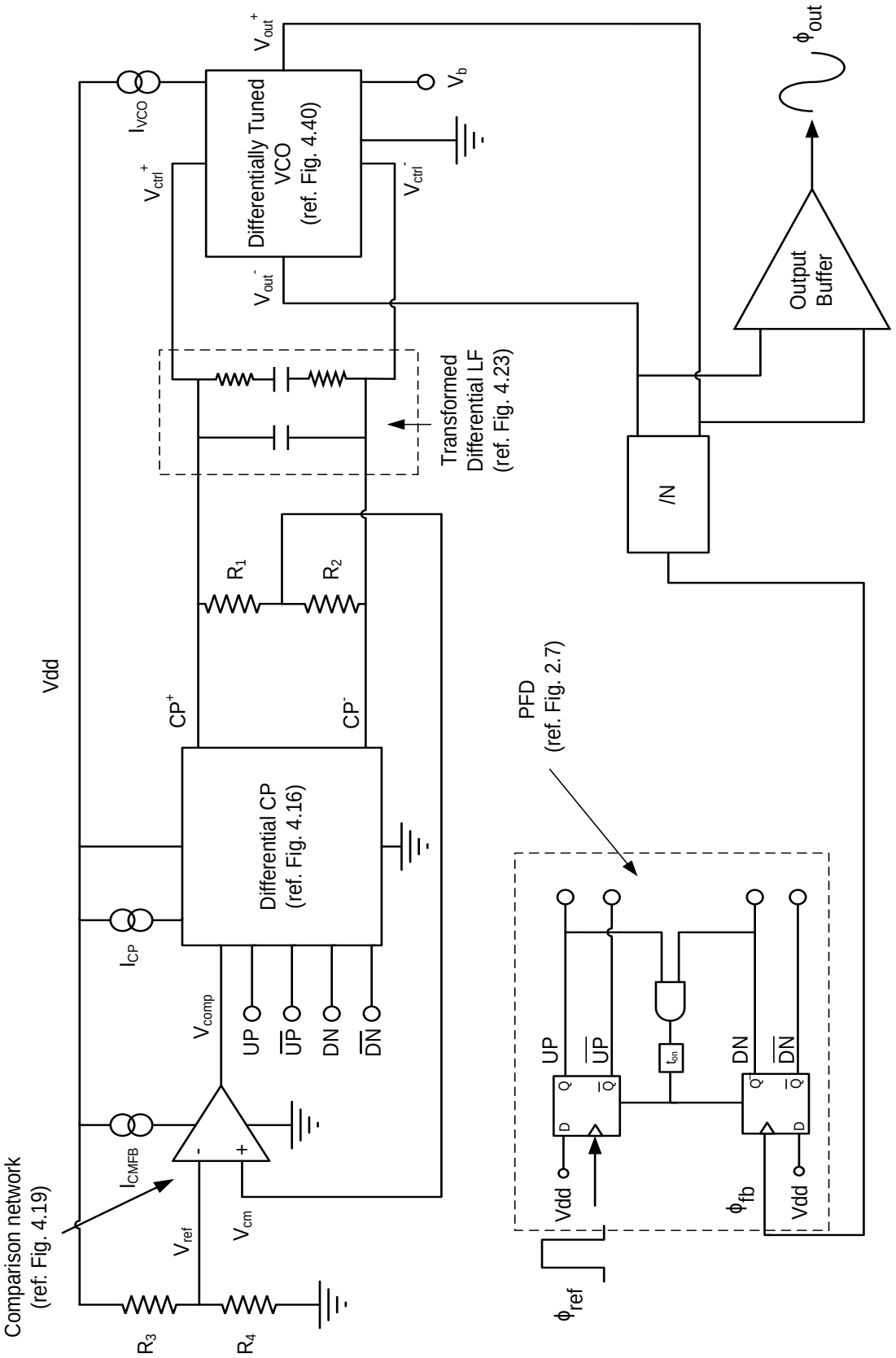



**Fig. 4.42:** Block diagram for a fully differential PLL

# CHAPTER 5

## Managing Loop Bandwidth Variation

The concept of loop bandwidth ($K$) was introduced in section 2.7 as the most important design parameter of a PLL. Variation of $K$ from its nominal value ($\Delta K$) was then shown in section 2.7.4 to be a major design concern giving rise to the many issues detailed in section 2.7.4. As such, the reduction of $\Delta K$ is important in PLL design. This chapter describes its various sources and how each can be individually reduced to result in an overall reduction of $\Delta K$. In particular, it focuses on one source whose reduction is not a straight forward task, thus requiring unconventional novel approaches to address it.

For reasons discussed in section 2.6.4, the final PLL of this thesis employs a second-order passive lag-lead LF thereby rendering it a third-order type 2 PLL. As such, all discussions pertaining to $\Delta K$ reduction will herein be with reference to this PLL architecture.

## 5.1 Sources of Loop Bandwidth Variation

The loop bandwidth of a third-order type two PLL was approximated in (2.44), under the assumption that the ratio of the LF capacitance's ($C_2/C_1$) was sufficiently large. Using this approximation (and assumption), $\Delta K$ can be defined as follows:

$$\Delta K = \frac{\Delta I_{cp} \Delta K_{VCO} \Delta R_1}{2\pi \Delta N} \tag{5.1}$$

From (5.1), the following contributors to $\Delta K$ can be identified.

*Variation of feedback divider ratio ($\Delta N$)*: To enable multiple output frequencies from the PLL, $N$ must vary thereby resulting in $\Delta N$. For a frequency synthesizer (see chapter 1),

$\Delta N$ is determined by the number of channels required by the applied wireless standard. Since a large number of channels are typically employed (*for example*: WCDMA standard employs 196 channels), $\Delta N$ is typically large thereby significantly contributing to $\Delta K$.

*Variation of LF resistor ($\Delta R_1$)*: Resistances always vary from their nominal values in practice with the resulting variations being largely dependant on the type of resistor used. For off-chip LFs, $R_1$ is realised as a surface mount device (SMD) placed on the printed circuit board (PCB). SMD resistors are typically realised by placing a layer of metal oxide resistance onto a ceramic substrate whose resistance value is controlled by increasing the desired thickness, length or type of deposited film being used. This process is highly accurate in manufacturing thereby enabling resistance variations as low as 0.05% [78] to be realised. As such, for off-chip LFs, $\Delta R_1$ does not significantly contribute to $\Delta K$. The situation is however much different for on-chip LFs whose resistances are realised either in an $n$-well or with polysilicon. Although polysilicon resistors are more commonly employed due to their lower temperature and voltage co-efficients, they still exhibit large resistance variations over process, voltage and temperature (PVT) variation and so significantly contribute to $\Delta K$ (by up tp 35%, see section 6.3.1).

*Variation of charge-pump current ($\Delta I_{cp}$)*: In (4.16), $I_{cp}$ was shown to be derived from the bandgap voltage ($V_{bg}$) as a "bandgap over R" current. Therefore, any variations in the current defining resistor ($R_{I_{cp}}$) gives corresponding variations in $I_{cp}$. For off-chip resistors, such variation ($\Delta I_{cp}$) is small (see above). However, for on-chip resistors, $\Delta I_{cp}$ is significantly larger (see above) leading to correspondingly significant variations in $K$. Section 4.3.2 also showed $I_{cp}$ to vary over the CP output voltage swing ($\Delta_{i_{cp,V_{cp}}}$) as a result of channel length modulation effects. As Table 4.3 showed $\Delta_{i_{cp,V_{cp}}}$ values up to 4% occurring in practice, such variation therefore also significantly contributes to $\Delta K$.

*Variation of VCO gain ($\Delta K_{VCO}$)*: Section 3.4.3 showed $K_{VCO}$ to arise due to varactor non-linearity. This is termed in-band $K_{VCO}$ variation ($\Delta K_{VCO_{inb}}$) which simulations have shown can vary by as much as 50% over the CP output voltage swing. In section 5.2.3 a second type of $K_{VCO}$ variation will be discussed which also significantly contributes to its overall variation ($K_{VCO}$). As such, $\Delta K_{VCO}$ is a major contributor to $\Delta K$.

The above discussions alone show the extent of $\Delta K$ to be very extreme. Fortunately, various techniques can be used to effectively eliminate most of its sources. Firstly, $\Delta K$ due to $\Delta N$ can be effectively eliminated by making $I_{cp}$ a function of $N$ such that the resulting $I_{cp}(N)$ varies in proportion to $N$. This is achieved in practice by digitally adjusting $I_{cp}$ such that when $N$ increases by a factor of $x$, $I_{cp}$ decreases by the same factor (and vice

versa) thereby resulting in no net change to $\Delta K$ from $\Delta N$.

Secondly, $\Delta K$ due to $\Delta R_1$ and $\Delta I_{cp}$ can be simultaneously effectively eliminated by observing the following from (5.1).

$$\Delta K \propto \Delta I_{cp} \quad and \quad \Delta K \propto \Delta R_1 \tag{5.2}$$

Inserting (4.16) into the first proportionality thus yields:

$$\Delta K \propto \frac{1}{\Delta R_{I_{cp}}} \quad and \quad \Delta K \propto \Delta R_1 \tag{5.3}$$

In other words, if the resistance variation in the LF resistor ($R_1$) is the same as that for the $I_{cp}$ current defining resistor ($R_{I_{cp}}$), their resistance variations will give no net change to $\Delta K$. In practice this reduces to making both resistors of the same type. For example, if the LF is implemented off-chip, $R_{I_{cp}}$ must be realised using the same SMD resistor type as $R_1$. This can be seen in Analog Devices ADF4351 frequency synthesizer IC [22] employing an off-chip LF where, to reduce $\Delta K$, a separate pin (pin 23 - "$R_{SET}$") is connected to an external resistor to accurately define $I_{cp}$. As such, off-chip LFs typically require one extra pin in addition to those required for the LF input and outputs. For the case of on-chip LFs, $R_1$ and $R_{I_{cp}}$ must be realised using the same material (typically polysilicon) and be laid out very close to each other such that their mismatches are localised (i.e. affect both resistors equally).

Thirdly, $\Delta K$ due to $\Delta_{i_{cp,V_{cp}}}$ can be decreased by increasing the output conductance's of the matching critical transistors within the CP as discussed in section 4.3.2.

Therefore, applying the above techniques eliminate many sources of $\Delta K$, thereby simplifying the problem to an issue of $\Delta K_{VCO}$. The issue of in-band $K_{VCO}$ variation ($\Delta K_{VCO_{inb}}$) was somewhat addressed by choosing diode varactors over AMOS varactors due to their higher linearity seen in section 3.4.3 for UMCs 90nm CMOS process. However, the issue still remains prevalent with a second source of $\Delta K_{VCO}$ occurring for sub-banded VCOs being potentially more prevalent. Before this source of $K_{VCO}$ variation can be discussed however, the concept of VCO sub-banding must first be introduced.

## 5.2 VCO Sub-banding

As stated in section 3.9, modern day VCOs must exhibit large tuning ranges to account for PVT variation and to enable multi-band (or standard) operation in wireless communication system. This, coupled with the reduced supply voltages that accompany modern low technology nodes, imply a high $K_{VCO}$ is necessary. However, as shown in sections 4.2.2 and 4.5.4, phase noise increases with $K_{VCO}$ thereby making the simultaneous realisation of large tuning ranges and low phase noise performance, extremely challenging.

This issue was partially addressed in chapter 4 with differential tuning which, as shown in section 4.5.4 halves $K_{VCO}$ requirements for a specified tuning range thereby leading to the phase noise improvements seen in Fig. 4.39. This issue can then be further addressed with sub-banding [79].

The concept of sub-banding is simply to divide the specified tuning range into $n$ discrete sub-bands such that it can be realised with much smaller $K_{VCO}$ values, as illustrated in Fig. 5.1.

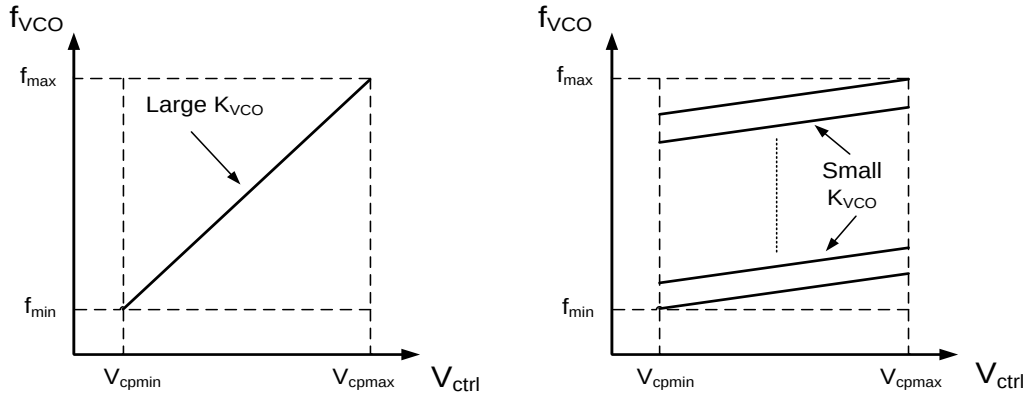



**Fig. 5.1:** Concept of sub-banding

As shown in Fig. 5.1, sub-banding greatly reduces the $K_{VCO}$ requirements for a specified tuning range thereby enabling large tuning ranges to be realised with improved phase noise performance (see section 4.2.2) over the case without sub-banding.

### 5.2.1 Principles of VCO Sub-banding

Dividing the tuning range into $n$ sub-bands is conventionally achieved using a switched capacitor array (SCA) which consists of $n-1$ equi-valued (or binary weighted) switchable capacitors. The switching in(out) of one capacitor adds to (subtracts from) the total tank capacitance, forcing VCO operation to move down(up) one sub-band respectively. The switches themselves are digitally controlled thereby requiring digital calibration methods, discussed in section 6.4.3.

Each switchable capacitor comprises a branch, and so the division of a tuning range into $n$ sub-bands requires $n-1$ such branches. This is illustrated in Fig. 5.2 which shows the implementation of a basic SCA in a VCO based on the hybrid VCO topology of Fig. 3.37. From this illustration we can see each branch to be selectable via a thermometer encoded digital word, $n-1$ bits long in practice. For example, if it is desired to divide a tuning range into 4 sub-bands, a 3 branch SCA is required which is controlled by a 3 bit digital word. The first branch is thus selectable by the word "001", the second by the

word "011" and the third by the word "111", with all branches being switched out by the word "000" thereby enabling operation in the highest frequency band.

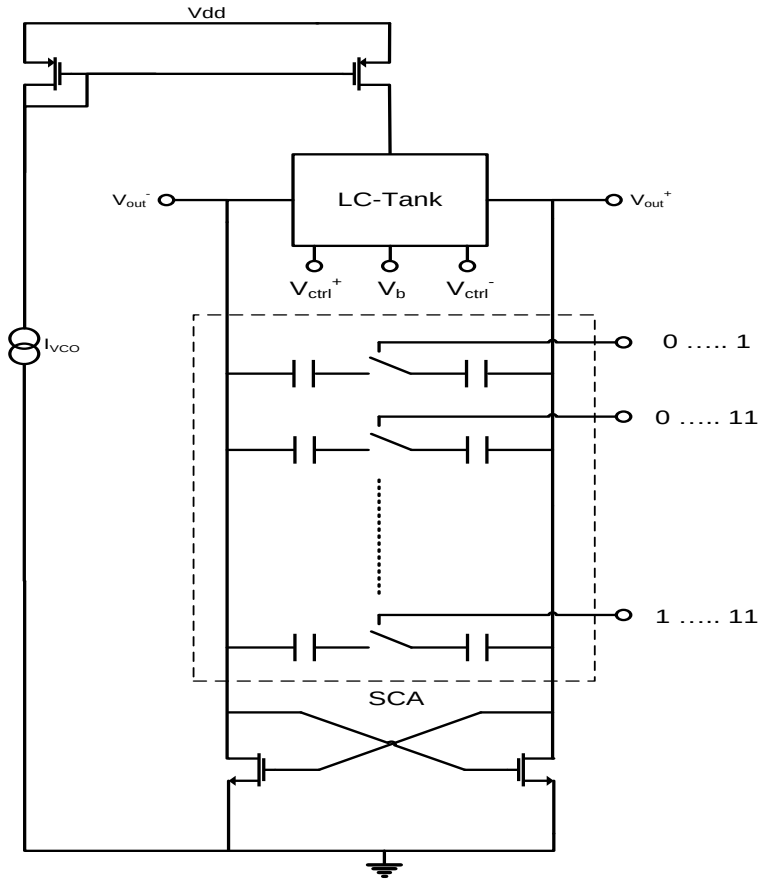



**Fig. 5.2:** Implementation of a basic SCA in a VCO

The choice of how many sub-bands to use is largely dictated by phase noise (although specified power consumption does also play a role) and hence by the desired value for $K_{VCO}$. Ignoring $K_{VCO}$ variation, the $K_{VCO}$ required to cover a specified frequency range can be expressed as follows (see Appendix A.13):

$$K_{VCO} = \frac{\Delta F}{nV_{swing_{cp}}}(1 + OV) \tag{5.4}$$

In (5.4), the factor $\Delta F$ represents the total frequency range of the VCO (defined as $f_{max} - f_{min}$) where $OV$ represents the percentage overlap between sub-bands. This is required to ensure the entire frequency spectrum of $\Delta F$ is covered over PVT variation where, for VCOs designed using UMCs 90nm CMOS process, percentage overlaps of $\geq 30\%$ (i.e. $OV \geq 0.3$) were found to be sufficient.

Equation (5.4) shows $K_{VCO}$ to be inversely proportional to $n$ and so decreases by increasing the number of branches in the SCA. This alone would suggest including as

many branches in the SCA as possible to make $K_{VCO}$ (and hence phase noise) as low as possible. In practice however this can result in diminishing returns regarding phase noise improvement in addition to increasing overall power consumption. Why this is so can be seen by examining the parallel resistance of the branches $R_{p_{br}}$.[1] Given that these are placed parallel to each other in the SCA, the resulting parallel resistance of the SCA ($R_{p_{SCA}}$) is quantified as follows:

$$R_{p_{SCA}} = \frac{R_{p_{br}}}{n} \tag{5.5}$$

Typically in practice $R_{p_{br}}$ varies from branch to branch, in which case the worst case (i.e. lowest) value for it should be used in calculations. As the SCA is in parallel to the tank, its parallel resistance reduces that of the VCO ($R_p$) by the following factor ($X_{SCA}$) (see Appendix A.14):

$$X_{SCA} = \frac{R_{p_{SCA}}}{R_{p_{SCA}} + R_{p_{Tank}}} \tag{5.6}$$

where $R_{p_{Tank}}$ represents the specific parallel resistance of the tank.

Firstly, re-calling (3.20) this will increase the $g_m$ requirements to sustain oscillation and hence overall power consumption by a factor of $X_{SCA}$. Inserting (5.5) into (5.6) reveals $X_{SCA} \propto n$ and so increases with $n$ (i.e. as the number of branches increases). This therefore leads to increases in overall power consumption for growing $n$.

Secondly, reworking (3.11), $Q_{tank}$ at resonance can be approximated as:

$$Q_{tank} \approx \sqrt{\frac{R_p}{R_s}} \tag{5.7}$$

Therefore, $Q_{tank}$ will be reduced (or loaded down) by $\sqrt{K_{SCA}}$ which, recalling (3.27) increases VCO phase noise by $10 \cdot log(K_{SCA})$ dB. As before, this effect increases with growing $n$ i.e. as the number of branches in the SCA increases.

In addition to this, each branch has a parasitic capacitance ($C_{par_{br}}$) associated with it (ignored by (5.4)) which reduces the tuning range by a factor of $1/\Delta C_p$ (see Appendix A.15). The factor $\Delta C_p$ is defined as:

$$\Delta C_p = \frac{C_{VCO} + (n \cdot C_{par_{br}})}{C_{VCO}} \tag{5.8}$$

where the overall capacitance of the VCO, neglecting that due to the parasitics of the branch, is represented by $C_{VCO}$. This reduction needs to be compensated for by increasing $K_{VCO}$ by a specific factor (defined in (5.10)) such that the specified tuning range is restored. As seen in (5.8), $\Delta C \propto n$ thereby resulting in progressively larger $K_{VCO}$ values

[1] Using $S$-parameters, the parallel resistance of a branch is computed as $R_p = 1/Re\{Y\}$ or $R_p = (Re\{Z\}^2 + Im\{Z\}^2)/Re\{Z\}$, where $Re\{Y\}$ represents the real part of the series admittance and $Re\{Z\}$ and $Im\{Z\}$ represent the real and imaginary parts of the series impedance respectively.

required to restore the specified tuning range as the number of branches in the SCA increases. With this comes a hand in hand increase in phase noise for growing $n$.

Therefore, as the number of branches in a SCA increases, the phase noise improvement reduces, eventually resulting in diminishing returns whilst increasing overall power consumption. As such, the number of sub-bands used becomes limited with 4, 8 or 16 bands being typically employed in practice.[2]

Once the number of sub-bands has been chosen, the required capacitance to switch in ($C_{sw}$) for a specified percentage overlap (assuming equi-valued capacitors are employed) can be calculated as follows (see Appendix A.16):

$$C_{sw} = \frac{\left(\left(\frac{f_{max_i}}{(f_{max_i} - f_{min_i})OV + f_{min_i}}\right)^2 - 1\right)}{L(2\pi f_{max_i})^2} \tag{5.9}$$

The subscript $i$ in (5.9) refers to the $i^{th}$ sub-band, where in practice it is easiest to calculate $C_{sw}$ with reference to the top sub-band i.e. by setting $f_{max_i} = F_{max}$ and $f_{min_i} = F_{max} - (K_{VCO}V_{swing_{cp}})$. Equation 5.9 is the total capacitance to be switched in by the branch and thus represents the difference between the on and off capacitance's of the branch. Since the off capacitance of the branch (i.e. the branch capacitance when switched off) is undesired, it is referred to as a parasitic capacitance $C_{par_{br}}$ which must be added onto (5.9) to prevent it reducing the effective capacitance switched in by the branch. This approach can however result in an endless iterative loop, for which the design procedure of Appendix B4 should be used to avoid.

### 5.2.2 SCA Switch Design

In Fig. 5.2, the SCA switches were shown as ideal devices. In practice these are realised with a MOSFET device whose basic implementation is shown in Fig. 5.3.

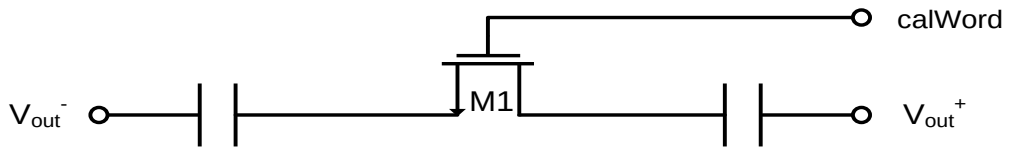



**Fig. 5.3:** Basic implementation of an SCA switch

In Fig. 5.3, the SCA switch is realised using a NMOS device ($M1$) (although a PMOS device could also be used) which ideally switches on or off upon the application of a logic high ('1') or low ('0') signal respectively from the calibration word ("calWord"). In practice

[2]If the resulting $K_{VCO}$ values for a specified tuning range are still too large after the number of sub-bands has been saturated, a multiple VCO approach could be pursued as is done in Analog Devices AD4350 wideband frequency synthesizer IC [80].

however this does not occur as the source of $M1$ is floating resulting in an undefined gate-source voltage ($V_{gs}$). As such, it is not possible to guarantee if $V_{gs} > V_{t_{M1}}$ or $< V_{t_{M1}}$ to switch $M1$ on or off respectively so as the corresponding branch can respectively add to or subtract from the tank capacitance. Therefore, a more practical implementation of an SCA switch is shown in Fig. 5.4 [54]. This is formed by adding NMOS devices $M2$ and $M3$ onto the basic implementation of Fig. 5.3. The role of $M2$ is to clamp the source of $M1$ to Vss upon the application of a logic high signal hence guaranteeing $V_{gs} > V_{t_{M1}}$ and that $M1$ turns on. The role of $M3$ is then to clamp the drain of $M1$ to the same potential as its source (Vss) such that the drain-source voltage across $M1$ ($V_{ds_{M1}}$) is zero. This (ideally) results in zero on-resistance($R_{on}$) for $M1$ hence minimising its loss. In practice however, $R_{on}$ will never be exactly zero where losses can be further reduced by making $M1$ as wide as possible without significantly contributing to $C_{par_{br}}$.

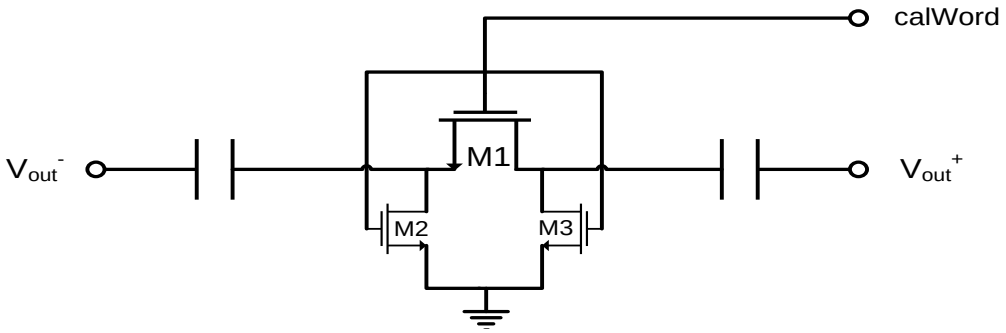



**Fig. 5.4:** Practical implementation of an SCA switch

It is important to minimise losses in $M1$ and the entire branch as this will maximise its parallel resistance ($R_{p_{br}}$). From (5.5) this increases $R_{p_{SCA}}$ which from (5.6) reduces $X_{SCA}$ thereby leading to reductions in power consumption and phase noise degradation due to the branch. In addition to this, it is important to minimise the parasitic capacitance of the branch ($C_{par_{br}}$) such that the tuning range is not significantly degraded (see (5.9)). In fact this is the reason why $M1$ was realised using an NMOS device over a PMOS device, as NMOS devices will in general be smaller for given losses than PMOS devices hence contributing less to $C_{par_{br}}$. Realising $M1$ using an NMOS device then mandates $M2$ and $M3$ to also be realised as NMOS devices which should be made narrow, to reduce their contribution to $C_{par_{br}}$, and long, so that their output impedance prevents significant signal loss to Vss.

The implementation of Fig. 5.4 is effective in optimising the SCA switch in its on state. However, when in its off state (i.e. upon the application of a logic low signal) the source and drains of $M1$ are left floating which, due to the large swing of the VCO output signal, can be momentarily pulled below ground and slightly turn on $M1$. This will reduce the parallel resistance of the branch in its off state and can be addressed with the modification

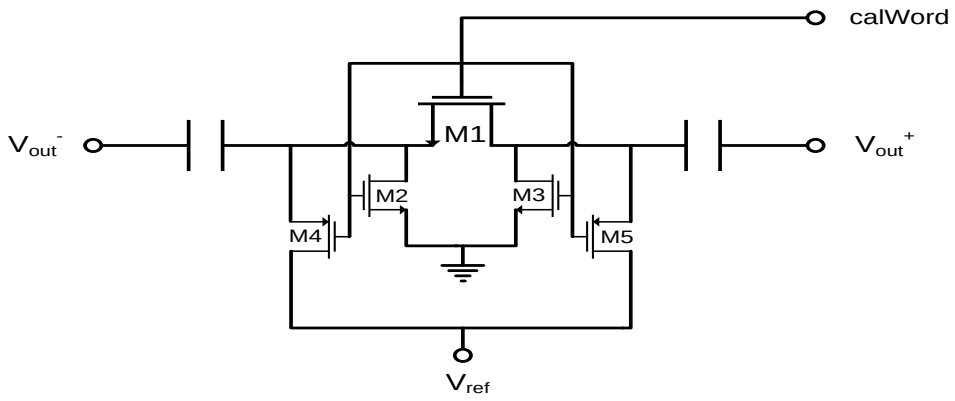



**Fig. 5.5:** Modified implementation of an SCA switch

shown in Fig. 5.5 [39]. This is formed by adding PMOS devices $M4$ and $M5$ onto the practical implementation of Fig. 5.4 whose role is to clamp the source and drains of $M1$ to $V_{ref}$ when it is off. Given that a logic low signal (i.e. 0V) is applied to the gate of $M1$, its gate-source voltage is thus equal to $-V_{ref}$ thereby ensuring it remains off over the entire swing of the VCO output signal. As such, $V_{ref}$ can be set to any biasing potential as long as it is stable and as noise free as possible [39]. As before with $M2$ and $M3$, $M4$ and $M5$ should be made long and narrow to prevent signal loss (increase $R_{p_{br}}$) without significantly contributing to $C_{par_{br}}$.

It is instructive to analyse the effect increasing the lengths of $M4$ and $M5$ has on $R_{p_{br}}$ and $C_{par_{br}}$ for this branch. This is shown in Fig. 5.6 which plots $R_{p_{br}}$ and $C_{par_{br}}$ for various values of lengths for $M4$ and $M5$ ($L_{M4,M5}$). For this simulation, the branch was designed using UMCs 90nm CMOS process where contributions to $R_{p_{br}}$ and $C_{par_{br}}$ from $M1 \rightarrow M3$ were minimised by making $M1$ short and wide and $M3, M4$ long and narrow (see above). Contributions to $C_{par_{br}}$ from the widths of $M4$ and $M5$ were also minimised by employing minimum dimensions for the width ($0.12\mu$m). The lengths of $M4, M5$ ($L_{M4,M5}$) were then swept from 80nm to $20\mu$m where, for an applied 4.8GHz sine wave, the resulting values for $R_{p_{br}}$ and $C_{par_{br}}$ were plotted.

In Fig. 5.6 the parallel resistance of the branch ($R_{p_{br}}$) over $L_{M4,M5}$ is plotted by the solid blue line whose corresponding values are shown on the left y-axis. This clearly shows $R_{p_{br}}$ to increase with $L_{M4,M5}$ up to $5.5\mu m$ where it reaches a maximum value of 1.85MΩ. After this, it appears to gradually decrease again due to some unaccounted for effect becoming increasingly dominant. The parasitic capacitance of the branch ($C_{par_{br}}$) is then plotted by the green trace whose corresponding values are shown on the right y-axis. This clearly shows $C_{par_{br}}$ to steadily increase with increases in $L_{M4,M5}$, reaching its highest value (in this simulation) of 8.7fF for $L_{M4,M5} = 20\mu m$.

Fig. 5.6 suggests that in terms of $R_{p_{br}}$, $L_{M4,M5} = 5.5\mu m$ is potentially optimal. However, this value should only be settled on if the resulting parasitic capacitance (6.1fF

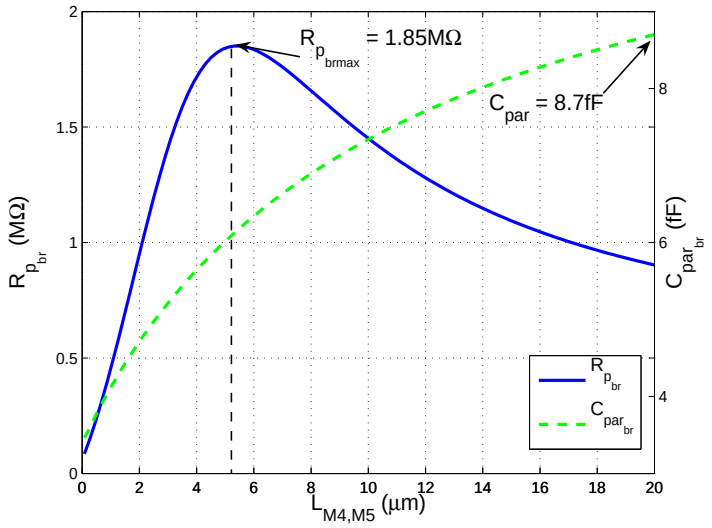



**Fig. 5.6:** $R_{p_{br}}$ and $C_{par_{br}}$ versus $L_{M4,M5}$

for this case) does not significantly affect the overall capacitance of the branch. Therefore, the design of an SCA switch always entails a trade-off between $R_{p_{br}}$ and $C_{par_{br}}$ with the optimum transistor dimensions being found in practice through parametric sweeps such as that shown in Fig. 5.6. A design procedure for an SCA switch is outlined in Appendix B4.

### 5.2.3 Issues with the SCA

The main issue with an SCA is that when a branch is switched in, it adds a bulk capacitance to the tank thereby increasing the capacitance which the varactor must overcome to produce a frequency variation at the VCO output. As a result, the varactors effective capacitance variation reduces hence resulting in a lower $K_{VCO}$. Therefore, as more and more branches are switched in, $K_{VCO}$ becomes less and less giving rise to what is known as band-to-band $K_{VCO}$ variation ($\Delta K_{VCO_{btb}}$) (in contrast to in-band $K_{VCO}$ variation, $\Delta K_{VCO_{inb}}$, discussed in section 5.1). The variation in $K_{VCO}$ due to this effect was shown in [81] to be approximated by the following factor:

$$\Delta K_{VCO_{btb}} \approx \Delta C\sqrt{\Delta C} \tag{5.10}$$

where $\Delta C$ represents the change in capacitance resulting from switching in one (or a number of) SCA branches. The reason (5.10) only approximates the $K_{VCO}$ band-to-band reduction factor is that it ignores varactor non-linearity (i.e. in-band $K_{VCO}$ variation) thereby generally resulting in factors slightly on the higher side of what is seen in practice.

The effect of (5.10) is two-fold. Firstly, it contributes to the overall $K_{VCO}$ variation ($\Delta K_{VCO}$) which from (5.1), increases loop bandwidth variation ($\Delta K$). As $\Delta K_{VCO_{btb}}$ values of up to 60% have been seen in practice, this significantly contributes to $\Delta K_{VCO}$

and hence $\Delta K$, thereby greatly emphasising the various issues discussed in section 2.7.4. Secondly, reductions in $K_{VCO}$ by $\Delta K_{VCO_{btb}}$ reduce the frequency range of the VCO ($\Delta F$) by the same factor which, assuming the percentage ($OV$) overlap remains constant (discussed later), reduces the tuning range to (see Appendix A.17):

$$TR = \frac{2\Delta F/\Delta K_{VCO_{btb}}}{2f_{max} - (\Delta F/\Delta K_{VCO_{btb}})} \tag{5.11}$$

Increasing $\Delta F$ in (5.11) by the factor $\Delta K_{VCO_{btb}}$ will restore the original tuning range (see (3.22)) implying that $K_{VCO}$ must be increased by $\Delta K_{VCO_{btb}}$. This is unattractive to low phase noise performance which degrades due to reasons discussed in section 4.2.2, in addition to reductions in the tanks $L/C$ ratio which, from (3.25), will reduce $Q_{tank}$.

The previous discussion was based on the assumption that the percentage overlap ($OV$) between sub-bands remains constant. This holds true in practice as $OV$ exhibits the following important proportionality [82] (see Appendix A.18):

$$OV \propto \frac{f_{res}}{K_{VCO}} \tag{5.12}$$

where $f_{res}$ represents the frequency difference between two respective sub-bands at a particular control voltage, otherwise known as the sub-band spacing resolution. This also reduces due to the same mechanism that gives rise to $\Delta K_{VCO_{btb}}$, and as such, reduces by the same factor. Therefore, since both $K_{VCO}$ and $f_{res}$ reduce by $\Delta K_{VCO_{btb}}$, $OV$ from (5.12) remains constant, implying that no change in percentage overlap occurs over all the sub-bands. This is an extremely important characteristic as it means the issue of band-to-band $K_{VCO}$ variation does not present any concerns regarding PVT robustness and will play a pivotal role in section 5.3.

To both verify and illustrate the above discussions, a sub-banded VCO was designed using UMCs 90nm CMOS process. The VCO employed single-ended tuning and 16 sub-bands (i.e. 15 SCA branches) to achieve an ideal tuning range (neglecting $K_{VCO}$ band-to-band variation) of 22%. The simulated tuning characteristics of the VCO are shown in Fig. 5.7 where they are plotted with reference to the differential tuning voltage ($V_d$) of the varactor configuration.

The differential tuning voltage was defined in (4.33) to be the difference in the differential tuning inputs $V_{ctrl^-}$ and $V_{ctrl^+}$. As these are in practice connected to the differential CP outputs, the differential tuning voltage ($V_d$) is determined by the CP output voltage swing. Therefore, assuming the same CP output voltage swing shown in Fig. 4.13 applies, where $V_{cp_{min}} = 0.25V$ and $V_{cp_{max}} = 0.75V$, the differential tuning voltage, from (4.7) can be seen to range from:

$$V_d : (V_{ctrl^+_{max}} - V_{ctrl^-_{min}}) \rightarrow (V_{ctrl^+_{min}} - V_{ctrl^-_{max}}) \tag{5.13}$$

$$V_d : (0.75V - 0.25V) \rightarrow (0.25V - 0.75V) \tag{5.14}$$

$$V_d : 0.5V \rightarrow -0.5V$$

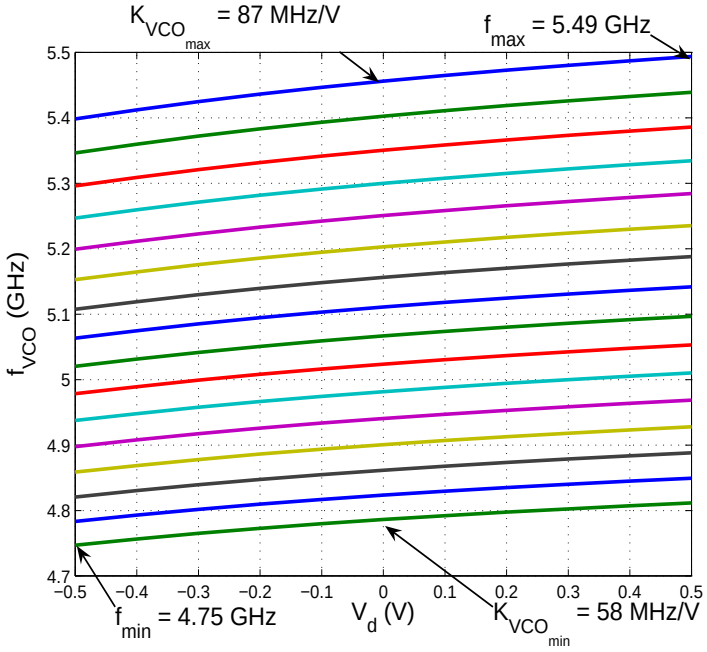



**Fig. 5.7:** Simulated tuning Characteristics

The performance of the simulated VCO is summarised in Table 5.1 where all the necessary parameters are detailed.

| $TR_{ideal}$ (%) | $TR_{sim}$ (%) | $\Delta F_{ideal}$ (GHz) | $\Delta F_{sim}$ (MHz) | $\frac{\Delta F_{ideal}}{\Delta F_{sim}}$ | $\Delta K_{VCO_{btb}}$ | $f_{res_{max}}$ (MHz) | $f_{res_{min}}$ (MHz) | $\Delta f_{res}$ |
|---|---|---|---|---|---|---|---|---|
| 22 | 14.5 | 1.11 | 740 | 1.5 | 1.5 | 55 | 37 | 1.5 |

**Table 5.1:** Performance summary

In Table 5.1, the ideal and simulated tuning ranges are represented by $TR_{ideal}$ and $TR_{sim}$ respectively. The ideal and simulated frequency ranges are then respectively represented by $\Delta F_{ideal}$ and $\Delta F_{sim}$, where the maximum and minimum sub-band spacing resolutions and their corresponding reduction factor are represented by $f_{res_{max}}$, $f_{res_{min}}$ and $\Delta f_{res}$ respectively. The first observation to make from Table 5.1 is that $\Delta K_{VCO_{btb}} = 1.5$, which from Fig. 5.7 corresponds to a reduction in $K_{VCO}$ by $\approx 33\%$. This is in good agreement with (5.10) since the total capacitance of the VCO with all SCA branches

switched out (i.e for the top sub-band) at $V_{ctrl} = 0.5V$ was 165fF, whereas that with all SCA branches switched in (i.e. for the bottom sub-band) was 225fF. This results in $\Delta C = 1.36$ and $\Delta C\sqrt{\Delta C} = 1.59$. The reason this number does not exactly equal $K_{VCO_{btb}}$ is that, as already mentioned, (5.10) ignores varactor non-linearity thereby resulting in factors slightly on the higher side of what is seen in practice. The second observation to make from Table 5.1 is that $\Delta F_{ideal}/\Delta F_{sim} = 1.5 = \Delta K_{VCO_{btb}}$. In other words, the frequency range of the VCO has reduced by the same factor as its $K_{VCO}$ values which, in agreement with (5.11), reduces the tuning range to 14.5%. This can be seen from Fig. 5.7 by applying (3.22) to its maximum ($f_{max}$) and minimum ($f_{min}$) frequencies. The third and final observation to be made from Table 5.1 is that $\Delta f_{res} = 1.5$, (i.e. a 33% reduction). In other words the sub-band spacing resolutions have reduced by the same factor as $K_{VCO}$ and $\Delta F$.[3] According to (5.12), this should enable a constant percentage overlap ($OV$) to be maintained. This is verified in Fig. 5.8 where $OV$ is plotted over all sub-bands and shown to be more or less constant at 42%. In addition, to give an illustrative overview of the extent of variation present in this VCO, Figs. 5.9 ad 5.10 plot $K_{VCO}$ and $f_{res}$ over all the sub-bands respectively.

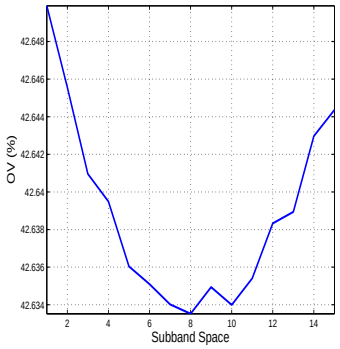



**Fig. 5.8:** $\Delta OV$

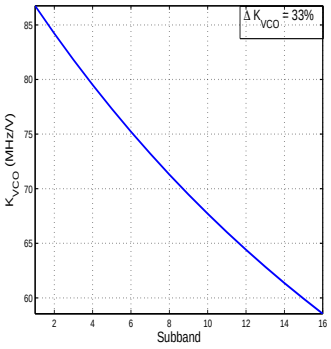



**Fig. 5.9:** $\Delta K_{VCO}$

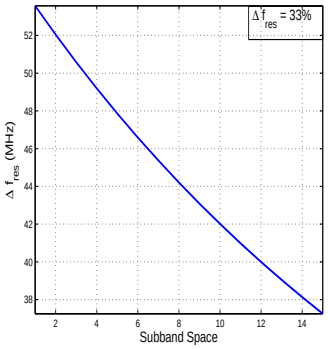



**Fig. 5.10:** $\Delta f_{res}$

To restore the tuning range back to its ideal value, (5.11) suggests increasing $\Delta F$ by the factor $\Delta K_{VCO_{btb}}$, achievable in practice by increasing $K_{VCO}$ by the same factor. To verify this, a second VCO was designed using the same process and architecture of the first, except that its $\Delta F$ was increased by a factor of 1.5 to restore the ideal tuning range of 22%. The resulting tuning characteristics are shown in Fig. 5.11. Comparing this with Fig. 5.7 shows $K_{VCO}$ to have increased by a factor of $\approx 1.5$ leading to an increase in $\Delta F$ by the same factor, hence restoring it back to its ideal value of 1.11GHz. Applying $f_{max}$ and $f_{min}$ to (3.22) then show this increase in $K_{VCO}$, and hence $\Delta F$, to have successfully restored the tuning range back to its ideal value of 22%.

However, as already discussed, the cost of this compensation for $\Delta K_{VCO_{btb}}$ is an

[3]Measurements for $f_{res_{max}}$ and $f_{res_{min}}$ were made at $V_{ctrl} = 0.5$V to enable a fair comparison with $\Delta K_{VCO_{btb}}$ which, as can be seen from Fig. 5.7, was also measured with reference to $V_{ctrl} = 0.5$V.

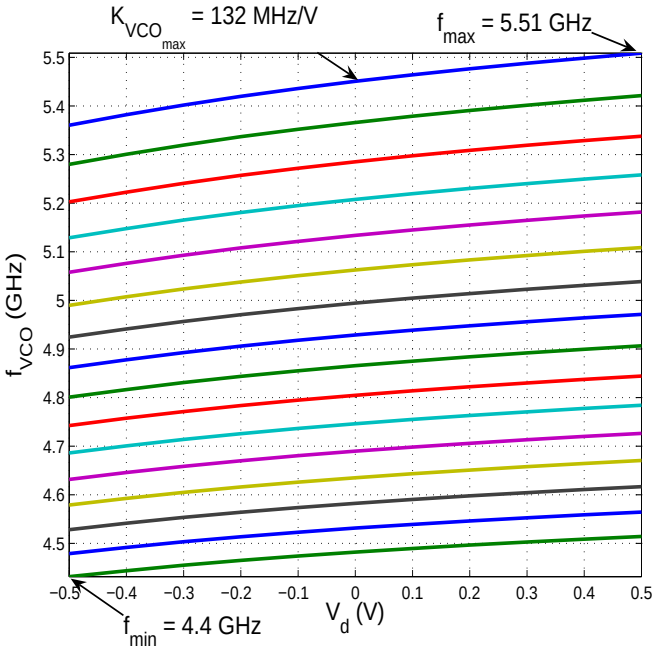



**Fig. 5.11:** Compensated Tuning Characteristics

increase in phase noise. This is verified in Fig. 5.12 which plots the simulated phase noise performance for the top bands of both VCOs at $V_{ctrl} = 0.5$V. In this plot, $VCO_1$ represents the VCO with tuning characteristics shown in Fig. 5.7, while $VCO_2$ represents the VCO with tuning characteristics shown in Fig. 5.11. Measurements taken at 100kHz offset then show $VCO_2$ to exhibit 3dB more phase noise than $VCO_1$ due to its larger $K_{VCO}$. What is interesting to note is the improvement in phase noise performance of $VCO_1$ over $VCO_2$ is largest for close-in frequencies, becoming less and less as we move further out from the carrier frequency. This implies $VCO_1$ to exhibit significantly less flicker noise than $VCO_2$.

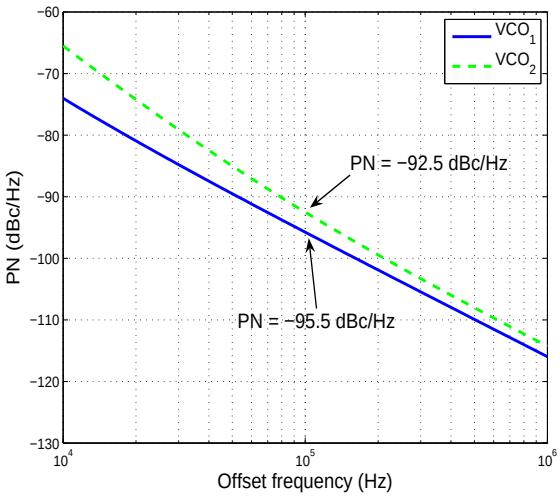



**Fig. 5.12:** Phase noise degradation due to $\Delta K_{VCO_{btb}}$ compensation

## 5.3 Reducing $\Delta K_{VCO_{btb}}$

The previous section showed the primary issue with SCAs to be $K_{VCO}$ band-to-band variation ($\Delta K_{VCO_{btb}}$). As shown, this significantly contributes to loop bandwidth variation in addition to reducing the overall tuning range, where compensation for this reduction results in increased phase noise. As such, there have been some techniques seeking to reduce $\Delta K_{VCO_{btb}}$ reported in the literature, each exhibiting various weaknesses.

### 5.3.1 Related Work

In [83] the use of an additional serial LC-tank with a variable inductor configuration was proposed to reduce $\Delta K_{VCO_{btb}}$. However, due to the additional LC-tank this solution consumes large power and die area. In [84] the use of additional varactors to reduce the $\Delta K_{VCO_{btb}}$ of groups of sub-bands was proposed. This solution however requires an additional complex biasing scheme to reduce $\Delta K_{VCO_{btb}}$ down to a specified level. In addition, both techniques do not address $\Delta f_{res}$ which is their main weakness since, from (5.12), in order to maintain a constant percentage overlap between bands, both $K_{VCO}$ and $f_{res}$ must be reduced by the same factor. Reducing $\Delta K_{VCO_{btb}}$ but not $\Delta f_{res}$ may reduce the percentage overlap leading to reduced PVT robustness and in extreme cases, frequency deadzones (as observed in [83]). In [85], [65], the use of an additional varactor array in conjunction with the conventional switched capacitor array was proposed to achieve simultaneous reductions in both $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$. In [85] unused varactors in the array are simply switched out whilst those in [65] are connected to a fixed potential. However, due to the additional array, $Q_{tank}$ will be severely degraded over conventional approaches, leading to degraded phase noise performance and increased power consumption.

### 5.3.2 Proposed Technique

Where [85], [65] achieved simultaneous reductions in $\Delta K_{VCO}$ and $\Delta f_{res}$ using an array of switchable varactors and switchable capacitors, we propose the use of a single varactor array to simultaneously reduce both $\Delta K_{VCO}$ and $\Delta f_{res}$ [82]. The advantage of this approach is it reduces loading of $Q_{tank}$ (i.e. increases $R_p$) thereby leading to reductions in power consumption and phase noise, as shown in section 5.2.1. Specifically, the varactor array consists of $n-1$ switchable varactor branches (to split the specified tuning range into $n$ sub-bands) and is hence termed a switched varactor array (SVA). One such branch of this array is shown in Fig. 5.13. From this, the varactor branch can be seen to employ cathode tuning (for reasons discussed in section 3.4.2) with its varactor configuration based on that of Fig. 3.27. Transistors $M1$ and $M2$ act as switches which switch the branch in or out upon the application of a logic high or low signal from the calibration word ("calWord") respectively. Switching the branch out when not in use is more favourable to fixing it to

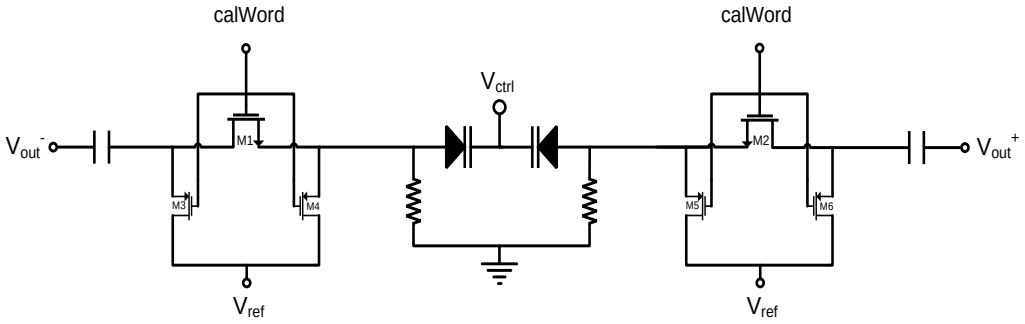



**Fig. 5.13:** Single branch of an SVA

a fixed potential [65], as it avoids unnecessary loading of $Q_{tank}$ for the higher frequency bands, where the majority of the branches will be switched out. Transistors $M3 \rightarrow M6$ are then employed to maintain the switches completely off over the entire VCO output voltage swing upon the application of a logic low signal (similar to Fig. 5.5). As was the case for $M4$ and $M5$ in Fig. 5.5, $M3 \rightarrow M6$ should be made long and narrow to prevent signal loss (increase $R_{p_{br}}$) without significantly contributing to $C_{par_{br}}$. It should be noted that additional transistors (similar to $M2$ in Fig. 5.4) are not needed to enable the switches to turn on upon the application of a logic high signal. This is because due to the varactor biasing scheme (see section 3.4.2), the sources of $M1$ and $M2$ are tied to Vss thereby ensuring that upon the application of a logic high signal, $V_{gs_{1,2}} > V_{t_{1,2}}$ to enable both switches completely turn on. It could however be argued that the inclusion of NMOS devices similar to $M2$ and $M3$ in Fig. 5.4 is still worthwhile to minimise losses within the switches. However it was seen in practice that the resulting contributions to $C_{par_{br}}$ for such devices (due to their long lengths necessary to prevent signal loss), far outweighed any benefits to be gained by their reductions in $R_{p_{br}}$. As such they were omitted to maintain $C_{par_{br}}$ at a reasonable level, with $R_{p_{br}}$ being addressed by making $M1$ and $M2$ short and as wide as possible within the constraints of $C_{par_{br}}$.

### 5.3.3 Design Procedure for a Switched Varactor Array (SVA)

Each varactor branch is sized according to its required $C_{min}$ and $C_{max}$ values necessary to achieve the specified $K_{VCO}$ and $f_{res}$. The procedure for calculating these values is as follows:

1. Calculate $C_{min}$ for the sub-band of interest ($C_{min_n}$):

$$C_{min_n} = \frac{1}{L(2\pi f_{max_n})^2} \tag{5.15}$$

where $f_{max_n}$ is the maximum frequency of the sub-band, taking into account the specified $f_{res}$. This is calculated as follows:

$$\begin{aligned} f_{max_n} &= f_{max_{n-1}} - f_{res} \\ &= f_{max_{n-1}} - (\Delta f_{n-1}(1 - OV)) \end{aligned} \tag{5.16}$$

where the maximum frequency and frequency range covered by the previous sub-band are $f_{max_{n-1}}$ and $\Delta f_{n-1}$ respectively.

2. Calculate the change in $C_{min}$ between the sub-band of interest and the previous one ($\Delta C_{min_n \to n-1}$):

$$\Delta C_{min_n \to n-1} = C_{min_n} - C_{min_{n-1}} \tag{5.17}$$

where $C_{min_{n-1}}$ is the minimum capacitance of the previous sub-band.

3. Calculate $C_{max}$ for the sub-band of interest ($C_{max_n}$):

$$C_{max_n} = \frac{1}{L(2\pi f_{min_n})^2} \tag{5.18}$$

where $f_{min_n}$ is the minimum frequency of the sub-band, taking into account the specified $K_{VCO}$. This is calculated as follows:

$$f_{min_n} = f_{max_n} - (K_{VCO} V_{swing_{cp}}) \tag{5.19}$$

4. Calculate the change in $C_{max}$ between the sub-band of interest and the previous one ($\Delta C_{max_n \to n-1}$):

$$\Delta C_{max_n \to n-1} = C_{max_n} - C_{max_{n-1}} \tag{5.20}$$

where $C_{max_{n-1}}$ is the maximum capacitance of the previous sub-band.

Equations (5.17) and (5.20) give the required $C_{min}$ and $C_{max}$ values respectively for the sub-band of interest. Once obtained, the relevant varactor branch is sized to achieve both values and inserted into the array. Repeating this procedure $n - 1$ times thus completes the array.

To provide an illustrative view of a VCO employing an SVA, Fig. 5.14 shows the schematic of a differentially tuned VCO architecture (similar to that shown in Fig. 4.40) which employs an SVA consisting of $n - 1$ branches.

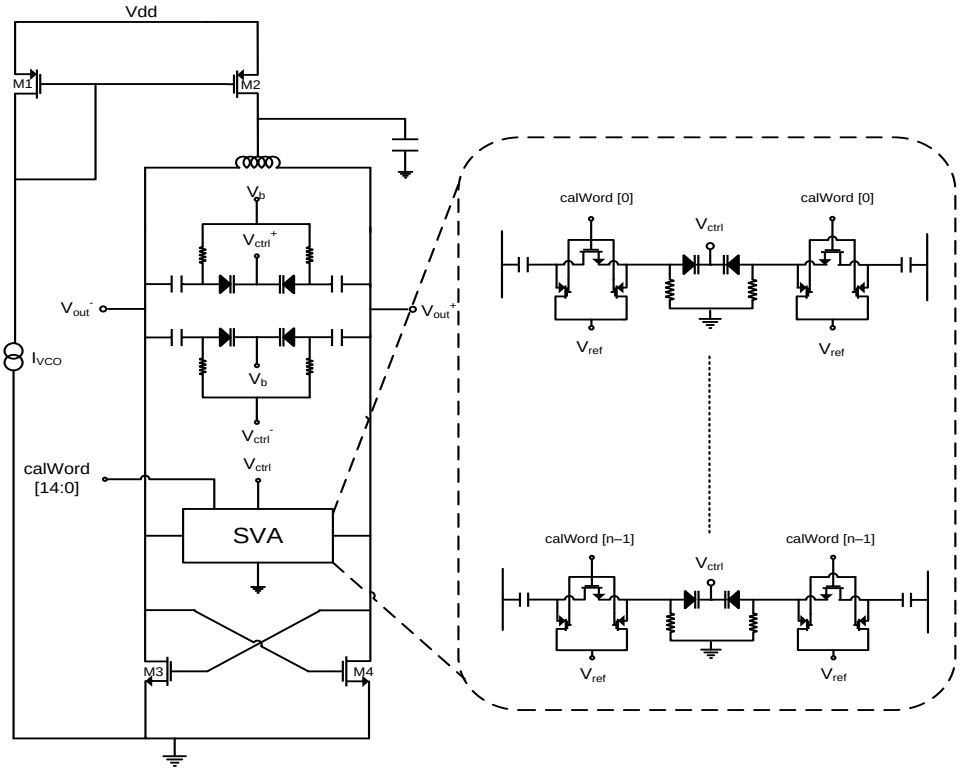



**Fig. 5.14:** Differentially tuned VCO with SVA containing $n-1$ branches

Due to its excellent performance (shown in section 5.4) this was the VCO used in the final PLL of this thesis whose corresponding W/L ratios, operating points and component dimensions are detailed in section 6.4. It should be observed from Fig. 5.14 that although the LC-tank employs differential tuning, each branch of the SVA employs single-ended tuning ($V_{ctrl}$). Therefore in order to tune each branch, the differential LF outputs must first be converted to single-ended form. As this is achieved with a differential amplifier (similar to that shown in Fig. 4.19), it comes at the various costs discussed in section 4.5 and is an issue this thesis attempted to address (discussed in section 5.5).

## 5.4 Performance Analysis

To analyse the performance of the proposed technique, the differentially tuned VCO of Fig. 5.14 employing a switched varactor array (SVA) was designed and simulated using UMCs 90nm CMOS process. It was designed for a centre frequency of 4.8GHz and tuning range of 23% which was split into 16 bands using a 15-branch SVA to exhibit reductions $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$. To demonstrate these reductions, the resulting VCO was compared with a differentially tuned VCO employing a conventional switched capacitor array (SCA) designed using the same process and to meet the same tuning range. The resulting tuning characteristics of both VCOs are shown in Fig. 5.15 with reference to $V_d$ (see (4.33)).

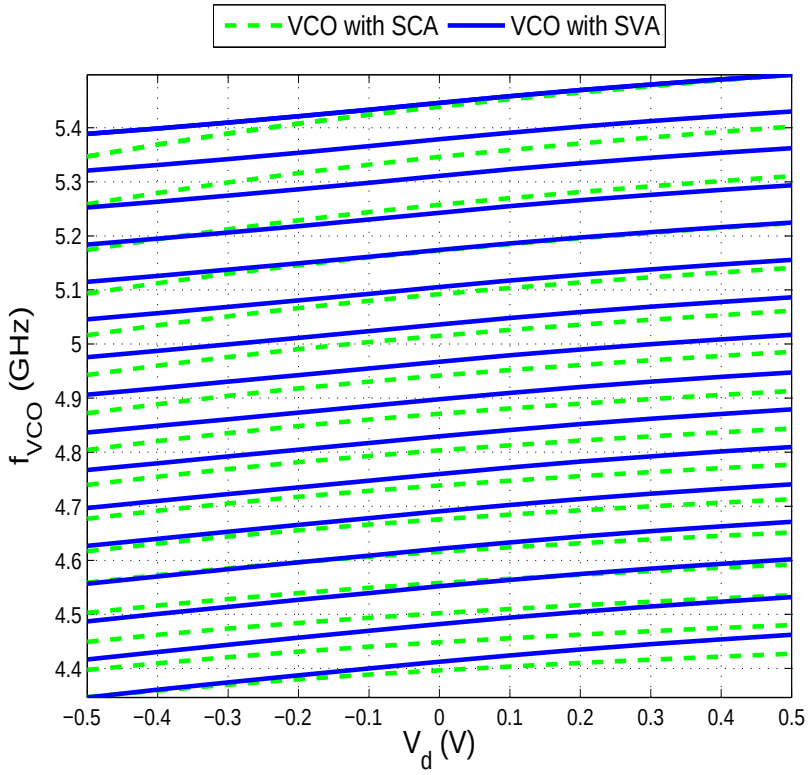



**Fig. 5.15:** Simulated tuning characteristics

A performance comparison of both circuits is then given in Table 5.2.

| | Conventional VCO | Proposed VCO |
|---|---|---|
| Technology | 90nm CMOS | |
| Power Supply | 1V | |
| $\Delta F$ | 1150 MHz (4.35GHz - 5.5GHz) | |
| TR | 23% | |
| $\Delta K_{VCO_{btb}}$ | ± 30% | ± 4.6% |
| $\Delta f_{res}$ | ± 30% | ± 1.7% |
| OV | 36.5% | ≈ 38% |
| Power Consumption | 900 $\mu$W | 850 $\mu$W |

**Table 5.2:** Performance summary comparison

Table 5.2 clearly shows the VCO employing an SVA to achieve reductions in $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$ by factors of 6 and 17 respectively over the VCO employing an SCA. This is shown in further detail in Figs. 5.16 and 5.17 which plot $K_{VCO}$ and $f_{res}$ respectively over all sub-bands for both VCOs.

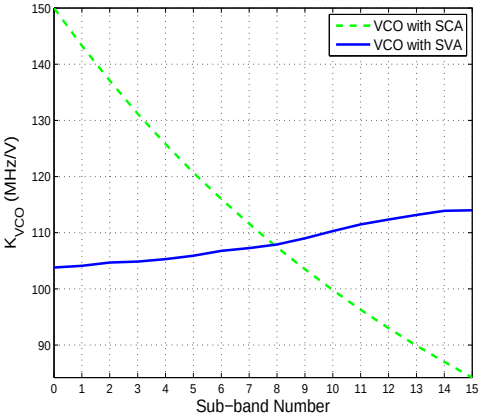



**Fig. 5.16:** $K_{VCO}$ over sub-bands

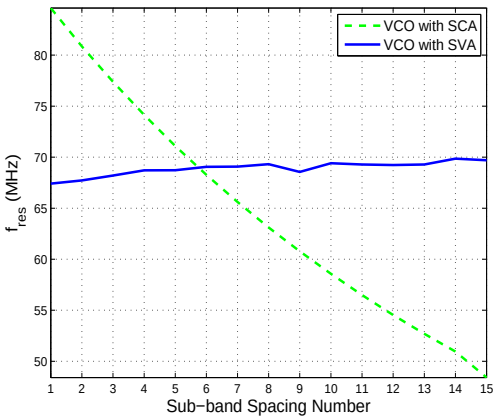



**Fig. 5.17:** $f_{res}$ over sub-bands

Table 5.2 also shows $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$ to be the same for the VCO with SCA which, from section 5.2.3, leads to a constant percentage overlap ($OV$) between bands of 36.5%. Although the reductions in $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$ are not exactly equal, they are seen to be very close for the VCO with SVA, resulting in a near constant $OV$ of $\approx$ 38%. This is shown in Fig. 5.18 which plots $OV$ for both VCOs across all sub-bands.

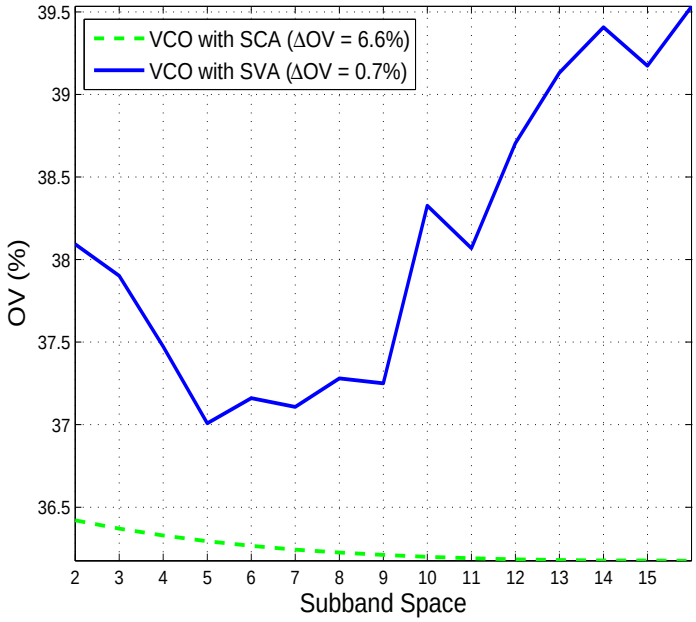



**Fig. 5.18:** Percentage overlap across all sub-bands

As can be seen from Fig. 5.18, $OV$ for the VCO with SCA (plotted by the green trace) is near constant at 36.5% where an overall variation in percentage overlap across all bands ($\Delta OV$) of 0.7% was measured. However, $OV$ for the VCO with SVA (plotted by the blue line) varies a little more (due to differences in $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$) with a

$\Delta OV$ of 6.6%. Although slightly larger than for the VCO with SCA, from the perspective of PVT robustness this variation is negligible and thus presents no concerns.

As explained in section 5.2.3, $\Delta K_{VCO_{btb}}$ reduces the tuning range creating the need for larger $K_{VCO}$ values to restore it back to its specified value. Therefore, it follows that designing with reduced $\Delta K_{VCO_{btb}}$ enables the specified tuning range to be covered with smaller $K_{VCO}$ values, thus enabling improved phase noise performance, for the reasons discussed in section 5.2.3. This is verified in Fig. 5.19 which plots the simulated phase noise performance of the top frequency bands for both VCOs. In general this shows the VCO with SVA to achieve superior phase noise performance over the VCO with SCA, where measurements taken at 1 MHz offset from the carrier frequency show an improvement of 2dB to be achieved (i.e. an improvement of $\approx 40\%$).

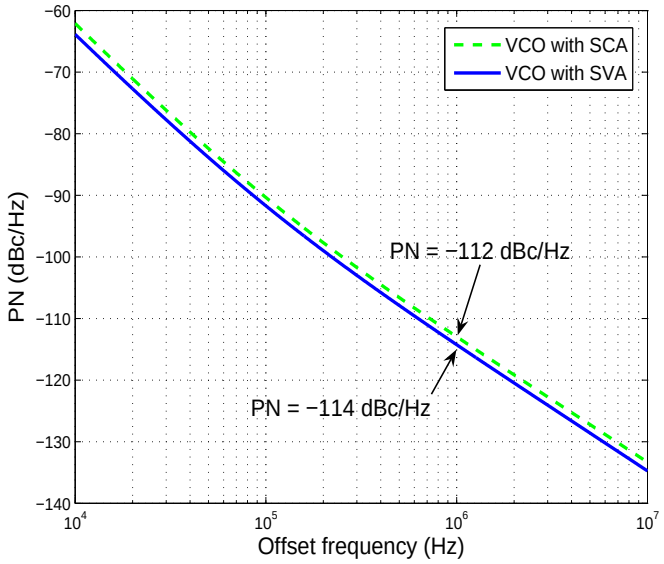



**Fig. 5.19:** Phase noise due to reductions in $\Delta K_{VCO_{btb}}$

Table 5.2 also shows the power consumption of the VCO with SVA to be slightly less than that of the VCO with SCA, attributed to its slightly higher $L/C$ tank ratio (see (3.25)). However the savings in power between the two VCOs ($50\mu$W) is negligible. The real achievements in power savings are seen when comparing the power consumption of the proposed technique (i.e. the VCO with SVA) with other techniques recently reported in the literature, concerned with reducing $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$. This is provided in Table 5.3 which displays the overall performance of the proposed technique against such recent publications, showing it to achieve the lowest reported power consumption by an order of magnitude. Although some of this power saving is due to the 1V supply for the process used to simulate the VCO, a significant proportion of it is, as discussed in section 5.3.2, due to the proposed technique employing one single array consisting of varactor branches which can be completely switched out when not in use. In addition,

Table 5.3 also shows the proposed technique to achieve reductions in $\Delta K_{VCO_{btb}}$ and $\Delta f_{res}$ up there with the state of the art published at the time of writing.

| Ref. | [83] | [84] | [85] | [65] | This Work |
|---|---|---|---|---|---|
| $\Delta K_{VCO_{btb}}$ ($\pm$%) | 12 | 4.4 | 20.4 | 12.5 | 4.6 |
| $\Delta f_{res}$ ($\pm$%) | N/A [a] | N/A [a] | N/A [a] | 9 | 2.2 |
| $\Delta F$ (MHz) | 1320 | 1050 | 720 | 825 | 1150 |
| Technology | 0.25$\mu$m BiCMOS | 0.13$\mu$m CMOS | 0.18$\mu$m CMOS | 0.18$\mu$m CMOS | 90nm CMOS |
| Power Supply (V) | 2.8 | 2.8 | 1.8 | 1.8 | 1 |
| Power (mW) | 11.2 | – [b] | 9 | – [b] | 0.85 |

[a] $\Delta f_{res}$ not addressed, hence reducing PVT robustness.

[b] Not specified for VCO used.

**Table 5.3:** Performance comparison against previous publications

## 5.5 Differentially Tuned SVA

The switched varactor array (SVA) branch of Fig. 5.13 employs single-ended tuning. Therefore when implemented in a differentially tuned VCO, as noted in section 5.3.3, the differential CP outputs must first be converted to single-ended form using a differential amplifier (similar to that shown in Fig. 4.19). However, as noted in section 4.5, this comes at the cost of increased design complexity, cost, time and resources, in addition to consuming additional silicon area, increasing power consumption and possible even degrading the noise performance of the PLL. Therefore, similar to section 4.5, an attractive progression would be to convert the SVA of Fig. 5.13 which employs single-ended tuning, to one which employs differential tuning thereby eliminating the need for a differential amplifier and its associated disadvantages. However as will be seen, this is by no means a straight forward task.

### 5.5.1 Differentially Tuned SVA Branch Attempt

In section 4.5.3, the modified cathode differentially tuned varactor configuration of Fig. 4.35 was shown to provide optimal performance over other configurations, namely due to its improved common-mode noise rejection capability. Therefore, an obvious approach would be to convert the single-ended tuned SVA branch of Fig. 5.13 using the configuration of Fig. 4.35 as a blueprint. Doing this results in the branch shown in Fig. 5.20. As can be seen, the top branch of this configuration effectively applies the same biasing as that of

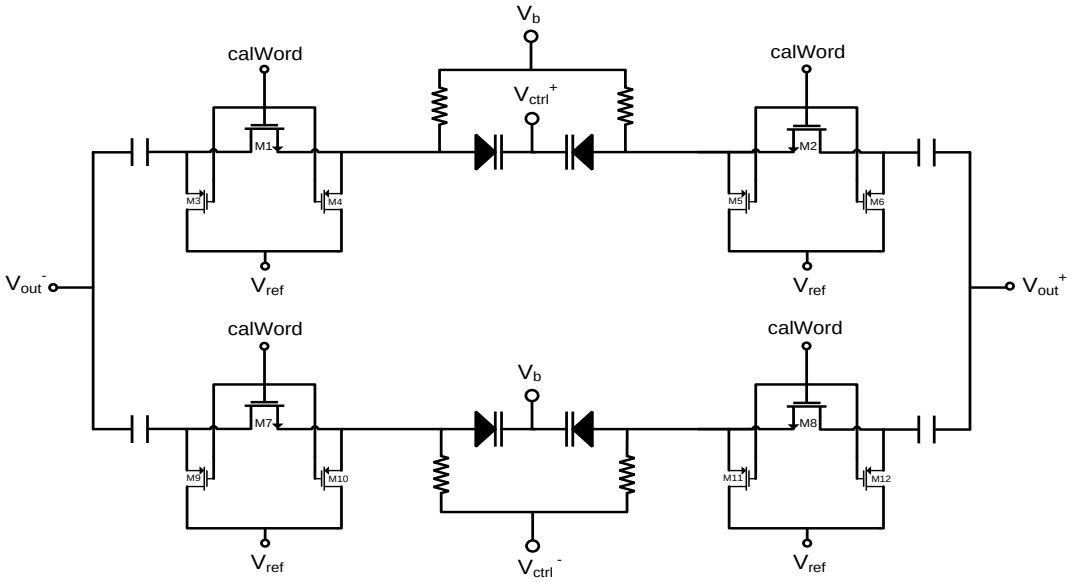



**Fig. 5.20:** Differentially tuned SVA branch attempt

Fig. 5.13 (i.e. a tuning voltage is applied to the cathodes with a fixed bias applied to the anodes of each varactor) and as such exhibits similar behaviour. However as the bottom branch applies opposite biasing to the top, it encounters two very severe and limiting problems. These are related to the switches $M7$ and $M8$ and arise due to the following:

*Gate-source voltages of the switches*: Since $V_{ctrl^-}$ is applied to the anodes of the varactors, the gate-source voltages of the switches $M7$ and $M8$ ($V_{gs_{7,8}}$) is defined as:

$$V_{gs_{7,8}} = V_{calWord}(High) - V_{ctrl^-} \tag{5.21}$$

This implies that in order for the switches to turn on, the following must be satisfied:

$$V_{calWord}(High) - V_{ctrl^-} \geq V_{t_{7,8}} \tag{5.22}$$

where the threshold voltages of $M7$ and $M8$ are represented by $V_{t_{7,8}}$. This then limits the maximum value of $V_{ctrl^-}$ as follows:

$$V_{ctrl^-} \leq V_{calWord}(High) - V_{t_{7,8}} \tag{5.23}$$

In other words, the signal swing of $V_{ctrl^-}$ becomes limited by one threshold voltage which, for low technology nodes where $V_{calWord}(High)$ can be as low as 1V, represents a significant reduction. The result of this limited swing is increased $K_{VCO}$ requirements to achieve a specified tuning range, thereby increasing phase noise due to the reasons discussed in section 4.2.2.

After the switches turn on, they will typically operate in their linear regions and so exhibit on-resistances ($R_{on_{7,8}}$) approximated by:[4]

$$R_{on_{7,8}} = \frac{1}{\mu_n C_{ox}(V_{gs_{7,8}} - V_{t_{7,8}})^2} \tag{5.24}$$

where $C_{ox}$ and $\mu_n$ are process dependant parameters representing the oxide capacitance and electron mobilities of $M7$ and $M8$.

Equation (5.24) shows $R_{on_{7,8}}$ to be inversely proportional to $V_{gs_{7,8}}$ and so, as would agree with intuition, decreases for increasing $V_{gs_{7,8}}$. This variation in $R_{on}$ gives rise to a corresponding variation in signal amplitudes across the varactors resulting in a changing time-dependant capacitive behaviour which affects the C(V) characteristics of the branch. As this behaviour is not seen in the top branch, it contributes to the asymmetry of the differential tuning characteristics which, as discussed in section 4.5.2, degrades common-mode noise rejection capability. However, this effect on common-mode noise rejection (and general differential operation) has negligible impact in comparison to the effect of the second problem arising due to the biasing of the bottom branch.

*Source capacitance's of the switches*: If we disconnect the top branch of Fig. 5.20 and plot the C(V) characteristics of the bottom branch for an increasing $V_{ctrl-}$, we would expect an increasing C(V) characteristic to result. This is because increases in $V_{ctrl-}$ correspondingly decrease the widths of the depletion regions which, from (3.23), leads to an increasing C(V) characteristic. However, what is seen in practice can in fact be the exact opposite. This is verified in Fig. 5.21 which plots the C(V) characteristics for the bottom branch of the differentially tuned SVA branch of Fig. 5.20.

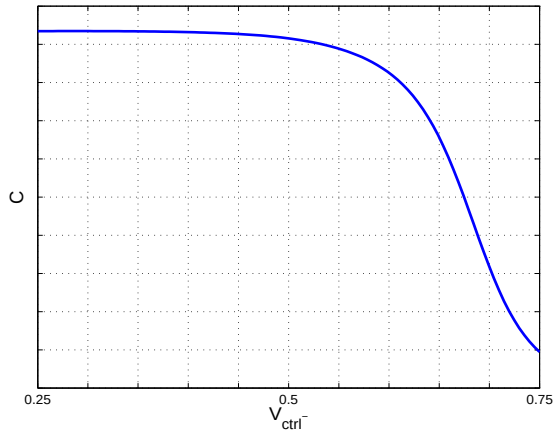



**Fig. 5.21:** C(V) curve for the bottom branch of Fig. 5.20

[4]This assumes a parabolic behaviour of MOSFET drain current [86] which looses accuracy as technologies decrease. Nevertheless, as it provides meaningful insights into the various dependencies of $R_{on}$, it provides a useful approximation.

For the simulation of Fig. 5.21, the SVA branch was designed using UMCs 90nm CMOS process, where $V_{ctrl^-}$ was swept from 0.25V $\rightarrow$ 0.75V, to replicate the CP output voltage swing of Fig. 4.13. Applying a 4.8GHz sine wave to the branch and plotting the resulting capacitance for each value of $V_{ctrl^-}$ then yielded the corresponding C(V) characterisation curve. Exactly why the resulting behaviour occurs can be explained with reference to Fig. 5.22.

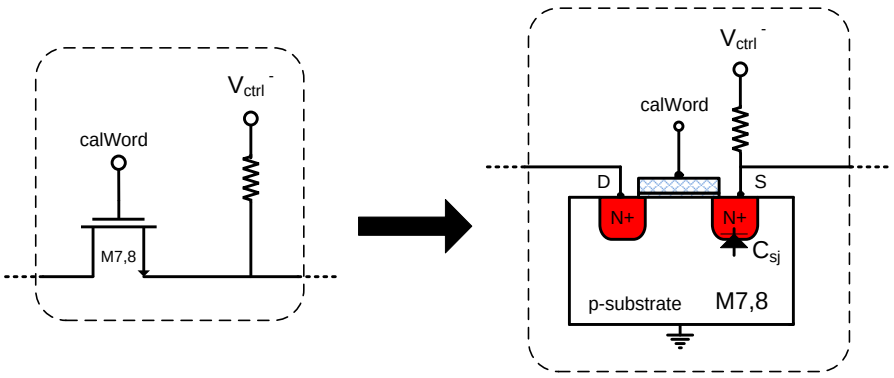



**Fig. 5.22:** Physical device representation of the SVA switches

Fig. 5.22 is simply a close in view of the switches $M7$ and $M8$ in Fig. 5.20 with reference to $V_{ctrl^-}$. Viewing the switches as their physical counterparts (as seen on the right diagram in Fig. 5.22) shows a parasitic diode to exist at the junction between the source (S) of the NMOS and the $p$-substrate. This gives rise to a parasitic capacitance known as the source-substrate junction capacitance ($C_{sj}$). What is important to observe from Fig. 5.22 is that the voltage across $C_{sj}$ equals $V_{ctrl^-}$. As such, the width of the depletion region at this junction increases with increasing $V_{ctrl^-}$ which, from (3.23), gives rise to a decreasing $C_{sj}$ characteristic. If $C_{sj}$ is considerable larger than the capacitive contributions from the varactors (may result from the use of large switches to reduce $R_{p_{br}}$) it will dominate the overall C(V) characteristics of the branch. This is what has occurred for the branch characterised in Fig. 5.21 which is verified in Figs. 5.23 and 5.24. In Fig. 5.23, the C(V) characteristics of the SVA branch were simulated under the same conditions used for the simulation of Fig. 5.21, except this time with both varactors removed to enable the C(V) characteristics specific to $C_{sj}$ for the branch to be analysed. This shows $C_{sj}$ to display a decreasing characteristic for increasing $V_{ctrl^-}$, as in agreement with the previous discussion. In Fig. 5.24 then, the C(V) characteristics of the SVA branch were simulated under the same conditions as for Figs. 5.21 and 5.23, except this time with the switches removed to enable the C(V) characteristics specific to the varactors of the branch ($C_{var}$) to be analysed. This shows $C_{var}$ to display an increasing characteristic for increasing $V_{ctrl^-}$ as would be conventionally expected. This reason this characteristic is

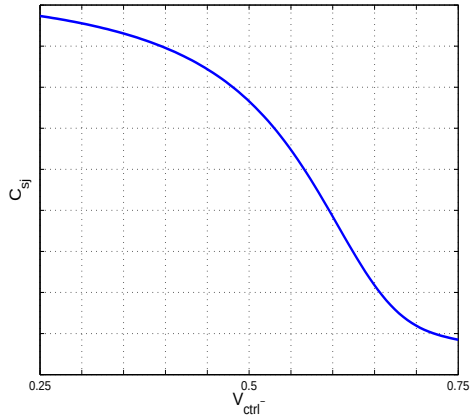



**Fig. 5.23:** $C_{sj}$ versus $V_{ctrl-}$

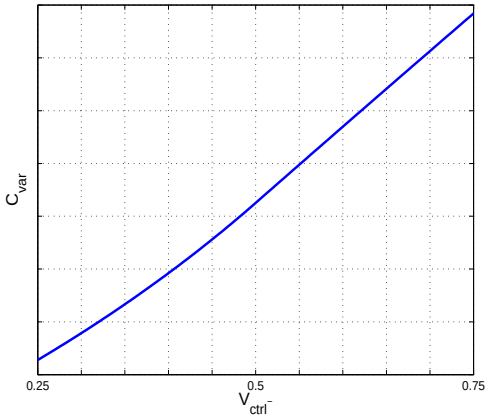



**Fig. 5.24:** $C_{var}$ versus $V_{ctrl-}$

not seen in the overall C(V) characteristics of the branch is because $C_{sj}$ clearly dominates it resulting in an overall decreasing C(V) characteristic for increasing $V_{ctrl-}$ (seen from comparison of Figs. 5.21 and 5.23).

It should be noted that the previous simulations represent an extreme case where $C_{sj} >> C_{var}$, i.e. when the switches are made large in comparison to the varactors. Although such extremities may not always occur in practice, irrespective of switch and varactor dimensions, $C_{sj}$ will always influence (to some extent) the C(V) characteristics of the bottom branch. As such behaviour is not seen in the top branch, this further contributes to the asymmetry of the differential tuning characteristics thereby degrading common-mode noise rejection capability, as discussed in section 4.5.2. In addition to this, as was seen in Fig. 5.21 for the case where $C_{sj} >> C_{var}$, the differential functionality of the entire branch may not even be realised.

Therefore in short, the attempt at converting an SVA branch to differential tuning shown in Fig. 5.20 simply doesn't work. However, due to the potential benefits of realising a working differentially tuned SVA branch, other solutions were explored.

### 5.5.2 Attempted Approaches for a Differentially Tuned SVA Branch

Given that the various shortcomings of the branch in Fig. 5.20 are due to the interaction of $V_{ctrl-}$ with the switches $M7$ and $M8$, a first attempt might be to simply place the switches on the opposite sides of the ac-coupling capacitors. Although this effectively eliminates any deterious effects due to $V_{ctrl-}$, it renders the switches susceptible to similar effects due to the output voltage swing of the VCO, in addition to severely loading down the tank. Therefore, such an approach mandates the switches to also be ac-coupled from the tank, as shown in Fig. 5.25.

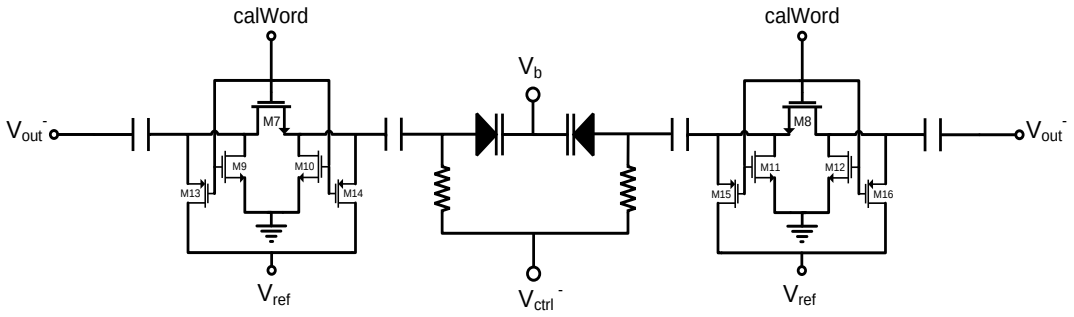



**Fig. 5.25:** Ac-coupling approach

As this approach ac-couples the sources of $M7$ and $M8$ from a defined DC bias, NMOS devices $M9 \rightarrow M12$ are required to clamp the sources of $M7$ and $M8$ to Vss in addition to reducing their drain source voltages when switched on (similar to $M2$ and $M3$ in Fig. 5.4). The use of these additional transistors however presents additional loading on the tank. In addition to this, it was seen that due to the series connections of the ac-coupling capacitors, their resulting capacitance's needed to be made very large (with respect to the varactors) to allow sufficient signal swing across the varactors. As such large capacitance's, in addition to losses from $M9 \rightarrow M16$, were seen to severely load down the tank (significantly reduce $R_{b_{br}}$), whilst significantly contributing to the branches overall parasitic capacitance ($C_{par_{br}}$), this approach was found not to prove an applicable solution.

A more practical solution might be to replace the switches with high voltage devices whose corresponding requirements for $V_{calWord}(High)$ in (5.21) will be typically larger than the maximum value for $V_{ctrl^-}$. This enables the switches to remain on under the application of $V_{calWord}(High)$ over the entire voltage swing thereby relaxing $K_{VCO}$ requirements for a specified tuning range and improving phase noise performance. Nevertheless, when the switches turn on, their on-resistance variation was seen to significantly contribute to asymmetries in the differential tuning characteristic. In addition, high voltage devices typically require large dimensions whose associated source-substrate junction capacitance's also significantly affect the overall C(V) characteristics of the branch (see Fig. 5.20). Therefore, as this approach results in a very asymmetrical differential tuning characteristic, it was seen to also not prove to be an applicable solution.

Another approach might be to realise the switches using transmission gates. Transmission gates are formed by connecting one NMOS and one PMOS device in parallel, with their gates controlled by opposite logic signals (i.e. when a logic '1' is applied to one gate, a logic '0' is applied to the other). The realisation of an SVA branch using transmission gates is shown in Fig. 5.26 where the switches $M7$ and $M8$ in Fig. 5.20 can be seen to be replaced with transmission gates $M1, M2$ and $M3, M4$ respectively. The gates of $M1$ and

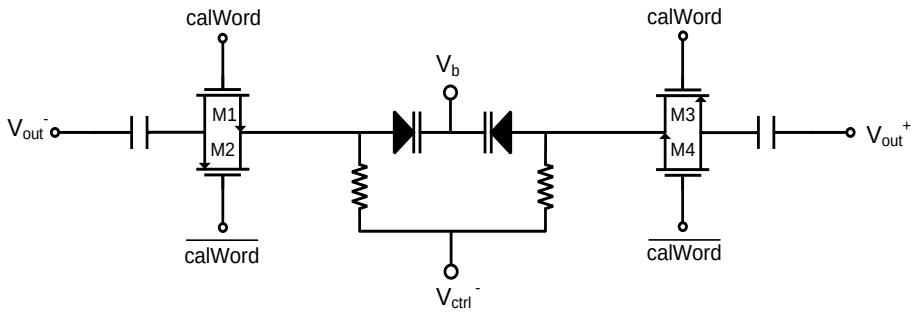



**Fig. 5.26:** Transmission gate approach

$M3$ are connected to the logic signal $calWord$, with $M2$ and $M4$ being connected to its inverse logic signal $\overline{calWord}$.

One advantage of this approach is that at least one switch in the transmission gate is guaranteed to be on over the entire voltage swing of $V_{ctrl^-}$. For example, switches $M1$ and $M3$ are on for $V_{ctrl^-} \leq V_{calWord}(High) - V_{t_{1,3}}$, but switch off once $V_{ctrl^-}$ comes within one threshold voltage of $V_{calWord}(High)$. However, as switches $M2$ and $M4$ are on for $V_{ctrl^-} \geq V_{t_{2,4}}$, these will remain on when $M1$ and $M3$ turn off. Since a similar situation occurs for $V_{ctrl^-} < V_{t_{2,4}}$, the swing of $V_{ctrl^-}$ is not limited leading to reduced $K_{VCO}$ requirements for a specified tuning range and hence, improved phase noise performance.

In addition to this, if the PMOS and NMOS devices are sized correctly, the on-resistance variation of the gates over the voltage swing of $V_{ctrl^-}$ will be significantly reduced. However, achieving this in practice requires the PMOS devices to be larger than the NMOS devices to account for hole mobilities being less than electron mobilities (i.e. $\mu_p < \mu_e$). Given that the NMOS devices themselves will be made quite large (to reduce $R_{p_{br}}$), this was seen to result in very large PMOS devices which significantly contributed to the parasitic capacitance of the branch ($C_{par_{br}}$). In addition, such large PMOS devices will exhibit large drain-substrate capacitance's ($C_{dj}$), similar to the source-substrate capacitance's ($C_{sj}$) discussed in section 5.5.1. Although these cancel out the net effect of the source-substrate capacitance's from the NMOS devices, they will themselves significantly contribute to the C(V) characteristics of the branch hence causing asymmetries in the differential tuning characteristic. Due to these issues, the use of transmission gates were also seen not to prove a viable solution.

Therefore, the various approaches aimed at realising a differentially tuned SVA branch attempted in this thesis and discussed in this section, all failed in realising a true viable solution. As such, further research into the area is required to realise the full potential of the SVA.

## 5.6 Summary and Achievements of this Chapter

This chapter was written with three goals in mind. The first goal was to follow on from discussions in section 2.7.4 on the issues arising due to loop bandwidth variation ($\Delta K$), by defining exactly what contributes to $\Delta K$. This was achieved in section 5.1 which showed that although many factors contribute to $\Delta K$, most can be effectively eliminated through clever design. Following from this, $K_{VCO}$ variation ($\Delta K_{VCO}$) was shown to be the most problematic factor of $\Delta K$ whose reduction, as stated in section 3.9, is one of the primary challenges facing VCO design today.

The second goal of this chapter was to follow on from the differentially tuned VCO of chapter 4 in achieving low noise performance whilst maintaining a large tuning range which, as stated in section 3.9, is a major issue for modern day VCO designs. To address this, section 5.2.1 introduced the concept of splitting the VCO tuning range into a number of sub-bands, which together cover a large tuning range with the $K_{VCO}$ values of each sub-band being small so as to reduce noise contributions (see section 4.2.2). This was shown to be achieved using an array of switchable capacitors which can be switched in or out depending on the desired sub-band of operation, typically termed a switched capacitor array (SCA). Sections 5.2.1 and 5.2.2 together then provided a comprehensive overview of the design of an SCA in practice, by detailing its governing equations and optimum switch architectures to be employed.

Following from the previous two goals, the third goal of this chapter could be pursued which was to highlight the main issue with an SCA. In section 5.2.3 this was shown to be due to the fact that it introduces another factor contributing to $K_{VCO}$ variation (and hence $\Delta K$), namely that of band-to-band $K_{VCO}$ variation ($\Delta K_{VCO_{btb}}$). This effect and its consequences were thoroughly defined in section 5.2.3 with the resulting equations being verified through presented simulations. Such a thorough description was necessary to purvey to the reader how severe a problem $\Delta K_{VCO_{btb}}$ is, in addition to equipping them for forthcoming discussions on how it can be reduced. Such discussions followed in section 5.3.1 which reviewed the various attempts at reducing $\Delta K_{VCO_{btb}}$ reported in the literature. The various weaknesses exhibited by these approaches were highlighted, prior to section 5.3.2 introducing our proposed technique at addressing this problem. The proposed technique achieves sub-banding by replacing the conventional switched capacitor array with one single array of switchable varactors, hence termed a switched varactor array (SVA). As shown in section 5.3.3, each varactor branch can, through a succession of simple equations, be designed to reduce $\Delta K_{VCO_{btb}}$ without severely loading down the quality factor of the LC-tank ($Q_{tank}$), hence leading to reductions in loop bandwidth variation ($\Delta K$), power consumption and phase noise. In addition to this, the proposed technique maintains a near constant percentage overlap ($OV$) between bands to achieve

a PVT robust solution. All these claims were verified in section 5.4 which presented a complete performance analysis of the proposed technique showing it to achieve significant reductions in $\Delta K_{VCO_{btb}}$ over a VCO employing a conventional SCA, without requiring additional power whilst improving phase noise performance. As such, the proposed technique becomes highly attractive to low noise, low power applications particularly concerned with reducing loop bandwidth variation ($\Delta K$). Unfortunately, as detailed in section 5.5.1, all efforts failed in adapting the proposed technique to differential tuning. This would require further research which should be invested to realise the full potential of the switched varactor array.

Therefore, upon completing this chapter the reader should be convinced that the use of the novel SVA is extremely effective in simultaneously achieving a large tuning range with low noise performance, which significantly reduces loop bandwidth variation ($\Delta K$) at the cost of no additional power. As such, it should leave the reader satisfied that at this point in the thesis, all the issues with modern day PLL operation proposed throughout chapters 2 and 3, have now been effectively addressed.

# CHAPTER 6

## Simulations for the Final PLL of this Thesis

Up to this point in the thesis a wide spectrum of topics pertaining to PLL operation have been discussed. Through this, various issues with PLLs have been highlighted and arguments constructed in support of solutions proposed. Such solutions have therefore completely determined the final PLL of this thesis. For example, from discussions in chapter 2 it was decided to adopt a charge-pump PLL (CP-PLL) architecture which employs a second-order passive lag lead loop filter (LF). Then, from discussions in chapters 3 and 4 it was decided to make the PLL fully differential by employing a differential CP, transformed differential LF and a differentially tuned VCO. Finally, from discussions in chapter 5 it was decided to replace the conventional switched capacitor array (SCA) within the VCO with a switched varactor array (SVA). As a result, the final PLL of this thesis is a fully differential third-order type 2 CP-PLL, employing a second-order passive lag lead transformed differential LF, and differentially tuned VCO using an SVA.

To bring together the contributions from the previous chapters it is necessary to design and simulate such a PLL, which for brevity will be simply denoted as a fully differential PLL. The resulting simulations were performed using UMCs 90nm CMOS process, which are documented in this chapter where both the performance and functionality of the fully differential PLL are detailed.

## 6.1 Specifications

The specifications which the fully differential PLL was designed to achieve are presented in this section.

### 6.1.1 System Level Specifications

The system level specifications for the PLL are shown in Table 6.1.

| PLL architecture | CP-PLL |
|---|---|
| $f_{ref}$ | 30MHz |
| $f_{out_{max}}$ | 5.2GHz |
| $f_{out_{min}}$ | 4.4GHz |
| $f_{out_{mid}}$ | 4.8GHz |
| PM | $50^{\circ}$ [a] |
| $t_s$ | $< 220\mu$s [b] |
| $K$ | 1MHz [c] |
| $\Delta K$ | Reduce as much as possible |
| Power consumption | |
| Noise | |
| Area | |

[a] Based on recommendations from [20] for the chosen PLL architecture.

[b] Based on Bluetooth specifications.

[c] Based on feasible simulation times (see section 6.6).

**Table 6.1:** System level specifications for the PLL

The central frequency in Table 6.1 ($f_{out_{mid}}$) was chosen at 4.8GHz as this frequency achieves a very high inductor quality factor (19, see section 3.5) and can be divided down by two to make the PLL applicable to products operating in the highly popular 2.4GHz - 2.5GHz unlicensed industrial, scientific and medical (ISM) frequency bands occupied by standards such as Wi-Fi (IEEE 802.11b/g/n) and Bluetooth.

### 6.1.2 PFD Specifications

This thesis is primarily concerned with the analog blocks of a PLL (i.e. the CP, LF and VCO). As such, the PFD was not designed at gate level but synthesized using VHDL code to model the behaviour of the architecture shown in Fig. 2.3. Given that the worst case turn-on time for the CP switches was found through simulation to be $\approx 0.5$ns, the propagation delay of the PFD ($t_{pfd}$) was set to 1ns, such that any deadzone of operation could be safely avoided (see section 2.3).

### 6.1.3 Differential CP Specifications

The specifications for the differential CP are shown in Table 6.2.

| CP architecture | Differential |
|---|---|
| $V_{cp_{max}}$ | 0.75V [a] |
| $V_{cp_{min}}$ | 0.25V [a] |
| $V_{swing_{cp}}$ | 1V |
| $\Delta_{i_{cp}}$ | $\leq 0.1\%$ [b] |
| $\Delta_{i_{cp},V_{cp}}$ | $\leq 1\%$ [b] |
| Power consumption | Reduce as much as possible |
| Area | |

[a] Based on the analysis in section 4.3.2.

[b] Based on benchmarks set by [21].

**Table 6.2:** Differential CP specifications

### 6.1.4 Differential LF Specifications

The specifications for the differential LF are shown in Table 6.3.

| LF architecture | Differential passive lag-lead |
|---|---|
| $PM$ | $50^\circ$ [a] |
| Area | Reduce as much as possible |
| Component count | |

[a] Based on recommendations from [20] for the chosen PLL architecture.

**Table 6.3:** Differential LF specifications

### 6.1.5 Differentially Tuned VCO Specifications

The specifications for the differentially tuned VCO are shown in Table 6.4.

### 6.1.6 Feedback Divider Specifications

Once again as the thesis is primarily concerned with the analog blocks of a PLL (i.e. the CP, LF and VCO), as was the case for the PFD, the feedback divider was only synthesized using VHDL code. Due to its simplicity, an integer N feedback divider was modelled with a constant feedback divider ratio ($N$) of 160.[1]

[1] Although a constant feedback divider ratio is not representative of real world applications (for example within a frequency synthesizer), it is sufficient to demonstrate the functionality of the PLL.

| VCO architecture | LC-Tank [a] |
|---|---|
| $f_{VCO_{max}}$ | 5.2GHz |
| $f_{VCO_{min}}$ | 4.4GHz |
| $f_{VCO_{mid}}$ | 4.8GHz |
| TR | 16% |
| $K_{VCO}$ | $\approx$ 100MHz/V |
| OV | $>$ 30% [b] |
| PN | -119dBc/Hz at 3MHz offset [c] |
| CMRR | $>$ 20dB [d] |
| Power consumption | Reduce as much as possible |
| Area | |

[a] Chosen over a ring architecture to reduce phase noise (see section 3.1).

[b] Found through simulation to ensure the specified frequency range is covered over PVT variation.

[c] Based on Bluetooth specifications.

[d] Based on the analysis summarised in Table 4.10.

**Table 6.4:** Differentially tuned VCO specifications

### 6.1.7 Process Specifications

For confidentiality reasons only the basic specifications of the process used to design and simulate the fully differential PLL can be provided. These are shown in Table 6.5.

| Supplier | UMC |
|---|---|
| Basic description | 1P9M 90nm bulk CMOS |
| Vdd | 1V |

**Table 6.5:** Basic specifications for the process used to design and simulate the fully differential PLL

## 6.2 Differential CP

The architecture used for the differential CP of the PLL was described in section 4.3.3 and shown in Fig. 4.16, where the procedure used to design it is outlined in Appendix B1. This resulted in a circuit with the following power and area requirements.

| | |
|---|---|
| Vdd | 1V |
| $I_{cp}$ | 50$\mu$A |
| Power consumption | 170$\mu$W |
| Area | 1080$\mu$m$^2$ |

**Table 6.6:** Power and area requirements of the differential CP

### 6.2.1 Transistor Descriptions for the Differential CP

A complete description of the transistors used in the differential CP is summarised in Table 6.7. This describes the transistors with reference to Fig. 4.16 (i.e. device $M1$ in Fig. 4.16 refers to $M1$ in Table 6.7), in terms of their models, dimensions and DC operating points at a standard process corner.

| Transistor reference | $M1 \rightarrow M4$ | $M5 \rightarrow M8$ | $M9 \rightarrow M12$ | $M13 \rightarrow M15$ |
|---|---|---|---|---|
| Transistor model | HVT NMOS | NMOS | NMOS | HVT PMOS |
| W ($\mu$m) | 90 | 6.15 | 7.45 | 42 |
| L ($\mu$m) | 2 | 0.5 | 0.4 | 2 |
| $V_{gs}$ (V) | 0.4 | 0.6 | 0.2 | -0.6 |
| $V_{ds}$ (V) | 0.4 | 0.05 | 0.05 | -0.5 |
| $V_t$ (V) | 0.35 | 0.15 | 0.15 | -0.37 |
| $V_{ov}$ (V) | 0.05 | n/a | n/a | -0.23 |
| Region of operation | Saturation | Linear [a] | Linear | Saturation |

[a] Only when switched on. Operates in sub-threshold region otherwise.

**Table 6.7:** Transistor descriptions for the differential CP

Firstly, Table 6.7 shows high threshold voltage (HVT) NMOS and HVT PMOS devices to be used for $M1 \rightarrow M4$ and $M13 \rightarrow M15$ respectively. The reason for this is to enable low overdrive voltages ($V_{ov}$) for these transistors ($V_{ov} = V_{gs} - V_t$), thereby enabling large CP output voltage swings (see (4.17) $\rightarrow$ (4.19)). Secondly, Table 6.7 shows the drain-source voltages ($V_{ds}$) across all the transistors. These should be examined with reference to (B.1) and (B.2) in Appendix B1 where they can be seen to realise a steady output voltage of 0.5V (i.e. Vdd/2), thereby further maximising the CP output voltage swing (see section 4.3.4). Finally, Table 6.7 shows large dimensions to be employed for $M1 \rightarrow M4$ and $M13 \rightarrow M15$. The reason for this is to reduce device mismatch (see (2.8)) and hence static phase error

(see section 2.3.1). Furthermore, as this resulted in long channel devices (both employing lengths of 2$\mu$m), their increased output conductance's make them more robust against channel length modulation effects, hence further reducing static phase error.

### 6.2.2 Performance Analysis

The main advantages of employing a differential CP were shown in section 4.3.2 to be a doubled output voltage swing over a single-ended CP, significant reduction in the effects of common-mode noise and reduced mismatch current by orders of magnitude over a single-ended CP. As such, these will be the metrics used to assess the performance of the differential CP of Fig. 4.16.

*Output voltage swing*: Applying the relevant values from Table 6.7 to (4.17) and (4.18) result in the following maximum and minimum CP output voltages:

$$\begin{aligned} V_{cp_{max}} &= 1V + (-0.23V) \\ &= 0.77V \\ V_{cp_{min}} &= 0.05V + 0.05V + 0.05V \\ &= 0.15V \end{aligned}$$

Together $V_{cp_{max}}$ and $V_{cp_{min}}$ above realise a differential CP output voltage swing of 1.24V thereby exceeding the CP output voltage specifications in Table 6.2. As such, this differential CP is well suited to the low voltage process (Vdd = 1V) used to design it. In addition, as shown in section 4.2.2, this reduces $K_{VCO}$ requirements to meet the specified tuning range thereby enabling improved phase noise performance (see section 4.5.4).

*Common-mode noise*: To analyse the effects of common-mode noise on the differential CP, an identical setup to that described in section 4.3.2 was used. Firstly, to provide an intuitive view of common-mode noise in the circuit, its effect during steady state in the time domain was examined. This was achieved by placing a a signal source in series with the Vdd line which injected a sine wave of frequency 1MHz and amplitude of 10mV (i.e. 0.001% of Vdd). The resulting perturbations of the output signal ($\Delta v_o$) from its steady state value over time are shown in Fig. 6.1 which show the differential CP to exhibit excellent common-mode noise rejection capability for such noise on the Vdd line. As can be seen in the top right corner of the plot, the rms value of the resulting perturbations measures only 0.14pV representing a relatively insignificant value resulting from the introduced noise. Furthermore, recalling Fig. 4.6, this represents an improvement for such common-mode noise rejection by almost 20dB over the differential CP of Fig. 4.5.

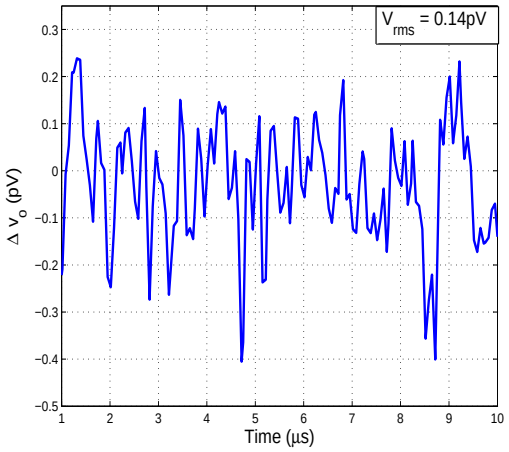



**Fig. 6.1:** $\Delta v_o$ for the differential CP

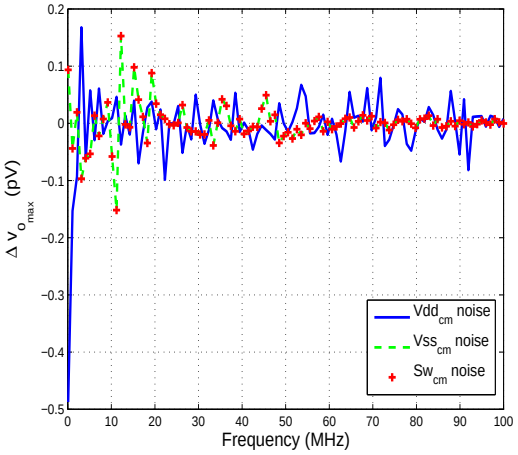



**Fig. 6.2:** $\Delta v_{o_{max}}$ for the differential CP

Although the exact reasons for this improvement were not analysed in this thesis, it is suspected that a major contributing factor is the increased use of stacking for the differential CP of Fig. 4.16 over that of Fig. 4.5, which could reduce such noise through the property of shielding [29].

Next, the effect of common-mode noise over frequency for all nodes susceptible to it was examined. Similar to the setup described in section 4.3.2, this was achieved by placing signal sources in series with the Vdd and Vss lines, and at the inputs to all the switches. These injected sine waves of amplitude 10mV, oscillating over a frequency range of 100kHz $\rightarrow$ 100MHz. The resulting maximum perturbations of the output signal from its steady state value ($\Delta v_{o_{max}}$), for each injected frequency at each susceptible node are plotted in Fig. 6.2. This shows the effects of common-mode noise on the Vdd line ("$Vdd_{cm}$ noise"), Vss line ("$Vss_{cm}$ noise") and at the inputs to the switches ("$Sw_{cm}$ noise"), to be reduced to negligible amounts. Furthermore, Fig. 6.2 shows this dramatic reduction to be held over frequency verifying the differential CP to exhibit excellent common-mode noise reduction capability for such noise occurring at both high and low frequencies.

*Static phase error*: Differential CPs were shown in section 4.3.2 to exhibit significant reductions in mismatch current, which from section 2.3.1, results in reduced static phase error. Therefore, one metric for analysing the static phase error performance of a CP is by examining its mismatch current.

The mismatch currents of the differential CP were analysed (similar to that for the differential CP of Fig. 4.5) by plotting its respective UP and DN currents ($I_{UP_1}$, $I_{UP_2}$, $I_{DN_1}$, $I_{DN_2}$) under steady state conditions over the CP output voltage swing specified in Table 6.2. These are shown in Fig. 6.3 where the respective currents are seen to be almost identical (i.e. $I_{UP_1} \approx I_{UP_2}$ and $I_{DN_1} \approx I_{DN_2}$), attributed primarily due to the excellent

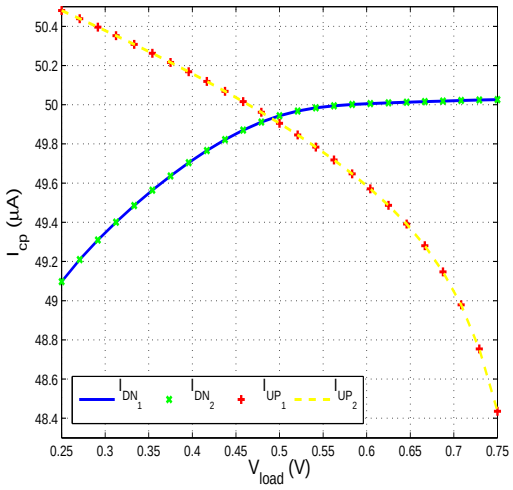



**Fig. 6.3:** $I_{UP}$ vs $I_{DN}$

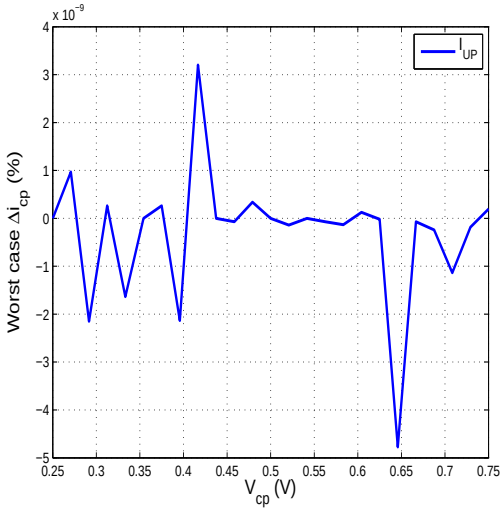



**Fig. 6.4:** $\Delta i_{cp}$

matching seen for UMCs 90nm CMOS process in section 4.3.2. The resulting mismatch current is plotted in Fig. 6.4 which shows its worst-case values [2] (Worst case $\Delta i_{cp}$), over the CP output voltage swing using (4.13). This shows the mismatch current to be reduced to negligible amounts, which in fact represents an improvement in its reduction by several orders of magnitude over the CP of Fig. 4.5. The reasons for this improvement are due to the large transistor dimensions used for the differential CP (see Table 6.2) and the use of current steering, inherent to its architecture (see section 2.3.1). Therefore, from the perspective of mismatch current reduction, the differential CP of Fig. 4.16 easily meets the specified values for $\Delta_{i_{cp}}$ in Table 6.2.

Recalling section 2.3.1, static phase error is also proportional to the length of time mismatch current flows during steady state over one period of the reference frequency. As such, another useful metric for analysing static phase error performance of a CP is by examining the length of time mismatch current flows for. In section 2.3.1 it was shown that for most CP architectures, this time duration is determined by the steady state pulse duration to maintain the CP switches on such that the deadzone region of operation can be eliminated. As such values are typically not much greater than one or two ns in practice (eg. $t_{pfd} = 1$ns for the fully differential PLL, see section 6.1.2), mismatch currents typically are restricted to flow for small time durations over each period of the reference frequency. However, the differential CP of Fig. 4.16 does not achieve this as it allows mismatch current to flow over the entire reference period. The reason this occurs is because all the switches ($M6 \rightarrow M8$) are realised using NMOS devices, any two of which will be on over the entire period of the reference frequency. Specifically, when the reference signal goes high, $M6$ and $M7$ will be on, whereas when it goes low, $M5$ and $M8$ will be on, thereby

[2] Plots the mismatches between $I_{UP_1}$ and $I_{UP_2}$.

enabling mismatch current to constantly flow during steady state.

Static phase error ($\phi_v$) was modelled by (2.7) under the assumption that mismatch current only flows for the steady state pulse duration ($t_{pfd}$). Adapting it to model static phase error when mismatch current flows over the entire period of the reference signal during steady state, results in the following:

$$|\phi_v| = 2\pi \frac{\Delta i_{cp}}{I_{cp}} \tag{6.1}$$

where mismatch current and CP nominal bias current are represented by $\Delta i_{cp}$ and $I_{cp}$ respectively. Dividing this by (2.7) show it to increase static phase error by the following factor:

$$|\phi_{v_{increase}}| = \frac{T_{ref}}{t_{pfd}} \tag{6.2}$$

where $T_{ref}$ represents one period of the reference frequency.

To show the potential significance of this increase, recall from Table 6.1 that the reference frequency ($f_{ref}$) for this PLL is set to 30MHz, thereby yielding $T_{ref} \approx$ 33ns. Given that $t_{pfd} =$ 1ns, this results in an increase in static phase error by approximately a factor of 33 over a differential CP exhibiting identical mismatch currents, but that only flow for the steady state pulse duration.

Given that the mismatch current for the differential CP of Fig. 4.16 was shown in Fig. 6.4 to be negligible, this increase does not significantly contribute to the static phase error of the fully differential PLL. Nevertheless, it should be noted as a limitation to the circuit since, when designed in processes which don't exhibit the same excellent matching seen for UMCs 90nm CMOS process, resulting mismatch currents may not be as negligible, whose contribution to static phase error will be significantly increased by (6.2). Therefore, from the perspective of overall static phase error reduction, the differential CP of Fig. 4.16 can be potentially problematic.

*Variation in CP current over its output voltage swing*: Fig. 6.3 shows a variation in CP current ($I_{cp}$) over its output voltage swing ($V_{swing_{cp}}$) to exist. Applying identical notation as seen in Fig. 4.13 results in the current measurements shown in Table 6.8. Inserting the relevant values from Table 6.8 into (4.14) and (4.15) yields $I_{cp}$ mismatches over $V_{swing_{cp}}$ ($\Delta_{i_{cp},V_{cp}}$) for the UP and DN networks of 2.1% and 1% respectively. The larger $\Delta_{i_{cp},V_{cp}}$ seen for the UP network occurs because its current defining transistors ($M14$ and $M15$ in Fig. 4.16) are directly connected to the output voltage, hence experiencing the entire CP output voltage swing across them. Since the current defining transistors in the DN network ($M3$ and $M4$ in Fig. 4.16) are effectively shielded by the CP switches ($M5 \rightarrow M8$) and the CMFB control transistors ($M9 \rightarrow M12$), the entire CP output

| Fig. 4.13 | Definition | Simulated value ($\mu A$) |
|---|---|---|
| $I_1$ | $I_{UP_{max}}$ | 50.48 |
| $I_3$ | $I_{UP_{min}}$ | 48.44 |
| $I_4$ | $I_{DN_{max}}$ | 50.03 |
| $I_6$ | $I_{DN_{min}}$ | 49.1 |

All quoted values are typical case i.e. taken from a standard process corner simulation

**Table 6.8:** Simulated values for $I_{UP}$ and $I_{DN}$ for the differential CP

voltage does not swing across them. As such, $M14$ and $M15$ become more susceptible to channel length modulation effects than $M3$ and $M4$.[3] Nevertheless, the worst case value for $\Delta_{i_{cp},V_{cp}}$ of 2.1% is seen to be greater than that specified in Table 6.2, whose end effect on loop bandwidth variation ($\Delta K$) will be discussed in section 6.5. Therefore, from the perspective of $I_{cp}$ variation over the CP output voltage swing, the differential CP of Fig. 4.16 becomes questionable for lower technology nodes where limited voltage supplies often prevent the use of stacking.

Overall, the analysis performed in this section show the differential CP of Fig. 4.16 to easily achieve the large specified output voltage swings, exhibit excellent reduction of common-mode noise effects whilst reducing mismatch current to negligible amounts. The disadvantages of the circuit however are that it allows the resulting mismatch current to constantly flow during steady state, where its variation in CP current over the output voltage swing is potentially inferior to other CP architectures. However, given that its advantages far outweigh its losses, this differential CP was decided in the early design phases to be employed as the differential CP in the fully differential PLL.

## 6.3 Transformed Differential LF

The transformed differential LF used in the final PLL of this thesis was identical to that analysed in section 4.4.2 and shown in Fig. 4.23, where the procedure used to design it is outlined in Appendix B2. In fact, as the LF was designed to meet a phase margin of 50° (see Table 6.3), its resulting component values and corresponding silicon area requirements are identical to those seen for the transformed differential LF described in Table 4.7. For reference, the LF component values are re-stated in Table 6.9.

[3]The differential CP of Fig. 4.5 exhibited superior values for $\Delta_{i_{cp},V_{cp}}$ as it employs stacking to a greater extent than the CP of Fig. 4.16.

| LF architecture | $R_1$ (kΩ) | $A_{R_1}$ ($\mu m^2$) | $C_1$ (pF) | $A_{C_1}$ ($mm^2$) | $C_2$ (pF) | $A_{C_2}$ ($mm^2$) | $A_{LF}$ ($mm^2$) | Component count |
|---|---|---|---|---|---|---|---|---|
| Differential | 36.56 | 26.76 | 113.42 | 0.06 | 19.6 | 0.01 | $\approx 0.07$ | 4 |

**Table 6.9:** Transformed differential LF requirements

To verify the specified phase margin in Table 6.3 was met, the open loop response of the fully differential PLL, employing the LF dimensions of Table 6.9, is plotted in Fig. 6.5. This plot was obtained using various values specified for the PLL in Tables 6.1, 6.3, 6.4 and 6.7, which clearly shows a phase margin of 50° to be achieved.

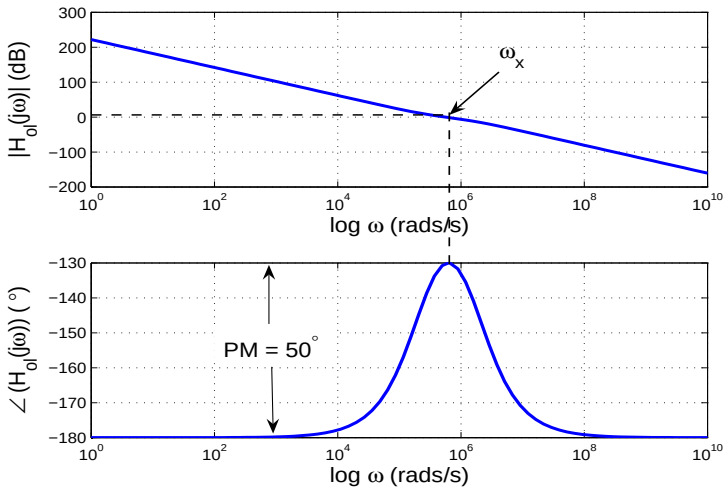



**Fig. 6.5:** Open-loop response for the final PLL of this thesis

### 6.3.1 Performance Analysis

The main advantages of employing the transformed differential LF were shown in section 4.4.3 to be reduced silicon area and component requirements. As such, these, and its behaviour over process and temperature variation (for on-chip implementation) will be the metrics used to assess the performance of the transformed differential LF in Fig. 4.23.

*Silicon area requirements*: Given that the transformed differential LF used in the fully differential PLL was identical to that described in section 4.4.3, its silicon area requirements ($\approx 0.07$ mm$^2$) were shown in Table 4.7 to be approximately half that for the single-ended LF of Fig. 2.24, attributed to its reduced capacitance requirements. As a result, it becomes more feasible to on-chip implementation hence realising the advantages discussed in section 4.4.1.

*Component count*: Similar to the above, Table 4.7 showed the transformed differential LF to require two less components over the conventional differential LF of Fig. 4.21, and only one additional component (a resistor) over the single-ended LF of Fig. 2.24. As explained in section 4.4.2, this is attractive to off-chip LF implementation with the transformed differential LF requiring less PCB effort to be realised than the differential LF of Fig. 4.21.

*On-chip component variation*: Due to its reduced silicon area requirements, the transformed differential LF was simulated in the fully differential PLL as an on-chip LF using polysilicon resistors and metal-insulator-metal (MIM) capacitors. In doing so, the variation of these components from their nominal values over process and temperature must be simulated. This is shown in Figs. 6.6 and 6.7 which plot the values of $R_1$ and $C_1$[4] for the LF of Fig. 4.23 over process and temperature variation, for UMCs 90nm CMOS process. Specifically this entailed simulating $R_1$ and $C_1$ at three temperatures (-40°, 27° and 125°) over three process corners (MAX, MIN and TYP (i.e. typical)) resulting in the nine simulation corners shown.

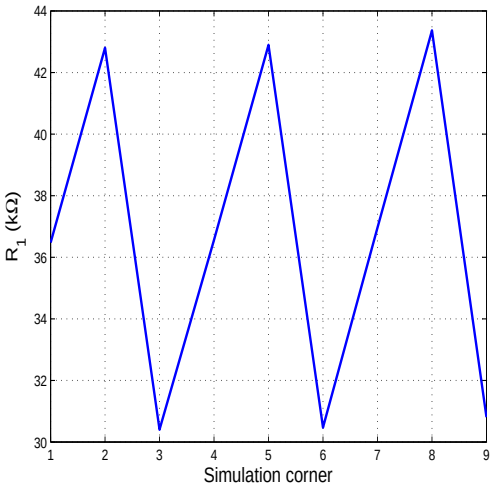



**Fig. 6.6:** $\Delta R_1$

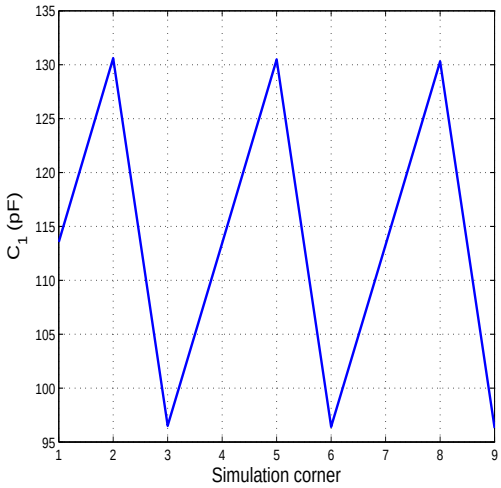



**Fig. 6.7:** $\Delta C_1$

The corresponding resistance and capacitance values at each corner plotted above are shown in Table 6.10. From this, $C_1$ can be seen to exhibit a worst case variation over temperature of 0.46%, occurring at the MAX process corner. The worst case variation of $R_1$ over temperature is then shown to be 1.3% occurring equally over all process corners. This indicates that the polysilicon in UMCs 90nm CMOS process exhibits a slightly larger temperature co-efficient that the silicon dioxide used as the dielectric within the MIM capacitors. Nevertheless, these temperature variations are insignificant in comparison to the process variations, which for $C_1$ and $R_1$ are seen to be $\approx 30\%$ and $\approx 34\%$ respectively.

[4] $C_2$ is not plotted over process and temperature variation as, assuming it is laid out close to $C_1$, its variations will be almost identical to those seen for $C_1$

| Simulation corner | Temperature (°) | Resistor model | $R_1$ (kΩ) | Capacitor model | $C_1$ (pF) |
|---|---|---|---|---|---|
| 1 | -40 | TYP | 36.48 | TYP | 113.55 |
| 2 | -40 | MAX | 42.8 | MAX | 130.6 |
| 3 | -40 | MIN | 30.4 | MIN | 96.5 |
| 4 | 27 | TYP | 36.56 | TYP | 113.45 |
| 5 | 27 | MAX | 42.89 | MAX | 130.48 |
| 6 | 27 | MIN | 30.47 | MIN | 96.42 |
| 7 | 125 | TYP | 36.96 | TYP | 113.3 |
| 8 | 125 | MAX | 43.36 | MAX | 130 |
| 9 | 125 | MIN | 30.8 | MIN | 96.29 |

**Table 6.10:** Simulated values for $R_1$ and $C_1$ over process and temperature

Due to the small temperature co-efficients previously discussed, these variations are then more or less equal over all temperatures. In total then, the resulting variations in $C_1$ and $R_1$ over process and temperature are shown to be $\approx 30\%$ and $\approx 35\%$ respectively.

Given these large variations, the obvious question to ask is what effect will they have on overall PLL performance. Stability was introduced in section 2.6 where it was stated to be the most important design criterion for a PLL, quantifiable by the PLLs phase margin ($PM$). For a third-order type 2 PLL employing a passive lag-lead LF, its $PM$ was shown in (2.43) to completely determine the ratio of the LF capacitance's $C_1/C_2$. Thinking of this another way, by re-working (2.43) to the form shown in (6.3), $PM$ can be viewed as being completely determined by the ratio of $C_2/C_1$ as follows:

$$PM = sin^{-1}\left(\frac{1}{1+2\,(C_2/C_1)}\right) \tag{6.3}$$

Therefore, provided $C_1$ and $C_2$ are realised using the same physical devices (MIM capacitors for example) and are laid out close to each other, their resulting variations over process and temperature will be very similar (i.e. their PVT variations will be localised). As such, the ratio of $C_2/C_1$ will not significantly change over process and temperature thereby yielding insignificant variations in $PM$. Therefore from a stability point of view, variation of the LF components over process and temperature is not an issue, implying the specified $PM$ in Table 6.3 will be maintained over such variations.

Loop bandwidth ($K$) was introduced in section 2.7 as the most important design parameter of a PLL, where section 2.7.4 detailed the many issues arising from its variation ($\Delta K$). For a third-order type 2 PLL employing a passive lag-lead LF, its loop

bandwidth was shown in (2.42) and (2.44) to be approximately independent on LF capacitance's, provided the ratio of $C_1/C_2$ is sufficiently large. Similar to the previous argument on stability, provided both $C_1$ and $C_2$ are realised using the same physical devices and are laid out close to each other, the ratio $C_1/C_2$ will not significantly vary over process and temperature variation. Therefore, assuming this ratio was large enough in the first place to ensure $K$ is independent on $C_2$ and $C_1$, this independence will be held over process and temperature variation. As such, variations in the LF capacitance's over process and temperature will also not significantly contribute to $\Delta K$.

Loop bandwidth ($K$) for a third-order type 2 PLL employing a passive lag-lead LF was shown in (2.44) to be directly proportional to the LF resistor ($R_1$) and so varies linearly with $R_1$ (see (5.1)). However, since $K$ is also directly proportional to charge-pump current ($I_{cp}$), as explained in section 5.1, provided the current defining resistor for $I_{cp}$ ($R_{I_{cp}}$) is realised using the same physical device as $R_1$ and laid out close to it, the effect of variations in $R_1$ over process and temperature on $K$ will be effectively cancelled by inverse variations in $I_{cp}$.[5] As such, variations in the LF resistor over process and temperature will also not significantly contribute to $\Delta K$.

Finally, section 2.8 introduced noise as being the second most important design criterion for a PLL (next to stability). Given that variations in the LF components over process and temperature do not significantly contribute to variations in loop bandwidth ($\Delta K$), noise contributions due to $\Delta K$ (see sections 2.7.4 and 2.8.3) will be insignificant. However, the same cannot be said for noise contributions from $R_1$ alone as any increases in it leads to direct increases in its associated thermal noise (see (4.32)). As variations in $R_1$ over process and temperature of $\approx 35\%$ were observed, $R_1$ and hence its thermal noise can potentially increase by 17.5% over process and temperature variation. This represents the only major issue with LF component variation over process and temperature, which becomes particularly prevalent in differential LFs as they employ two resistors (see Figs. 4.21 and 4.23). Therefore, for the transformed differential LF used in the final PLL of this thesis, its overall contributions to thermal noise can potentially increase by 2 x 17.5% (i.e. 35%) over process and temperature variation. Therefore, from the point of view of low noise operation, variation of the LFs resistor(s) presents a major issue, whose effect is doubled using a differential LF. As suggested in section 4.4.2, this issue can be addressed by increasing $I_{cp}$ such that $R$ in (4.32) is reduced (see Table B.2 in Appendix B1) hence generating less thermal noise. However, as this results in increased overall power, capacitance and hence silicon area requirements, a more effective solution should be research, potentially through the use of a dual path filter described in [87].

[5] This shows the importance in charge-pump biasing as, had it not been correctly achieved, the resulting variations in $R_1$ by $\approx 35\%$ could have resulted in variations in $K$ by the same amount.

Overall, the analysis performed in this section show the transformed differential LF of Fig. 4.23 to achieve the specified phase margin using significantly less silicon area than its conventional differential counterpart, over which it requires two less components to be implemented. When implemented on-chip, provided the relevant components of the LF are realised using the same physical devices and laid out close to each other, their variations over process and temperature were shown to induce negligible effects on stability and loop bandwidth variation. The disadvantage of the circuit however is that the increased thermal noise it exhibits due to the additional resistor required over its single-ended counterpart (see section 4.4.2), experiences further increases over process and temperature variation. However, given that a differential CP was used in the final PLL of this thesis (to realise the advantages discussed in section 6.4.2), a differential LF was always necessary, where due to the advantages over its conventional differential counterpart, the transformed differential LF of Fig. 4.23 was employed as the differential LF in the fully differential PLL.

## 6.4 Differentially Tuned VCO

The VCO used in the final PLL of this thesis was based on the PVT robust hybrid topology of Fig. 3.37, employing the modified symmetrical varactor configuration of Fig. 4.35 to maximise its common-mode rejection ratio (see Table 4.9). To achieve a large tuning range with low $K_{VCO}$ values (and hence improved phase noise), the VCO employed sub-banding (see section 5.2), achieved using a switched varactor array (SVA) to reduce $K_{VCO}$ band to band variation (see section 5.3). The resulting VCO was identical to that analysed in section 5.4 and shown in Fig. 5.14, where the design procedure used for it is outlined in Appendix B3.

### 6.4.1 Component Descriptions for the Differentially Tuned VCO

The various components of the VCO are described in Tables 6.11 $\rightarrow$ 6.15. Table 6.11 describes the biasing transistors of the VCO (i.e. $M1 \rightarrow M4$ in Fig. 5.14), in terms of their models, dimensions and DC operating points at a standard process corner. This shows the differential cross-coupled pair ($M3$, $M4$) to be realised with RF NMOS devices. These are simply NMOS devices which sit in their own specific $p$-well, separated from the $p$-substrate by a buried deep $n$-well. The reason for this is it isolates the devices from substrate noise thereby achieving superior noise performance over standard NMOS devices. Although such devices do require additional area over their standard counterparts, their use for sensitive transistors such as the high frequency switching cross-coupled differential pair, is generally advised.

| Transistor reference | $M1$, $M2$ | $M3$, $M4$ |
|---|---|---|
| Transistor model | PMOS | RF NMOS |
| W ($\mu$m) | 16.6 | 4 |
| L ($\mu$m) | 1 | 0.08 |
| $V_{gs}$ (V) | -0.5 | 0.5 |
| $V_{ds}$ (V) | -0.5 | 0.5 |
| $V_t$ (V) | -0.12 | 0.25 |
| $V_{ov}$ (V) | -0.38 | 0.25 |
| Region of operation | Saturation [a] | Saturation [a] |

[a] Small-signal operation.

**Table 6.11:** Biasing transistor descriptions for the differentially tuned VCO

Table 6.12 then describes the varactors used in the VCO tank in terms of the model used, dimensions and capacitance ($C$) at a standard corner, for an applied sine wave of 4.8GHz and control voltage ($V_{ctrl}$) of 0.5V.

| Varactor model | wf ($\mu$m) | lf ($\mu$m) | nf | C (fF) |
|---|---|---|---|---|
| Diode | 2 | 10 | 16 | 60 |

**Table 6.12:** Tank varactor descriptions for the differentially tuned VCO

In Table 6.12, the widths and lengths of the varactors fingers are represented as wf and lf respectively, with the number of fingers used being represented by nf. It should be noted that the dimensions of Table 6.12 resulted from various parametric sweeps, where they were seen to achieve an optimum quality factor of 117 for the complete varactor configuration. Due to their small capacitance values, the varactors dominate the overall capacitive characteristics of the tank which, for $V_{ctrl} = 0.5$V, measured a total capacitance of 110fF under the application of a 4.8GHz sine wave at a standard process corner.

Table 6.13 describes the biasing components of the varactor configuration with reference to Fig. 4.35, in terms of the physical devices used and their corresponding dimensions. The resulting capacitance ($C_s$) and resistance ($R_b$) values at a standard process corner are also provided, which for the capacitors was obtained under the application of a 4.8GHz sine wave.

| $C_s$ device | $C_s$ (fF) | $W_{C_s}$ ($\mu$m) | $L_{C_s}$ ($\mu$m) | $R_b$ device | $R_b$ (k$\Omega$) | $W_{R_b}$ ($\mu$m) | $L_{R_b}$ ($\mu$m) |
|---|---|---|---|---|---|---|---|
| MIM | 160 | 9 | 9 | Polysilicon | $\approx 1$ | 1 | 10 |

**Table 6.13:** Tank biasing component descriptions for the differentially tuned VCO

In Table 6.13, the widths and lengths of $C_s$ are represented by $W_{C_s}$ and $L_{C_s}$ respectively, with those for $R_b$ being represented by $W_{R_b}$ and $L_{R_b}$ respectively.

As described in section 4.5.4, the VCO employed a hollow spiral differential inductor whose dimensions were chosen to optimise its quality factor. A maximum quality factor of 19.4 for an applied 4.8GHz sine wave, was shown to be achieved in Fig. 3.29 with the dimensions provided in Table 3.3. These are re-stated in Table 6.14 for reference, along with the resulting inductance ($L$) and quality factor ($Q_L$), obtained at a standard process corner for an applied 4.8GHz sine wave.[6]

| Inductor model | w ($\mu$m) | s ($\mu$m) | nt | od ($\mu$m) | $Q_L$ | L (nH) |
|---|---|---|---|---|---|---|
| Differential hollow spiral | 3.5 | 2.9 | 5 | 136 | 19.4 | 4.4 |

**Table 6.14:** Inductor descriptions for the differentially tuned VCO

In Table 6.14, the widths of the metal conductors, corresponding spacings, number of metal turns and outer diameter are represented by w, s, nt and od respectively. The large dimensions of the inductor should be observed from Table 6.14 which, as will be shown in section 6.4.2, dominated the overall area requirements of the VCO.

As previously stated, the VCO was identical to that analysed in section 5.4 and so split the tuning range into 16 sub-bands using an SVA consisting of 15 branches. Identical transistors were employed within each branch which are described in Table 6.15 with reference to Fig. 5.13, in terms of their models, dimensions and DC operating points at a standard process corner. This shows devices $M1$ and $M2$ to be made wide and short. This is to increase the parallel resistance of the branch ($R_{p_{br}}$, see section 5.2.2), with their widths being limited by the resulting parasitic capacitance's of the branch ($C_{par_{br}}$). Similarly, Table 6.15 shows $M3 \rightarrow M6$ to be made narrow (employing the minimum allowable widths for UMCs 90nm CMOS process) to reduce $C_{par_{br}}$, with their lengths increased so as to optimise $R_{p_{br}}$ (see Fig. 5.6).

[6]It should be noted the inductor characteristics are the least susceptible to PVT variation in a VCO.

| Transistor reference | $M1$, $M2$ | $M3 \rightarrow M6$ |
|---|---|---|
| Transistor model | NMOS | PMOS |
| W ($\mu$m) | 5 | 0.12 |
| L ($\mu$m) | 0.08 | 0.3 |
| $V_{gs}$ (V) | 1 [a] | $\approx$ - 0.5 [b] |
| $V_{ds}$ (V) | $\approx$ 0 [a] | $\approx$ 0 [b] |
| $V_t$ (V) | 0.3 | -0.18 |
| $V_{ov}$ (V) | 0.82 | -0.32 |
| Region of operation | Linear [a] | Linear [b] |

[a] When the branch is switched on.

[b] When the branch is switched off.

**Table 6.15:** SVA transistor descriptions for the differentially tuned VCO

Identical resistors to those described in Table 6.13 were used in each branch of the SVA. The ac-coupling capacitors used were then realised as MIM devices whose widths and lengths were maintained constant at 5$\mu$m each. The required capacitance's from (5.17) and (5.20), to realise the specified tuning range whilst significantly reducing $K_{VCO}$ band to band variation ($\Delta K_{VCO_{btb}}$), were then obtained by varying the dimensions of the diode varactors within each branch as appropriate.

In addition to the components discussed, an MIM capacitor was placed at the drain of $M2$ to somewhat suppress flicker noise effects (see section 3.8), which required a total area of 20$\mu$m$^2$. The VCO also included an artificially introduced capacitance to account for parasitic capacitance's introduced during layout (routing, substrate and coupling capacitance's) which, for a similar VCO architecture laid out using UMCs 90nm CMOS process, were shown to total up to $\approx$ 400fF.

### 6.4.2 Performance Analysis

The primary metric used to analyse the performance of any VCO is its tuning range. In addition to this, other important metrics are phase noise, power and area consumption, and particularly relevant to this thesis, $K_{VCO}$ variation. As such, all of the above will be

used to assess the performance of the VCO of Fig. 5.14.

*Tuning range*: As previously stated, the VCO used in the fully differential PLL was identical to that analysed in section 5.4, whose tuning characteristics were shown in Fig. 5.15. From this, the VCO was shown to operate over a frequency range from 4.35GHz to 5.5GHz (i.e 23%), thereby satisfying the tuning range requirements of Tables 6.1 and 6.4.

*Phase noise*: The simulated phase noise performance of the VCO was plotted in Fig. 5.19 (along with that for a comparative VCO), with specific measurements being made at 1 MHz offset from the carrier frequency. The simulated phase noise performance of the VCO alone is plotted in Fig. 6.8.

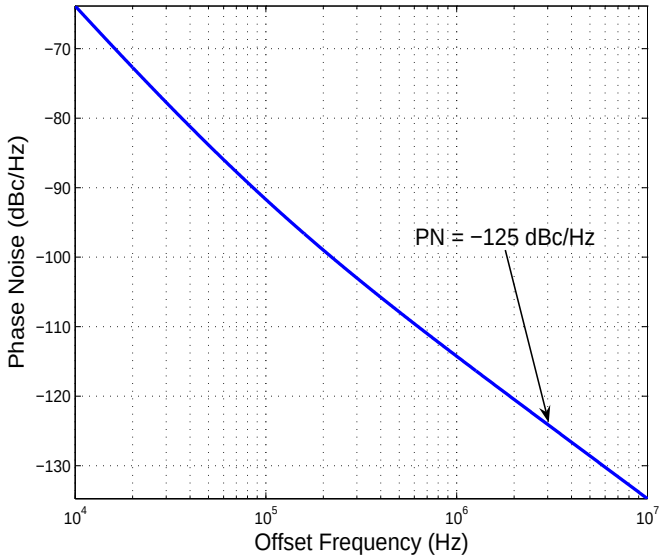



**Fig. 6.8:** Simulated phase noise performance of the VCO

As can be seen from Fig. 6.8, phase noise measurements were taken at 3 MHz offset from the carrier frequency to assess if the phase noise specifications of Table 6.4 have been met. From this, we can see a phase noise of -125dBc/Hz at 3MHz offset to be achieved, thereby exceeding the specified value of -119dBc/Hz in Table 6.4, by 6dB.

*Power consumption*: The power consumption of the entire VCO was shown in Table 5.2 to be 850$\mu$W ($I_{VCO}$ = 800$\mu$A), which from Table 5.3, was seen to be significantly less than previously reported values for similar VCOs. Therefore, from the perspective of the statement to reduce power consumption as much as possible in Table 6.4, the VCO proves an attractive solution.

*Area requirements*: The overall area requirements for the VCO were 0.018 mm$^2$. Table 6.16 shows an ordered breakdown of this area in terms of the area requirements for the various components of the VCO, discussed in section 6.4.1.

| VCO Component | Area ($\mu$m$^2$) |
|---|---|
| Inductor | 14,526 (0.0145 mm$^2$) |
| SVA | 2145 |
| Tank varactor configuration [a] | 1356 |
| Flicker noise suppression capacitor | 20 |
| Biasing transistors | 16.92 |
| Total area | 18,064 (0.018 mm$^2$) |

*a* Includes the biasing components ($R_b$ and $C_s$)

**Table 6.16:** Ordered breakdown of the overall VCO area requirements

Table 6.16 shows the inductor to dominate the overall area requirements of the VCO, where it accounts for $\approx$ 80% of the total VCO area. As suggested in Table 3.1, this represents one of the main disadvantages with on-chip inductors and hence LC-tanks in general. For off-chip inductors, the issue is simply dealt with by wrapping the metal conductors around a magnetic core to confine their magnetic fields, such that the required inductance can be achieved using smaller areas. However, realising such a solution in silicon has, up to this point in writing, not been achieved in research, thereby making on-chip inductors amongst the most area hungry components (in addition to the LF capacitors, see Table 6.9) of a PLL. Therefore, the statement to reduce area as much as possible in Table 6.4, has not been sufficiently met due to the physical limitations imposed by modern day fabrication processes.

*CMRR*: As previously stated, the VCO used in the fully differential PLL was identical to that analysed in section 5.4, where it was shown to achieve a CMRR of 22.5dB, thereby easily meeting the specified value in Table 6.4.

*$K_{VCO}$ variation*: In chapter 5, two sources of $K_{VCO}$ variation were shown to exist: in-band ($\Delta K_{VCO_{inb}}$) and band-to-band ($\Delta K_{VCO_{btb}}$) variation. As shown in section 5.3, the use of an SVA significantly reduces $\Delta K_{VCO_{btb}}$, with Table 5.1 showing it to be reduced

to ± 4.6% for the concerned VCO.

The use of diode varactors then somewhat reduced $\Delta K_{VCO_{inb}}$ due to their higher linearity over AMOS varactors, seen for UMCs 90nm CMOS process in section 3.4.3. Nevertheless $\Delta K_{VCO_{inb}}$ still remains prevalent, measuring an average variation across each band at a standard process corner of $\approx \pm$ 25%. Given the significant reductions in $\Delta K_{VCO_{btb}}$ shown to be achievable with an SVA, as will be shown in section 6.5, $\Delta K_{VCO_{inb}}$ thus becomes the primary contributing factor to loop bandwidth variation ($\Delta K$).

Section 3.9 stated $K_{VCO}$ variation to represent one of the primary challenges facing VCO (and hence PLL) design today. Given the significant reduction seen for $\Delta K_{VCO_{btb}}$, we can now restate this by specifying the reduction of $K_{VCO_{inb}}$ to be one of the primary challenges facing VCO (and hence PLL) design today. Apart from the use of diode varactors, no further measures were taken to reduce $K_{VCO_{inb}}$ in the VCO for the final PLL of this thesis. The recently reported distributed varactor biasing technique in [88] was however investigated, where it was shown to yield promising results, albeit at the cost of increased power consumption and reduced tuning range. Further research should therefore be invested into this promising technique to realise its full potential/optimisation.

### 6.4.3 Digital Calibration

As explained in section 5.2.1, the branches of a switched capacitor or switched varactor array are selectable via a thermometer encoded digital word $n-1$ bits long, where $n$ represents the number of sub-bands. The selection of the required branch to achieve a specific frequency of operation requires digital calibration which locates the correct sub-band of operation by either:

1. Measuring the VCO frequency ($f_{VCO}$) for a desired control voltage.
2. Measuring the VCO control voltage ($V_{ctrl}$) when the PLL is in lock.

In [26] approach 1 is taken by initially switching out the PLL loop, clamping $V_{ctrl}$ to Vdd/2, and comparing counts of the periods for $f_{VCO}$ with those for the input reference frequency ($f_{ref}$) using a separate calibration loop. Through this, $f_{VCO}$ can be assessed to be within a specified frequency window determined (apriori) by the desired frequency of operation and the frequency range covered by a sub-band. The advantage of this approach is that it is predominantly digital and thus more suited to lower technology nodes, with its main disadvantage being long calibration times due to the large number of counts required in the comparison process. An improvement to this is reported in [89], where the time taken to perform the required number of counts is reduced through up-sampling, thereby leading to shorter calibration times. In [90] approach 2 is used where $V_{ctrl}$ is monitored for a given input reference frequency ($f_{ref}$) to see if it lies within a voltage

window determined by the CP output voltage swing (see Fig. 4.12). The disadvantage of this approach is it relies heavily on the matching between two PLL loops thus making it less suited to lower technology nodes where device mismatch increases [12], [14]. In addition, the PLL loop must settle each time an adjustment is made to the calibration word before $V_{ctrl}$ can be measured, leading to long calibration times. An improvement to this approach is presented in [91] where only one loop is employed thus removing errors arising from mismatches between loops and reducing area. Nevertheless, the PLL loop still needs time to settle before each measurement of $V_{ctrl}$, leading to similar prolonged calibration times. In addition, both [90] and [91] employ comparators for $V_{ctrl}$ monitoring leading to concerns regarding offset voltages for lower technology nodes. An alternative approach is presented in [92] where $f_{VCO}$ is monitored by directly converting signal periods into voltages, thereby eliminating the need of waiting for loop settling times or long counts in the comparison process. The advantage of this is fast calibration ($< 4$ $\mu$s) with the disadvantage being the complex circuitry needed to achieve it. The resulting circuitry is area and power consuming, places heavy demands on matching and employs comparators, making it less suited to low power applications fabricated in lower technology nodes.

Therefore, due to its simplicity and applicability to lower technology nodes, the technique described in [26] was applied in the fully differential PLL. The operation of this technique is shown in Fig. 6.9 where the VCO output frequency ($f_{VCO}$) is plotted in the top subplot with its corresponding value ($f_{VCO}/N$),[7] when divided down by the integer value of $N = 160$ (see section 6.1.6), plotted in the bottom subplot. In addition, since the technique locates the correct sub-band with reference to the input reference frequency, $f_{ref}$ is also plotted in the bottom subplot where it can be seen to remain constant at 28.57MHz. Immediately obvious from this plot is the digital nature of the technique in locating the correct sub-band.

In the simulation of Fig. 6.9, the normal PLL loop was initially switched out with the calibration loop being switched in and VCO set to the bottom sub-band (i.e "calWord" in Fig. 5.14 was set to "11 ... 1"). As can be seen, this produced a frequency of 4.3GHz which, when divided down by $N = 160$, produced a frequency of 26.87MHz (i.e. 1.7MHz below $f_{ref}$). As a result, the counting process determined the bottom sub-band to operate over too low a frequency range, thereby moving operation up to the next sub-band. As explained in section 5.2.1, this is achieved by switching out one branch of the array, digitally achieved by decrementing the calibration word ("calWord" in Fig. 5.14) to "11 ... 10". As can be seen in Fig. 6.9, this produces a step-like increase in $f_{VCO}$ to 4.37GHz thereby producing a corresponding step-like increase in $f_{VCO}/N$ to 27.3MHz. Similar to before, the counting process determined the second from bottom sub-band to

[7] In Fig. 6.9, $f_{VCO}$ can be seen to be exhibit glitches (i.e. appear as non-constant). This is not representative of actual circuit behaviour and is due to an anomaly at the switching transients of the synthesized feedback divider in the ADMS mixed mode simulator used to perform the simulation.

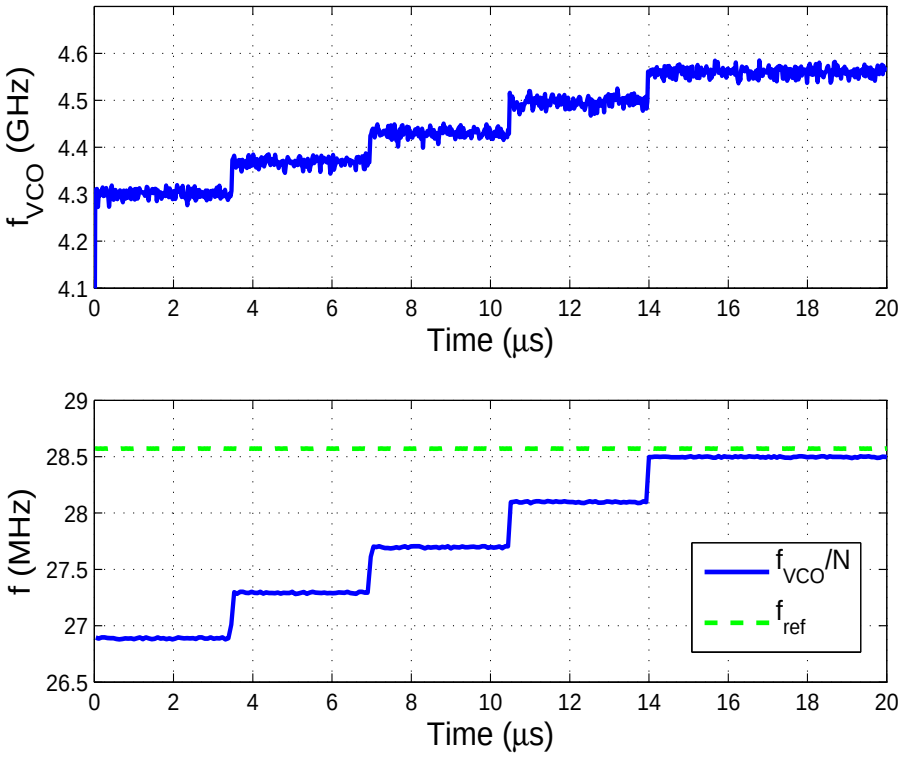



**Fig. 6.9:** VCO digital calibration simulation

also operate over too low a frequency range thereby moving operation up to the next sub-band. This process continued until the digital calibration technique moved operation up to the sub-band fifth from the bottom to produce an output frequency of 4.56GHz which, when divided down, produced a frequency of 28.5MHz (i.e. 70kHz below $f_{ref}$). Since this difference between $f_{ref}$ and $f_{VCO}/N$ is easily covered by the frequency range of a sub-band, the digital calibration technique, using apriori knowledge of the frequency range for a sub-band, determined the correct sub-band to now be located, hence switching out the calibration loop to allow normal PLL operation to proceed. Under normal operation then, the PLL will adjust $V_{ctrl}$ as appropriate to reduce the difference between $f_{ref}$ and $f_{VCO}/N$ to within the limitations of the occurring static phase offset (see section 2.3.1).

As previously mentioned, the main disadvantage with the employed digital calibration technique is the large number of counts required in the comparison process. The reason for these large counts is to minimise errors arising from initial phase uncertainties between $f_{ref}$ and $f_{VCO}/N$, where the length of the count determines the accuracy of the final measurement (or decision). For example: if 1% frequency accuracy is required, then at least 100 counts are required. This accuracy specification was adopted for the final VCO of this thesis which, from Fig. 6.9 can be seen to take $\approx 3.5\mu$s to make each decision/adjustment, leading to a worst case calibration time of $\approx 56\mu$s (i.e. 16 x 3.5$\mu$s).

As this calibration time is in addition to PLL locking time, it greatly adds to the overall settling time of the loop and so may not be optimum for frequency hopping systems such as those used in WCDMA technologies.

## 6.5 Loop Bandwidth Variation

Given the emphasis placed on loop bandwidth variation ($\Delta K$) in this thesis, it is appropriate at this stage to assess the performance of the fully differential PLL in terms of $\Delta K$.

The various factors contributing to loop bandwidth variation ($\Delta K$) were shown in (5.1), which are re-stated here for reference:

$$\Delta K = \frac{\Delta I_{cp} \Delta K_{VCO} \Delta R_1}{2\pi \Delta N}$$

Firstly, $\Delta K$ can be seen to be inversely proportional to the feedback divider ratio ($N$). However, as explained in section 5.1, provided the charge-pump current ($I_{cp}$) is made a function of $N$ (i.e. $I_{cp}(N)$), any changes in $N$ will be counteracted by corresponding changes in $I_{cp}$, such that no net change to $\Delta K$ will occur. As such, this source of $\Delta K$ can be ignored in the analysis.

Secondly, $\Delta K$ can be seen to be directly proportional to the LF resistor ($R_1$). Given that the LF was simulated as an on-chip LF, as shown in section 6.3.1, $R_1$ can experience up to 35% variation over process and temperature. If unaccounted for, this would contribute to $\Delta K$ by the same amount. However, as explained in sections 5.1 and 6.3.1, provided the current defining resistor for $I_{cp}$ ($R_{I_{cp}}$) is realised using the same physical device as $R_1$ and laid out close to it, the net contributions to $\Delta K$ will be negligible. As such, this source of $\Delta K$ can also be ignored in the analysis.

Thirdly, $\Delta K$ can be seen to be directly proportional to $I_{cp}$. Following from the previous discussion (and section 5.1), variations in $I_{cp}$ due to variations in its current defining resistor ($R_{I_{cp}}$) will have negligible effect on $\Delta K$. As such, this source of $\Delta I_{cp}$ can be ignored in the analysis, leaving the variation of $I_{cp}$ across the CP output voltage swing ($\Delta_{i_{cp,V_{cp}}}$) as the primary contributor to $\Delta I_{cp}$. From section 6.4.2, a worst case value for $\Delta_{i_{cp,V_{cp}}}$ of 2.1% was shown to result, leading to a corresponding variation in $K$. As such, out of $\Delta N$, $\Delta I_{cp}$ and $\Delta R_1$, $\Delta K = 2.1\%$.

This value does however significantly increase when we take into account the final contributor to $\Delta K$, and that is $\Delta K_{VCO}$. As shown in chapter 5, the two contributing factors to $\Delta K_{VCO}$ are in-band $K_{VCO}$ variation ($K_{VCO_{inb}}$) and band to band $K_{VCO}$ variation ($\Delta K_{VCO_{btb}}$). In section 5.4, the use of a switched varactor array (SVA) was shown to achieve significant reductions in $\Delta K_{VCO_{btb}}$ down to $\pm$ 4.6%. In other words, $\Delta K_{VCO_{btb}} = 9.2\%$ resulting in a total $\Delta K$ (including $\Delta N$, $\Delta I_{cp}$, $\Delta R_1$ and $\Delta K_{VCO_{btb}}$)

of 11.3%. Apart from the use of diode varactors however (see section 3.4.3), no further measures were taken to reduce $\Delta K_{VCO_{inb}}$ which, as stated in section 6.4.2, resulted in $\Delta K_{VCO_{inb}} \approx \pm 25\%$. In other words, $\Delta K_{VCO_{inb}} \approx 50\%$ resulting in an overall $\Delta K$ of $\approx 61.3\%$.

Although this is a large value, it is important to note that, without the use of an SVA to reduce $\Delta K_{VCO_{btb}}$, the resulting overall $\Delta K$ would (using the values in Table 5.2) have almost doubled at 112%.[8] This illustrates two points. Firstly it illustrates the need for $\Delta K_{VCO_{btb}}$ reduction to significantly reduce $\Delta K$. Secondly it illustrates the extent of the problem of reducing $\Delta K$ since, even with the significant reductions achieved in $\Delta K_{VCO_{btb}}$, resulting values for $\Delta K$ were still above 60%. Therefore as discussed in section 6.4.2, to gain further reductions in $\Delta K$, its remaining principal contributing factor $\Delta K_{VCO_{inb}}$ must also be addressed.[9]

The total loop bandwidth variation ($\Delta K$) and its contributing factors for the fully differential PLL are thus summarised in Table 6.17.

| Parameter | Variation (%) |
|---|---|
| $\Delta K$ | $\approx 61.3$ |
| Contributing parameters | |
| $\Delta I_{cp}$ | 2.1 |
| $\Delta K_{VCO_{btb}}$ | 9.2 |
| $\Delta K_{VCO_{inb}}$ | $\approx 50$ |

**Table 6.17:** $\Delta K$ and its contributing parameters for the final PLL of this thesis

## 6.6 PLL Locking Performance

By connecting together all the blocks thus far discussed in this chapter (using Fig. 2.1 as a blueprint) the fully differential PLL is realised, whose detailed schematic will be shown in Fig. 6.12. The general operation of such a PLL was summarised in Table 4.8 with reference to the CP outputs ($CP^-$, $CP^+$), the differential tuning inputs ($V_{ctrl}^-$, $V_{ctrl}^+$) and the reference ($\phi_{ref}$) and feedback ($\phi_{fb}$) signals. Therefore, to verify the fully differential PLL follows this general operation, its behaviour with respect to each of these inputs and outputs is plotted in Fig. 6.10. Due to the abstract nature of the phase of a signal however, the difference in phases at the inputs to the PFD were plotted, as opposed to the individual phases themselves. This entails plotting the input phase error ($\phi_e$), defined

[8] Actual $\Delta K$ would be even larger than 112% as, reducing $\Delta K_{VCO_{btb}}$ also slightly reduces $\Delta K_{VCO_{inb}}$.
[9] The recently reported technique in [88] shows some potential at reducing $\Delta K_{VCO_{inb}}$.

for the purposes of this simulation as:

$$\phi_e = \phi_{ref} - \phi_{fb} \tag{6.4}$$

In addition, due to the discrete nature of the CP outputs (see Table 2.1), the respective widths of the CP output pulses are plotted as opposed to their individual discrete values. Finally, since the function of a PLL is to lock onto both the phase and frequency of an input reference signal, the input reference ($f_{ref}$) and feedback ($f_{VCO}/N$) frequencies are also plotted.

For the simulation, the input reference frequency ($f_{ref}$) was set to 30.12MHz using a pulsed voltage source.[10] The VCO frequency ($f_{VCO}$) was then set to $\approx$ 4.83GHz such that, when divided down by the integer feedback ratio ($N$) of 160 (see section 6.1.6), a feedback frequency ($f_{VCO}/N$) of 30.18MHz resulted. In other words, at time $t_1 \approx 0$s for the simulation, $f_{VCO}/N$ was greater than $f_{ref}$ by 60kHz, resulting in an input phase error ($\phi_e$) of magnitude 220ps. It should be noted that the seemingly small initial frequency offset ($f_e = f_{VCO}/N - f_{ref}$) of 60kHz ($<< \Delta\omega_p$) was chosen to reduce simulation time. For PLL system level simulations, the combination of high frequency VCO signals with low frequency loop bandwidths typically result in long simulation times. Therefore as is commonly done, the PLL was initially set up close to lock to reduce pull in times such that the overall functionality of the loop could be verified in a reasonable simulation time frame. This, coupled with the relatively large loop bandwidth ($K$) of 1MHz (see Table 6.1), resulted in a simulation time for the plot of Fig. 6.10 of $\approx$ 2 days.

Following from sections 2.2.2 and 2.3, when out of lock, the PFD can be viewed as a frequency detector, changing its behaviour more and more to that of a phase detector as the reference and feedback frequencies approach each other. Therefore, since a frequency offset ($f_e$) of 60kHz occurs at time $t_1$, the PFD initially behaves as a frequency detector seeking to reduce $f_{VCO}/N$ such that it equals $f_{ref}$. As per Fig. 5.7, this is achieved by proportionally decreasing the differential tuning voltage ($V_d$), which from (4.33) is achievable by proportionally increasing $V_{ctrl}^-$ (achieved by increasing $CP^-$) and proportionally decreasing $V_{ctrl}^+$ (achieved by decreasing $CP^+$). This behaviour can be seen in Fig. 6.10 where, at $t_2 = 0.2\mu$s, $V_{ctrl}^-$ has increased to 0.55V (achieved by increasing $CP^-$ to 1.29ns) and $V_{ctrl}^+$ has decreased to 0.46V (achieved by decreasing $CP^+$ to 1ns[11]). As a result, by virtue of (4.33) $V_d$ now becomes -0.09V to reduce $f_{VCO}$ slightly such that $f_{ref} = f_{VCO}/N$.

However, this reduction in $f_{VCO}/N$ resulted in an increase in $\phi_e$, which from Fig. 6.10

[10] In practice $f_{ref}$ is derived from an external crystal oscillator. However, for simulation purposes a pulsed voltage source can be used without any loss in generality.

[11] The minimum CP output pulse width is determined by the PFD propagation time ($t_{pfd}$). As this was synthesised at 1ns (see section 6.1.2), the minimum CP output pulse width thus remains exactly constant at 1ns throughout the entire simulation.

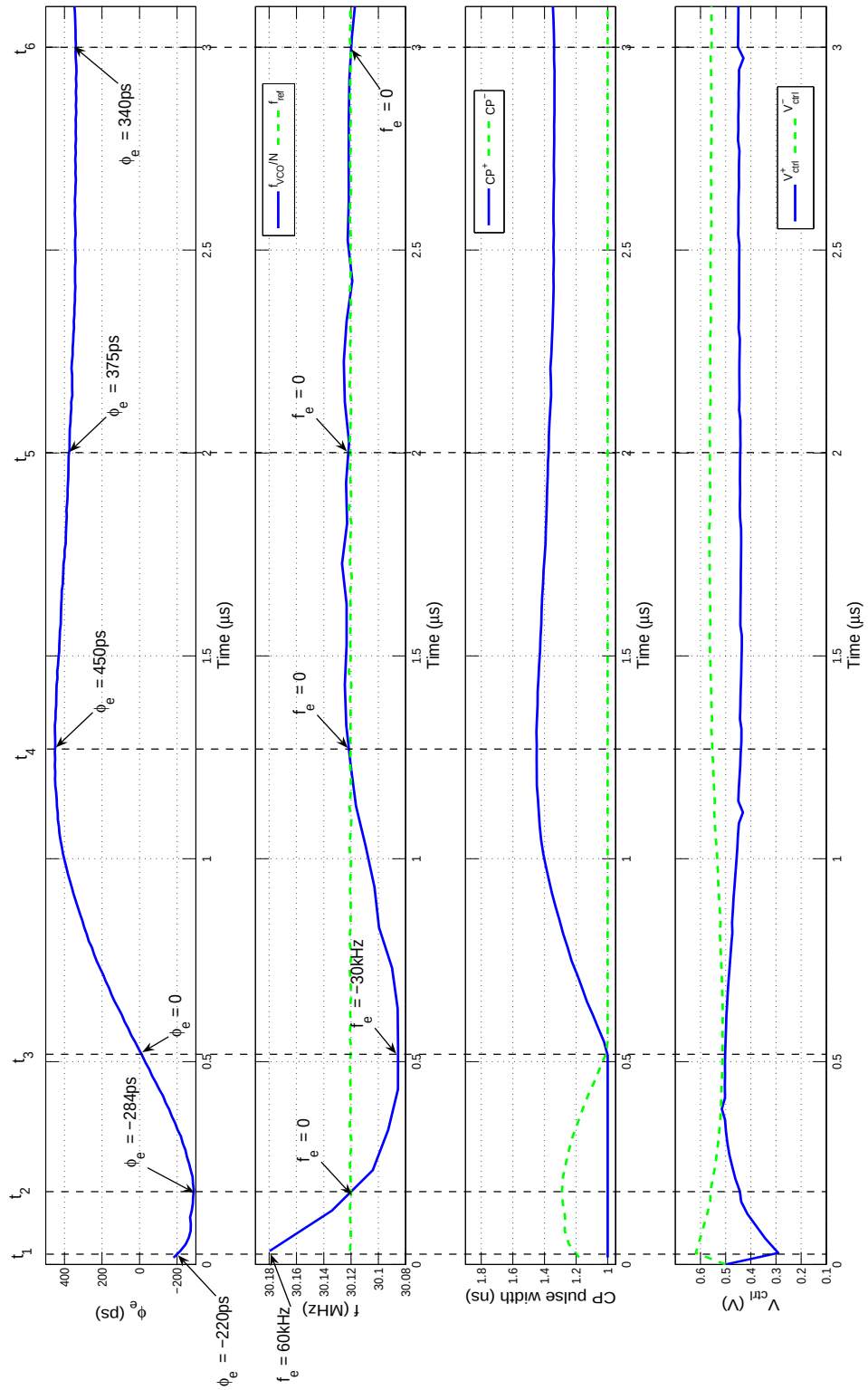



**Fig. 6.10:** Locking simulation of the fully differential PLL

can be seen to have increased in magnitude to 284ps at time $t_2$. Specifically, $\phi_e$ = -284ps, which from (6.4) implies $\phi_{ref}$ lags $\phi_{fb}$ by 284ps. At this point the PFD (behaving now as a phase detector) seeks to reduce this error, which from Table 4.8 is achievable by decreasing $V_{ctrl}^-$ (achieved by decreasing $CP^-$) and increasing $V_{ctrl}^+$ (achieved by increasing $CP^+$). This behaviour can be seen in Fig. 6.10 where, at time $t_3 = 0.53\mu$s, $V_{ctrl}^-$ has decreased to 0.51V (achieved by decreasing $CP^-$ to $\approx$ 1ns) and $V_{ctrl}^+$ has increased to 0.5V (interestingly $CP^+$ shows no change[12]) to yield $\phi_e = 0$.

However, this reduction in $\phi_e$ has resulted in a slight decrease in $f_{VCO}/N$, which from Fig. 6.10 can be seen to have decreased to 30.09MHz at time $t_3$, hence introducing a frequency offset ($f_e$) of -30kHz. To reduce this offset, the PFD reverts to behaving as a frequency detector by decreasing and increasing $CP^-$ and $CP^+$ respectively such that $f_{VCO}/N$ is proportionally increased. This behaviour can be seen in Fig. 6.10 where, at $t_4 = 1.3\mu$s, $CP^-$ has remained at its minimum value (1ns) with $CP^+$ increasing to 1.45ns to yield $f_{ref} = f_{VCO}/N$.

The resulting static phase error from this action can be seen to be +450ps, implying from (6.4) that $\phi_{ref}$ leads $\phi_{fb}$ by this amount. Once again the PFD reverts to behaving as a phase detector where, as per Table 4.8, it increases $V_{ctrl}^-$ and decreases $V_{ctrl}^+$ to reduce this phase error. At time $t_5 = 2\mu$s, $V_{ctrl}^-$ and $V_{ctrl}^+$ can be seen to be 0.56V and 0.44V respectively with $\phi_e$ = 375ps. Waiting a further 1$\mu$s (i.e. $t_6 = 3\mu$s) shows $\phi_e$ to have changed little with it now equal to 340ps. Given that $f_e$ has remained at zero, with $V_{ctrl}^-$ and $V_{ctrl}^+$ hardly changing in the time period from $t_4 \rightarrow t_5$, we can thus deduce the fully differential PLL at this point to have obtained lock, where $\phi_e$ = 340ps represents the static phase error ($\phi_v$). As per section 2.3.1, this will prevent the PLL ever achieving $\phi_e = 0$ hence resulting in reference spurs in the PLL output frequency spectrum.[13]

The behaviour of the fully differential PLL at each of the time points described above is neatly summarised in Table 6.18 with respect to $\phi_e$ and $f_e$.

| Time point | $t_1$ | $t_2$ | $t_3$ | $t_4$ | $t_5$ | $t_6$ |
|---|---|---|---|---|---|---|
| $\phi_e$ (ps) | -220 | -284 | 0 | +450 | +375 | +340 |
| $f_e$ (kHz) | 60 | 0 | 30 | 0 | 0 | 0 |

**Table 6.18:** Summarised locking behaviour of the fully differential PLL

Table 6.18 shows the PLL to engage in a sort of "cat and mouse" procedure regarding the reduction of $\phi_e$ and $f_e$, causing the PFD to alternate its behaviour between that of

[12]It is impossible for changes in $V_{ctrl}$ to occur without corresponding changes in the CP outputs. This therefore implies an anomaly in the ADMS mixed mode simulator used to perform the simulation.

[13]The reference spurs for the fully differential PLL could not be analysed as such spurs are only observable using a spectrum analyser placed at the output of a fabricated PLL. Since the fully differential PLL was not realised in silicon, such analysis is not possible.

a phase detector and frequency detector (as described above). In addition to this, Table 6.18 also shows the PLL to finally obtain lock once $f_e \approx 0$ and $\phi_e$ has been reduced to its minimum value, which as shown is limited by the occurring static phase error.

The most important observation to make from the analysis of this section is that the loop did lock onto the input reference signal. In addition to this, once it locked onto the signal, which can be seen to have occurred at $\approx 2.5\mu$s in Fig. 6.10, the PLL can be seen to maintain lock (i.e. $f_e$ remains at 0) thereby verifying its tracking capability once locked. All this was shown very rigorously in Fig. 6.10. However as a summarising view of the locking and tracking capabilities of the fully differential PLL, Fig. 6.11 plots only the input reference ($f_{ref}$) and feedback ($f_{VCO}/N$) frequencies (extracted from Fig. 6.10) against simulation time.

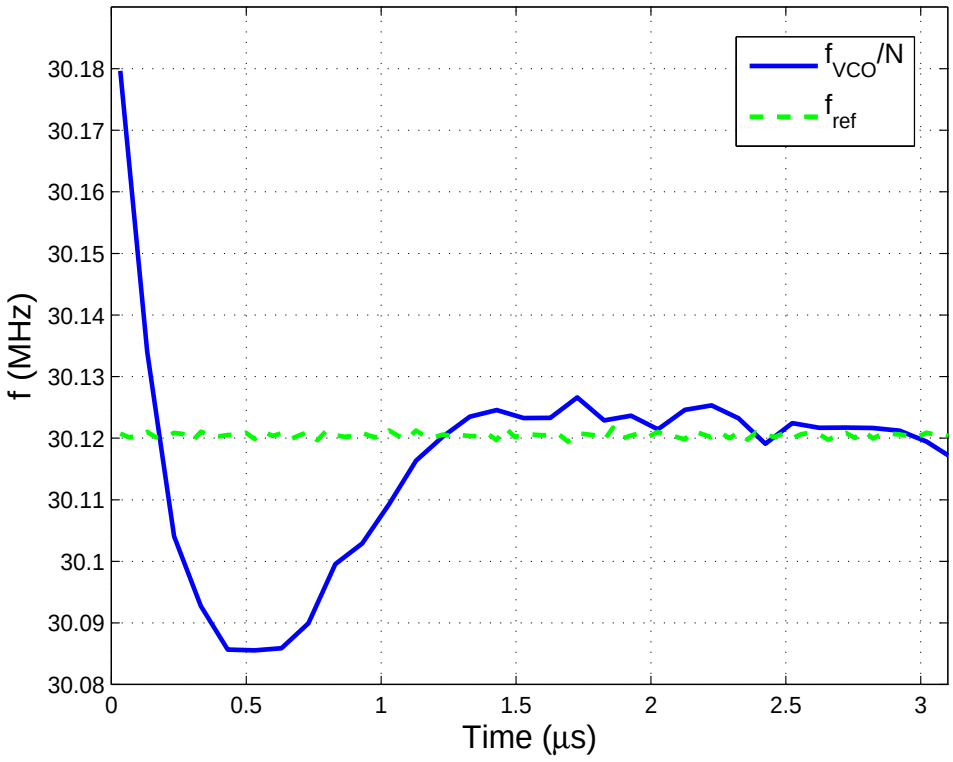



**Fig. 6.11:** $f_{VCO}/N$ locking onto $f_{ref}$

## 6.7 Summary and Achievements of this Chapter

This chapter was written with one goal in mind - to detail the achievements and performance of the fully differential PLL and verify its overall functionality. In doing so this chapter effectively documents the performance of the fully differential PLL which was designed for this thesis, in a manner similar to that of a datasheet such as [22] or [21].

Specifications for the PLL were supplied in section 6.1 which defined a high performance PLL applicable to the highly popular 2.4GHz - 2.5GHz ISM bands, particularly focusing on Bluetooth applications.

Following from this, the fully differential was broken down block by block with each of the analog blocks (i.e. the CP, LF and VCO) being thoroughly detailed and their performance assessed with reference to relevant criteria. Through this, the various advantages to be gained with employing a fully differential PLL (discussed and shown in chapters 4 and 5) were verified. For the differential CP these were verified in section 6.2 to be:

- Dramatic reduction of common-mode noise.
- Dramatic reduction in mismatch current.
- Doubled output voltage swing.

For the differentially transformed LF these were verified in section 6.3 to be:

- Reduction in silicon area requirements by approximately a factor of two.

For the differentially tuned VCO these were verified in section 6.4 to be:

- Eliminates the need for a differential amplifier between the differential LF and VCO.

Section 6.4 also showed the advantages to be gained from a applying the proposed sub-banded VCO architecture. Specifically these were:

- Achieve a wide output frequency range with low $K_{VCO}$ requirements.
- Dramatic reduction in band-to-band $K_{VCO}$ variation over a conventional sub-banded VCO.

Overall, this enabled the resulting PLL cover the highly popular 2.4GHz - 2.5GHz ISM bands with low phase noise performance (exceeding Bluetooth phase noise specifications by 6dB), whilst offering reductions in loop bandwidth variation by a factor of $\approx 2$ in comparison with a PLL using a VCO employing a conventional switched capacitor array (SCA). The functionality of the resulting PLL was then verified in section 6.6.

Most importantly, this chapter verified the two primary contributions of this thesis. These are as follows:

1. Fully differential PLLs were shown to achieve low noise operation without heavily relying on additional power, whilst consuming less silicon area over conventional PLLs and proving themselves suitable for operation in low technology nodes with reduced voltage supplies.

2. The use of the proposed switched varactor array (SVA) over a conventional switched capacitor array (SCA) was shown to achieve a reduction in loop bandwidth variation by a factor of $\approx 2$ without the requirement for additional power, in addition to offering a 1dB improvement in phase noise performance.

Upon completing this chapter, the reader should be convinced that the fully differential PLL of this thesis verifies all the concepts presented in preceding chapters, which it brings together to realise a functional phase-locked loop. Therefore to conclude the chapter, Table 6.19 summarises the fully differential PLL and its performance.

| | |
|---|---|
| Process | UMCs 1P90M 90nm bulk CMOS |
| Vdd | 1 V |
| PLL architecture | CP-PLL |
| PLL Type | Type 2 |
| PLL Order | Third-order |
| $f_{ref}$ | 30MHz |
| $f_{out_{max}}$ | 5.2GHz [a] |
| $f_{out_{min}}$ | 4.4GHz [a] |
| $f_{out_{mid}}$ | 4.8GHz [a] |
| PM | 50° |
| $t_s$ | $\approx 60\mu$s [b] |
| $\Delta K$ | 61.3% |
| Power consumption | 1.02mW [c] |
| Noise | -125dBc/Hz @ 3MHz offset [d] |
| Area | $\approx 0.09$mm$^2$ |

[a] Divide by two to cover the highly popular 2.4GHz - 2.5GHz ISM bands.

[b] Based on the lock time from Fig. 6.10 and the worst case calibration time from section 6.4.3.

[c] With reference only to the analog blocks (CP, LF and VCO).

[d] Taken from VCO noise simulations.

**Table 6.19:** Performance and summary of the fully differential PLL

A complete block diagram of the PLL is presented in Fig. 6.12. Similiar to Fig. 4.42, this gives a block level view of the differential CP and differentially tuned VCO (underlying schematics are referenced inside the blocks) whilst presenting a component level view of the transformed differential LF. The VCO can be seen to employ a switched varactor array (SVA) which, as discussed in section 5.3.3, requires a differential amplifier to convert the

differential LF outputs to single-ended form for control of each branch in the array. As discussed in section 5.2.1, the correct branch of the array must be digitally selected thereby creating the need for a calibration loop, shown at block level in Fig. 6.12. The operation of such a loop was described in section 6.4.3 where it was stated to be used only when locating the correct branch of the SVA. This therefore necessitates the inclusion of a lock detect circuit [15] (shown at block level in Fig. 6.12), whose function is to switch the loop in when locating the correct branch, switching it out once the correct branch has been located. In addition to this, similar to Fig. 4.42, a feedback divider (/N) and PFD are included at block level as these were synthesised using VHDL in the final design, where a buffer is placed at the VCO outputs to make it independent on loading conditions, in addition to enabling the PLL output signal be used elsewhere on the IC or off-chip.

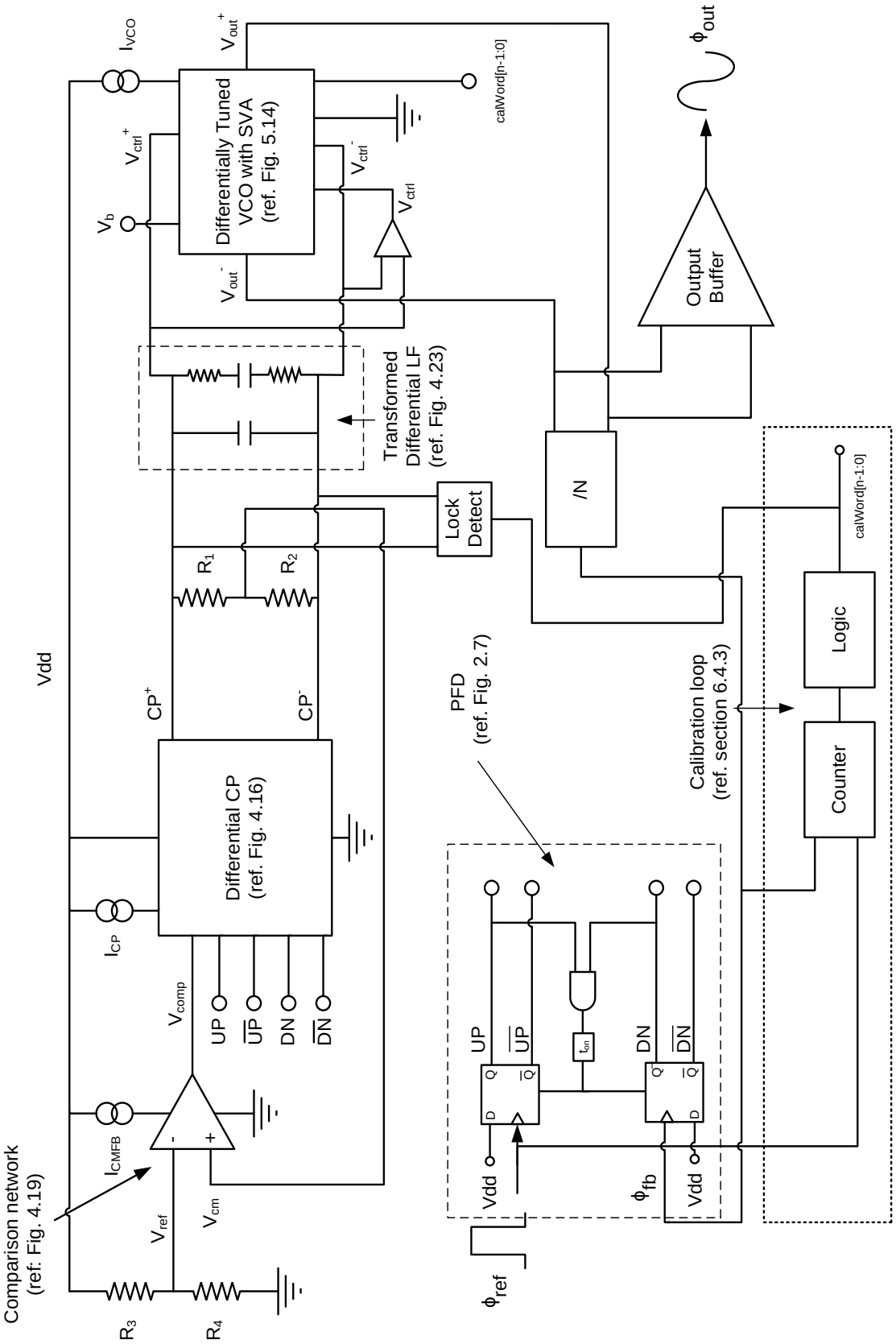



**Fig. 6.12:** Block diagram for the fully differential PLL with reduced loop bandwidth variation

# CHAPTER 7

# Conclusion and Future Work

## 7.1 Concluding Remarks

The frequency synthesizer (within a wireless transceiver) is the cornerstone of wireless technology. As stated in chapter 1, the typical implementation for a frequency synthesizer is with a PLL - the core focus of this thesis. Although an excellent implementation for a synthesizer, PLLs do however exhibit various weaknesses, some of which were identified in the fundamental discussions of chapters 2 and 3. Specifically, the weaknesses of the PLL in relation to wireless technology were addressed in this thesis which showed/achieved the following:

1. This thesis detailed conclusively the advantages to be gained from employing a fully differential PLL. Going through each of the differential blocks in a fully differential PLL, these are the following:

   (a) *Differential CP* (section 4.3):

   - Doubled output voltage swing over a single-ended CP. This makes differential CPs well suited to low noise operation, wideband operation and lower technology nodes with reduced voltage supplies.
   - Provides the capability to dramatically reduce common-mode noise. This makes differential CPs well suited for use in complex SOCs where such noise can be prevalent.
   - Achieves significant reductions in mismatch current over single-ended CPs. Measured reductions were shown to be by three orders of magnitude over single-ended CPs. This leads to significant reductions in static phase offset

and hence reference spurs which can severely degrade the spectral purity of the output frequency spectrum.

(b) *Differential LF* (section 4.4):

- Reduced silicon area requirements by a factor of $\approx 2$ over single-ended LFs. This makes differential LFs more feasible to on-chip implementation leading to various advantages, most notably reductions in project time and cost.

(c) *Differentially tuned VCO* (section 4.5):

- Eliminates the need for a differential to single-ended amplifier at the differential LF outputs, leading to savings in noise and power, in addition to reductions in project time and cost.

2. This thesis also proposed a sub-banded VCO architecture which achieves significant reductions in loop bandwidth variation. This was achieved using the proposed architecture of chapter 5 which, in addition to satisfying simultaneous requirements for large tuning ranges and low phase noise, achieved significant reductions in $K_{VCO}$ band-to-band variation. The specific advantages to be gained from the proposed architecture over a conventional sub-banded architecture are as follows:

- Reductions in loop bandwidth variation by a factor of $\approx 2$. This makes the resulting PLL more stable, improves its noise performance in addition to maintaining acquisition ranges and times close to their specified values.
- No additional increase in power consumption. The proposed architecture thus remains attractive to low power wireless applications.
- Reductions in phase noise by 2dB. The proposed architecture thus becomes more attractive to low noise operation.

Collectively, all these efforts make the resulting, fully differential PLL with reduced loop bandwidth variation, well suited for implementation as the frequency synthesizer within wireless transceivers embedded on complex SOCs, fabricated in low technology nodes. As such transceivers will become more and more commonplace with the increase in functionality of our everyday wireless devices, the resulting PLL effectively addresses many forthcoming issues which may be encountered in next generation wireless products. As such, it becomes a suitable candidate for the frequency synthesizer of choice in tomorrow's wireless world.

## 7.2 Future Work

Although much was achieved in this thesis, more can be achieved with the following possibilities for future work.

1. *Differential LF*: The differential LF was shown in section 4.4.3 to achieve reductions in silicon area requirements by a factor of $\approx 2$ over a single-ended LF. Nevertheless, from Table 6.19 it can be still seen to dominate overall area requirements for the PLL. Further reductions in LF area could therefore be possibly achieved by investigating the dual path method, reported in [87], with respect to differential LFs.

2. *Varactor non-linearity*: Varactor non-linearity was discussed in section 3.4.3 where section 5.1 showed it to result in a form of $K_{VCO}$ variation, known as in-band variation ($\Delta K_{VCO_{inb}}$). Given that $K_{VCO}$ band-to-band variation was significantly reduced with the proposed VCO architecture of chapter 5, $\Delta K_{VCO_{inb}}$ becomes the prevalent source of loop bandwidth variation, with Table 6.17 showing it to account for $\approx 50\%$ of the total variation. As such, the reduction of $\Delta K_{VCO_{inb}}$, achievable by reducing varactor non-linearity, is an obvious choice for future work. An additional benefit from such work would be an improvement in CMRRs for differentially tuned VCOs which, as stated in section 4.5.4, can be as much as $\approx$ 50dB less than those achievable with their differential to single ended amplifier alternatives. The reason for these relatively low CMRRs ($\approx$ 30dB) is due to asymmetries between the non-linear curves of the anti-parallel varactor configurations. Linearising these curves would almost certainly improve their corresponding symmetries, leading to direct improvements in CMRRs.

   The recently reported technique in [88] shows some promise at reducing varactor non-linearity, albeit at the cost of increased power consumption and reduced tuning range. This therefore should be investigated, with respect to differentially tuned VCOs, to assess the possible reductions in loop bandwidth variation and increases in CMRR.

3. *Differentially tuned switched varactor array*: Section 5.5.1 detailed the issues with achieving a differentially tuned switched varactor array, with section 5.5.2 discussing the failed attempts to overcome such issues. As discussed in section 5.3.3, the failure to realise a differentially tuned switched varactor array necessitates the inclusion of a differential amplifier to convert the differential LF outputs to single-ended form for control of each branch in the array. Converting the branches to differential control would eliminate the need for such an amplifier leading to various savings in addition to realising the full differential potential of the switched varactor array (SVA). As

such, an important progression on the SVA would be this conversion to differential control.

4. *On-chip inductor*: Improvements in on-chip inductors is an active area of research and is included here for completion on possible improvements to PLLs in general. In a nutshell, on-chip inductors are too big and too lossy. Nevertheless, they are required to avoid any discrete components in realising a fully monolithic VCO. In the early days of IC development, on-chip inductors with practical inductance values were simply too large to be used. In fact it wasn't until the early 1990's [40], [41] that improvements in lithography made possible the fabrication of practical on-chip inductors. Further advances in fabrication technology (namely interconnect material and chemical mechanical polishing - CMP) then brought initial quality factors from $\approx 5$ up to $\approx 15$, with this working reporting a very high quality factor of 19.4. Nevertheless, the inductor still dominates the overall area requirements of a VCO (Table 6.16 shows it to account for $\approx 80\%$ of the total VCO area), with its various loss mechanisms discussed in section 3.5 resulting in large power requirements to sustain oscillation in a VCO.

   Although the area and loss of an on-chip inductor does reduce with decreasing technology nodes, it still remains a bottleneck (particularly in relation to power consumption) for PLL design. As such, active research relating to the optimisation of on-chip inductors should be continued so as to make them more consistent with current trends in wireless technology.

## 7.3 Summary of this Chapter

This chapter concludes the entire thesis where it summarises the achievements/contributions of the thesis in addition to outlining future relevant work pertaining to PLL research.

# APPENDIX A

## A.1 Derivation of the Transfer Function for a PFD-CP

The on time for the CP switches ($t_{sw}$) over one period of the input reference signal is:

$$t_{sw} = \frac{\phi_e}{\omega_{ref}} \tag{A.1}$$

where the input phase error (rads) and frequency of the reference signal (rads/s) are represented by $\phi_e$ and $\omega_{ref}$ respectively. Since $\omega_{ref} = 2\pi f_{ref}$, where $f_{ref} = 1/T_{ref}$, $\omega_{ref}$ can be redefined as $\omega_{ref} = (2\pi)/T_{ref}$. Following from this, (A.1) can be redefined as:

$$t_{sw} = \frac{\phi_e T_{ref}}{2\pi} \tag{A.2}$$

When the CP switches are on, the CP output current ($I_{out}$) is:

$$I_{out} = I_{cp} t_{sw} \tag{A.3}$$

where $I_{cp}$ represents the CP source or sink current. Inserting (A.2) into (A.3) yields:

$$I_{out} = I_{cp} \frac{\phi_e T_{ref}}{2\pi} \tag{A.4}$$

Assuming the input signals are periodic where $K < 10\omega_{ref}$, (A.4) represents an averaged output over many cycles of the input reference signal (i.e. a time invariant output). Assuming the PLL is close to lock with $-2\pi < \phi_e > 2\pi$, the PFD-CP can be treated as a linear block whose overall transfer function becomes:

$$H_{PFD-CP}(s) = \frac{I_{cp}}{2\pi} \tag{A.5}$$

## A.2 Derivation of the Transfer Function for a VCO

In order to obtain its transfer function, it is necessary to express the VCO in terms of its output phase. Recalling that the output of a VCO (in the frequency domain) is:

$$\omega_{vco}(t) = \omega_a + K_{VCO}\ V_{ctrl}(t) \tag{A.6}$$

and the general definition for the phase of a signal ($\phi(t)$) is:

$$\phi(t) = \int \omega(t) + \phi_0 \tag{A.7}$$

the output phase of a VCO can be defined as:

$$\phi_{VCO}(t) = \int (\omega_a + K_{VCO}\ V_{ctrl}(t))dt + \phi_0 \tag{A.8}$$

Given that $\phi_0$ represents the initial output phase of the VCO, it is of little interest and so can be left out to yield:

$$\phi_{VCO}(t) = \int (\omega_a + K_{VCO}\ V_{ctrl}(t))dt \tag{A.9}$$

Assuming $K_{VCO}$ to be linear, it can be brought outside the integral to yield:

$$\phi_{VCO}(t) = K_{VCO} \int (\omega_a + V_{ctrl}(t))dt \tag{A.10}$$

Taking the Laplace Transform of both sides yields:

$$\Phi_{VCO}(s) = K_{VCO}\frac{V_{ctrl}(s)}{s} \tag{A.11}$$

Following from (A.11), the transfer function for a VCO becomes:

$$H_{VCO}(s) = \frac{K_{VCO}}{s} \tag{A.12}$$

## A.3 Derivation of the Open-Loop Transfer Function for a PLL

Assume the LTI model of a PLL is cut at point $x$, as indicated in Fig. A.1. This makes the PLL "open-loop", whose transfer function follows as:

$$H_{ol}(s) = H_{PFD-CP}(s)\ H_{LF}(s)\ H_{VCO}(s)\ H_{FB}(s) \tag{A.13}$$

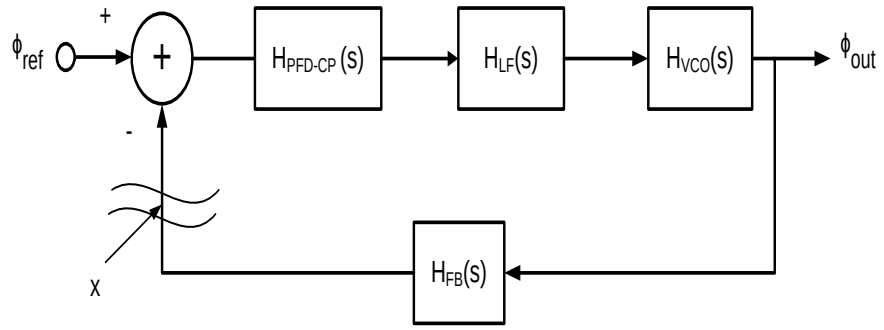



**Fig. A.1:** LTI model of a PLL

## A.4 Derivation of the Closed-Loop Transfer Function for a PLL

The generic model for a negative feedback system is shown in Fig. A.2.

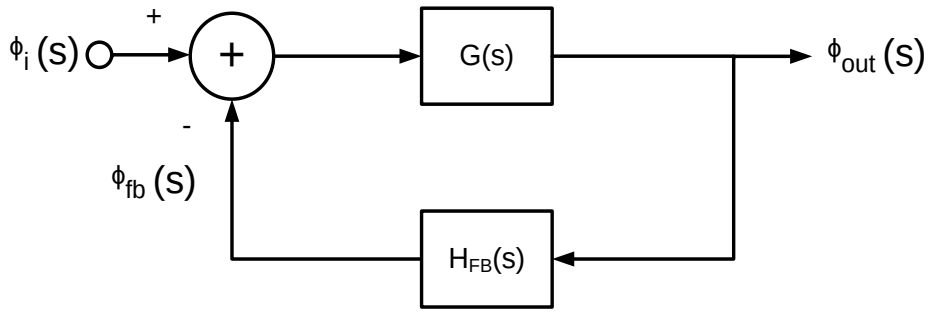



**Fig. A.2:** Generic model of a negative feedback system

where the input, output and feedback signals are represented as $\phi_i(s)$, $\phi_{out}(s)$ and $\phi_{fb}(s)$ respectively, with the transfer functions of the feedback network and the forward path being represented as $H_{FB}(s)$ and G(s) respectively.

Following from Fig. A.2, the output signal ($\phi_{out}(s)$) can be represented as:

$$\phi_{out}(s) = (\phi_i(s) - \phi_{fb}(s))G(s) \tag{A.14}$$

From Fig. A.2, the feedback signal can be redefined as:

$$\phi_{fb}(s) = \phi_{out}(s)H_{FB}(s) \tag{A.15}$$

Inserting (A.15) into (A.14) yields:

$$\begin{aligned}\phi_{out}(s) &= (\phi_i(s) - \phi_{out}(s)H_{FB}(s))G(s) \\ &= \phi_i(s)G(s) - \phi_{out}(s)H_{FB}(s)G(s)\end{aligned} \tag{A.16}$$

Re-arranging (A.16) yields:

$$\begin{aligned}\phi_{out}(s) + \phi_{out}(s)H_{FB}(s)G(s) &= \phi_i(s)G(s) \\ \phi_{out}(s)(1 + H_{FB}(s)G(s)) &= \phi_i(s)G(s)\end{aligned} \tag{A.17}$$

Following from (A.17), the general closed-loop transfer function for a negative feedback system becomes:

$$H_{cl}(s) = \frac{G(s)}{1 + H_{FB}(s)G(s)} \tag{A.18}$$

which from Appendix A.3 can be restated as:

$$H_{cl}(s) = \frac{G(s)}{1 + H_{ol}(s)} \tag{A.19}$$

## A.5 Derivation of the Transfer Function for a Second-Order, Passive Lag-Lead LF

Two equivalent impedance representations of a second-order, passive lag-lead LF are shown in Figs. A.3 and A.4.

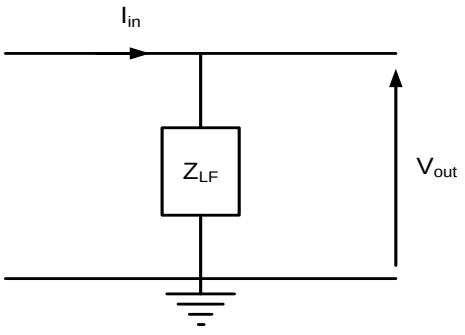



**Fig. A.3:** LF equivalent impedance

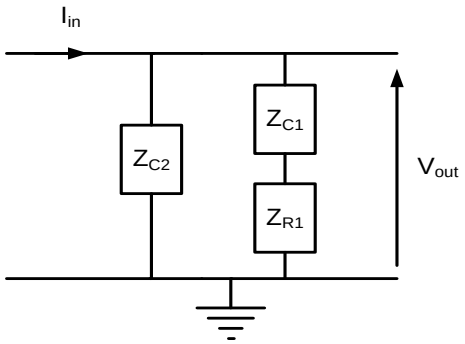



**Fig. A.4:** LF impedance components

Viewing Fig. A.3, $V_{out}$ can be expressed as:

$$V_{out} = I_{in} Z_{LF} \tag{A.20}$$

thereby proving the LF to be a linear system, thus enabling the function ($H_{LF}(z)$) to be defined as follows:

$$H_{LF}(z) = Z_{LF} = \frac{V_{out}}{I_{in}} \tag{A.21}$$

Viewing Fig. A.4, $Z_{LF}$ can be expressed as follows:

$$Z_{LF} = (Z_{R_1} + Z_{C_1})||Z_{C_2} \tag{A.22}$$

$$= \frac{(Z_{R_1} Z_{C_2}) + (Z_{C_1} Z_{C_2})}{Z_{R_1} + Z_{C_1} + Z_{C_2}} \tag{A.23}$$

where $Z_{R_1} = R_1$, $Z_{C_1} = 1/(j\omega C_1)$ and $Z_{C_2} = 1/(j\omega C_2)$. Inserting (A.23) into (A.21), and replacing each of the impedance components with their corresponding frequency equivalent expressions yields:

$$H_{LF}(j\omega) = \frac{(R_1/j\omega C_2) + ((1/(j\omega C_1))\ (1/(j\omega C_2)))}{R_1 + (1/(j\omega C_1)) + (1/(j\omega C_2))} \tag{A.24}$$

Converting (A.24) to the s-domain (where s = $j\omega$ for an undampened sinusoid) thus yields the transfer function:

$$H_{LF}(s) = \frac{(R_1/sC_2) + ((1/(sC_1))\ (1/(sC_2)))}{R_1 + (1/(sC_1)) + (1/(sC_2))} \tag{A.25}$$

which after some simplifying algebra reduces to:

$$H_{LF}(s) = \frac{(C_1 R_1)s + 1}{(C_2 C_1 R_1)s^2 + (C_1 + C_2)s} \tag{A.26}$$

## A.6 Derivation of the Loop Bandwidth for a Second-Order, Type 2 PLL with Passive Lag-Lead LF

The general transfer function for the above described PLL was defined in (2.36) which, when divided through by its dc gain $H(0)$ yields:

$$H(s)/H(0) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{A.27}$$

Assuming $\omega = \sqrt{2}\omega_n$, then:

$$s = j\omega = j\sqrt{2}\omega_n \tag{A.28}$$

Inserting (A.28) into (A.27) and performing some additional algebra thus yields:

$$H(j\sqrt{2}\omega_n)/H(0) = \frac{\omega_n^2 + j(2\sqrt{2}\omega_n^2\zeta)}{-\omega_n^2 + j(2\sqrt{2}\omega_n^2\zeta)} \tag{A.29}$$

Dividing the numerator and denominator of (A.29) by $\omega_n^2$ then yields:

$$H(j\sqrt{2}\omega_n)/H(0) = \frac{1 + j(2\sqrt{2}\zeta)}{-1 + j(2\sqrt{2}\zeta)} \tag{A.30}$$

The magnitude of (A.30) in dB is:

$$\begin{aligned} 20 \cdot \log(|H(j\sqrt{2}\omega_n)/H(0)|) &= 20 \cdot \log\left(\frac{\sqrt{1^2 + (j(2\sqrt{2}\zeta))^2}}{\sqrt{(-1)^2 + (j(2\sqrt{2}\zeta))^2}}\right) \\ &= 20 \cdot \log(1) \\ &= 0dB \end{aligned} \tag{A.31}$$

thereby proving that when $\omega = \sqrt{2}\omega_n$, $20 \cdot \log(|H(s)/H(0)|) = 0$dB. Following from this we can state:

$$\omega_x = \sqrt{2}\ \omega_n = K \tag{A.32}$$

## A.7 Dependance of $C_1/C_2$ on $PM$

Reworking (2.28), the capacitor $C_1$ of a LF can be expressed as:

$$C_1 = \frac{1}{R_1\omega_{z_1}} \tag{A.33}$$

Recalling (2.33) and noting that $\omega_x = K$, (A.33) can be expressed as:

$$C_1 = \frac{k}{R_1 K} \tag{A.34}$$

Reworking (2.30), the capacitor $C_2$ of a LF can be expressed as:

$$C_2 = \frac{C_1}{C_1 R_1 \omega_{p_2} - 1} \tag{A.35}$$

Inserting (A.34) into (A.35) thus yields:

$$C_2 = \frac{\frac{k}{R_1 K}}{\frac{k\omega_{p_2}}{K} - 1} \tag{A.36}$$

Recalling (2.32) and noting that $\omega_x = K$, (A.36) can be expressed as:

$$C_2 = \frac{k}{K R_1 (k^2 - 1)} \tag{A.37}$$

Putting (A.34) over (A.37) and simplifying yields:

$$\frac{C_1}{C_2} = k^2 - 1 \tag{A.38}$$

Inserting (2.34) into (A.38) and simplifying then yields:

$$\frac{C_1}{C_2} = \frac{2sin(PM)}{1 - sin(PM)} \tag{A.39}$$

for $PM < 90°$.

## A.8 Derivation of the Transfer Function for an Ideal LC-Tank

Two equivalent impedance representations of an ideal LC-Tank are shown in Figs. A.5 and A.6.

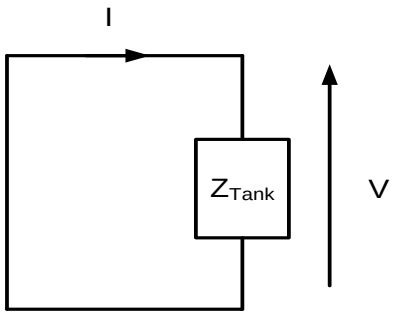



**Fig. A.5:** LC-tank equivalent impedance

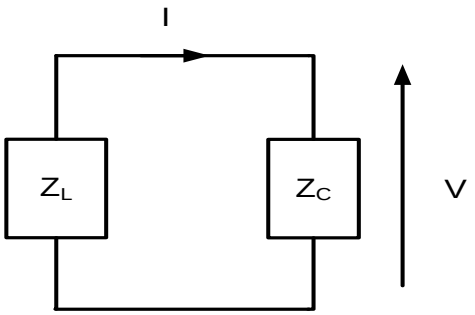



**Fig. A.6:** LC-tank impedance components

Viewing Fig. A.5, $V$ can be expressed as:

$$V = I Z_{Tank} \tag{A.40}$$

thereby enabling the function ($H(z)$) to be defined as follows:

$$H(z) = Z_{Tank} = \frac{V}{I} \tag{A.41}$$

Viewing Fig. A.6, $Z_{Tank}$ can be expressed as follows:

$$Z_{Tank} = Z_L || Z_C \tag{A.42}$$

$$= \frac{Z_L Z_C}{Z_L + Z_C} \tag{A.43}$$

where $Z_L = (j\omega L)$ and $Z_C = 1/(j\omega C)$. Inserting (A.43) into (A.41), and replacing each of the impedance components with their corresponding frequency equivalent expressions yields:

$$H(j\omega) = \frac{(j\omega L)(1/(j\omega C))}{(j\omega L) + (1/(j\omega C)} \tag{A.44}$$

Converting (A.44) to the s-domain (where s = $j\omega$ for an undampened sinusoid) thus yields the transfer function:

$$H(s) = \frac{(sL)(1/(sC))}{(sL) + (1/(sC)} \tag{A.45}$$

which after some simplifying algebra reduces to:

$$H(s) = \frac{Ls}{LCs^2 + 1} \tag{A.46}$$

## A.9 Derivation of the Transfer Function for an LC-Tank

Two equivalent impedance representations of an LC-Tank are shown in Figs. A.7 and A.8.

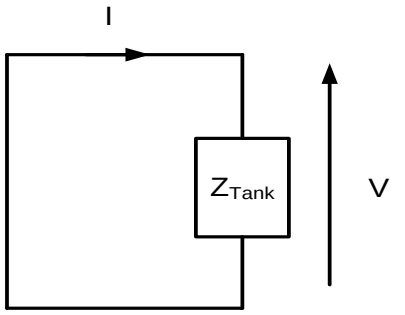



**Fig. A.7:** LC-tank equivalent impedance

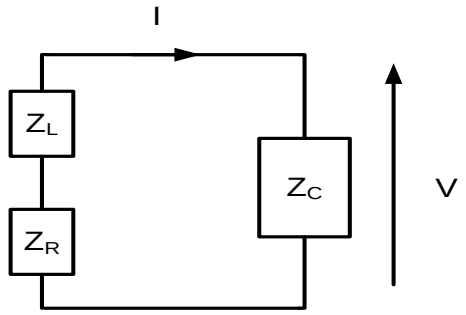



**Fig. A.8:** LC-tank impedance components

Viewing Fig. A.7, $V$ can be expressed as:

$$V = IZ_{Tank} \tag{A.47}$$

thereby enabling the function ($H(z)$) to be defined as follows:

$$H(z) = Z_{Tank} = \frac{V}{I} \tag{A.48}$$

Viewing Fig. A.8, $Z_{Tank}$ can be expressed as follows:

$$Z_{Tank} = (Z_L + Z_R)||Z_C \tag{A.49}$$

$$= \frac{(Z_L + Z_R)Z_C}{Z_L + Z_R + Z_C} \tag{A.50}$$

where $Z_L = (j\omega L)$, $Z_C = 1/(j\omega C)$ and $Z_R = R$. Inserting (A.50) into (A.48), and replacing each of the impedance components with their corresponding frequency equivalent expressions yields:

$$H(j\omega) = \frac{((j\omega L) + R)(1/(j\omega C))}{(j\omega L) + R + (1/(j\omega C))} \tag{A.51}$$

Converting (A.51) to the s-domain (where s = $j\omega$ for an undampened sinusoid) thus yields the transfer function:

$$H(s) = \frac{((sL) + R)(1/(sC))}{(sL) + R + (1/(sC))} \tag{A.52}$$

which after some simplifying algebra reduces to:

$$H(s) = \frac{Ls + R_s}{LCs^2 + +sR_sC + 1} \tag{A.53}$$

## A.10 Derivation of the Transfer Function for the Parallel Representation of an LC-Tank

The equivalent impedance representation of an LC-Tank is shown in Fig. A.9 with it parallel equivalent impedance shown in Fig. A.10.

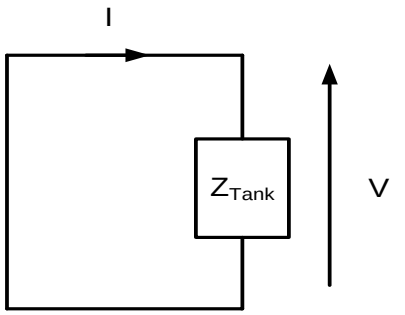



**Fig. A.9:** LC-tank equivalent impedance

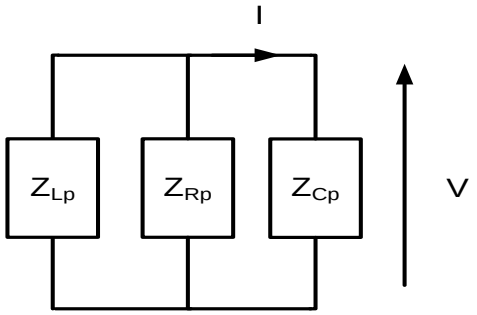



**Fig. A.10:** LC-tank impedance components

Viewing Fig. A.9, $V$ can be expressed as:

$$V = IZ_{Tank} \tag{A.54}$$

thereby enabling the function ($H(z)$) to be defined as follows:

$$H(z) = Z_{Tank} = \frac{V}{I} \tag{A.55}$$

Viewing Fig. A.10, $Z_{Tank}$ can be expressed as follows:

$$Z_{Tank} = Z_{L_p}||Z_{R_p}||Z_{C_p} \tag{A.56}$$

where $Z_{L_p} = (j\omega L_p)$, $Z_{C_p} = 1/(j\omega C_p)$ and $Z_{R_p} = R_p$. As solving (A.56) directly becomes quite cumbersome, a much more succinct approach is through viewing the tank in terms of its admittance ($Y_{Tank}$), thereby enabling the following:

$$Y_{Tank} = ((1/Z_{L_p}) + (1/Z_{R_p}) + (1/Z_{C_p})) \tag{A.57}$$

Replacing each of the impedance components with their corresponding frequency equivalent expressions, and performing some simplifying algebra yields:

$$Y_{Tank} = \frac{((j\omega)^2 L_p R_p C_p) + (j\omega L_p) + R_p}{j\omega L_p R_p} \tag{A.58}$$

Since $Z_{Tank} = 1/Y_{Tank}$, by taking the inverse of (A.58), $Z_{Tank}$, and hence $H(j\omega)$, become:

$$H(j\omega) = Z_{Tank} = \frac{j\omega L_p R_p}{((j\omega)^2 L_p R_p C_p) + (j\omega L_p) + R_p} \tag{A.59}$$

Converting (A.59) to the s-domain (where s = $j\omega$ for an undampened sinusoid) then yields the transfer function:

$$H(s) = \frac{LR_p s}{LR_p C s^2 + Ls + 1} \tag{A.60}$$

## A.11 Dependance of $TR$ on $C_{max}/C_{min}$

Tuning range ($TR$) is defined as:

$$TR(\%) = \frac{2(f_{max} - f_{min})}{f_{max} + f_{min}} \cdot 100 \tag{A.61}$$

where $f_{max} = 1/(2\pi\sqrt{LC_{min}})$ and $f_{min} = 1/(2\pi\sqrt{LC_{max}})$. Inserting these expressions for $f_{max}$ and $f_{min}$ back into (A.61) thus yields:

$$TR(\%) = \frac{2((1/(2\pi\sqrt{LC_{min}})) - (1/(2\pi\sqrt{LC_{max}})))}{(1/(2\pi\sqrt{LC_{min}})) + (1/(2\pi\sqrt{LC_{max}}))} \cdot 100 \tag{A.62}$$

Simplifying (A.62) through cumbersome algebra (which will not be repeated here) thus results in:

$$TR(\%) = 2\sqrt{\frac{C_{max}/C_{min} + 1 - 2\sqrt{C_{max}/C_{min}}}{C_{max}/C_{min} + 1 + 2\sqrt{C_{max}/C_{min}}}} \cdot 100 \tag{A.63}$$

## A.12 Dependance of the Output Voltage from the Sensing Network

The voltage across $R_2$ in Fig. 4.17 is defined as:

$$V_{out} - V_{CP^-} = IR_2 \tag{A.64}$$

Assuming first that $V_{CP^+} > V_{CP^-}$:

$$I = \frac{V_{CP^+} - V_{CP^-}}{R_1 + R_2} \tag{A.65}$$

Substituting (A.65) into (A.64) yields:

$$V_{out} - V_{CP^-} = \left(\frac{V_{CP^+} - V_{CP^-}}{R_1 + R_2}\right) R_2 \tag{A.66}$$

Following from (A.66), $V_{out}$ can be expressed as:

$$V_{out} = \left(\frac{V_{CP^+} - V_{CP^-}}{R_1 + R_2}\right) R_2 + V_{CP^-} \tag{A.67}$$

$$= \frac{(R_2 V_{CP^+}) + (R_1 V_{CP^-})}{R_1 + R_2} \tag{A.68}$$

Equation (A.69) also holds for the case where $V_{CP^+} < V_{CP^-}$, which when $R_1 = R_2$ reduces to:

$$V_{out} = \frac{V_{CP^+} + V_{CP^-}}{2} \tag{A.69}$$

## A.13 Derivation of the Average $K_{VCO}$ for a Sub-banded VCO

By definition (and ignoring $K_{VCO}$ variation), the required $K_{VCO}$ to achieve a specific frequency range ($\Delta F$), when employing no sub-banding, is defined as:

$$K_{VCO} = \frac{\Delta F}{V_{swing_{cp}}} \tag{A.70}$$

When employing sub-banding, the specified frequency range ($\Delta F$) will be split into $n$ sub-bands, thereby (ignoring $K_{VCO}$ variation) requiring the following $K_{VCO}$ for each sub-band:

$$K_{VCO} = \frac{\Delta F}{nV_{swing_{cp}}} \tag{A.71}$$

To account for x% of overlap ($OV\%$) between sub-bands, $K_{VCO}$ in effect needs to be increased by $OV$ thereby yielding the following required $K_{VCO}$ for each sub-band (ignoring $K_{VCO}$ variation):

$$K_{VCO} = \frac{\Delta F}{nV_{swing_{cp}}}(1 + OV) \tag{A.72}$$

## A.14 Reduction in Parallel Resistance due to a Switched Capacitor Array (SCA)

The total parallel resistance of a sub-banded VCO can be de-composed as follows:

$$\begin{aligned} R_p &= R_{p_{tank}} || R_{p_{SCA}} \\ &= \frac{R_{p_{tank}}}{1 + \frac{R_{p_{tank}}}{R_{p_{SCA}}}} \end{aligned} \tag{A.73}$$

Given that without the use of an SCA, $R_p = R_{p_{tank}}$, the use of an SCA can be seen from (A.73) to reduce $R_p$ by $(1/(1 + (R_{p_{tank}} R_{p_{SCA}})))$, or equivalently by the factor $X_{SCA}$ as follows:

$$X_{SCA} = \frac{R_{p_{SCA}}}{R_{p_{SCA}} + R_{p_{Tank}}} \tag{A.74}$$

## A.15 Reduction in Tuning Range due to Parasitic Capacitance

Following from (A.61), tuning range ($TR$) can defined as:

$$TR = \frac{2\Delta F}{f_{max} + f_{min}} \tag{A.75}$$

where $\Delta F = f_{max} - f_{min}$.

In [81], a change in capacitance ($\Delta C$) was shown to reduce $\Delta F$ by approximately a factor of $\Delta C\sqrt{\Delta C}$. Given that such a chance in capacitance can also be shown to reduce VCO frequency by a factor of $\sqrt{\Delta C}$, the overall tuning range ($TR$) thus reduces as follows:

$$\begin{aligned} TR &= \frac{1/(\Delta C\sqrt{\Delta C})}{1/\Delta C} \\ &= 1/\Delta C \end{aligned} \tag{A.76}$$

## A.16 Derivation of $C_{sw}$

The required capacitance to move VCO operation down one sub-band can be most easily derived with reference to the two adjacent sub-bands illustrated in Fig. A.11.

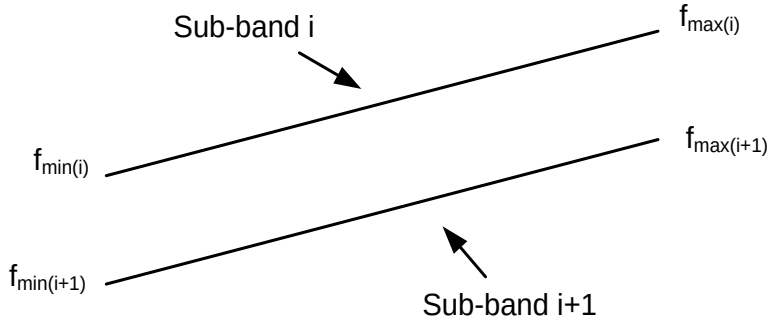



**Fig. A.11:** Ideal illustration of two adjacent sub-bands

Following from (3.3), $f_{max_i}$ and $f_{max_{(i+1)}}$ in Fig. A.11 can be expressed as:

$$f_{max_i} = \frac{1}{2\pi\sqrt{L(C_{min_i} + C_{par})}} \tag{A.77}$$

$$f_{max_{(i+1)}} = \frac{1}{2\pi\sqrt{L(C_{min_{(i+1)}} + C_{par})}} \tag{A.78}$$

where $C_{par}$ represents a lumped sum of parasitic capacitance's.

Following from (A.77) and (A.78), $C_{min_i}$ and $C_{min_{(i+1)}}$ can be respectively expressed as:

$$C_{min_i} = \frac{1}{(2\pi f_{max_i})^2 L} - C_{par} \tag{A.79}$$

$$C_{min_{(i+1)}} = \frac{1}{(2\pi f_{max_{(i+1)}})^2 L} - C_{par} \tag{A.80}$$

Given that $C_{sw}$ represents the required capacitance to move VCO operation from sub-band $i$ down to sub-band $(i+1)$ in Fig A.11, it can be defined as follows:

$$C_{sw} = C_{min_{(i+1)}} - C_{min_i} \tag{A.81}$$

Substituting (A.79) and (A.80) into (A.81), and performing the necessary algebra, yields:

$$C_{sw} = \frac{\left(\left(\frac{f_{max_i}}{(f_{max_i} - f_{min_1})OV + f_{min_i}}\right)^2 - 1\right)}{L(2\pi f_{max_i})^2} \tag{A.82}$$

## A.17 Reduction in Tuning Range ($TR$) due to $K_{VCO}$ Band-to-band Variation ($\Delta K_{VCO_{btb}}$)

Following from (A.75), $TR$ can be defined as:

$$TR = \frac{2\Delta F}{2f_{max} - \Delta F} \tag{A.83}$$

Given that $\Delta F$ reduces by $\Delta K_{VCO_{btb}}$ due to $K_{VCO}$ band-to-band variation, it follows that $TR$ reduces to:

$$TR = \frac{2\Delta F/\Delta K_{VCO_{btb}}}{2f_{max} - (\Delta F/\Delta K_{VCO_{btb}})} \tag{A.84}$$

## A.18 Dependance of Percentage Overlap ($OV$) on $K_{VCO}$ and Sub-band Spacing Resolution ($f_{res}$)

Referring back to Fig. A.11, $OV$ can be defined as follows:

$$OV = \frac{f_{max_{i+1}} - f_{min_i}}{f_{max_i - f_{min_i}}} \tag{A.85}$$

where $f_{max_{i+1}}$ is defined as:

$$f_{max_{i+1}} = f_{max_i} - f_{res_i} \tag{A.86}$$

where $f_{res_i}$ represents the frequency resolution between the $i^{th}$ and $(i+1)^{th}$ sub-bands.

Substituting (A.86) into (A.85) yields:

$$OV = \frac{f_{max_i} - f_{res_i} - f_{min_i}}{f_{max_i - f_{min_i}}} \tag{A.87}$$

Letting $\Delta f_i$ represent $f_{max_i} - f_{min_i}$, (A.87) can now be expressed as:

$$\begin{aligned} OV &= \frac{\Delta f_i - f_{res_i}}{\Delta f_i} \\ &= 1 - \frac{f_{res_i}}{\Delta f_i} \end{aligned} \tag{A.88}$$

Letting $\Delta f_i = K_{VCO_i} V_{swing_{cp}}$, (A.88) becomes:

$$OV = 1 - \frac{f_{res_i}}{K_{VCO_i} V_{swing_{cp}}} \tag{A.89}$$

from which it follows:

$$OV \propto \frac{f_{res}}{K_{VCO}} \tag{A.90}$$

# APPENDIX B

## B.1 Design Procedure for a Differential CP

The following is a design procedure for the differential CP of Fig. 4.20.

1. Define a table of specifications:

| Parameter | Recommendation |
|---|---|
| Vdd | Determined by process technology |
| Power Consumption | Determined by end application |
| $V_{bg}$ | Typically is 1.262 V. Where Vdd $<$ 1.262 V, it must be specified |
| $V_{cm}$ | Set to Vdd/2 (see section 4.3.4) |
| $V_{cp_{max}}$ | Define as per (4.17) |
| $V_{cp_{min}}$ | Define as per (4.18) |
| $I_{cp}$ | Dependant on various trade-offs |

**Table B.1:** Table of specifications for a differential CP

As stated in Table B.1, the choice of $I_{cp}$ entails various trade-offs. These are summarised in Table B.2.

| Parameter | $I_{cp}$ too small | $I_{cp}$ too large |
|---|---|---|
| Power consumption | Low | High |
| Noise | High | Low |
| LF capacitors | Small | Large |
| LF resistor | Large | Small |

**Table B.2:** Parameters directly affected by $I_{cp}$

2. Define $V_{cm}$:

   This is achieved as follows:

$$V_{cm} = V_{ds1\to4} + V_{ds_{5\to8}}(on) + V_{ds_{9\to12}} \tag{B.1}$$
$$= Vdd + V_{ds_{13\to15}} \tag{B.2}$$
$$= Vdd/2 \tag{B.3}$$

   Analysis of (B.1) and (B.2) shows an inherent mismatch between the UP and DN currents to occur due to the differences in drain-source voltages across $M1 \to M4$ and $M13 \to M15$. This difference is quantified in (B.4), which must be minimised.

$$\Delta V_{ds} = V_{ds_{5\to8}}(on) + V_{ds_{9\to12}} \tag{B.4}$$

3. Calculate the aspect ratio for $M1 \to M4$ of the CP:

   The aspect ratio for $M1 \to M4$ ($(W/L)_{1\to4}$) can be approximated as follows:[1]

$$\left(\frac{W}{L}\right)_{1\to4} = \frac{2I_{cp}}{\mu_n C_{ox} V_{ov_{1\to4}}^2} \tag{B.5}$$

   where $C_{ox}$ and $\mu_n$ are process dependant parameters representing the oxide capacitance and electron mobilities of $M1 \to M4$ respectively.

   The overdrive voltage of $M1 \to M4$ ($V_{ov_{1\to4}}$) is found by re-working 4.18 as follows:

$$V_{ov_{1\to4}} = V_{cp_{min}} - V_{ds_{5\to8}}(on) - V_{ds_{9\to12}} \tag{B.6}$$

   Initially insert guesstimated values for $V_{ds_{5\to8}}(on)$ and $V_{ds_{9\to12}}$ at $<< V_{ds1\to4}$ into (B.6) to obtain a first cut approximation for $(W/L)_{1\to4}$. Then set $L \geq 10 \cdot L_{min}$

[1] Assumes a parabolic behaviour of MOSFET drain current [86] which maintains reasonable accuracy for long-channel devices typically used for current mirroring.

(minimum channel length for the process technology used) to make $M1 \rightarrow M4$ more resilient to channel length modulation effects. Using this, $W$ is calculated as follows:

$$W = (10 \cdot L_{min})(W/L) \tag{B.7}$$

4. Calculate the aspect ratio for $M13 \rightarrow M15$ of the CP:

   The aspect ratio for $M13 \rightarrow M15$ ($(W/L)_{13\rightarrow15}$) can be approximated as follows:[1]

$$\left(\frac{W}{L}\right)_{13\rightarrow15} = \frac{2I_{cp}}{\mu_p C_{ox} V_{ov_{13\rightarrow15}}^2} \tag{B.8}$$

   where $\mu_p$ represents the hole mobilities of $M13 \rightarrow M15$.

   The overdrive voltage of $M13 \rightarrow M15$ ($V_{ov_{13\rightarrow15}}$) is found by re-working 4.17 as follows:

$$V_{ov_{13\rightarrow15}} = V_{cp_{max}} - Vdd \tag{B.9}$$

   As before, set $L \geq 10 \cdot L_{min}$ and use to calculate $W$ from (B.7). Adjust for inaccuracies in the calculations then through simulation.

5. Calculate the aspect ratio for $M5 \rightarrow M8$ of the CP:

   $M5 \rightarrow M8$ should be made small to reduce charge injection and input gate capacitance. They should not be made too small however as this will result in poor matching, potentially increase sub-threshold leakage and result in large drain-source voltages which increase mismatch current via (B.4). Therefore, the optimum value for their aspect ratio ($(W/L)_{5\rightarrow8}$) is most practically found through simulation. Once simulated, insert $V_{ds_{5\rightarrow8}}(on)$ back into (B.6) to obtain a more accurate approximation for $V_{ov_{1\rightarrow4}}$.

6. Calculate the aspect ratio for $M9 \rightarrow M12$ of the CP:

   $M9 \rightarrow M12$ should exhibit drain-source voltages large enough to allow efficient CMFB control, with the optimum value for their aspect ratio ($(W/L)_{9\rightarrow12}$) being most practically found through simulation. Once simulated, insert $V_{ds_{9\rightarrow12}}$ back into (B.6) to obtain the correct calculation for $V_{ov_{1\rightarrow4}}$.

7. Calculate the aspect ratios for the differential amplifier:

   The aspect ratios for the differential amplifier were found according to the procedure detailed in [64] which will not be repeated here. The biasing current $I_{CMFB}$ should be set as large as the specified power consumption allows with $C_c$ being sized as per (4.31) to achieve $PM = 60°$ [64].

## B.2 Design Procedure for a Differential LF

The following is a design procedure for the differential LF of Fig. 4.23.

1. Define a table of specifications:

| Parameter | Recommendation |
|---|---|
| $PM$ | Set to 50°, (see section 2.6.4) |
| Loop Bandwidth ($K$) | Define as per section 2.7.4 |
| $I_{cp}$ | See Appendix B1 |
| $K_{VCO}$ | Determined by the varactor $C_{max}/C_{min}$ ratio (see section 3.4) |
| Feedback integer (N) | $\omega_{out}/\omega_{ref}$ |

**Table B.3:** Table of specifications for a differential LF

   In Table B.4, $\omega_{out}$ represents the PLL nominal output frequency which is defined based on the inductor characterisation (see section 3.5) and end application requirements. The PLL reference frequency is then represented by $\omega_{ref}$ which is determined by end application requirements.

2. Calculate $R_1$ for a single-ended LF:

   Rework the formula for loop bandwidth ($K$) in (2.44) as follows:

$$R_1 = \frac{2\pi NK}{I_{cp}K_{VCO}} \tag{B.10}$$

   Inserting the specified values into (B.10) thus gives the required value for $R_1$.

3. Calculate $C_1$ for a single-ended LF:

   Rework (2.28) to give the following expression for $C_1$:

$$C_1 = \frac{1}{R_1\omega_{z_1}} \tag{B.11}$$

   Inserting (2.33) into (B.11), and recalling from section 2.7.2 that $\omega_x = K$ yields the following expression for $C_1$:

$$C_1 = \frac{k}{R_1K} \tag{B.12}$$

   Inserting the specified values into (B.12) thus gives the required value for $C_1$.

4. Calculate $C_2$ for a single-ended LF:

   Rework (2.30) to gives the following expression for $C_2$:

$$C_2 = \frac{C_1}{(C_1 R_1 \omega_{p_2}) - 1} \tag{B.13}$$

   Inserting (2.32) into (B.13), and recalling once again that $\omega_x = K$, yields the following expression for $C_2$:

$$C_2 = \frac{C_1}{(C_1 R_1 k K) - 1} \tag{B.14}$$

   Inserting the specified values into (B.14) thus gives the required value for $C_2$.

5. Calculate $C_1$ and $C_2$ for a differential LF:

   Transform the previously calculated values for $C_1$ and $C_2$ for use in a differential LF via (4.34) and (4.35) as follows:

$$C_1 = C_1/2 \tag{B.15}$$

$$C_2 = C_2/2 \tag{B.16}$$

   Note that $R_1$, as calculated in (B.10), applies to a differential LF with the only exception being that now two $R_1$ resistors are required (see Fig. 4.23).

6. Calculate the area requirements of the LF:

   Calculate the overall area requirements based on the values of $C_1$ and $C_2$ above. Using the capacitance to area ratio for the process technology ($K_{CA}$), this can be approximated as:

$$A_{LF} \approx \frac{(C_1 + C2)}{K_{CA}} \tag{B.17}$$

   Pending on the result from (B.17) and various other factors, an informed decision as to whether to implement the LF on- or off-chip can be made.

## B.3 Design Procedure for a Differentially Tuned VCO

The following is a design procedure for the differentially tuned VCO of Fig. 4.40.

1. Define a table of specifications:

| Parameter | Recommendation |
|---|---|
| Centre frequency ($f_c$) | $\omega_{out}$, see Appendix B2 |
| Tuning range ($TR$) | Determined by end application |
| $I_{cp}$ | See Appendix B1 |
| $K_{VCO}$ | See Appendix B2 |
| $V_{swing_{cp}}$ | See section 4.3.2 |
| $V_b$ | Define as per (4.40) |
| $L$ | Initially set to optimum value based on the inductor characterisation in section 3.5. |
| $C_{par}$ | Introduced to account for layout parasitics. Defined based on apriori layout knowledge of VCOs for the process technology [a] |

[a] $C_{par}$ for VCO laid out using UMCs 90nm CMOS process was found to be $\approx$ 4000fF.

**Table B.4:** Table of specifications for a differentially tuned VCO

2. Calculate maximum and minimum oscillation frequencies:

   The maximum ($f_{max}$) and minimum ($f_{min}$) oscillation frequencies are determined as follows:

$$f_{max} = f_c + (f_c(TR/2)) \tag{B.18}$$

$$f_{min} = f_c - (f_c(TR/2)) \tag{B.19}$$

3. Calculate initial values for $C_{max}$ and $C_{min}$:

   Initial values for $C_{max}$ and $C_{min}$ are determined by reworking (3.3) and inserting the required values as follows:

$$C_{max} = \frac{1}{L((2\pi f_{min})^2)} - C_{par} \tag{B.20}$$

$$C_{min} = \frac{1}{L((2\pi f_{max})^2)} - C_{par} \tag{B.21}$$

4. Calculate the theoretical $C_{max}, C_{min}$ combinations over a range of values for $L$:

   The initial $C_{max}, C_{min}$ combination from (B.20) and (B.21) is often not physically realisable. Therefore, all possible $C_{max}, C_{min}$ combinations must be calculated for various values of $L$. This is achieved by sweeping $L$ over a range of practically realisable inductance values and calculating the corresponding $C_{max}$ and $C_{min}$ values for each value of $L$. Plotting $C_{max}/C_{min}$ against $C_{max} - C_{min}$ then produces a curve containing all the theoretical $C_{max}, C_{min}$ combinations over the range of $L$. An example plot is shown in Fig. B.1.

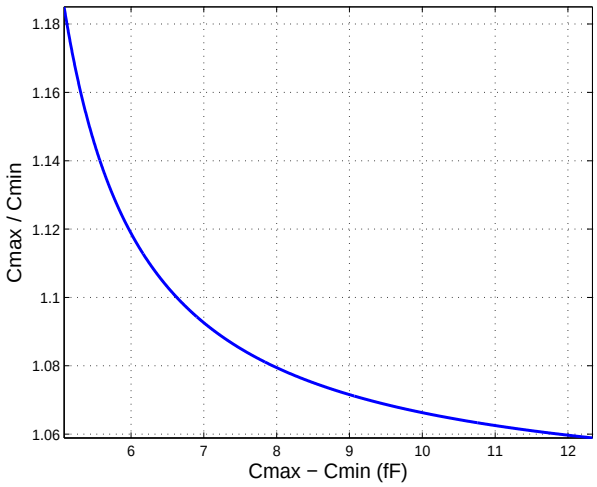



**Fig. B.1:** Theoretical $C_{max}$, $C_{min}$ combinations over an applied inductance seep

   The reason for plotting $C_{max}/C_{min}$ against $C_{max} - C_{min}$ will become apparent later.

5. Characterise the chosen varactor configuration:

   Assuming the correct varactor configuration has been chosen based on discussions in section 4.5.3, first characterise the configuration to achieve the highest quality factor. Using the resulting varactor dimensions from this characterisation, next vary the dimensions of the ac-coupling capacitors ($C_s$ in Fig. 4.35), recording the individual values for $C_{max}$ and $C_{min}$ for each dimensional variation of $C_s$.[2] Plotting $C_{max}/C_{min}$ against $C_{max} - C_{min}$ this time then produces a curve containing all the

[2]The best approach in terms of layout is to vary the dimensions of $C_s$ so as to maintain the same aspect ratio (i.e. vary $W$ and $L$ by the same amount).

physically realisable $C_{max}, C_{min}$ combinations over the range of $L$. An example plot is shown in Fig. B.2.

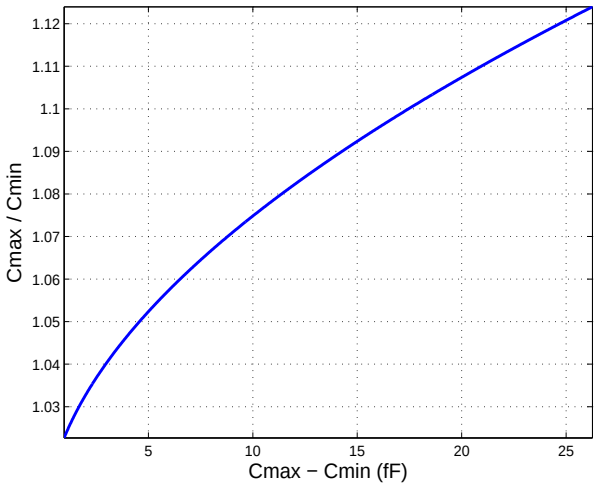



**Fig. B.2:** Physically realisable $C_{max}$, $C_{min}$ combinations for a varactor configuration

If necessary, repeat for multiple parallel connections of the varactor configuration to produce multiple characterisation curves. This is recommended to obtain a good general overview of all possible $C_{max}, C_{min}$ combinations obtainable.

6. Find the theoretical $C_{max}, C_{min}$ combination that is physically realisable:

   Superimpose the curve containing all theoretical $C_{max}, C_{min}$ combinations over the applied inductance sweep, onto the characterisation curve(s) containing all physically realisable $C_{max}, C_{min}$ combinations. Where the two curves intersect is thus where theory meets practise as this represents a $C_{max}, C_{min}$ combination that achieves the specified tuning range whilst being physically realisable. The beauty of this intersection point is that it represents a unique $C_{max}, C_{min}$ combination, only made possible by the of plotting $C_{max}/C_{min}$ against $C_{max} - C_{min}$.

   An example plot is shown in Fig. B.3 which is simply the superposition of Fig. B.1 onto Fig. B.2.

   The co-ordinates of the intersection point are then found using a numerical algorithm [93], where back calculating enables the precise values for $C_{max}$, $C_{min}$, $L$ and $W, L$ dimensions for $C_s$ to be extracted.

   This procedure is strongly advised as it enables a complete overview of the theoretical and practical $C_{max}, C_{min}$ combinations over the specified conditions. In addition, it is seen to be a much faster approach to calculating the required $C_{max}$ and $C_{min}$ values than simply attacking equations (B.20) and (B.21) via brute force.

7. Size the Inductor:

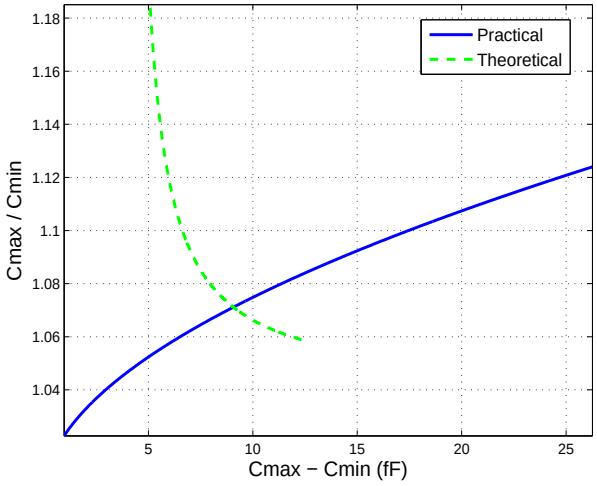



**Fig. B.3:** Theoretical and practical $C_{max}$, $C_{min}$ combinations for a varactor configuration

Through simulation, size the inductor so as to achieve the extracted value for $L$ from step 6. Once found, record the inductors quality factor ($Q_L$) and series resistance ($R_s$).

8. Approximate the required biasing necessary to sustain oscillation:

   Using $Q_L$ and $R_s$ from step 7, calculate the parallel resistance of the LC-tank ($R_p$) via (3.11). Apply the resulting $R_p$ to (3.20) to calculate the minimum $g_{m_{min}}$ requirements necessary to sustain oscillation. Using this value for $g_{m_{min}}$, the required bias current to sustain oscillation in the VCO ($I_{VCO}$) can be loosely approximated as follows:[3]

$$I_{VCO} \approx g_{m_{min}}(V_{gs_{cc}} - V_{t_{cc}}) \tag{B.22}$$

   where the gate source and threshold voltages for the cross-coupled differential pair are represented by $V_{gs_{cc}}$ and $V_{t_{cc}}$ respectively.

9. Calculate the aspect ratio for the differential cross-coupled pair:

   Using the values for $g_{m_{min}}$ and $I_{VCO}$ from step 8, the aspect ratio for the differential cross-coupled differential par ($(W/L)_{cc}$)can be loosely approximated as follows:[1]

$$\left(\frac{W}{L}\right)_{cc} = \frac{g_{m_{min}}^2}{\mu_n C_{ox} I_{VCO}} \tag{B.23}$$

   where $C_{ox}$ and $\mu_n$ represent the oxide capacitance and electron mobilities of the cross-coupled differential pair. Due to the various approximations made to arrive at

[3]Provides very loose approximations as it assumes the differential cross-coupled pair are always in saturation with a resulting parabolic drain current characteristic.

this point, (B.23) can only serve as an initial guess for $(W/L)_{cc}$. Its correct value will need to be found through simulation for a drain-source voltage equal to the VCO DC bias level ($V_{DC}$) (see Fig. 4.40).

10. Approximate the aspect ratio for the biasing transistors:

    Using the value for $I_{VCO}$ from step 8, the aspect ratio for the biasing transistors ($(W/L)_{bias}$)can be approximated as follows:[1]

$$\left(\frac{W}{L}\right)_{bias} = \frac{2I_{VCO}}{\mu_p C_{ox} V_{ov^2_{bias}}} \tag{B.24}$$

    where the overdrive voltage and hole mobilities of the biasing transistors are represented as $V_{ov_{bias}}$ and $\mu_p$ respectively. Once again due to various approximations, (B.24) can only serve as an initial guess for $(W/L)_{bias}$, with its correct value being found through simulation for a drain-source voltage equal to the VCO DC bias level ($V_{DC}$) (see Fig. 4.40).

11. Find the boundary between the $I$- and $V$-limited regions of operation:

    By adjusting $I_{VCO}$ and simulating the phase noise ($PN$) for each adjustment, find the boundary between the $I$- and $V$-limited regions of operation, as shown in Fig. 3.33. Once found, set the corresponding value for $I_{VCO}$ as the final value for the VCO bias current.

## B.4 Design Procedure for an SCA Branch

The following is a design procedure for the SCA branch of Fig. 5.5.

1. Calculate $C_{sw}$:

    Assuming equi-valued capacitors are employed in the SCA, calculate the required switched capacitance's from (5.9) using apriori knowledge of the percentage overlap ($OV$) and the maximum ($f_{max}$) and minimum ($f_{min}$) frequencies for the top VCO band.

2. Calculate the aspect ratios for $M1 \rightarrow M5$:

    In order to reduce losses (which will reduce $R_{p_{br}}$) without significantly contributing to the overall parasitic capacitance of the branch ($C_{par_{br}}$), $M1$ should be made wide and short with $M2 \rightarrow M5$ being made long and narrow. Based on these guidelines, their exact dimensions can be found through simulations similar to that of Fig. 5.6.

3. Find a practically realisable $C_{sw}, C_{par_{br}}$ combination:

$C_{par_{br}}$ must be accounted for by adding it onto $C_{sw}$ thereby further increasing $C_{par_{br}}$, which must again be accounted for and so forth. A fast approach to obtaining a practical $C_{sw}, C_{par_{br}}$ combination is through a characterisation similar to that used in Appendix B3. First, plot $C_{sw}$ against $(C_{sw} + C_{par_{br}})$ over a range of values for $C_{par_{br}}$. This represents the practical $C_{sw}, C_{par_{br}}$ combinations for which an example plot is shown in Fig. B.4.

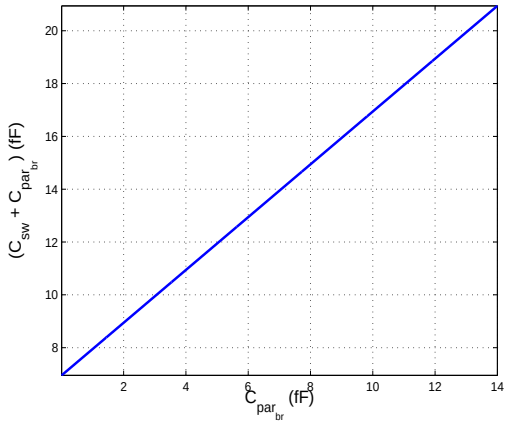



**Fig. B.4:** Theoretical $C_{sw}, C_{par_{br}}$

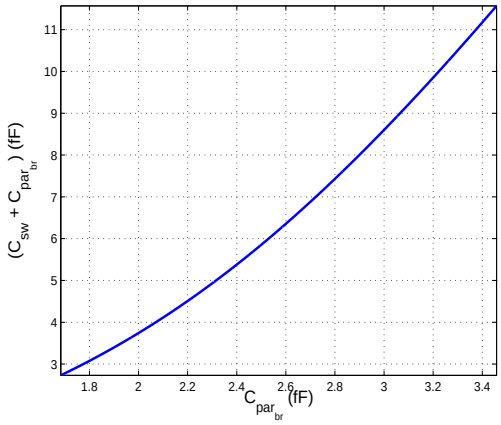



**Fig. B.5:** Practical $C_{sw}, C_{par_{br}}$

Next characterise the branch by varying one of the capacitor dimensions. Plot the resulting on capacitance's $(C_{sw})$ against off capacitance's $(C_{par_{br}})$ to give the practical $C_{sw}, C_{par_{br}}$ combinations. An example plot is shown in Fig. B.5.

Superimpose both plots on top of each other as shown in Fig. B.6.

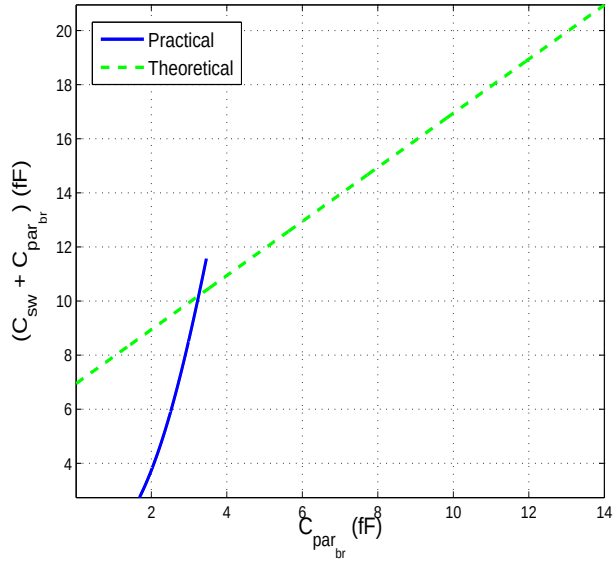



**Fig. B.6:** Practical and theoretical $C_{sw}, C_{par_{br}}$ combinations

The intersection point between the two curves represents a physically realisable $C_{sw}$ to enable the required percentage overlap which compensates for $C_{par_{br}}$. As in Appendix B3, back calculating from the intersection point enables the corresponding capacitor dimensions to be obtained.

This procedure is strongly advised as it avoids an endless iterative loop that can otherwise result.

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