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Automatic Control and Machine Learning for Semiconductor Manufacturing: Review and Challenges ⋆

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Abstract: Semiconductor manufacturing is one of the most technologically advanced industrial sectors. Process quality and control are critical for decreasing costs and increasing yield. The contribution of automatic control and statistical modeling in this area can drastically impact production performance. For this reason in the past decade major collaborative research projects have been undertaken between fab industries and academia in the areas of Virtual Metrology, Predictive Maintenance, Fault Detection, Run-to-Run control and modeling. In this paper we review some this research, discuss its impact on production and highlight current challenges.

Keywords: Intelligent manufacturing systems, Predictive maintenance, Fault detection, Soft Sensor, Virtual Metrology, Run-to-Run Control, Machine Learning

1. INTRODUCTION

The field of semiconductor manufacturing, while being among the most technology-oriented and cost-intensive industrial sectors, has a massive impact on everyday life. As a matter of fact, semiconductor-based devices are pervasive: personal computers, mobile phones and cars are only the most straightforward examples. Given such premises, it is not surprising that semiconductor manufacturing companies are spending effort and resources to improve quality and open the way to smaller, faster, higher quality devices.

In the milestone paper Edgar et al. (2000), the (at that time) future challenges for modeling and control in microelectronics manufacturing were presented. In the past 12 years intense research activity has been going on in this area, largely enabled by the advances in machine learning and computation capability. As described in Edgar et al. (2000), the variations in process and tool properties due to long-term production runs, the limited understanding on such complicated processes and the lack of automated operational practices (especially from the maintenance point of view), suggest that there is a huge margin for improvements in this area.

In this paper the contributions of non-parametric modeling, machine learning, filtering and prediction, and run-to-run control to semiconductor manufacturing are reviewed. In particular, we show some examples in the following applications areas:

- *Virtual Metrology (VM)* systems;
- *Fault Detection (FDC)* systems;
- *Predictive Maintenance (PdM)* systems;
- *Run-to-Run (R2R)* control.

All of these technologies have proliferated in the past few years in semiconductor manufacturing facilities, called *fabs*, in order to improve the productivity and decrease costs. The final goal of this work is to prove through several examples and applications that the use of statistical modeling algorithms and control systems can improve the efficiency, yield and profits of a manufacturing environment such as the semiconductor one, where lots of data are recorded and can be employed in mathematical models. Semiconductor companies are investing more and more resources in these topic to improve their manufacturing capabilities; recently, for example, the major European Nanoelectronics Industries have focused their efforts on developing statistical metrology/predictive systems to decrease the number of defective products, increase process stability and even decrease the number of physical measures performed, see IMPROVE (2012).

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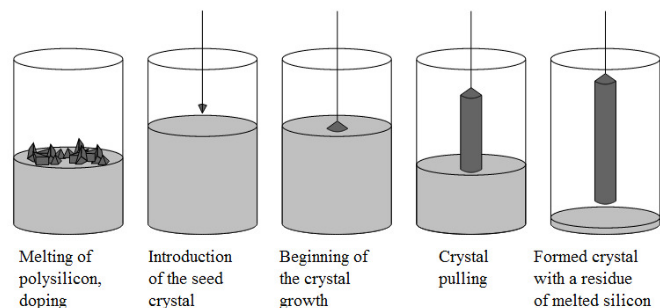

Fig. 1. The main stages of the Czochralski process.

The paper is organized as follows: in Section 2 an overview of semiconductor fabrication is provided. The most common practices in *Advanced Process Control (APC)* systems and the major issues for engineers and statisticians working in this area are then presented: in Section 3 Virtual Metrology systems are discussed, while in Section 4 we present Predictive Maintenance technologies. Fault Detection and Classification and Run-to-Run control techniques are presented in Section 5 and 6 respectively. Finally in Section 7 some final remarks are provided.

2. FABRICATION OF SEMICONDUCTOR DEVICES

This section describes, with no aim of completeness, the fabrication process for a semiconductor device. For a deeper description of the technology behind a semiconductor manufacturing company, the interested reader is referred to Quirk and Serda (2001).

2.1 Description of the process

The entire semiconductor manufacturing process, from the first stage up to final product shipping, takes usually six to eight weeks and is performed in highly specialized fabrication plants. The process is composed of four main steps (Chang (1997)):

i) Wafer formation: a wafer is a thin (125 - 300mm diameter and 525 - 775 μm) slice of semiconductor material - usually silicon crystal - that serves as the substrate for microelectronic devices. Wafers are formed from extremely pure (99.9999% purity) crystalline material; the process to create such crystalline wafers, is the Czochralski process, depicted in Figure 1.

ii) Front end processing: this step relates to the formation of transistor chips on the silicon wafer and is performed in controlled environments known as *clean rooms*; in such rooms the level of *pollutants* (dust, vapors, particles) is artificially kept at a fixed level by means of air filtering and restricted access policies. The front end process encompasses the following sub-steps:

(1) *Wafer-cleaning*: since Ultra-Large Scale Integration (ULSI) technology is characterized by strict requirements concerning surface smoothness and particle contamination, the wafers need to be prepared for further processing by means of cleaning procedures. Table 1 summarizes the sources and effects of the various contaminations (Chang and Chao (1996)).
(2) *Deposition*: dieletric and polysilicon film deposition is widely used in Integrated Circuits (IC) fabrication. Dieletric films, including silicon dioxide and silicon nitride, serve as isolation, mask, and passivation layers; polysilicon film can be used as a conducting layer, semiconductor, or resistor by proper doping with different impurities. The main deposition techniques are *CVD* (Chemical Vapor Deposition) and *PVD* (Physical Vapor Deposition); other processes include plasma-assisted deposition, photo CVD, laser CVD, Rapid-Thermal Processing CVD (RTPCVD), and Electron-Cyclotron Resonance (ECR) CVD, see Cheng (1996).
(3) *(Photo)Lithography*: several techniques may be used to create ULSI circuit patterns on wafers; the most common process relies on *photomask* exposition. An ultraviolet radiation is transmitted through the clear part of the mask, while the opaque part blocks the rest of the radiation. The resist film, being sensitive to the radiation, is then coated on the wafer surface. The mask is aligned within the required tolerance on the wafer; then radiation is applied through the mask and the resist image is developed, see Nakamura (1996).
(4) *Etching*: devices are built from a number of different layer materials sequentially deposed. Lithography techniques are used to replicate circuit and device features, and the desired patterns are transferred by means of etching. In ULSI technology, the etching process is very sensitive because of strict dimensional requirements (fraction of a micrometer). The etching process can be *dry* or *wet*, see Lii (1996).

It should be noted that the above mentioned process steps are repeated several times during front-end processing to produce multiple interconnected layers on the wafer surface.

iii) Testing: before a wafer is sent to chip preparation, every single IC on the wafer is tested for functional defects (test end-of-line) (Palma (2005)). The tests can be *parametric* and *electrical*.

- Parametric tests are performed on *ad-hoc structures* prepared on the device to monitor the efficiency of process steps and the goodness of the design. Such structures are called *TAG*, and lie in the *scribe lines*. Usually there are less than 10 TAGs per wafer. Parametric tests consist of electric measurements of physical quantities (impedance, capacitance, resistance, etc.).
- Electrical tests verify that the behavior of each device is consistent and within specifications; this capability is assessed by means of electrical testing with sequential measurements; if some value is out of specification range, the circuit is flagged as faulty. The non-passing die is marked with a small dot of ink, and the passing\non-passing information stored in a *wafermap*.

iv) Packaging (or Back end): the purposes of packaging are to provide electrical connection, protect the chip from mechanical and environmental stress and provide a proper thermal path for the heat that the chip generates. Packaging plays a crucial role with respect to performance and reliability of the chip and the system in which the package is applied (Tachikawa (1996)).

Table 1. Sources and effects of the various contaminations

Contamination	Possible source	Effects
Particles	Equipment, ambient, gas, chemical	Low oxide breakdown
Metal	Equipment, chemical, reactive ion etching	Low breakdown field, reduced minority lifetime
Organic	Vapor in room, residue of photoresist	Change in oxidation rate
Microroughness	Initial wafer material, chemical	Low oxide breakdown
Native oxide	Ambient moisture	Degraded gate oxide, high contact resistance

The Front end processing part is the one where machine learning and automatic control techniques can affect the most the production quality. We will give in the next sections an overview of the main technologies that have been developed in the last years in this area.

3. VIRTUAL METROLOGY

3.1 Introduction and Modeling

A VM system consists of a mathematical model of the system under consideration (Ringwood et al. (2010)) for estimating a 'costly to measure' physical variable where tool variables are used as inputs. These quantities are usually 'costly' to measure in economic or temporal terms: the prediction is based on process variables and/or logistic information on the production that, instead, are always available and that can be used for modeling without further costs.

VM systems have been proposed in the literature for CVD (Hung et al. (2007); Cheng et al. (2007); Huang et al. (2008); Ferreira et al. (2009)) , Etching (Kang et al. (2009); Lynn et al. (2009); Cheng et al. (2008); Lin et al. (2009)), and Lithography Huang et al. (2009) processes. Also, fab-wide VM structures have been proposed by Khan et al. (2007); Huang et al. (2007); Su et al. (2008)

Besides high prediction accuracy, desirable properties of an efficient VM system are:

- *reasonably low computational times*, since new products are added monthly to fab production and the behavior of tools change over their maintenance cycles, therefore models need to be constantly updated and computed;
- *interpretability*, so that it is possible to identify which variables in the model are the most meaningful, a very appealing property for FDC purposes.

The problem of modeling semiconductor processes has been approached by using different techniques, both Linear, such as Ordinary Least Square (OLS) and Partial Least Squares (PLS), and Non-Linear, such as Artificial Neural Networks (NNs). It has been shown (Hung et al. (2007); Kang et al. (2009); Lynn et al. (2009); Himmel et al. (1992); Himmel and May (1993)) that NNs guarantee better performance in modeling semiconductor manufacturing processes than other linear approaches. NNs are flexible computing frameworks and universal approximators that can be applied to a wide range of learning problems with a high degree of accuracy (Khashei and Bijari (2010)). A common and widely adopted type of NN is the *Multilayer Perceptron (MLP)*; the central idea of MLPs is to extract linear combination of the inputs (in the problem considered here, the tool and logistic data) and then model the target (the critical dimension to be estimated) as a nonlinear function of such features (Besnard and Toprac (2006)). However, NNs can be really hard to train in learning problems with high dimensionality, as is the case in semiconductor manufacturing modeling. Moreover, given the use of non-linear features of the inputs during the algorithm training, the results often lack interpretability.

3.2 Challenges

As partly described in Susto and Beghi (2012c), modeling of semiconductor manufacturing processes is a challenging task mostly due to four main factors:

1. *high dimensionality* - hundreds of input variables are available making the regression problem computationally expensive and difficult to solve;
2. *data fragmentation* - hundreds/thousands of products are run on the same machine, with different tool settings (called *recipes*); in the case of some tools, the dataset is even further complicated by the fact that each product has a different target, and the equipment may be composed of 2 or 3 separated chambers that exhibit different behaviors. As shown in the example reported in Fig. 2, chambers of the same tool can usually be considered as completely different machines.
3. *time series input data* - many semiconductor modeling problems require the estimation of a scalar output from one or more time series. Such VM problems are usually tackled by extracting a fixed number of features from the time series (like their statistical moments), with a consequent loss in information that leads to suboptimal predictive models. Moreover, feature extraction techniques usually make assumptions that are not met by real world settings (e.g. uniformly sampled time series of constant length), and fail to deliver a thorough methodology to deal with noisy data.
4. *multi processes modeling* - semiconductor production processes involve a high number of sequential operations and the quality features of a certain wafer depend on the whole processing and not only on the last step before measurement; unfortunately VM modules proposed to date only take into account one physical process.

A substantial part of modern VM literature is focused on how to tackle the aforementioned issues.

Two basic approaches to deal with issue (1) have been proposed in the VM literature:

- the use of *dimensionality reduction* techniques, like correlation analysis (Susto et al. (2011b); Cheng et al. (2008)) and Principal Components Analysis (PCA) (Zeng and Spanos (2009)), that, when applied before

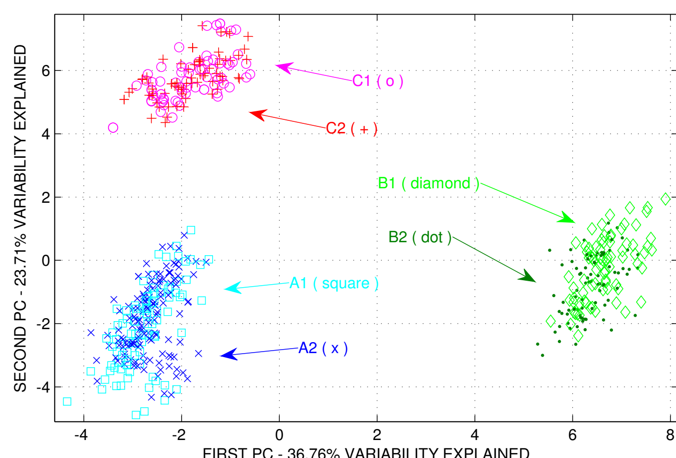

Fig. 2. The first two Principal Components (PCs) of the physical variables of a CVD tool with three chambers (A, B and C), each one with 2 sub-chambers (1 and 2). Taken from Susto and Beghi (2012c).

the actual modeling part in a two-step approach, reduce the size of the dataset;

- the use of *variable selection* techniques, like Stepwise Selection (SS), where parsimonious models are created during the modeling phase.

The results of variable selection techniques are usually easy to interprete, given the fact that only variables that matter 'enter' the model. However SS Regression, that has been widely adopted (Ferreira et al. (2009); Kang et al. (2009); Lynn et al. (2009); Ragnoli et al. (2009)), is considered in the Statistical Learning community as a really 'greedy' approach where important variables may not enter the model due to the algorithm procedure. Usually *Stagewise Selection (SgS)* Hastie et al. (2009) is preferred for prediction accuracy, but it is much more onerous from the computational point of view. Other variable selection methodologies have been proposes: in Susto and Beghi (2012b) Least Angle Regression (LARS) (Efron et al. (2004)) has been proposed, a model selection algorithm which provides equivalent solutions to SgS, but at the cost of SS; in Pampuri et al. (2011b) the LASSO (Tibshirani (1996)) has been employed, another popular variable selection technique.

Huge data fragmentation (2) cannot be dealt with by considering separately every specific case, since there is insufficient data to identify and validate a reliable mathematical model for each product. It is therefore necessary to group together data collected under different equipment operating conditions. A smart data clustering, as shown in Susto and Beghi (2012a), can enhance prediction accuracy and it is necessary to model all the fab production. A different approach has been proposed in Schirru et al. (2011), where Multi-Task techniques have been proposed to model the different logistic paths that a wafer may take.

In Schirru et al. (2012), inspired by issue (3), a methodology based on functional learning has been proposed to overcome the problems of dealing with time series where features must be extracted; the proposed Supervised Aggregative Feature Extraction (SAFE) approach allows continuous, smooth estimates of time series data to be derived (yielding aggregate local information), while simultaneously estimating a continuous shape function providing optimal predictions. To our knowledge, this in the first approach presented in the literature to deal with issue (3).

Regarding (4), a solution has been proposed in Pampuri et al. (2012). Unfortunately, the modeling of multiple steps makes the dimensionality of the regression problem even bigger and for this reason research has not proceeded far in this direction. However, this is the next step in the VM research, given the fact that the variability of a process cannot be fully captured without looking at the wafer state that is related to the previous processing steps performed.

4. PREDICTIVE MAINTENANCE

4.1 Definition

Efficient management of maintenance and control actions on a process is essential to decrease the costs associated with defective wafers and equipment inactivity. Maintenance policies can be divided into four categories, with different levels of complexity and efficiency, Susto et al. (2012a); Mobley (2002):

- *Run-to-Failure (R2F) Maintenance*: when repairs or restoration actions are performed after the occurrence of a failure. This is the simplest approach to maintenance management and usually the most costly one due to the large number of defective products obtained as a consequence of the failure.
- *Preventive Maintenance (PVM)* (or Scheduled Maintenance): when the maintenance is carried out periodically on a planned schedule with the aim of anticipating the process failures. In this approach, failures are usually avoided, on the other hand, unnecessary maintenances are sometimes performed.
- *Condition-Based Maintenance (CBM)*: when the actions on the process are taken after the verification of one or more conditions indicating a degradation in the process or equipment. This approach is based on continuous monitoring of the machine/process health and enables maintenance to be performed only when actually needed. The drawback of CBM management is that maintenance cannot be planned in advance.
- *Predictive Maintenance (PdM)* (or Statistical Based Maintenance): similarly to CBM, maintenance actions are taken only when necessary. However, prediction tools are used to assess when such actions are likely to be required, facilitating implementation of planning and scheduling schemes. PdM systems can employ ad-hoc defined health factors or, in general, statistical inference methods.

Sophisticated maintenance tools, such as those belonging to the CBM and PdM classes, are clearly associated with initial, installation, and development costs, that are however paid off by the increase in system uptime and percentage of non defective products and decrease in the number of test wafers employed. Besides the above mentioned advantages, it has also been shown (Hyde et al. (2004)) that the introduction of a PdM system in the production line can increase the Process Capability Index C_{pk} (Montgomery (2007)).

The PdM techniques usually define and exploit a *Health Factor (HF)*, Chen and Blue (2009), that is a quantitative index of the status of the equipment. It is a function of observable facilities parameters (historical time series, characteristic behavior of the equipment, sensor data, and so on) and can be employed to:

- assess future status of the equipment or one of its components;
- take strategic decisions about maintenance scheduling;
- provide information for dynamic sampling plans, Pasadyn and Toprac (2002).

The concept of HF is usually widely adopted also in Fault Detection and Classification (FDC) systems and this leads to some overlap between the two categories (see Section 5).

4.2 Review and Challenges

While all VM problems can be tackled with regression approaches, for PdM, depending on the problem, several techniques may be suitable for modeling and predicting faults and scheduling maintenance interventions, making this area more complex and challenging than VM. As a result the PdM area is much less developed than VM, albeit significant progress has been made in the last decade. For example:

- in Rying (2001) a *wavelet*-based approach has been used to identify important features for detection of process faults;
- in Pampuri et al. (2011a) *survival models theory* is employed for the same goal;
- *regression methods* have been employed also in this area; linear approaches, such as Ridge Regression and Elastic Nets, have been used in Susto et al. (2012c), while NNs have been adopted for modeling in Wu et al. (2007);
- *Filtering and Prediction* techniques, like Kalman Predictor and Particle Filters, have also been recently employed in PdM for semiconductor manufacturing processes in Butler and Ringwood (2010); Schirru et al. (2010b) and Susto et al. (2011a);
- *Classification Methods*, more specifically, Support Vector Machines have been considered in Baly and Hajj (2012).

Given all the various methodologies it can be understood how PdM topics are so different one from each other and every new PdM problem should be studied separately with a customized solution.

The PdM problems usually suffer, even more than the VM ones, from the *lack of a sufficient amount of observations* to prepare a reliable statistical model: this is due to the fact that the maintenance interventions are of course in far fewer than the number of measured wafers (observations for VM problems). For this reason, it is of paramount importance in the modeling to exploit the information coming from similar processes/equipments. This concept has been adopted in Susto et al. (2012b) with the employment of Multi-Task techniques.

Another major issue is represented by the *non-trivial evaluation of the impact of a PdM* in an industrial environment and the comparison of the performance of a PdM system versus a R2F/PvM approaches. In Susto et al. (2012c,a) the performances of the proposed PdM systems are evaluated in terms of two indicators:

(1) *type I error* - number of not prevented maintenances N_{UB};
(2) *type II error* - number of process iterations that may have been performed if the maintenance interventions suggested by the PdM systems would not have been performed N_{BL}.

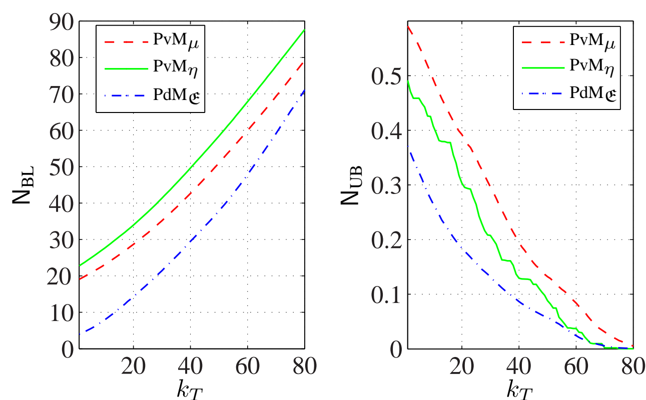

Fig. 3. The performances of two PvM systems (PvM$_\mu$ and PvM$_\eta$) versus the ones of the PdM system PdM$_\mathcal{E}$ as a function of the threshold k_T. Taken from Susto et al. (2012c).

Based on the costs associated with the two errors, the maintenance system can be tuned to be more or less reactive: in the example reported in Fig. 3 the tuning is done through the choice of scalar parameter k_T, see Susto et al. (2012c) for details. Clearly this performance evaluation can only be done on R2F dataset and this is a huge limitation. Not only that, but before adopting a PdM approach instead of a PvM, the costs associated with the lack of planned scheduling should be taken into account, see Susto et al. (2012c).

5. FAULT DETECTION AND CLASSIFICATION

Fault Detection and Classification (FDC) methods have been widely applied in the past years (Adamson et al. (2006); Moore et al. (2006); Schirru et al. (2010a).) In contrast to PdM techniques, an FDC system does not predict the future behavior of the tool/process, but, in the case of a fault, aims to identify the root cause of the abnormal behavior. This is of particular interest in the everyday work of a semiconductor plant: the root causes of faults in a complex process may be dozens, sometimes hundreds, and even expert process engineers have difficulty understanding the pathology and, therefore, how to properly cope with the faulty process/tool.

Sometimes PdM modules/approaches are based on FDC systems and this is the reason why FDC is sometimes a misused word for PdM; in Goodlin et al. (2003) for example the PdM module constantly monitor the FDC results as a sort of HF. In that work the FDC system simultaneously detects and classifies different faults from different *control charts*. Another work where control charts

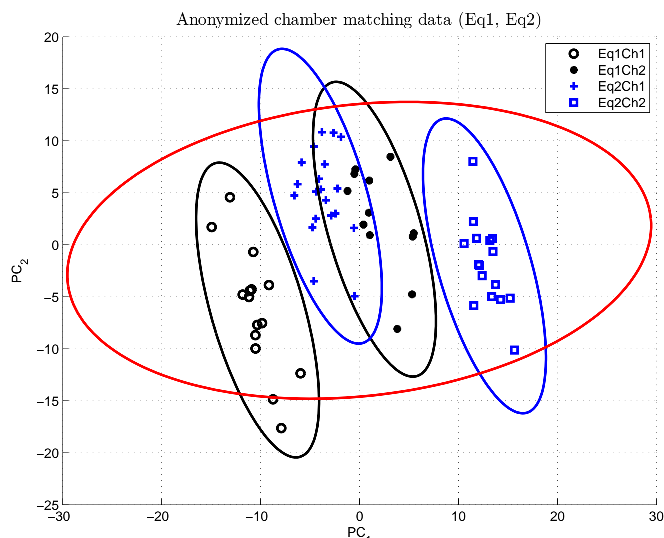

Fig. 4. Figure taken from Schirru et al. (2010a). The ellipses represent the confidence intervals for single chambers and intra-chambers: this enables a double level of monitoring of the process under examination.

are used for defining a FDC system is Schirru et al. (2010a), where chamber matching is obtained with multi-level linear models (see Fig. 4).

The FDC modules usually employ *classification* techniques, Hastie et al. (2009); for example *K-Nearest-Neighbour (kNN)* in He and Wang (2007), *Principal Component-based kNN* in He and Wang (2010) and *Support Vector Machines (SVMs)* in Sarmiento et al. (2005).

FDC systems are affected by some of the same data challenges described for VM and PdM: lack of observations, huge data fragmentation, high-dimensionality, multi process causes. A common problem for FDC and PdM is usually the lack of structured data for maintenances; usually faults and corrective actions are recorded manually by process/maintenances engineers and the resulting lists are incomplete or the same maintenance or fault cause may be indicated with different names. This, and several other problems not cited in this paper, underline how, to be successful in the work of applying machine learning and control methods to semiconductor manufacturing, it is of paramount importance to closely collaborate with people in the industry to understand the problem and the complexity of the datasets.

6. RUN-TO-RUN CONTROL

Run-to-Run (R2R) has become the standard approach for process control in Semiconductor plants (Boning et al. (1996); Toprac et al. (1999)) in the last decades. Despite its simplicity, R2R control presents several advantages such as improved process and device performance, decreased tool downtime, improved process throughput, reduction of defective wafers and early detection of process drifts (Anderson and Hanish (2007)).

R2R techniques are based on physical measurements of quality parameters (such as layer thickness or Critical Dimensions). Considering the common sampling practices of measuring a small number of wafers for each lot (usually 1 out of 25 wafers), it is apparent why R2R controllers operate on a Lot-to-Lot (L2L) control policy that allows for corrective actions to be taken at lot level (Toprac et al. (1999)). R2R controllers are generally implemented through EWMA-based algorithms, see Chen and Guo (2001).

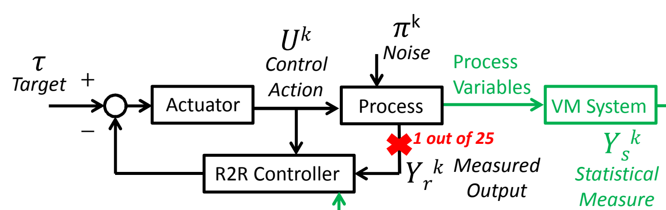

Fig. 5. R2R control scheme with Physical and VM (statistical) Measures.

With the development and adoption of VM systems in recent years, this scenario has changed as control systems have the possibility of incorporating this new information source in their calculations. The presence of statistical measurements for each wafer and the reduction of physical measure should be taken into account when implementing a control strategy. In Fig. 5 a qualitative block scheme for R2R controllers with VM module in the loop is depicted.

In Cheng et al. (2008) and Susto et al. (2012d) VM and physical measurements are treated differently depending on their probabilistic distributions, with different approaches. This research topic is however in its infancy, largely because VM has only become a well established technology in the last few years.

7. CONCLUSIONS

An overview on the major applications of machine learning and automatic control for semiconductor manufacturing have been presented. This is a challenging research area of growing interests; as explained in Section 3.2, 4.2, 5 and 6 several of the problems of this area are still open or have just been recently tackled.

Several other APC works (for example Vincent et al. (2011) and Prakash et al. (2012)) in the area of statistical modeling/automatic control that cannot be included in the categories of Virtual Metrology/Predictive Maintenance/Fault Detection/Run-to-Run have been presented in recent years underlying the extents of the possibilities of machine learning and control systems in semiconductor manufacturing.

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