Using large signal S-parameters to design low power class-B and class-C CMOS cross-coupled voltage controlled oscillators.

Wykorzystanie wielkosygnalowych parametrow S do projektowania generatorow VCO niskiej mocy w technologii CMOS pracujacych w klasie B i klasie C.

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Abstract: This article presents a method for design of cross-coupled LC oscillators using open-loop technique and large signal scattering matrix parameters (S-parameters) in place of well known and established negative resistance approach. Thanks to the open-loop methodology, the main circuit parameters such as loaded quality factor, steady-state oscillation amplitude and signal frequency under large signal regime can be extracted without, often tedious and time consuming, transient simulations. The most important aspect of the proposed method is its ability to provide relatively simple and intuitive representation of a cross-coupled oscillator under changing bias conditions, with 10% accuracy in comparison to analysis in time domain. The presented methodology is not technology specific, however CMOS was chosen due to its availability, relative low cost and popularity of circuit implementation. The article shows two low power, sub-1 V voltage controlled oscillator prototypes, one operating in class-B, the other one in class-C, designed using the described method and operating under the reduced power supply requirements yet retaining a state of the art Figure of Merit (FoM) of various VCO reported in the literature.
Keywords: CMOS voltage controlled oscillators, open loop analysis, large signal S-parameters.

Streszczenie: Artykuł prezentuje metode projektowania oscylatorów wzajemnie sprzężonych przy użyciu wielkosygnałowych parametrów rozproszenia (macierzy S) w otwartej pętli, w przeciwieństwie do ogólnie stosowanej metody ujemnej rezystancji. Przedstwione podejście pozwala na analizę takich parametrów jak dobroć, amplitudę drgań w stanie ustalonym oraz częstotliwość drgań przy wymuszeniu wielkosygnałowym. Zaprezentowana metoda nie jest zależna od użytej technologii, jednak ze względu na dostępność i poplularność, wyniki pokazane są przy użyciu procesu CMOS. Artykuł prezentuje dwa prototypy oscylatorów zasilanych niskim napięciem, poniżej 1 V, pracującymi w klasie B i klasie C. Pomimo zmniejszonego poboru mocy, zparezentowane układy plasują się na równi z czołowymi układami tego typu przedstawionymi w najnowszej literaturze.
Słowa kluczowe: Generatory CMOS sterowane napięciem, analiza ukłdów z otwartą pętlą, wielkosygnałowe parametry S.

Introduction.

Low power consumption and stringent phase noise requirements for LC oscillators operating in modern wired and wireless systems, pushes the designs close to the technology limits. It is even more challenging to design a high-performance RF circuit operating under limited voltage headroom, nowadays a typical scenario for battery operated systems implemented using deep-submicron, cost effective technologies as CMOS. All of the above can lead to serious performance trade-offs in oscillators, that have to be accounted for at early stages of the design process.

From a perspective of battery operation, power consumption of an oscillator can be improved recognising that the circuit requires less energy to sustain oscillations than to start them. This can be explained using a mechanical example of a revolving doors. When the door are stationary, a person willing to pass, have to push to overcome friction between bearings and a central shaft. Once the door are set in motion only a fraction of initial energy is required to sustain the movement as the revolving mechanism conserves some of it in form of a kinetic energy. When external forces are no longer applied, the door will stop after some time as the energy will be dissipated by friction.

The same rule applies to CMOS LC oscillator depicted in Figure 1. This is a classical low voltage headroom cross-coupled VCO architecture considered throughout this article, with a single differential planar inductor (formed by *L*1, *L*2), the tank capacitance being a combination of MIM capacitor and MOS varactors, and NMOS pair forming a differential amplifier for the compensation of energy losses in the resonator. The electrical energy is stored by a electromagnetic field through the use of the inductor and capacitors and dissipated by resistive components of the circuit (in form of losses not depicted here). Once the oscillator signal becomes stable i.e. it reaches a steady amplitude after circuit start-up, the amount of power required to sustain the oscillations can be reduced as long as a circuit losses are not excessive. If a supply voltage is kept constant, this can be obtained decreasing of DC bias voltage of transistors operating as amplifiers in the oscillator circuit. Therefore the transistors conduct less current and for a shorter amount of time, resulting in lower RMS power levels drawn from the supply (RMS form of power description is the most convenient way of comparing powers of periodic signals of various shapes) within one oscillation period.

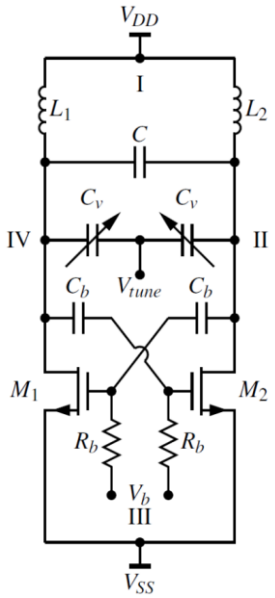

Fig. 1. Low voltage LC CMOS VCO.
Rys. 1. Niskonapięciowy generator VCO w technologii CMOS.

Being a rather trivial solution, the described DC bias change after the oscillator reached its steady-state complicates the design procedure. In case of CMOS cross-coupled LC oscillator circuit, typical approach to oscillator design requires transistors in the oscillator core to be biased with DC current to produce negative conductance used to compensate resonator losses. If both MOS transistors become biased in or below cut-off points (class-B; *Vgs=Vth*, class-C; *Vgs<Vth*, respectively) they don't produce any negative conductance as their respective transconductances are equal to zero. In this case the transistors are periodically switched on and off only by the signal generated in the oscillator. Also, because oscillators designed using negative conductance approach are always closed-loop systems (negative resistance in transistor circuits requires feedback), it is impossible to observe how the loaded quality factor of the circuit changes with bias conditions, and how it affects the phase noise performance of the oscillator. When the negative conductance approach to the oscillator design becomes no longer practical, a feedback analysis can be used instead, even if the original circuit of interest is not normally considered to be a feedback oscillator [1-3]. This paper presents a new methodology of cross-coupled oscillator analysis and design based on two techniques known as Alechno virtual ground circuit transformation [1] and Randall-Hock open loop gain correction [2,3].

2. Open loop analysis of a cross-coupled LC oscillator.

A. Oscillation criteria.

The feedback approach to oscillator design relies on two important parameters: open loop gain and phase response of the loop. As depicted in Figure 2, a feedback oscillator consists of generic transconductance block, where the output is sampled back to the input. Under certain conditions, this circuit has the potential to become unstable if for zero input excitation $X_{in}(j\omega)$ the output response $Y_{out}(j\omega)$ becomes non-

zero. These conditions are widely known as Barkhausen's criteria and can be derived by analysis of the closed-loop gain of circuit from Figure 2:

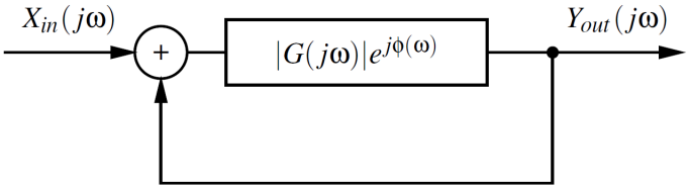

Fig. 2. Generic feedback model of an oscillator.
Rys. 2. Ogólny model generatora ze sprzężeniem zwrotnym.

$$\frac{Y_{out}(j\omega)}{X_{in}(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega)} \tag{1}$$

$$|G(j\omega)| = 1 \rightarrow \text{Amplitude condition} \tag{2}$$

$$\varphi(\omega) = 2k\pi \text{ for } k = 0, 1, \ldots \rightarrow \text{Phase condition} \tag{3}$$

that is the system has unity open loop gain *G(jω)* and the total phase shift of the open loop equals zero (or multiple of 2π). The phase *φ(ω)* of open loop leads to a loaded quality factor Q_L is described by:

$$Q_L = -\frac{\omega_0}{2}\frac{\partial\varphi(\omega)}{\partial\omega}\bigg|_{\omega=\omega_0} \tag{4}$$

It is worth noting that amplitude and phase conditions (2) and (3) must not be treated as criteria defining instability of the circuit *per se*. When the open loop gain is larger than one (during oscillator start-up), a non-zero output requires finite input stimulus $X_{in}(j\omega)$ typically provide by thermal noise
and power supply transients in the circuit. Periodic signal can subsequently build up if (1) has a pair of complex conjugate poles placed in the right hand side of the complex plane. Thus, the presented Barkhausen criteria indicate only a boundary for which the amplitude and frequency of the oscillations become constant. For these reasons, in this paper we assume *a priori* that the circuit is potentially unstable when its open loop gain is larger than one and the transfer function has a pair of complex poles.

B. Loop identification.

Having (2)-(4) at hand, one is able to analyse the oscillator, providing that the feedback loop around the circuit can be recognised. In many negative conductance oscillators the loop is usually obscured and circuit transformations have to be employed to define it. One of methods, Alechno technique [1], allows one to rearrange an oscillator circuit by introducing a virtual ground in one of the nodes that under normal operation is not grounded, a signal output for example. In cross-coupled oscillator, this transformation becomes essential as its amplifier operates in a differential mode. When circuit parameters are thus extracted using single ended ports, the ports have to be referenced to a different potential than electrical ground of the circuit to capture the behaviour of the differential phenomena.

Alechno transformation results in a circuit rearrangement where the feedback loop can be easily recognised and analysed as such. The method has limitations. As the arrangement of circuit parasitics has been changed, their influence on the resonant frequency of the oscillator may be affected [2]. However, if the parasitics are much smaller than the LC components, the resulting mismatch with practical circuit is acceptable. Applying Alechno transformation to the circuit from Figure, yields an open loop equivalent presented in Figure 3.

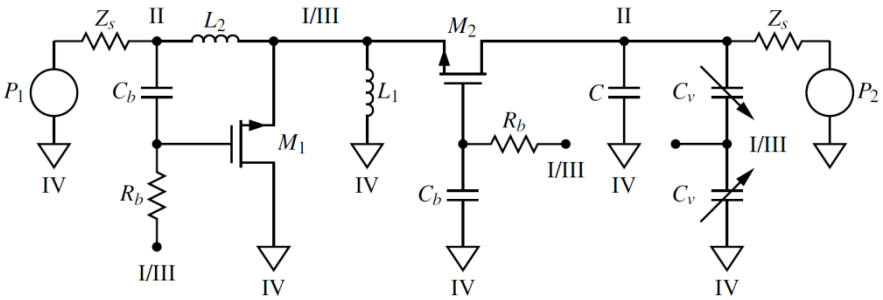

Fig. 3. Open loop model of cross-coupled CMOS VCO. Bias not shown.
Rys. 3. Model generatora VCO w technologii CMOS. Pominięto układ zasilania.

Roman numerals on both figures correspond to the same nodes in both circuits. Note that there are two loops present in the network. The main loop is formed between drain of *M*2 and gate of *M*1, and the second one, made of the inductors around *M*1 and its parasitic capacitances. In general, the LC-*M*1 loop can also become unstable, however normally at much higher frequency. Thus only in a presence of *M*2 the proper Barkhausen's criteria for the main loop can be defined. This is due to the fact that in practical situations, the oscillation conditions (2)-(4) for both loops are much different. The loop has been opened between the two transistors, creating an open loop cascade at node II, with respective ports P1 and P2. The transformation has been conducted in steps. First, all of the points at RF ground have been connected together (*Vdd*, *Vss* and *Vb*). Then, the outputs at node IV has been connected to the virtual ground, leading to a single feedback loop between *M*1 and *M*2 with a single reference to the virtual ground. After transformation, both transistors have to be DC biased through set of blocking capacitors and RF chokes, omitted from Figure 3 for clarity. Equations (2)-(4) can be calculated using two port network S-parameter analysis in any RF circuit simulator. We have recognised for the first time that since an oscillator operates under a large signal regime, large signal S-parameters are the most suitable for the characterisation. Small signal behaviour can be still extracted, provided that relatively low magnitudes of test signals are applied.

C. Gain correction.

The last important step of the analysis is a correction of calculated results due to unmatched impedances between the circuit ports *Zs* and the test generators. In theory, during circuit simulation, the corresponding reflection coefficients on each port could be found and then used to calculate the proper test generator impedances. However this process is tedious, especially if the bias conditions change (as in the case of a class-B and class-C oscillators). It is then more practical to use Randall-Hock correction of open loop gain accounting for unmatched port impedances [2,3].

$$G_{corr}(j\omega) = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}} \tag{5}$$

where S_{ij} represent large signal S-parameters defined for the two ports respectively using test sources. The corrected gain formula (5) allows to estimate (2)-(4), at the same time capturing small and large signal behaviour of an open loop cascade depicted in Figure 3.

3. Class-B and class-C oscillator designs.

Using the circuit presented on Figures 1 and 3, together with UMC 130 nm RF process libraries (*Vth*=400 mV), two low power CMOS oscillators has been designed. In steady-state, first circuit operates at 5 GHz with a class-C bias (*Vb*<*Vth*) [4], the second design is a class-B VCO with centre frequency of 10 GHz (*Vb*=*Vth)* [5]. The most important of circuit parameters are presented in Table 1. The loaded quality factor values for both resonators average around 10 at resonant frequencies of 5 GHz and 10 GHz, respectively. In each VCO, gates of both transistors are biased through DC block capacitor C_b and high resistance RF resistor, forming RF block to ground. In both cases, cross-coupled pair is formed using minimum length devices. As the circuits are intended to operate well under 1 V and with a limited headroom, no current source was used, allowing for relatively large output signal swing, in the range of *Vdd*, especially important if output stages in form of CML frequency dividers are to be used. In the case of class-B VCO, steady state *Vdd* is decreased in order to further reduce oscillator power. Class-C oscillator was designed for even smaller power consumption, where *Vdd* is kept as low as 350 mV. Oscillators produce two out-of-phase sinusoidal signals at nodes II and IV respectively, that in the practical circuit have to be extracted through the buffer amplifiers, not included in this article. To account for parasitic capacitances of layout and buffer amplifiers, two 0.15 pF capacitors were included in the circuits, connected in parallel between nodes II-III and IV-III, respectively.

4. Simulated results.

Open loop oscillator circuit from Figure 3 has been co-simulated in Eldo RF and MATLAB for separately for class-C [4] and class-B [5] bias schemes. Large signal steady state (SST) simulation allows to extract scattering parameters matrix of interest as function of frequency and port amplitude. When the correction algorithm (8) is employed, a real source impedance of 50 Ω can be used directly. To achieve good accuracy, SST has been set to 11 harmonics.

Parameter	5 GHz Class-C		10 GHz Class-B		Comments
	Dimensions	Value @ 5 GHz	Dimensions	Value @ 10 GHz	
L_1+L_2	OD=220 µm, W=9.7 µm, S=1.6 µm, NT=2	1,4 nH, Q=19	OD=116.5 µm, W=9.7 µm, S=1.6 µm, NT=2	0.5 nH, Q=22	Differential inductor
C	W=0.2 µm, L=20 µm, NF=10, M=4, nm=5	440 fF, Q=50	W=0.2 µm, L=20 µm, NF=10, M=4, nm=5	220 fF, Q=47	MOM RF
C_v	W=2.54 µm, L=0.25 µm, NF=6, M=5	221.3 fF, Q=40-80	W=2.54 µm, L=0.25 µm, NF=6, M=5	210 fF, Q=30-100	MIS RF
M_1, M_2	W=1.2 µm, L=0.12 µm, NF =5, M=6	-	W=1.2 µm, L=0.12 µm, NF =7, M=4	-	RF
C_b	W=0.2 µm, L=20 µm, NF=40, M=5, nm=5	2 pF, Q=50	W=0.2 µm, L=20 µm, NF=40, M=5, nm=5	2 pF, Q=47	MOM RF
R_b	W=1 µm, L=7 µm, M=1	7 kΩ	W=1 µm, L=7 µm, M=1	7 kΩ 500 mV	RF
Start-up Vdd	-	350 mV	-	500 mV	
Steady state Vdd	-		-	400 mV	
Start-up Vb	-	500 mV	-	500 mV	
Steady state Vb	-	350 mV	-	400 mV	

Tab. 1. Design parameters of proposed VCOs.
Tab. 1. Parametry proponowanych generatorów VCO.

A. Class-C VCO.

During start-up, the circuit is biased with *Vb* = 500 mV, initially consuming RMS power of 0.82 mW from 350 mV supply voltage. When oscillator reaches steady state, the power consumption increases to 0.94 mW RMS. The increased power consumption can be attributed to two factors. Firstly, large signal swings influence voltage controlled parasitics of the transistors, such more current is drawn by them during operation of the oscillators. Secondly, because drain currents of cross-coupled pair in any LC oscillator have a form of short pulses, they introduce harmonics on top of DC signal required for bias. Thus, in steady state some additional power from the source is transferred into the harmonics. Figures 4 and 5 present the results of gain and phase calculations of corrected open loop transfer function, *Gcorr*(*jω*). When the signal amplitude of the test sources is small, in the range of 30 µV, the circuit provides gain margin of approximately 8.44 dB at frequency of 4.82 GHz where phase shift around the loop is 0, Figures 4 and 5.
This rather excessive gain margin during start-up is due to size of the transistors used. When in class-C the same devices have to deliver narrow current pulses yet with enough amplitude to compensate the total resonator losses and finite output conductances of cross-coupled pair. When the same transistors are biased, such a DC current flows through them (i.e. during oscillator start-up), the drain currents in the range of 1.2 mA introduce the open loop gain of 8 dB.

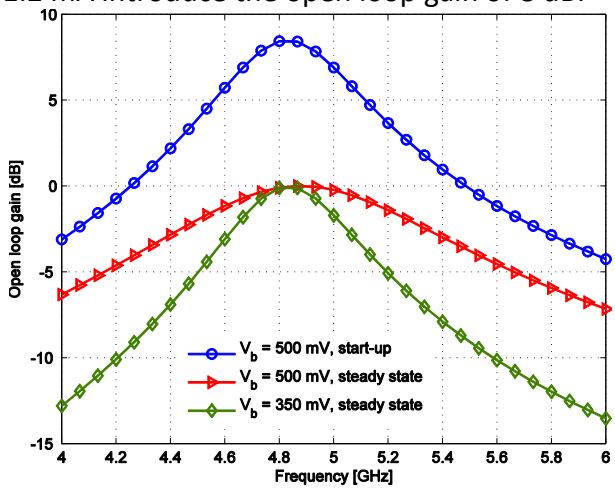

Fig. 4. Open loop gain of class-C VCO.
Rys. 4. Wzmocnienie otwartej pętli generatora VCO pracującego w klasie C.

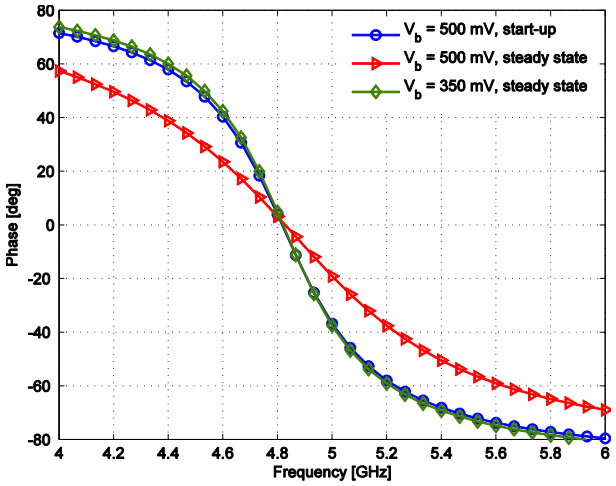

Fig. 5. Open loop phase of class-C VCO.
Rys. 5. Charakterysyka fazowa otwartej pętli generatora VCO pracującego w klasie C.

Figure 5 shows that the resonant frequency of the open loop cascade is only 5% lower than of the closed loop case, approximated from transient analysis to be equal to 5.08 GHz. When signal amplitude rises, the

non-linearities of both transistors cause compression of gain, until it's margin drops to 0 dB. This is the moment when oscillator reaches its steady state. To observe this behaviour, the amplitude on both ports of open loop cascade has to increase from initial small signal value to 470 mV.

Under large signal conditions, a loaded quality factor of the oscillator, as depicted on Figure 6, drops by 50% from its initial value of 9.4 down to 4.71. This can be explained by instantaneous drain current increase during switching, effectively increasing drain to source conductances in both transistors and present higher load to the resonator.

In the last case Figures 4-6 show steady state response of the same oscillator where the bias conditions has been modified. Both transistors are now biased as class-C devices and *Vb* = 350 mV for *Vth* = 400 mV. Less power drawn from the source reduces the amount of current in the circuit, resulting in smaller oscillation amplitude. When the oscillator operates in class-C, the voltage amplitude on both ports necessary to decrease the open loop gain to 0 dB is close to 250 mV. The transient simulation conducted to compare these results showed the signal with amplitude of 268 mV, that is 7% larger than found using the open loop technique. The main source of this error comes from the use of varactors, that are inherently non-linear, and therefore introducing additional set of amplitude dependant parasitics that are distributed differently in the closed and open loop circuits. Although in the case of class-C bias scheme a generated RF amplitude is smaller, the transistors stay "on" for shorter period than during start-up, effectively reducing a loading presented to the resonator. This manifests itself in a improvement of loaded quality factor, that as depicted in Figure 6, now much closer to the value of original, unloaded tank.

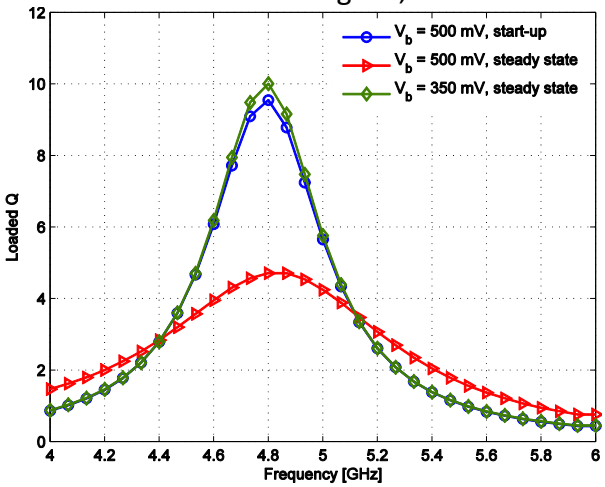

Fig. 6. Loaded quality factor of class-C VCO.

Rys. 6. Dobroć pod obciążeniem dla generatora VCO pracującego w klasie C.

B. Class-B VCO.

Similar methodology has been employed to design a 10 GHz, class-B oscillator [5]. The gates of both transistors in cross-coupled pair were biased such *Vb* = 500 m*V*. When the signal amplitude of the test sources is small (*Pin* =−80 dBm, *Vin* = 30 µV), the circuit provides gain margin of approximately 7 dB at frequency of 9.9 GHz where phase shift around the loop equals 0, Figures 7 and 8. As in the case of class-C prototype, an excessive gain margin during start-up is due to the size of transistors used to operate with reduced power in steady state.

In steady state, the frequency of oscillations increased to 10.2 GHz as a result of large voltage swing through non-linear LC resonator with varactors. As quality factor of the tank is low, drain current pulses delivered by both transistors cannot be translated into a pure sinusoidal voltage by such LC resonator. This introduces a non-zero mean (DC shift) voltage in the output signal, reducing a varactor capacitance and results in higher oscillation frequency. This behaviour is not seen in class-C prototype as 150 mV difference in supply voltages (and varactor bias) between circuits reduces this effect. Under large signal conditions, a loaded quality factor of the oscillator, as depicted on Figure 9, drops by 50% from its initial value of 10 down to less than 5 due to the same mechanism as in class-C VCO.

When both transistors are biased as class-B devices and *Vb*=*Vdd*=*Vth*=400 mV, less power is drawn from the source and this the voltage amplitude on both ports necessary to decrease the open loop gain to 0 dB is close to 450 mV. The transient simulation of to complete oscillator circuit conducted to compare these

results showed the signal with amplitude of 370 mV. The main source of this error comes from the placement of varactors at port P2 and introduction of additional set of amplitude dependant parasitics, distributed differently between the closed and open loop circuits. When varactors were moved to port P1, the results in the range of few percent difference between SST and transient simulations can be obtained. This shortcoming of high nonlinearity placement along the cascade has not been indicated previously by Randall and Hock [2].

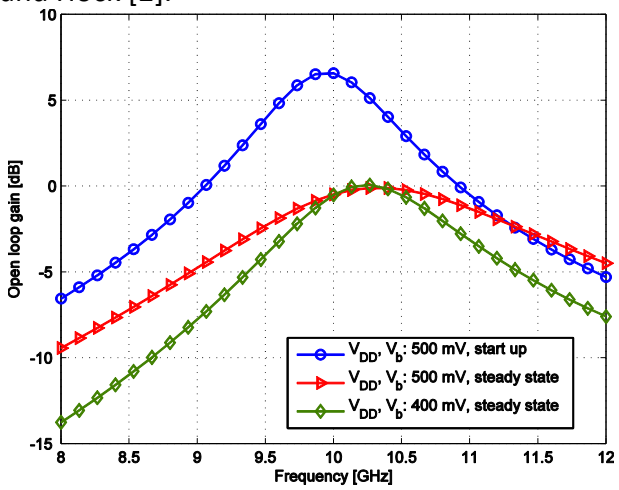

Fig. 7. Open loop gain of class-B VCO.
Rys. 7. Wzmocnienie otwartej pętli generatora VCO pracującego w klasie B.

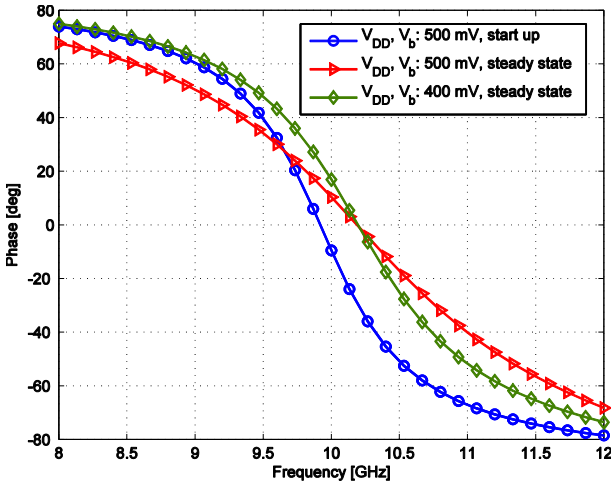

Fig. 8. Open loop phase of class-B VCO.
Rys 8. Charakterysyka fazowa otwartej pętli generatora VCO pracującego w klasie B.

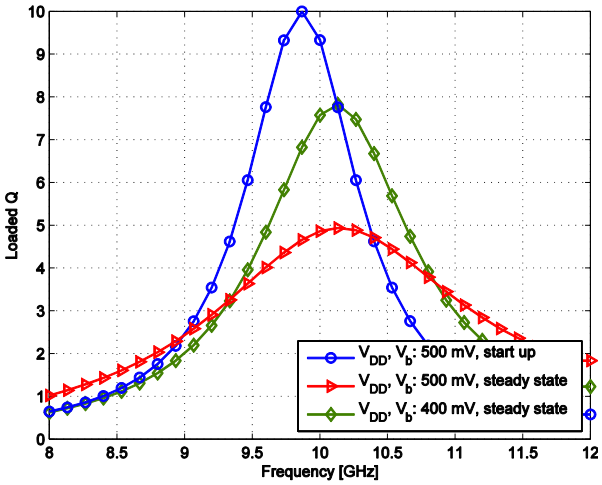

Fig. 9. Loaded quality factor of class-B VCO.
Rys. 9. Dobroć pod obciążeniem dla generatora VCO pracującego w klasie B.

As before, an improvement of loaded quality factor in steady state is observed, as depicted in Figure 7. One can think that the *QL* increase should immediately translate into smaller phase noise, however in the case of class-B and class-C oscillators this mechanism is not straightforward. Firstly, relatively short current pulses consist of larger number of spectral components that are responsible for noise folding in the oscillators [6]. Secondly, the proposed class-B and class-C VCOs operate under smaller RMS power and generate smaller amplitudes that may not necessarily translate into an improved phase noise performance.

C. Phase noise and figure of merit comparison.

To compare the performance of various oscillators, a normalized parameter known as figure of merit with tuning range (*FOMT*) can be used. This function allows fair benchmark of phase noise of oscillators working at different frequencies, tuning ranges, fractional bandwidths and power consumption. One generally accepted *FOMT* has the following form:

$$FOMT = L(f_m) + 20\log_{10}\left(\frac{f_m}{f_0}\cdot\frac{FBW}{10}\right) + 10\log_{10}(P) \qquad (6)$$

where $L(f_m)$ is phase noise at frequency offset of f_m, f_0 is resonant frequency, *FBW* is fractional bandwidth of the carrier and *P* is a maximum DC power consumption of the core expressed in mW. Since the presented class-B and class-C oscillators do not consume power in a static sense, (6) is modified such a RMS power is taken into account instead. Table 2 presents a performance comparison of realised state of the art class-C VCOs presented in the literature.

Even though the results presented in this paper are simulated, there is still 5 to 7 dB safety margin of theoretical FOMT in comparison to the VCOs with tuning ranges below 10%. Authors of [9] and [10] employed switched capacitor or varactor arrays, effectively increasing FOMT over a single varactor solution presented in this paper by the cost of the chip area, not included in the comparison.

Ref	CMOS	VDD	f0	fm	L(fm)	FBW	P	FOMT
	µm	V	GHz	MHz	dBc/Hz	%	mW	dBc/Hz
[7]	0.18	1.2	4.84	1	-125	2.1	3.4	-180
[8]		0.2	4.5	1	-104	1	0.114	-166
[9]		1	3.1	1	-123	20	1.57	-197
[10]	0.13	1	5.2	3	-131	14	1.4	-197
[11]	0.09	0.6	5.1	3	-127	2.6	0.86	-181
Class-C	**0.13**	**0.35**	**5**	**1**	**-115**	**5.6**	**0.5**	**-187**
Class-B		**0.5/0.4**	**10.2**	**1**	**-110**	**7.5**	**1.3**	**-186**

Tab. 2. Performance comparison between state of the art class-C CMOS VCO and the proposed circuits.

Tab. 2. Porównanie generatorów VCO w technologii CMOS pracujących w klasie C z zaproponowanymi układami.

5. Conclusion.

In this paper we have presented a new analysis and design methodology of class-B and class-C cross-coupled CMOS oscillators. The use of open loop approach and large signal S-parameter simulations allow to estimate oscillation amplitude and load quality factor of the circuit, and subsequently optimise it if necessary for low phase noise and low power operation. The obtained results match simulations of complete VCO circuits, confirming that the proposed open loop technique provides a simple and intuitive yet effective tool improving the design of high performance, low voltage CMOS oscillators as the one presented in this paper.

Acknowledgements.

This material is based upon works supported by the Science Foundation Ireland under Grant No. 10/CE/I1853. The authors gratefully acknowledge this support.

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