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Research Article

Study of Linearity and Power Consumption Requirements of CMOS Low Noise Amplifiers in Context of LTE Systems and Beyond

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This paper presents a study of linearity in wideband CMOS low noise amplifiers (LNA) and its relationship to power consumption in context of Long Term Evolution (LTE) systems and its future developments. Using proposed figure of merit (FoM) to compare 35 state-of-the-art LNA circuits published over the last decade, the paper explores a dependence between amplifier performance (i.e., combined linearity, noise figure, and gain) and power consumption. In order to satisfy stringent linearity specifications for LTE standard (and its likely successors), the paper predicts that LNA FoM increase in the range of +0.2 dB/mW is expected and will inevitably translate into a significant increase in power consumption—a critical budget planning aspect for handheld devices, active antenna arrays, and base stations operating in small cells.

1. Introduction

Long Term Evolution (LTE) is a next generation communication standard developed by 3rd Generation Partnership Project (3GPP) [1], allowing a high data rate transmission over radio interface. It represents a natural progression from voice transmission systems as GSM through UMTS (with increased spectral efficiency for data transmission) to data transmission scheme, where the majority of system throughput is used for high quality audiovisual streaming, internet access, file sharing, and gaming, with peak downlink bandwidths in excess of 100 Mbps [2].

Such a dramatic increase in data throughput corresponds to proportional increase in either a bandwidth (BW) or signal to noise ratio (SNR) or both at the same time. Both quantities cannot be made arbitrary high. SNR is a function of maximum transmitted power allowed for the system, distance to the receiver, and modulation scheme, and these parameters are usually optimised for the transmission. BW is controlled by the availability of a radio spectrum allocated for the system and, to certain extent, more bandwidth can be assigned to increase channel capacity if needed (providing that there is enough amount of unoccupied bandwidth left). Nowadays, the number of various wideband radio systems coexisting with LTE is significant and as a result, the radio spectrum has become relatively congested. For example, 3GPP specifies LTE frequency separation between frequency-division duplex (FDD) uplink and in the range of 45–400 MHz or even smaller distance (for time-division duplex (TDD) transmission bands) [1].

From a radio receiver perspective, in order to prevent unwanted signals from reaching processing stages, small frequency separation between bands imposes high selectivity (or signal rejection). Historically, the most practical one has been the use of high quality factor preselection filters (duplexers in transceivers) after the antenna; however in context of the wideband operation of LTE system, this approach becomes less practical. Since LTE transceivers operate in UHF band, 0.7–2.7 GHz (note that the range is not continuous), it is impossible to design a single RF preselection filter that is simultaneously wideband and has high roll-off

characteristics and its centre frequency can be tuned to any band of interest.

When high performance wideband filter is not available, together with a wanted signal, radio receiver detects and tries to process many unwanted components of the spectrum, in most cases having an average power much larger than that of the signal of interest. This would not present a serious problem if the receiver was a completely a linear system (also not limited by maximum power supply voltages and currents), having ability to process signal of any strength with constant performance. In practice, however, the receiver subcircuits consist of number of transistors and the relationship between input and output is nonlinear.

As a result, all of the unwanted signals in the receiver cross-modulate into wanted frequencies, dramatically reducing the effective SNR and transmission throughput. Nonlinearities also reduce gain of a wanted signal through two mechanisms known as *compression* and *blocking*, reducing SNR of received signal even further. Thus, in order to mitigate problem of the destructive interference, special care has to be taken to design a receiver system with high linearity, especially where a preselection filtering is far from ideal.

This paper addresses the question of how high linearity levels of LNA have to be to satisfy LTE requirements for given SNR and what is a possible power penalty for achieving this goal, providing a vital information on how much power has to be budgeted for an RF receiver front-end design. Linearity and power relationship is important not only for battery operating systems as handsets but also for base stations in femto-, pico-, and metro-cells, operating with reduced power budget and multiple receivers. To our knowledge, a presented study on LTE linearity performance in relation to various CMOS LNA designs and its power budgets has not been conducted before.

This paper is organised as follows. Section 2 introduces fundamental aspects of amplifier linearity together with the corresponding metrics. Section 3 describes three basic linearization techniques used in many state-of-the-art LNA designs, with special emphasis on power consumption. Using system specification from 3GPP, the linearity requirements for LTE receiver are derived in Section 4, whereas Section 5 discusses their impact on both standalone LNA circuit and RF front-end design. Finally, Section 6 introduces a figure of merit function that enables fair comparison between different published state-of-the-art CMOS LNA circuits. Also we formulate a prediction of relative power supply levels necessary for future designs of LTE-compatible and beyond for integrated RF LNAs.

2. Amplifier Linearity Analysis

2.1. Taylor Series Description of Soft Nonlinearity. Circuits utilising transistors are characterised by a nonlinear relationship between their inputs and outputs. The main source of this behaviour comes from the features of semiconductor materials, where electrical properties are strongly dependant on electrical potential energy. In general, transistors are used as switches and/or amplifiers (or more precisely transducers providing some form of proportional transformation between voltages and currents). When used as an amplifier, MOS transistor can be characterised by a soft nonlinearity [3]; that is, one can find a polynomial of a finite order, sufficiently describing the nonlinearity within a limited range of input signal levels around certain bias point. In the simplest of cases, Taylor series defines such a polynomial; however when reactive components (e.g., transistor capacitances) become important, Volterra series approach is used instead [3]. As an example, consider a simple low voltage LNA transconductance amplifier in common source (CS) configuration, biased using a NMOS current mirror, depicted in Figure 1.

Inductors L_D and L_G have high impedance at frequency of interest; C_C capacitors provide AC coupling to a following stage connected to the LNA. Please note that for the following linearity analysis we assume that impedance matching, noise figure, and bandwidth are not critical. In practice all of these constraints have to be optimised simultaneously, which leads to a more complex relationship between parameters and circuit architecture. The output AC current of M_1 flowing through C_C can be described by the following polynomial:

$$i_o(t) = \sum_{k=1}^{\infty} g_k v_{\text{in}}^k(t) \approx \sum_{k=1}^{N} g_k v_{\text{in}}^k(t), \tag{1}$$

where g_k is kth coefficient of the polynomial, defined as

$$g_k = \frac{1}{k!} \frac{\partial^k i_{\text{out}}(V_0)}{\partial v^k}. \tag{2}$$

That is, g_k represents kth derivative of $i_o(t)$ in respect to the input voltage, for the device biased at certain DC point. Note that when the quiescent point of a soft nonlinearity changes, the coefficients described by (2) have to be recalculated. Typically, the infinite series given by (1) is well approximated by the first 3 to 5 elements, as g_k is inversely proportional to factorial of k.

Polynomial description reveals the effects of intermodulation, gain compression, and blocking taking place in a nonlinear amplifier. Using trigonometric identities and assuming that input voltage consists of two signals operating at different frequencies, we can show (for nonzero g_2 and g_3 coefficients)

$$v_{\text{in}}(t) = A \cdot \cos(\omega_1 t) + B \cdot \cos(\omega_2 t), \tag{3}$$

$$g_2 v_{\text{in}}^2(t) \propto g_2 AB \cdot \cos(\omega_1 t \pm \omega_2 t), \tag{4}$$

$$g_3 v_{\text{in}}^3(t) \propto \frac{3}{4} g_3 A^2 B \cdot \cos(2\omega_1 t \pm \omega_2 t), \tag{5}$$

$$g_3 v_{\text{in}}^3(t) \propto \frac{3}{4} g_3 A B^2 \cdot \cos\left(2\omega_2 t \pm \omega_1 t\right). \quad (6)$$

The output current (1) consists of many different harmonic components: these given by (4) are the second order intermodulation products, IM2, whereas (5) and (6) are known as the third order intermodulation products, IM3. Note that the magnitudes of IM2 and IM3 are proportional to A and B, and they increase much faster than the first order output terms given by

$$i_{o1}(t) \approx \left(g_1 A + \frac{3}{4} g_3 A^3 + \frac{3}{2} g_3 A B^2\right) \times \cos\left(\omega_1 t\right), \quad (7)$$

$$i_{o2}(t) \approx \left(g_1 B + \frac{3}{4} g_3 B^3 + \frac{3}{2} g_3 B A^2\right) \times \cos\left(\omega_2 t\right). \quad (8)$$

Equations (7) and (8) show that the transconductor output at ω_1 and ω_2 depends on amplitudes of both signals. Interestingly, for $g_3 < 0$, the output current $i_o(t)$ is reduced by large amplitudes of wanted input signal (gain compression) and the strong interference (known as blocking, AB^2, and BA^2 terms, resp.).

Formulas (4)–(8) are used as basic metrics for linearity analysis, known as *input intercept points* (IIP) [4, 5]. As mentioned previously, IM products amplitude increases faster than the amplitude of fundamental signal; therefore it is possible to find theoretical input amplitudes A and B for which the resulting IM products equalize with the fundamental. The second order (IIP2) and third order (IIP3) intercept points are, respectively, defined as [4, 5]

$$\text{IIP2} = \left|\frac{g_1}{g_2}\right|, \qquad \text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}. \quad (9)$$

Typically, values for IIP2 and IIP3 are much larger than the maximum voltages and currents allowed in the circuit. The intercept points are approximated by finding crossover points of the tangent lines from measurements of IM2, IM3, and fundamental response. As far as a linearity of LNA is concerned, the higher the IIP2 and IIP3, the better the performance of the amplifier. Note that RF literature and vendor datasheets typically express both intercept points in terms of power referred to 50 Ω. And this standard notation is followed in this paper.

2.2. IIP2 and IIP3 Analysis Example. As an example, consider large signal model of an UMC 130 nm NMOS RF transistor ($L = 0.12\,\mu$m, $W = 0.9\,\mu$m, NF = 4, $M = 1$, and $V_{\text{DD}} = 1.2$ V) operating in the LNA circuit from Figure 1. The polynomial coefficients (2) were obtained using Eldo RF simulator. Using (9) we can calculate IIP2 and IIP3 as function of gate bias voltage V_G for the amplifier in question. The results are depicted in Figure 2.

The presented curves show that there are three possible bias points for improved linearity, where IIP2 and IIP3 are at their respective maximums:

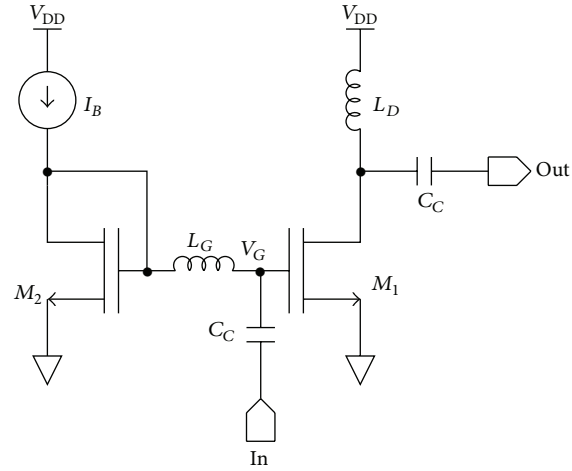

Figure 1: Simple low voltage transconductance LNA.

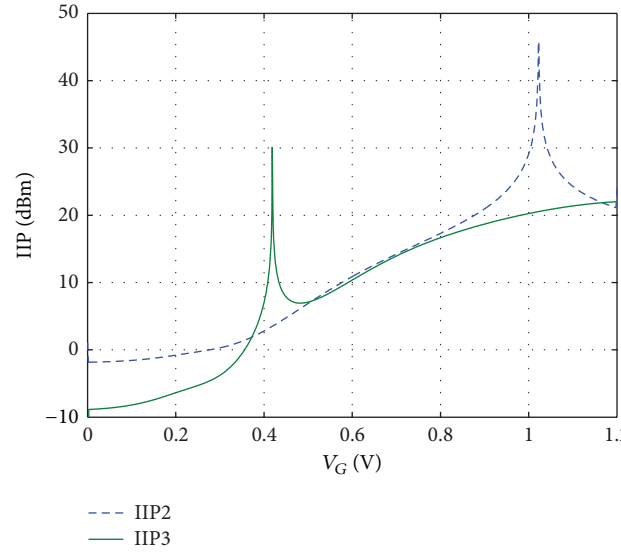

Figure 2: IIP2 and IIP3 of the amplifier from Figure 1.

(i) $V_G \approx 420$ mV, ID = 87 μA, $gm = 1.19$ mA/V, PDC = 0.104 mW, IIP2 ≈ 4.5 dBm, and IIP3 ≈ 30 dBm.

At this point IM3 products are minimised as well as a power consumption. Transistor is biased, where $g_3 \approx 0$, resulting in high IIP3. IM2 products are not minimised, but they are usually not a limiting factor for a linearity performance of the receiver when originated from LNA [4, 5]. However, at this bias point, small gm value translates into reduced gain and from a noise perspective; this has a negative impact on system SNR. Since unity gain frequency f_t of the transistor is proportional to gm, the maximum operation frequency of the circuit is limited.

(ii) $V_G \approx 1080$ mV, ID = 1.87 mA, $gm = 3.17$ mA/V, PDC = 2.24 mW, IIP2 ≈ 45 dBm, and IIP3 ≈ 20 dBm.

At this point IM2 products are minimised; IM3 products are relatively small as well. The transconductance

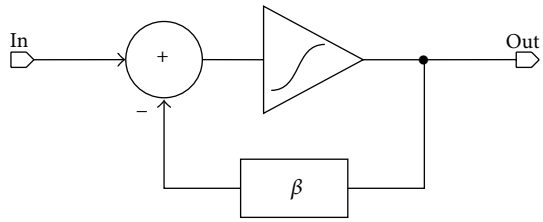

Figure 3: Feedback loop linearization concept.

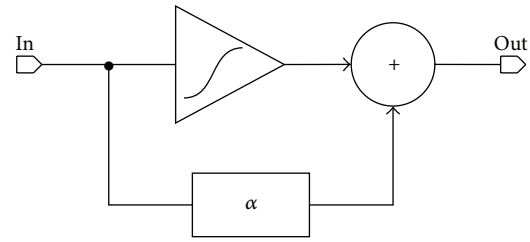

Figure 4: Feed-forward loop linearization concept.

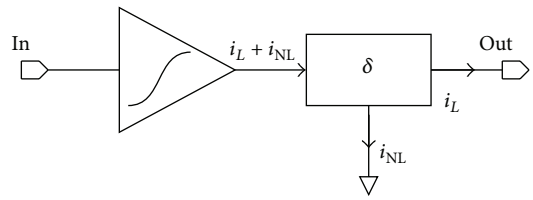

Figure 5: Postdistortion linearization concept.

is at its maximum, 2.6 times larger than in the previous case, improving both gain and f_t. The cost however is 21 times more power dissipated by the transistor than before.

(iii) $V_G \approx 700$ mV, ID = 0.71 mA, gm = 2.86 mA/V, PDC = 0.85 mW, IIP2 ≈ 13 dBm, and IIP3 ≈ 13 dBm.

Depending on the system requirements (discussed in detail later in this paper), this point may represent a design trade-off between power consumption and linearity, delivering 90% of maximum gain with more than a 60% of power reduction in comparison to the previous case.

As mentioned before, in practice the design of LNA has to involve a simultaneous optimisation of noise, impedance matching, gain, stability, and linearity (as all of these cannot be maximised at the same time); however the presented methodology can be used as a starting point for a linear LNA design with a limited power budget.

3. Linearization Techniques

It is natural to expect that the relationship between power consumption and linearity of an LNA is much more complex than highlighted in the previous section (in other words it is not only the function of transistor bias point). In the context of this work it is important to shed more light on how linearity of an amplifier can be improved by various circuit techniques that among other design constraints significantly affect the power consumption as well.

3.1. Negative Feedback. Figure 3 depicts well known *negative feedback* (FB) circuit configuration. FB samples a fraction of the output signal and transmits it back to the amplifier input out of phase. Gray et al. [6] show that effects of soft nonlinearity can be improved because both gain and its sensitivity on input signal are chiefly controlled by a transfer function of feedback loop block β. If β can be made linear, this translates directly to improved linearity of the whole closed loop system.

Zhang and Sánchez-Sinencio [7] show that if amplifier gain is equal to G, IIP2 is improved by as much as $1 + G\beta$, whereas increase in IIP3 is proportional to $(1 + G\beta)^{3/2}$ but only for $g_2 \approx 0$. When the second order polynomial coefficient is finite, resulting IM2 products are fed back to an amplifier and intermodulate into IM3, quickly deteriorating theoretical improvements in IIP3. The main advantage of FB method is the use of passive components that do not consume power (majority of typical designs employs highly linear RLC components as β). The main drawback is strong dependence of circuit linearity on $G\beta$ product that is generally known to vary significantly at RF frequencies, especially in wideband applications.

3.2. Feed-Forward and Derivative Superposition. Another approach to improve LNA linearity is a *feed-forward* (FF) technique, depicted in Figure 4. In this method, input signal is connected to the inputs of nonlinear amplifier and a parallel block α, whereas the output signal is a difference of corresponding output signals from each of the blocks. The block α scales input signal by the factor of $\gamma > 1$, passes this signal through auxiliary amplifier with the same nonlinearity as the one of the LNA, and then scales the response down by γ^{-3}. As a result, after the final addition, IM3 products from both paths are ideally cancelled out [8, 9]. In practice, due to process variations, IM3 cancellation is limited, requires twice the power (due to an auxiliary amplifier), and increases noise. The FF method relies heavily on constant and precise value for γ which is hard to obtain in practice and input matching may be problematic, especially in wideband applications [7].

One of the modifications of FF approach, known as *derivative superposition* (DS), uses nonlinearity α with 3rd order polynomial of the opposite sign to the one of the LNA; that is $g_{3\alpha} = -g_{3\mathrm{LNA}}$ [10, 11]. The main advantage of this method is that IM3 products are automatically out of phase, without necessity of using γ scaling factor as in the standard FF approach. In addition, an auxiliary amplifier operates in weak inversion with minimal impact on the power consumption [10, 11]. The disadvantage is a limited range of relatively low input amplitudes α block can operate with [7].

3.3. Postdistortion. Last method, presented in Figure 5, is known as *postdistortion* (PD) and involves the auxiliary nonlinearity δ supplied after the LNA [12]. This block is

Table 1: Sensitivity and noise for LTE Band 2.

Param.	Bandwidth (MHz)					
	1.4	3	5	10	15	20
P_{REFSENS} (dBm)	−103	−100	−98	−95	−93	−92
Noise floor (dBm)	−113	−109	−107	−104	−102	−101
Rx Margin (dB)	12	9	6	6	7	9
Int BW (MHz)	1.4	3		5		

characterised by the same nonlinearity as LNA however with opposite sign, effectively grounding IM products but passing linear response to the output. The most important advantage is that input matching of LNA is not affected as in the case of FF methods mentioned previously. The drawback is increased power consumption as δ is usually biased in saturation for robust distortion cancellation.

The three fundamental linearization techniques referenced in this work show that in some cases nonlinear behaviour of the amplifier can be improved without power increase (FB), whereas a further suppression of IM products requires more energy. As a result, in practice the prediction of power consumption required for certain linearity is a more complex process. We will focus on this issue towards the end of this paper.

4. LTE Linearity Requirements

4.1. 3GPP LTE Specification and System Parameters. The linearity requirements for LTE are not reported specifically by 3GPP; however after some elaboration they can be derived from the intermodulation specifications 36.101 and 36.104 [1] for both user equipment (UE) and base station (BS) receivers, respectively. In this paper we use the most recent version of aforementioned LTE specification, Revision 11, March 2013, and we limit our calculations to UE, as BS has more scenarios differing in performance (namely, Wide Area, Medium Range, Local Area, and Home). However, the presented formulation can be successfully applied to any type of BS if necessary. In order to represent performance variations in different propagation scenarios, 3GPP considers reference carriers with QPSK, 16QAM, and 64QAM modulations and following bandwidths: 1.4, 3, 5, 10, 15, and 20 MHz. In this work we present calculations for QPSK case for all bandwidths and for a single LTE Band 2 (uplink, UL, centred 1960 at MHz, downlink, DL, at 1880 MHz, 60 MHz bandwidth, 80 MHz separation) [2]. Finally, as mentioned previously, we will focus only on IIP3 as assuming that the second order distortion in LNA is not usually a limiting factor for the linearity of complete receiver.

All system parameters necessary to calculate IIP3 are presented in Table 1.

(i) P_{REFSENS} is a minimum average power applied to UE antenna ports (LTE assumes 2 Rx antennae for diversity scheme) to achieve at least 95% of maximum throughput.

(ii) Thermal noise floor for given bandwidth at temperature of 290 K.

(iii) *Rx Margin* is a required increase in minimum average received signal power in the presence of blockers and interferers over nominal P_{REFSENS} value.

(iv) 3GPP derives intermodulation requirements for two interfering signals; one is a continuous wave (CW); the other one is a modulated carrier with bandwidth ranging in between 1.4 and 5 MHz.

4.2. In-Band IIP3 Specification. In-band linearity requirement defines receiver robustness against cross modulation products of other channels of the same band or any CW interferer present within the band of interest. According to 36.101 rev.11 specification, the receiver has to be able to detect a wanted signal in presence of two interferers with average power of −46 dBm each. CW interferer is placed at −BW/2 − 7.5 MHz (low side) or BW/2 + 7.5 MHz (high side) from the carrier frequency of the band of interest, whereas the modulated interferer is located at twice the frequency of the CW signal. For example, considering high side interferers and BW of a wanted signal of 10 MHz, the CW interferer is located at 12.5 MHz from the carrier, whereas 5 MHz modulated interferer is 25 MHz above the carrier. It is easy to show that one of their IM3 products at $2f_{\text{CW}}$-f_{IM} is centred around the carrier as well:

$$f_{\text{IM3}} = 2\left(f_c + 12.5\,\text{MHz}\right) - \left(f_c + 25\,\text{MHz}\right) = f_c. \quad (10)$$

Assuming that the intermodulation products are allowed to increase noise floor from Table 1 by Rx Margin of 6 dB (assuming channel bandwidth of 10 MHz), resulting in maximum noise floor of −98 dBm. Since thermal noise and IM3 products are not correlated, we can calculate the maximum power of intermodulation components:

$$P_{\text{IM3}} = 10\log_{10}\left(10^{-98/10} - 10^{-104/10}\right) = -99.26\,\text{dBm}. \quad (11)$$

As the interferer bandwidth is 5 MHz for the considered case, IM3 product occupies exactly half of the signal BW. Thus, (11) has to be corrected by the ratio of two quantities, which now represents an equivalent average IM level for 10 MHz wanted signal [13]:

$$P_{\text{IM3}} = -99.26 - 10\log_{10}\left(\frac{10\,\text{MHz}}{5\,\text{MHz}}\right) = -102.24\,\text{dBm}. \quad (12)$$

Finally, IIP3 can be estimated taking power of interferers and calculated power of the third order intermodulation product [13]:

$$\text{IIP3} = 0.5\left(3P_{\text{INT}} - P_{\text{IM3}}\right) = +17.88\,\text{dBm}. \quad (13)$$

Table 2 presents the results of in-band IIP3 calculations for all the possible BW values. Note that our calculations are 3-4 dB more stringent to the results of Sesia et al. [13], where the authors used an average implementation margin of 2.5 dB in their calculation but did not provide any explanation behind this choice. Thus, we assumed that in practice more implementation margin may be necessary, for example, due to process variations.

Table 2: Calculated IIP3 for LTE assuming two −46 dBm interferers (in-band) and −31 dBm interference (out-of-band).

BW (MHz)	P_{IM3} (dBm)	In-band IIP3 (dBm)	Out-of-band IIP3 (dBm)
1.4	−101.28	−18.36	+4.19
3	−100.58	−18.71	+3.84
5	−102.24	−17.88	+4.68
10	−102.24	−17.88	+4.68
15	−100.74	−18.63	+3.92
20	−98.59	−19.70	+2.85

4.3. Out-of-Band IIP3 Specification. Due to a limited performance of receiver preselection filters and finite isolation of duplexer in radio transceiver, strong signals from the transmitter side are injected into the receiver and are mixed together with interferers into IM3 products, as presented in Figure 6. This is chiefly a problem for FDD system, where the transmitter and receiver are operating simultaneously. Taking a maximum average power of LTE signal from the transmitter output of +24 dBm, a typical duplexer isolation of 50 dB, and 2 dB losses in the receive path [13], interferer as strong as −28 dBm can reach the receiver. If a strong CW signal falls between Rx and Tx bands (namely, at half the duplex distance) IM3 products will fall into the band of interest. As previously, IIP3 specification is reported directly by 3GPP; however it can be derived from out-of-band blocking requirements [13, 14]. The maximum power of CW interferer depends on its distance from the edge of a wanted band and is, respectively (in reference to the upper limit), −4 dBm from 15 MHz to 60 MHz, −30 dBm from 60 MHz to 85 MHz, and −15 dBm above 85 MHz offset [1]. For Band 2 considered in this paper, the duplex separation is equal to 80 MHz; thus a −44 dBm CW interferer at 40 MHz offset from the received band cross-modulates with the transmitter leakage. As Band 2 has a relatively wide UL and DL bandwidths in relation to the duplex distance (60 MHz versus 80 MHz), the resulting filtering of CW between bands will be limited. As an example consider a commercially available Band 2 duplexer from Avago Tech., ACMD-7410, that provides approximately 4 dB attenuation at CW frequency [15]. Thus, interferer of −48 dBm has to be considered. As both CW and the leakage signal power in relation to the receive band are strong functions of duplexer transfer function, Sesia et al. [13] suggests using an average interference power to calculate IIP3. In the presented example, the average power of the interference from −28 dBm leakage and −48 dBm CW is equal to −31 dBm. Using (13) and assuming allowed power of IM3 products from (11) and (12), the resulting out-of-band IIP3 values are presented in Table 2.

It can be seen that the out-of-band requirement is much more stringent than in the case of in-band calculation (−17 dBm against +5 dBm). In the case of the former, a duplexer specification determines the linear performance of the receiver (this is most likely why 3GPP does not define IIP3). In the case of stronger interferers and limited filtering in wideband applications, this leads to further increase in out-of-band IIP3 levels.

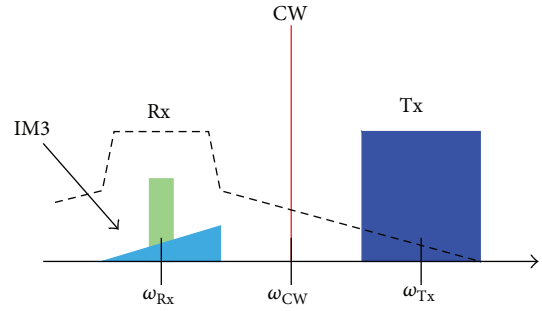

Figure 6: Out-of-band IM3 due to a finite Rx filter roll-off.

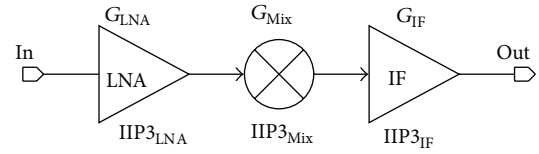

Figure 7: LNA, mixer, and IF amplifier cascade.

5. Linearity: Amplifier versus LTE Front-End

In order to show how system level linearity translates to IIP requirements of LNA, let us consider a simplified model of cascaded RF heterodyne front-end, depicted in Figure 7. The system consists of an LNA, followed by a mixer and intermediate frequency (IF) amplifier. Each block is described by the power gain as well as IIP3. We assume that all blocks are impedance matched, which in practice is valid only for a limited range of frequencies. For clarity, any interstage filters were omitted, assuming that at frequency of interest they introduce negligible insertion loss and their respective IIP3 levels are relatively high.

Well known approximation of 3 stage cascade from Figure 7 is given by [4, 5]

$$\frac{1}{IIP3_{tot}} \approx \frac{1}{IIP3_{LNA}} + \frac{G_{LNA}}{IIP3_{MIX}} + \frac{G_{LNA}G_{MIX}}{IIP3_{IFA}}, \quad (14)$$

where G represents power gain and IIP3 is power referred to a characteristic impedance common for all the blocks. Although simple, (14) allows us to analyse how LNA affects the performance of the cascade. The rule of thumb is that the linearity of the cascade is defined by the last stage (IF amplifier in Figure 3) as its IIP3 is scaled down by the total gain of previous stages. This is generally true assuming that linearity of LNA and mixer are not limiting factors. In practice, however, in order to provide wide bandwidth, constant gain, and low noise figure, linearity of the LNA cannot be designed arbitrarily high. In addition, in order to reduce front-end power consumption and improve noise figure and linearity, a passive mixer with negative conversion gain can be used. Thus, the more detailed analysis is necessary. As an example consider a typical IF amplifier with power gain of

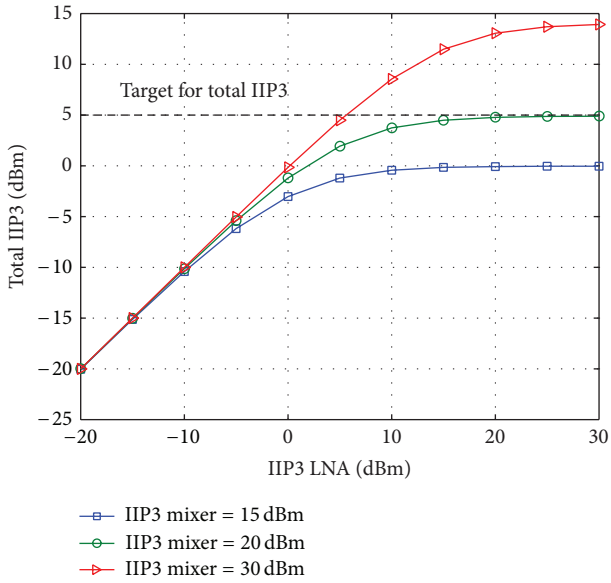

Figure 8: IIP3 of the cascade versus IIP3 of LNA.

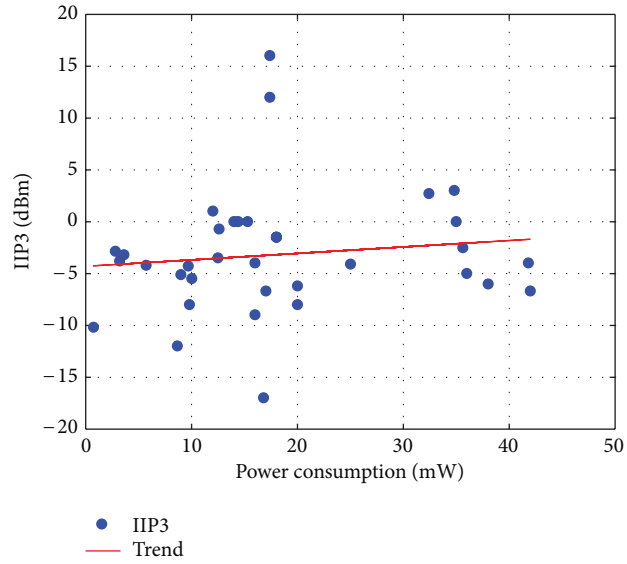

Figure 9: Comparison of LNAs: IIP3 versus power.

20 dB and IIP3 in the range of 25 to 30 dBm [16]. Assuming a constant gain of the LNA and passive mixer, equal to 15 dB and −6 dB, respectively, we can show that the total IIP3 of the cascade from (14) is strongly dependent on both intercept point levels of LNA and mixer.

Figure 8 depicts the results of total IIP3 calculation as a function of LNA linearity for the parametric sweep of mixer third order intercept point. Dashed line represents a +5 dBm IIP3 target corresponding to LTE out-of-band specification calculated in Section 4.

It can be seen that for low values of LNA IIP3 $\ll$ 0 dBm, the amplifier limits the linearity of the cascade. The curves start to diverge strongly where LNA IIP3 reaches 0 dBm. At this point the mixer intercept point is reduced by the LNA gain and becomes the dominant factor. Finally, a highly linear LNA has no effect on the total IIP3 of the cascade, now controlled fully by the intermodulation performance of the mixer. Thus, in order to achieve out-of-band IIP3 performance of the LTE system, it is critical to use both highly linear mixer and LNA combinations. Providing that typical RF passive mixers in discrete implementations achieve IIP3 in the range of 25 to 35 dBm [16], a rough estimation of intercept point for LNA operating in LTE receiver yields +5 dBm. In practice, we should expect limited performance due to impedance mismatches, nonuniform gain changing with frequency, and nonideal duplexer transfer function. It is therefore safe to assume that IIP3 of +10 dBm is more realistic target for LTE wideband low noise amplifier.

6. LNA Power Consumption in Context of LTE

This section presents the results of performance comparison of 35 different CMOS wideband LNA circuits published in recent years (Table 3, on a following page) [17–49]. To allow fair comparison, every circuit is characterised by power gain (G, dB), noise figure (NF, dB), minimum and maximum frequency of operation ($f_{\min}$ and $f_{\max}$ resp., MHz), fractional bandwidth (FBW), IIP3 (dBm), and DC power (P_{DC}, mW). Note that some of the published circuits use a voltage gain in place of power gain. In order to follow system level design standards, we translated gain of all LNAs into power domain. It is assumed that the DC power consumption is referred to LNA core, as many of the authors do not report it explicitly. Fractional bandwidth follows a standard RF definition of a ratio of difference between $f_{\max}$ and $f_{\min}$ to the centre frequency between the two. In cases where G and NF were varying over the band of interest, the best of the reported values was chosen.

In order to show that the relationship between linearity of RF LNA and DC power is not straightforward, consider the results of IIP3 comparison, depicted in Figure 9. Dots correspond to the third order intercept points from Table 3, whereas the solid line represents a linear trend calculated on the dataset. It can be seen that IIP3 is weakly dependent on power consumption (+0.06 dB/mW). Counterintuitive at first, this behaviour is expected. As indicated previously in Section 2, power increase can help to reduce intermodulation effects in simple LNAs; however it may not necessarily yield the best noise, impedance matching, and stability performance. For example, in comparison with other circuits, two LNAs with the highest linearity have either relatively low fractional bandwidth [27] or high noise figure [38]. Note that among the reported state-of-the-art CMOS LNAs, only the two described topologies meet IIP3 requirement from Section 3.

In order to include effects of gain, noise, and linearity, figure of merit (FoM) function has to be used. Usually the DC power consumption contributes to total FoM; however

Table 3: Performance comparison of wideband CMOS LNA circuits.

Reference	Year	Linear method	CMOS (nm)	Gain (dB)	NF (dB)	f_{min} (MHz)	f_{max} (MHz)	FBW (%)	IIP3 (dBm)	P_{DC} (mW)	FoM (dBm)
[17]	2004	FB	250	6.85	2.4	2	1600	199.5	0	35	**27.45**
[18]	2005	FF	180	9.7	5	1200	11900	163.4	−6.2	20	**20.63**
[19]		FF	130	9.5	3.5	100	6500	193.9	1	12	**30.01**
[20]		FB	130	16	5.7	2000	5200	88.9	−6	38	**23.79**
[21]		FB	130	13	4	100	900	160	−10.2	0.72	**20.84**
[22]	2006	FF-DS	180	12.5	4.5	470	860	58.6	−4	16	**21.68**
[23]		FB	90	12.5	2.6	500	8200	177	−4	41.8	**28.38**
[24]		FB	90	12	2	500	7000	173.3	−6.7	42	**25.69**
[25]		FF	90	10	3.5	800	6000	152.9	−3.5	12.5	**24.85**
[26]	2007	FB	90	8	5.3	400	1000	85.7	−17	16.8	**5.03**
[27]		PD	130	12.5	2.7	800	2100	89.7	16	17.4	**45.33**
[28]		FB	130	15.1	2.5	3100	10600	109.5	−5.1	9	**27.89**
[29]		FB	130	17	2.4	1000	7000	150	−4.1	25	**32.26**
[30]		FB	90	17.4	2.6	0	6000	200	−8	9.8	**29.81**
[31]		FF	65	15.6	3	200	5200	185.2	0	14	**35.28**
[32]	2008	FB/FF	180	20.5	3.5	20	1180	193.3	2.7	32.4	**42.56**
[33]		FB	90	16.5	2.7	0	6500	200	−4.3	9.7	**32.51**
[34]		FB	90	8	6	100	8000	195.1	−9	16	**15.90**
[35]	2009	FB	180	10.5	3.5	300	920	101.6	−3.2	3.6	**23.87**
[36]		FB	130	7	3.7	1900	2400	23.3	−6.7	17	**10.27**
[37]		FF-DS	180	14	3	48	1200	184.6	3	34.8	**36.66**
[38]		PD	65	16	5.5	800	5000	144.8	12	17.4	**44.11**
[39]		FB	65	16.5	3.9	1000	10000	163.6	−5	36	**29.74**
[40]	2010	FB	180	8.45	3.2	1050	3050	97.6	−0.7	12.6	**24.44**
[41]		FB	130	9	2.5	100	5000	192.2	−8	20	**21.34**
[42]		FB/FF	130	9.5	3.4	200	3800	180	−4.2	5.7	**24.45**
[42]		FB/FF	130	7.5	4.1	200	3800	180	−3.8	3.2	**22.15**
[43]		FF-DS	180	9.75	3	50	860	178	−2.5	35.6	**26.75**
[44]		FB	90	13.1	3.9	470	750	45.6	−5.5	10	**20.32**
[45]		FB/FF	180	8.2	3.4	50	900	178.9	0	14.4	**27.33**
[46]	2011	FB	90	10.5	1.7	2	2300	199.7	−1.5	18	**30.30**
[46]		FB	90	20	1.9	20	1100	192.9	−1.5	18	**29.45**
[47]		FB	90	11.5	2.35	100	1770	178.6	−2.85	2.8	**28.82**
[48]	2012	FF	180	11.75	2.7	320	1000	103	0	15.3	**29.18**
[49]	2013	FF	65	12	3	100	10000	196	−12	8.64	**19.92**

in order to analyse the performance of LNA as a function of the power, we calculate FoM (without power) in dBm:

$$\text{FoM} = G + \text{IIP3} + 10\log_{10}(\text{FBW}) - \text{NF}. \quad (15)$$

Note that all of the elements in (15) contribute equally to the total FoM; thus a high performance LNA is characterised by minimum noise, wide tuning range, high gain, and IIP3, resulting in proportionally high FoM values.

Figure 10 depicts the results of FoM calculation. As before, dots represent the data points from Table 3, whereas solid line is a linear trend. The average FoM is equal to 26.8 dBm, with average power consumption of 18.3 mW. It can be seen that higher FoM requires more DC power, which confirms our assumption that optimised wideband LNA consumes more energy. Note that this relationship is not strong as the slope of a trend line is approximately +0.19 dB/mW. In order to increase FoM of CMOS LNA by 3 dB, a corresponding increase in power of 16 mW is necessary. Assuming IIP3 of +10 dBm as a target for LTE LNA (derived in Section 4), together with an average power gain of 15 dB for RF LNA [16], a fractional tuning range of 120% (0.7–2.7 GHz LTE band), and NF of 5 dB (a fair assumption for total NF of 9 dB for the wideband UE LTE receiver), a target FoM of 41 dBm is obtained.

Therefore, the corresponding FoM increase of +14.2 dB over the average, results in a proportional change in DC power by +75 mW, the expected increase in FoM is equal to +14.2 dB, which corresponds to the required increase in

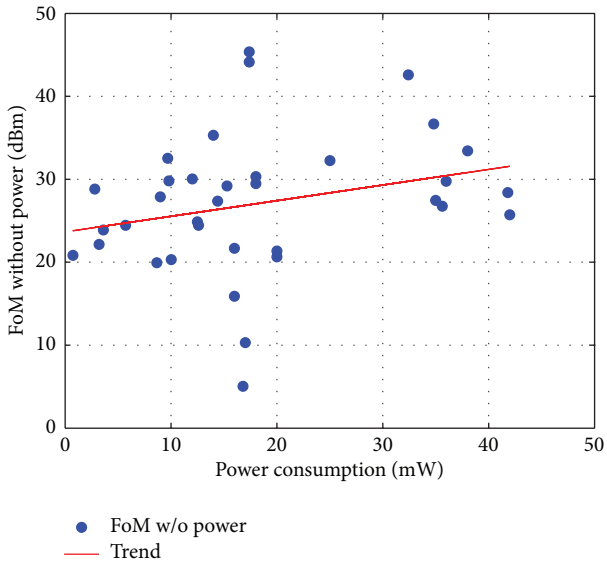

Figure 10: Comparison of LNAs: FoM versus power.

power of +75 mW. Note that four of the reported LNAs [23, 27, 32, 38] meet the FoM requirement; however either a bandwidth is smaller, IIP3 is inadequate, or noise is too high for an LTE system (note that the authors usually present the best performance rather than the average over bandwidth). A validity of the presented discussion can be confirmed by a comparison to the state-of-the-art commercial LNA chip ADL5521 from Analog Devices [16]. Although realised in GaAn pHemt technology (higher f_t and lower noise than CMOS), its performance follows the trend of FoM presented in this paper. The reported parameters are (averaged) NF = 1 dB, G = 15 dB, IIP3 = 21 dBm, and FBW = 163.6%, and calculated FoM is equal to 57 dBm, that is, +30.2 dB above the CMOS average presented in this paper. According to our prediction the LNA core should consume +159 mW more than the CMOS average, resulting in a total of 177 mW. The reported value for ADL5521 is 300 mW from 5 V supply; however the core power consumption is not disclosed (some of the reported power is used by active replica bias). Thus it can be seen that, in practice, high performance LTE LNAs are power hungry circuits, as shown in this paper.

7. Conclusion

The presented results show that, in general, LNA linearity as a standalone parameter is indirectly dependent on power. In theory, for a certain IIP3 performance, LNA circuit can be designed without the penalty of increase in power, as indicated by Figure 8. However, taking into account the rest of design constraints as noise figure, gain, and bandwidth, more power has to be delivered to the amplifier, and hence, increasing LNA linearity levels will inevitably translate into higher power consumption. This is especially crucial for the wideband systems (LTE and beyond), where inadequate filtering leads to more stringent intermodulation specifications that, in turn, present a significant impact on the power consumption of the whole receiver.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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