Wide Band Switched Delay Line using MEMS Switches

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***Abstract*—This paper presents a high precision wide band switched delay line with fine tuning capability and low insertion loss. The circuit is designed to operate in the frequency range from 1 GHz to 5 GHz and tuned using MEMS switches targeting a minimum delay step of 7 ps. The delay line uses a single layer of a high permittivity substrate (ε_r =10), and the MEMS devices are interconnected using conventional coplanar waveguide technology (CPW). The circuit was designed and simulated using CST Microwave Studio. The simulated group delay shows a small deviation from the linear phase of less than 1^o over a wide bandwidth compared to the performance of SAW and ceramic filters [1]. The simulation results shows an insertion loss and a return loss of better than 1 dB and 20 dB respectively.**

***Index Terms*—Switched delay line, MEMS switches, Wide band RF**

I. Introduction

Group delay elements are one of the essential components employed in RF transceivers. They are used in power amplifier predistortion, feed-forward linearisation and active cancellation techniques. Delay elements can be classified according to the input power level. Traditionally, high power delay elements were realized either using coaxial cables or the less expensive waveguide cavity resonators. Both types of filters can provide up to 50 ns delay, however, their bulky structures usually consume a significant space. Alternative techniques were developed to eliminate these high power delays in the transmitter path [2]. Thus only low power delay filters are needed such as interdigital, ceramic and ladder-type SAW delay filters [3]. They usually suffer from high insertion loss which can directly degrade the receiver sensitivity. Now, research is more concerned with eliminating both ceramic and SAW filters from transceivers as well as developing fully adaptive technique for introducing group delays.

II. Requirements and Specifications

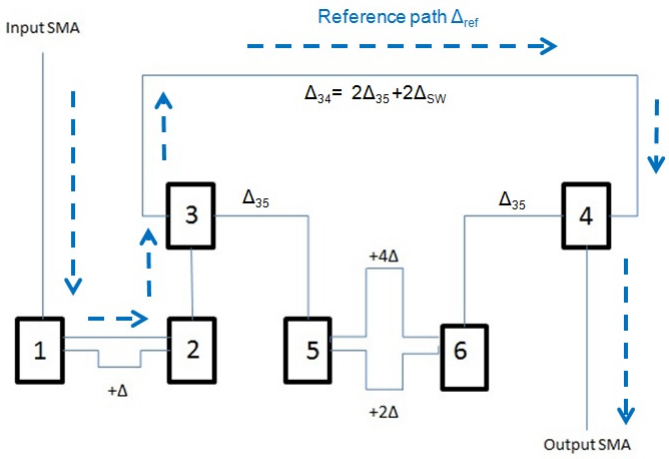

Figure 1. Block diagram of the proposed switched delay lines

The main objective is to develop a wide band switched group delay with a fine tuning and low insertion loss. MEMS devices with integrated switch driver are selected as the switching elements for their fast response and low losses. MEMS switches are integrated to multilayer PCB by means of golden-wires thermosonic ball-soldering bonding [4] which adds complexity to the manufacturing process. Thus, a more accessible technique was required for attaching the switches to the PCB. Fig. 1 shows a block diagram of the proposed PCB which consists of six MEMS devices, it also shows the group delay of each of the routing paths. This design can precisely adjust the delay of the signal with a minimum resolution Δ of 7 ps and the total delay can be tuned by multiples of Δ (2Δ-5Δ).

III. Circuit Realization using Conventional CPW Technology

Care has to be taken when design delay lines based on integrated MEMS devices. These are

mainly due to the MEMS having a large number of pins underneath the package need to be connected to several transmission lines. Thus the first difficulty is creating the transition from the switches to the RF tracks that perfectly matches the impedance of the pins (50Ω) which are only 0.5 mm apart, yet maintaining a low signal coupling at frequencies above 1 GHz. Fig. 2 shows the layout of the circuit where a single layer substrate is used (ε_r= 10) with a thickness of 1.9 mm, and all transmission lines were realized using standard copper cladding whose thickness is 35 μm. Other transitions are designed to connect the narrow CPW RF tracks to the input/output SMA connectors. From SW1 to SW2, the distance between the reference path and the first delay path is only 1.6 mm, thus a fine tuning for the group delay can be achieved with a step of 7 ps. And from SW5 to SW6, two delay lines were designed to deliver 14 ps and 28 ps.

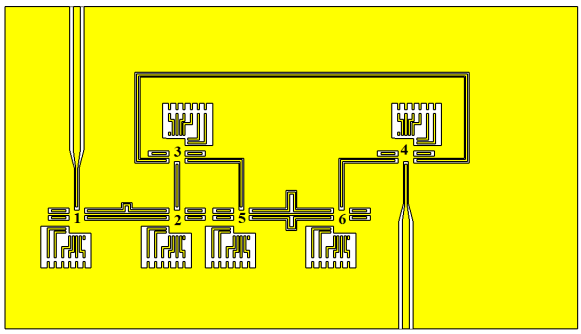

Figure 2. Circuit layout (45 x 80 mm^2)

IV. Simulation Results

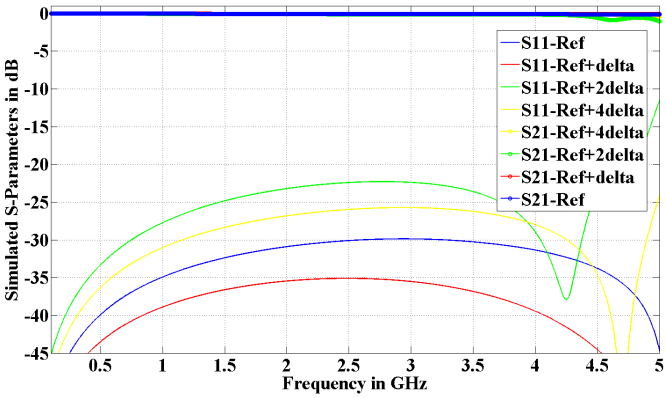

Figure 3. The simulated s-parameters of the four delay paths

Fig. 3 shows the simulated S-parameters for the four delay paths which indicate an insertion loss and a return loss of better than 1 dB and 20 dB respectively. Resonances appeared in the simulation of delay lines at frequencies above 4 GHz due to the excitation of finite ground CPW higher modes. These resonances also appears in the simulated group delay as shown in Fig. 4. These higher modes can be avoided by introducing air bridges to all the bends of each transmission line [3]. Fig. 5 shows the effect of introducing wire airbridges to the CPW line bends on the simulated S-parameters of the path between SW3 and SW4. It indicates an insertion loss of less than up to GHz which is much lower when compared to earlier designs [4], [5]. A deviation of less than 1^o from the linear phase is achieved over a wider bandwidth compared to both SAW and ceramic delay filters, which can typically deliver a similar phase deviation over a maximum of 20 MHz [1]. Currently, the circuit is being implemented using Rogers 6010 substrate and measurements will be presented at the conference.

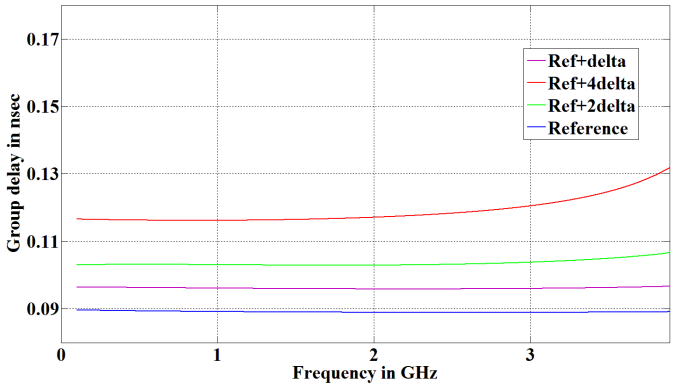

Figure 4. The simulated group delay for the four delay paths

V. Experimental Validation

Fig. 6 shows the fabricated PCB with the MEMS devices which were manually soldiered at NUIM Labs. Unfortunately, airbridges weren't built due to limited fabrication tools. Fig. 7 shows the measured S-parameters for the longest delay path between the input and output SMA connectors, while Fig. 8 shows the corresponding group delay.

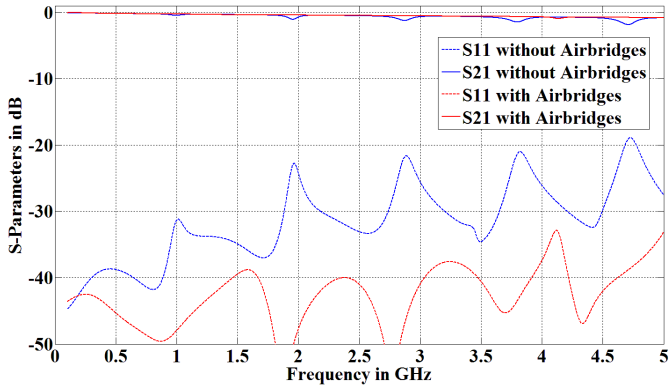

Figure 5. The simulated s-parameters of the path between SW3 and SW4

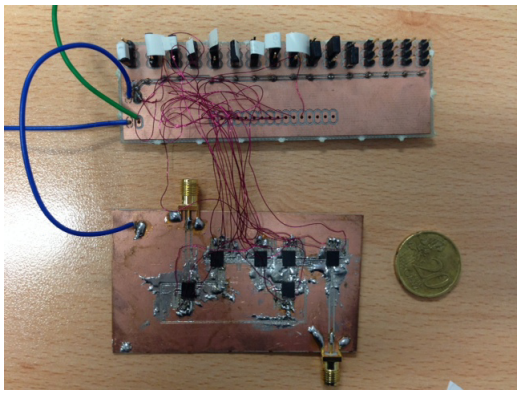

Figure 6. The fabricated switched delay PCB

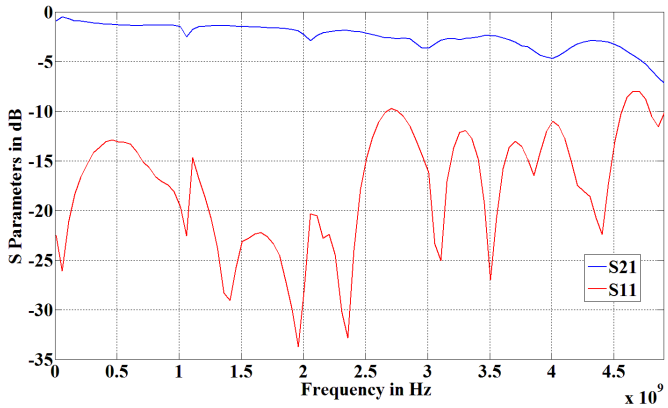

Figure 7. The measured S-parameters of the longest path between input and output SMA connectors

VI. Conclusion

A wide band high precision MEMS switched delay line with a fine tuning capability was designed and simulated showing a delay step of 7 ps from 1 GHz up to 5 GHz. The simulation results of the delay lines without wire airbridges show a low insertion loss (< 1dB) and a return loss of better than 20 dB up to 4 GHz. After adding airbridges, the simulated insertion and return losses were reduced down to 0.6 dB and -33 dB, respectively.

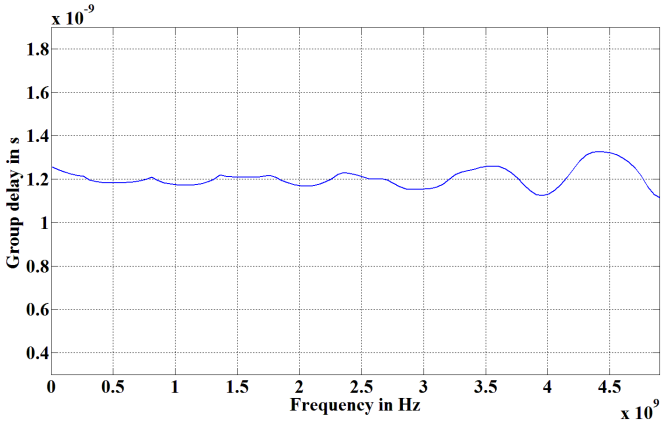

Figure 8. The measured delay of the longest path between input and output SMA connectors

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