NUI MAYNOOTH

Ollscoil na hÉireann Má Nuad

Analysis and Design of ΣΔ Modulators for Radio Frequency Switchmode Power Amplifiers

by

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Abstract

Power amplifiers are an integral part of every basestation, macrocell, microcell and mobile phone, enabling data to be sent over the distances needed to reach the receiver's antenna. While linear operation is needed for transmitting *WCDMA* and *OFDM* signals, linear operation of a power amplifier is characterized by low power efficiency, and contributes to unwanted power dissipation in a transmitter. Recently, a switchmode power amplifier operation was considered for reducing power losses in a RF transmitter. A linear and efficient operation of a PA can be achieved when the transmitted RF signal is ΣΔ modulated, and subsequently amplified by a nonlinear device. Although in theory this approach offers linearity and efficiency reaching 100 %, the use of ΣΔ modulation for transmitting wideband signals causes problems in practical implementation: it requires high sampling rate by the digital hardware, which is needed for shaping large contents of a quantization noise induced by the modulator but also, the binary output from the modulator needs an RF power amplifier operating over very wide frequency band.

This thesis addresses the problem of noise shaping in a ΣΔ modulator and nonlinear distortion caused by broadband operation in switchmode power amplifier driven by a ΣΔ modulated waveform. The problem of sampling rate increase in a ΣΔ modulator is solved by optimizing structure of the modulator, and subsequent processing of an input signal's samples in parallel. Independent from the above, a novel technique for reducing quantization noise in a bandpass ΣΔ modulator using single bit quantizer is presented. The

technique combines error pulse shaping and 3-level quantization for improving signal to noise ratio in a 2-level output. The improvement is achieved without the increase of a digital hardware's sampling rate, which is advantageous also from the perspective of power consumption. The new method is explored in the course of analysis, and verified by simulated and experimental results. The process of RF signal conversion from the Cartesian to polar form is analyzed, and a signal modulator for a polar transmitter with a $\Sigma\Delta$-digitized envelope signal is designed and implemented. The new modulator takes an advantage of bandpass digital to analog conversion for simplifying the analog part of the modulator. A deformation of the pulsed RF signal in the experimental modulator is demonstrated to have an effect primarily on amplitude of the RF signal, which is correctable with simple predistortion.

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List of published contributions and patents

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- Patent application for the 2-level bandpass modulator with improved coding efficiency was filled and submitted to European Patent Office by Alcatel-Lucent, “Modulation”, Application No: 12360069.4-2215, 20.09.2012.

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Chapter 1

Introduction

1.1 Motivation

Over the past decades wireless systems were dynamically evolving. Nowadays radiowaves are used for transmitting voice, video, but also countless gigabytes of data.

Every transmitting, wireless device needs a power amplifier (PA), in order to send data over some distance to the receiver's antenna. Low power efficiency of the amplifier brings a number of problems: it causes unnecessary dissipation of power, contributes to a short battery life in a mobile handsets and finally, it increases the volume and cost of the transmitter due to the need for a cooling system. Thus, the efficient operation of the RF *PA* becomes an important point for wireless transmission of data.

The power efficiency depends on the class of operation, but also on the transmitted RF signal. A constant envelope signal, such as *GMSK* used in the second mobile generation (2G) has the information encoded in the phase of the RF signal. Subsequently, this modulation is insensitive to amplitude distortion and the use of nonlinear, power efficient RF amplifiers is possible for this type of signal. *GMSK* modulation is however inefficient from the point of view of the occupied frequency bandwidth and offers low data rate. More efficient modulations such as $QPSK$, $8-PSK$, $16-QAM$ allow for a

transmission of more bits per second, while the use of a pulse-shaping restricts the bandwidth occupied by the RF signal. This efficient utilization of a frequency spectrum comes however at the cost of amplitude variation of the RF signal, and subsequent need for a linear amplification.

The drawback from the use of linear RF amplifiers is that very often only a fraction of the power consumed by the PA is used for transmitting the radio signal, while the dominant part is lost in the PA and turned into heat. In general, the efficiency of a linear power amplifier decreases as the peak to average power ratio $(PAPR)$ of the RF signal increases. Unfortunately, the RF signals used in third (3G) and fourth (4G) mobile generations can have large amplitude variation, being proportional to the number of multiplexed data streams in the case of $W-CDMA$ or to the number of sub-carriers in the case of multicarrier transmission. While these signals utilize efficiently the available frequency spectrum, their amplification with linear devices can cause great waste of power.

Recently, the use of switchmode power amplifiers has been considered in wireless communication for improving power efficiency of RF transmitters. A $\Sigma\Delta$ modulator can be employed to convert an RF, amplitude and phase modulated signal into a 2-level waveform, which subsequently drives a nonlinear, but also power efficient Class-D power amplifier, while appropriate band-pass filtering allows for a reconstruction of the RF signal before the transmitting antenna. Although this approach increases the complexity of a conventional power amplifier system, it also offers a power efficient yet linear operation. On the other hand, the use of a binary signal to drive a wideband amplifier coupled with programmable digital logic modulating the input RF signal allows for reconfiguration of the PA system and change of e.g. transmission frequency without the need of physical modifications in the device.

The $\Sigma\Delta$ modulation used in the digital power amplifier system adds design challenges, such as very broadband operation of the nonlinear RF PA, degradation of signal to noise

ratio due to the quantization noise, nonlinear distortion or requirement for high sampling rate of the digital logic. The above problems are addressed in the following chapters of this thesis.

1.2 Contributions of the work

This work focuses on the signal processing in two types of RF transmitters utilizing ΣΔ modulation: Class-S and digitized polar transmitter (DPT). It aims to identify and reduce the distortion induced in the course of signal conversion in a digital power amplifier. Crucial for signal to noise ratio (SNR) and adjacent channel leakage ratio $(ACLR)$ of the digital power amplifier are: sufficiently high sampling rate in a digital signal processor (DSP), coding efficiency of a modulator and linearity of the transmitter.

The following problems are addressed in this work:

- Topologies of ΣΔ modulators are studied and structures are optimized for implementation in digital hardware operating at high clock frequency.

- A time-domain description of a modulator is used for parallel expansion of $LP\Sigma\Delta$ and $BP\Sigma\Delta$ modulators, increasing modulator's sampling frequency. The first and second order, $LP\Sigma\Delta$ modulators are proven to be parallel-expandable by factor of 4 $(400\,MHz)$ and to factor of 8 $(800\,MHz)$ when $BP\Sigma\Delta$ modulator is implemented in experimental platform $Virtex-II\,Pro\,FPGA$.

- An observation is made that under certain conditions, the output of a 3-level, $BP\Sigma\Delta$ modulator is not affected by displacement of one of the levels due to shape of error-pulses. The shaping of error pulses technique is subsequently used for a novel requantizing of the 3-level signal to a 2-level signal. Provided with a predistortion block based on simple arithmetic and first-order, high-pass filter, the new modulator

can provide $6dB$ better *SNR* than equivalent 2-level *BP*ΣΔ modulator of order one and two operating at the same sampling frequency.

- A digitized polar transmitter is analyzed, providing insight into the magnitude of distortion caused by bandlimiting of phase and envelope signals and time delay error. Also, an aliasing effect is observed in the transmitter.

- A new concept for signal modulator for a *DPT* is presented. The new modulator uses a *DSP* for generating phase signal, which reduces the analog signal processing in the phase path to a $1bit$ *DAC* and an analog bandpass filter. The digitization of the phase signal enables movement of the signal processing operations into the digital-domain, which increases reconfigurability of the modulator.

- The modulator is implemented and measured results are demonstrated for a high carrier frequency $f_C = 2113MHz$. It is observed that deterioration of pulses in the output of a *DPT* depends on the sampling frequency of the *LP*ΣΔ modulator and on RF amplitude. A linearization for the *DPT* is proposed and demonstrated.

1.3 Organization of results

This work is organized as follows:

Chapter 2 provides an overview of classes of power amplifiers and techniques for improving power efficiency. The second part of the chapter focuses on ΣΔ modulation used in digital power amplifiers.

The focus of Chapter 3 is on developing structures for ΣΔ modulators suitable for high clock frequency operation. Subsequently, a technique of a parallelization for ΣΔ modulators, which aims in an increase of the effective sampling rate is introduced and verified.

Chapter 4 proposes a new, 2-level bandpass modulator, which combines a 3-level ΣΔ modulation with an error pulses shaping. The analysis, simulations and experimental results are provided.

Chapter 5 analyzes the process of signal conversion in a digitized polar transmitter. The results of spectral limitation of the signals, delay difference between phase and envelope signals and the aliasing effect on modulator's performance are discussed for a bandlimited, bandpass signal. Subsequently, a new modulator with a digitized-phase signal is proposed.

The scope of Chapter 6 is a practical implementation of the new modulator for the digitized polar transmitter described in Chapter 5, including all steps of signal-conversion. The experimental results are demonstrated for a bandlimited signal of bandwidth $1.1\,MHz$ at a carrier frequency of $2113\,MHz$.

Chapter 7 provides conclusions for the work.

Chapter 2

Efficiency and linearity of power amplifiers

This chapter provides an overview of the classes of operation of power amplifiers, highlighting the problems of their linearity and efficiency. In general, nonlinear devices can offer very high power efficiency, in theory reaching up to 100 %. These amplifiers are however insensitive to the changes of the input RF signal's amplitude, and subsequently their use is limited to constant-envelope, phase-modulated signals. Linear amplification is needed when the signal is amplitude-modulated to avoid distortion and a subsequent increase in the signal bandwidth. The fundamental problem with a linear power amplifier is low power efficiency. The discussion on PA operation is followed by the description of techniques aiming in an improvement of the power efficiency in PA systems. The second part of the chapter focuses on $\Sigma\Delta$ modulation, which plays a key role in *SNR* and efficiency of a digital PA.

2.1 Classes of operation

This section describes the classes of operation of power amplifiers. The analysis of operation is based on a piecewise-linear approximation of an n-channel field-effect transistor (FET) characteristic when the transistor operates in the active region. The amplifiers operating in switchmode are analyzed assuming two states of transistor: OFF, corresponding to zero drain current, and ON, corresponding to an open transistor channel.

2.1.1 Transistor model

A transfer characteristic of a FET is a nonlinear function of drain current and gate-source voltage $I_D = f(V_{GS})$. For the purpose of analysis, this nonlinear function is approximated by a piecewise-linear characteristic, which simplifies operation of transistor to three regions: active-linear, cut-off, and open channel. The linear approximation is obtained by applying tangent lines to the device's characteristic at chosen points. The piecewise linear approximation used in this chapter is shown in Fig.2.1(A). The characteristic gives a clear indication for pinch-off voltage of the transistor, denoted as V_P, and maximum voltage denoted as V_{MAX}, which are useful when estimating drain efficiency of a linear power amplifier for selected bias voltage V_{bias}.

When operated in switchmode, the transistor is driven by two voltage levels. The

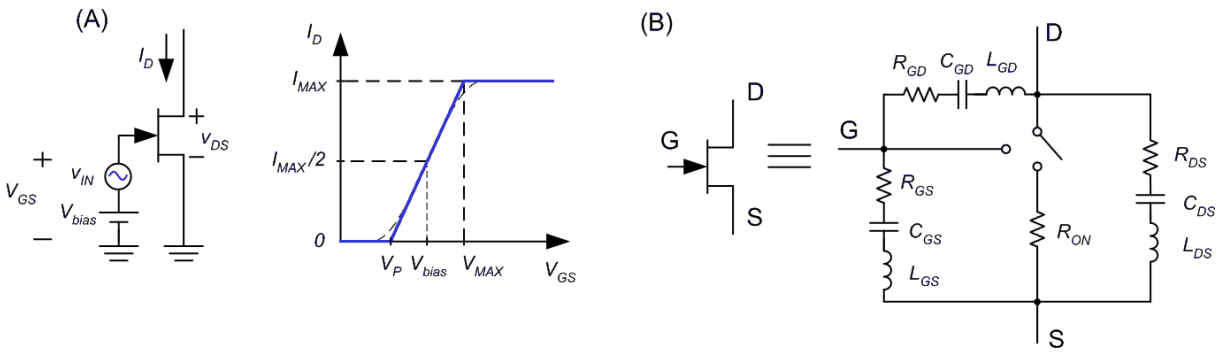

Figure 2.1: Transistor models. (A) Linear approximation of transistor's current-voltage characteristic. (B) Switchmode operation.

gate-source voltage is less than pinch-off voltage, and the drain current is zero or, the gate-source voltage is sufficiently large to obtain near-zero drain-source voltage. These two states are often modeled by opening and closing of a switch characterized by some small resistance R_{ON}, which represents conduction losses in the transistor during the *ON* time interval. In order to account for power losses associated with opening and closing the switch, a drain-to-source, as well as a gate-to-source and gate-to-drain capacitances can be added to the transistor model along with inductive and resistive elements [11, 28, 63]. The transistor model with series R-L-C branches representing impedances between drain, gate and source is shown in Fig.2.1(B).

2.1.2 Definitions

2.1.2.1 Power output capability

The power output capability of a power amplifier is defined as the ratio of RF power delivered to a load, to the product of the maximum instantaneous drain current and the maximum instantaneous drain-source voltage occurring in the amplifier.

$$C_P = \frac{P_{L_{MAX}}}{I_{D_{MAX}} V_{DS_{MAX}}} \tag{2.1}$$

The maximum output power can be calculated as a function of power output capability and maximum transistor ratings $I_{D_{MAX}}$ and $V_{DS_{MAX}}$ [63], which is useful when comparing amplifiers of different classes of operation.

2.1.2.2 Drain efficiency

The drain efficiency of a power amplifier is defined as the ratio of the output RF power to the DC power supplied to the drain of a transistor.

$$\eta_D = \frac{P_L}{P_{DC}} \tag{2.2}$$

The definition of drain efficiency does not include power needed to drive the amplifier.

2.1.2.3 Power added efficiency

Power added efficiency (PAE) of a power amplifier is defined as the ratio of RF power delivered to load resistance, reduced by the power needed to drive the transistor, to the DC power supplied to a drain of the transistor in the power amplifier.

$$\eta_{PAE} = \frac{P_L - P_{DRIVE}}{P_{DC}} = \frac{P_L}{P_{DC}}\left(1 - \frac{1}{k}\right) \tag{2.3}$$

where $k = P_L/P_{DRIVE}$ is a power gain of an amplifier.

2.1.2.4 Crest factor and peak to average power ratio

A Crest Factor (CF) is defined as a ratio of a peak value to a root mean square (rms) value of a signal,

$$CF = 20log_{10}\left(x_{PEAK}/x_{rms}\right) \tag{2.4}$$

A Peak to average power ratio gives the relation of the peak power of an RF signal to its average power. The peak power is calculated by integrating over a single RF period, while the average power is calculated for the total duration of the RF signal,

$$PAPR = 10log_{10}\left(P_{PEAK}/P_{AV}\right) \tag{2.5}$$

When expressed in decibels, the CF is higher than the $PAPR$ by $3\,dB$.

2.1.3 Class-A

Class-A operation assumes that the operating point of an amplifier is set in the middle of the linear part of the characteristic shown in Fig.2.1(A), and the input amplitude is bounded by pinch-off, and the maximum voltage. Due to the operation in the linear part

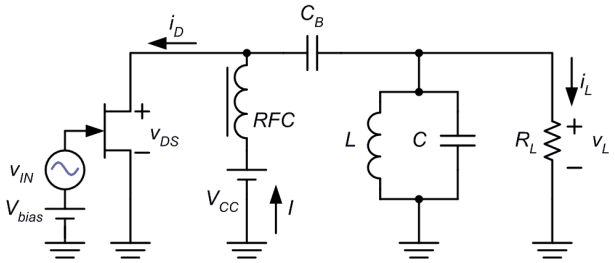

Figure 2.2: Common scheme of Class-A, B, AB, and C power amplifier.

of the characteristic, the input RF signal is amplified without distortion, and the amplifier is said to have a conduction angle of 360°. Fig.2.2 shows the amplifier with the FET device operating as a voltage-controlled current source, and waveforms for a Class-A power amplifier with an input cosine voltage waveform are shown in Fig.2.3.

Due to the use of an RF choke, the supply current I in the amplifier is constant and equal to half of the maximum load current's amplitude, $I = \frac{I_{MAX}}{2} = \frac{V_{MAX}}{2R_L}$. Subsequently the power supplied from the voltage source V_{CC} is constant and does not depend on the power delivered to the load resistance,

$$P_{DC} = V_{CC}^2/R_L \tag{2.6}$$

The drain efficiency of a Class-A amplifier is expressed as the ratio of the power supplied to the load resistance and the DC power supplied to the amplifier,

$$\eta_D = P_L/P_{DC} = \frac{1}{2}\left(\frac{V_L}{V_{CC}}\right)^2 \tag{2.7}$$

The amplifier operates most efficiently when the amplitude across the load resistance has the maximum value, $V_{L_{MAX}} = V_{CC}$, yielding $\eta_{D_{MAX}} = 50\,\%$. The largest power dissipation occurs when the input signal's amplitude is zero, and 100% of the DC power is burned in the transistor. The output power capability of a Class-A power amplifier when the transistor is described by the piecewise linear characteristic becomes,

$$C_{P_A} = \frac{P_{L_{MAX}}}{I_{D_{MAX}} V_{DS_{MAX}}} = \frac{1}{2}\frac{V_{CC}^2}{R_L}\frac{1}{\frac{2V_{CC}}{R_L}2V_{CC}} = 0.125 \tag{2.8}$$

For signals used in wireless communication and characterized by large *PAPR*, such as OFDM, the average drain efficiency can be much lower than the maximum 50%. In practice the efficiency of Class-A power amplifiers can reduce to as low as 5% for a $10\,dB$ PAPR signal [20]. Class-A power amplifiers can be used in applications where the primary concern is linearity, and where power efficiency is a less important problem.

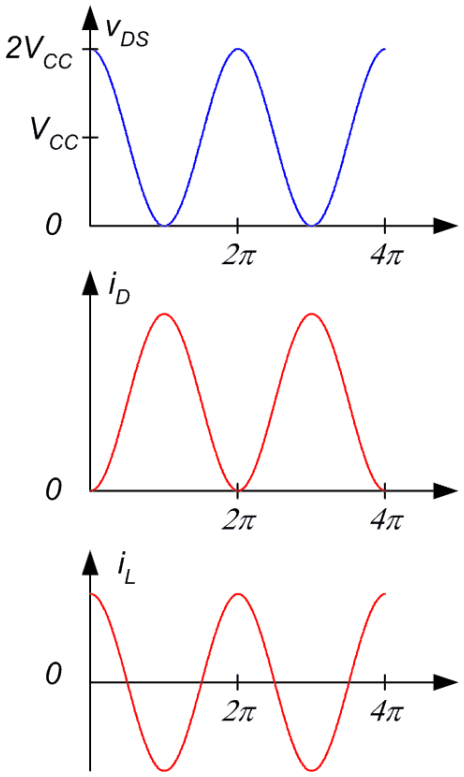

Figure 2.3: Class-A waveforms.

2.1.4 Class-B and AB

The operating point of the transistor in a Class-B amplifier is chosen exactly as the pinch-off voltage of a transistor in the characteristic of Fig.2.1(A). Subsequently, the drain current in the RF Class-B amplifier is a half rectified cosine wave. The Class-B power amplifier is said to have a conduction angle of 180° as the device is active only for half of the input signal's period. The parallel resonant circuit in Fig.2.2 attenuates all harmonics except the fundamental component, creating a cosine voltage waveform across the load resistance. As a result of the reduced conduction angle, the DC power supplied from the

voltage source V_{CC} is no longer constant as it is in Class-A power amplifier, but it is now a function of output amplitude,

$$P_{DC} = \frac{2}{\pi}\frac{V_{CC}V_L}{R_L} \tag{2.9}$$

and it is less than P_{DC} in Class-A. The drain efficiency of a Class-B PA is given by,

$$\eta_D = \frac{\pi}{4}\frac{V_L}{V_{CC}} \tag{2.10}$$

The maximum drain efficiency occurs when the amplitude of the load voltage is the same as the supply voltage V_{CC}, yielding $\eta_{D_{MAX}} = 78.54\%$. While characterized by higher drain efficiency than Class-A, power output capability is the same for both classes,

$$C_{P_B} = 0.125 \tag{2.11}$$

Although the change of conduction angle to 180° in Class-B improves the efficiency of the power amplifier, the output signal suffers from a distortion induced when the input signal's amplitude approaches the nonlinear part of the current-voltage characteristic near the pinch-off voltage of the transistor. The distortion caused by operation in the nonlinear region is reduced in Class-AB by moving the operating point of the transistor slightly above the pinch-off voltage. A Class-AB amplifier is characterized by a conduction angle higher than 180°, but lower than 360° and it comprises features of both classes of operation, A and B. It is more linear than Class-B operation, but the linearity improvement is achieved at the cost of a reduction in the drain efficiency, which is lower than in Class-B. Both Class-B and Class-AB amplifiers can be implemented in a push-pull configuration, which cancels even harmonics in their outputs.

2.1.5 Class-C

The operating point of a Class-C amplifier is below the pinch-off voltage V_P in the characteristic of Fig.2.1(A), and the subsequent conduction angle is less than 180°. Sim-

ilarly to Class-B, harmonics are attenuated by a parallel *LC* circuit tuned at a fundamental frequency. The output power capability of Class-C amplifiers has a maximum value at a conduction angle of 120°, $C_{P_{120}} = 0.0978$ with corresponding drain efficiency $\eta_{120} = 89.68\%$ [63].

The drain efficiency of the amplifier increases, as the conduction angle decreases. The increase in efficiency however is accompanied by a reduction in the output power capability. As the conduction angle approaches 0°, the drain efficiency increases to nearly 100%, but the output power capability is also very low. Because the operating point of the amplifier is set below the pinch-off voltage, amplification of an amplitude-modulated signal would result in AM distortion in the output of the amplifier. Consequently a Class-C PA can be suitable in applications where the RF amplitude variation is small and the efficiency is more important than linearity of the power amplifier.

2.1.6 Class-F

A Class-F amplifier uses harmonic resonators to shape the drain-source voltage waveform (or drain current waveform), such that the average product of the voltage and drain current waveforms reduces, hence improving amplifier efficiency. The voltage (or current) waveform is shaped by controlling particular harmonics amplitudes and phases. The amplifier's resonators can be tuned to either odd harmonics or even harmonics (inverse Class-F). The amplifier usually has a conduction angle of 180°, similarly as in Class-B amplifiers. The voltage across the load resistance is sinusoidal as per the use of a parallel *LC* network tuned to the fundamental frequency. The drain-source voltage waveform in the Class-F amplifier is shaped by resonators tuned to subsequent odd-harmonics. As the number of resonators increases, the voltage waveform flattens, approximating a square-pulse with zero voltage at the time interval corresponding to non-zero drain current. The scheme of a Class-F power amplifier with third harmonic resonator is shown in Fig.2.4

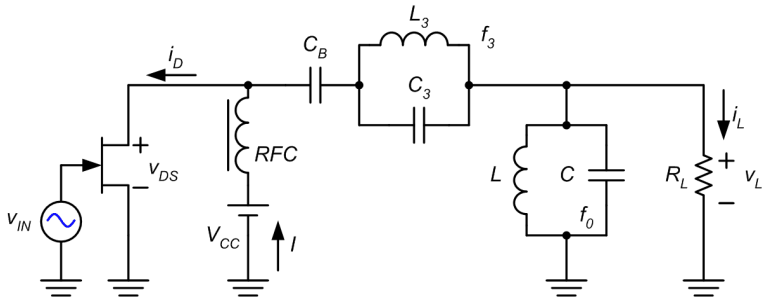

Figure 2.4: Class-F_3 power amplifier.

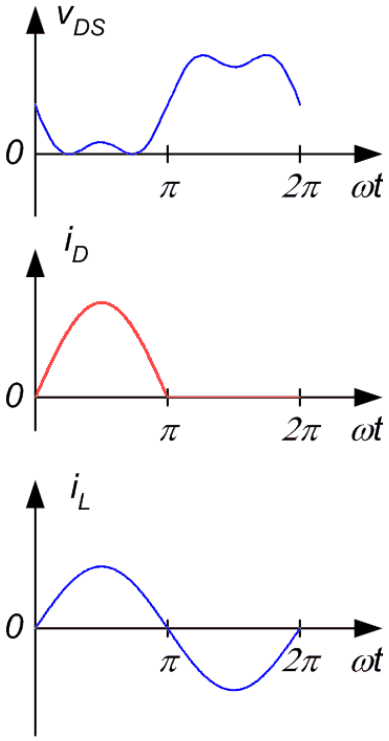

Figure 2.5: Current and voltage waveforms for Class F_3 amplifier.

and current and voltage waveforms are shown in Fig.2.5.

The efficiency of the Class-F amplifier increases towards 100% as the number of controlled harmonics increases towards infinity. The drain efficiencies are $\eta_{D_3} \approx 90.67\%$, and $\eta_{D_{3,5}} \approx 94.8\%$, for Class F_3 and Class F_{35} respectively, and output power capability is $C_{P_{35}} = 0.1509$. In a practical Class-F circuits due to lossy LC elements, the number of resonators is often limited to control either third, or third and fifth harmonics. Control over all harmonics can be achieved by using a quarter-wavelength transmission line rather than the LC elements.

2.1.7 Class-D

A voltage switching Class-D ($VSCD$) power amplifier is shown in Fig.2.6. The power amplifier consists of two complementary transistors driven by ideally square waveforms of opposite phases such that when T_1 is driven ON (or OFF), T_2 remains OFF (or ON). The ideal Class-D operation assumes that the transistors act as switches, showing infinite resistance when they are OFF, and zero resistance when they are ON. Consequently the

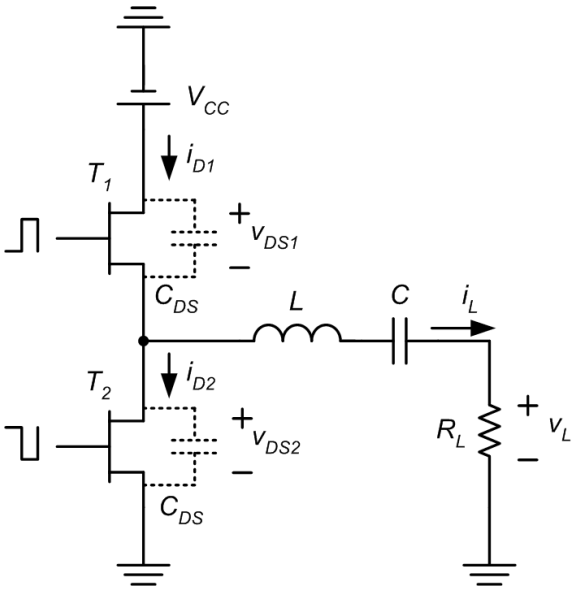

Figure 2.6: Class-D power amplifier.

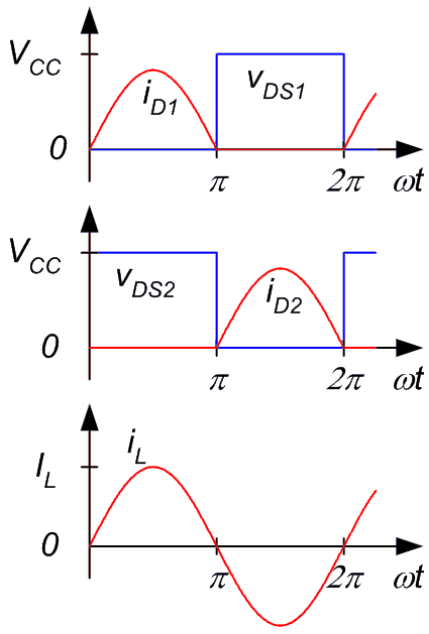

Figure 2.7: Class-D power amplifier - waveforms.

product of drain current and drain-source voltage is always zero and no power dissipation occurs in the transistors. The amplifier's output waveform is created by connecting the midpoint to a load resistance through LC circuit tuned to the frequency of the amplified signal. When the drive signal is a 50% duty ratio square wave, the operation of the Class-D power amplifier can be divided into two time intervals. During one half of a period, T_1 is ON, while T_2 is turned OFF yielding V_{CC} voltage in the input to the resonant circuit. During second half of the period T_1 is driven OFF and T_2 is ON, and the voltage in the input to the resonant circuit is zero. The quality factor of the resonant circuit is usually chosen sufficiently large to attenuate all harmonics except the fundamental, producing a sinewave voltage in the output. The waveforms for a $VSCD$ are shown in Fig.2.7.

The load network of a voltage switching Class-D exhibits impedance equal to the load resistance at the operating frequency, and a large absolute value of impedance for frequencies higher or lower than the operating frequency. The bandwidth of a Class-D power amplifier calculated for the $3\,dB$ power reduction is defined by $BW = \frac{f_C}{Q_L}$, where the quality factor is $Q_L = \frac{\sqrt{\frac{L}{C}}}{R_L + R_{ON}}$. When filter elements are purely reactive and $R_{ON} = 0$, no power losses occur in the amplifier an its efficiency is 100%. The output power capability of a VSCD power amplifier is $C_{P_D} = 0.159$.

The Class-D amplifier can be used for amplifying constant envelope RF signals. The use of varying envelope is also possible, but it requires modulation of the input signal. Subsequently the varying envelope signal is reconstructed in the output of the band pass filter, such as is done in the Class-S power amplifier described in Section 2.2.4.

2.1.8 Class-E

In Class-E PA the transistor operates as a switch, providing potentially 100% power efficiency. The attractive feature of a Class-E amplifier is that a transistor's output capacitance can be absorbed into the amplifier's network, which minimizes turn-on loss in the

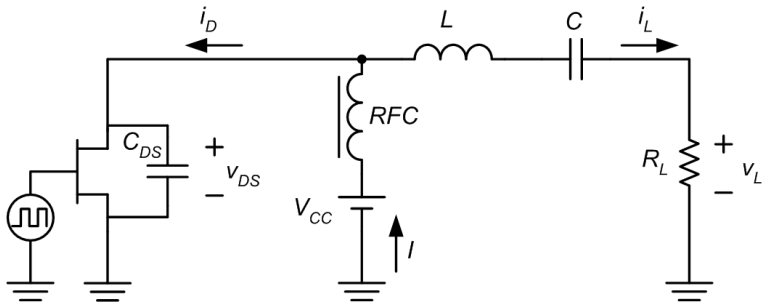

Figure 2.8: Class-E power amplifier.

transistor [105]. The zero-voltage switching Class-E amplifier is shown in Fig.2.8.

The amplifier consists of an RF-choke sufficiently large to ensure nearly DC current in the V_{CC} branch, series LC resonant circuit and shunt capacitance C_{DS}, which can be the same as the transistor's capacitance. The load network of the amplifier is characterized by two resonant frequencies. When the switch is turned ON, the resonant network consists of elements L and C and the resonant frequency is $f_1 = \frac{1}{2\pi\sqrt{LC}}$. When the transistor is turned OFF, the resonant network consists of two connected in series capacitances C_{DS} and C and inductance L, and the resonant frequency is $f_2 = \frac{1}{2\pi\sqrt{L\frac{C\cdot C_{DS}}{C+C_{DS}}}}$. The frequency f_2 in Class-E amplifiers is higher than the operating frequency f_C while frequency f_1 is lower than frequency f_C. The Class-E operation assumes that during transistor's OFF interval, the capacitance C_{DS} is charged to some maximum voltage and next, before the $OFF-ON$ transition occurs, it is discharged to a zero voltage, avoiding the turn-on loss. The optimum operation of Class-E amplifiers assumes two conditions: zero drain-source voltage and zero voltage derivative, $v_{DS} = 0$ and $\frac{dv_{DS}(\omega t)}{d(\omega t)} = 0$ at the turn-ON instant $\omega t = 2\pi$ which is seen in Fig.2.9. A parameter that limits the operation of the RF Class-E power amplifier is the maximum frequency dependent upon parasitic capacitance of a transistor used,

$$f_{C_{max}} \approx 0.05066\frac{P_L}{C_{DS}V_{cc}^2} \tag{2.12}$$

The parasitic capacitance C_{DS} may appear as a limiting factor for the carrier frequency

in the RF range. The Class-E PA can be used for amplifying constant-envelope RF signals with high power efficiency. The amplification of varying-envelope RF signals can be done by modulating the supply voltage for the amplifier [88].

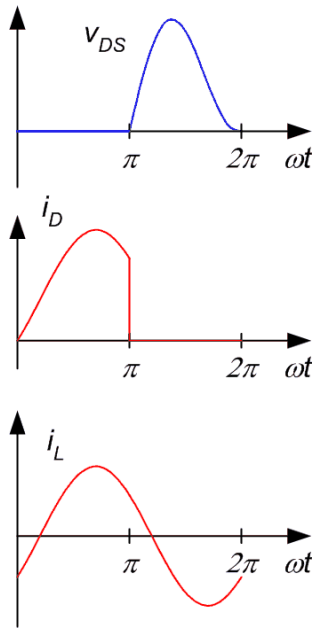

Figure 2.9: Current and voltage waveforms for Class-E amplifier.

2.1.9 Conclusion

The summary of efficiencies and output power capabilities for amplifiers reviewed in this section is listed in Tab.2.1. A linear amplification requires that transistors operate in active regions, which in turn causes power dissipation in the amplifier. The best linearity is achieved in Class-A, but at the same time the amplifier yields the lowest power efficiency.

Table 2.1: Summary for classes of operation.

Class of operation	Output power capability	Maximum drain efficiency
A	0.125	50%
B	0.125	78.54%
AB	0.125 to 0.134	50% to 78.54%
C	0.125 to > 0	78.54% to $< 100\%$
VSCD, CSCD	0.159	100%
E	0.0981	100%
F_3	0.1443	90.67%
F_2	0.1545	90.03%
F_∞	0.1592	100%

The improvement in efficiency is achieved by moving the operating point towards or below the pinch-off voltage in classes AB, B, and C. The efficiency increases however at the cost of linearity of the amplifiers. In theory 100% drain efficiency is achievable in amplifiers of classes D, E, F, which however cannot be used directly for amplifying varying-envelope RF signals without inducing a distortion. The interest of this work is in achieving high linearity and high efficiency in an RF PA. The techniques allowing for the use of nonlinear devices for amplifying RF signal with varying envelope without inducing distortion are described in the next section.

2.2 PA efficiency improvement

Nonlinear amplifiers of classes D, E, F allow for power efficient amplification of a constant envelope signal, however their direct use for amplifying RF signals with varying envelope would result in a distortion and a subsequent expansion of the RF bandwidth. On the other hand, linear amplifiers of classes A, AB or B suffer from low drain efficiency when the RF signal is characterized by large *PAPR*. This section describes power amplifiers systems, where nonlinear devices are employed to achieve a high efficiency, while appropriate conversion of the RF signal allows for a maintenance of a linear input-output relationship.

2.2.1 Envelope tracking

The efficiency of a linear RF amplifier of Class-A, AB or B depends on the ratio of output amplitude to supply voltage. It achieves a maximum when $\frac{V_L}{V_{CC}} = 1$, and decreases when $\frac{V_L}{V_{CC}}$ decreases. To avoid the efficiency degradation, the amplifier with envelope tracking (ET) changes the supply voltage V_{CC} for a linear PA accordingly with the change of the RF amplitude, such that $\frac{V_L}{V_{CC}}$ is always close to unity.

In theory, the maximum drain efficiency of Class-A of 50% or 78.54% for Class-B would be possible for an RF signal characterized by a large value of PAPR if ET was applied. The varying V_{CC} can be supplied from a high efficiency switchmode power supply $(SMPS)$ as it is shown in Fig.2.10 [111]. In practical implementation, the magnitude response of the $SMPS$ should be characterized by a roll-off frequency at least two times larger than the RF bandwidth, which is needed for reconstruction of an envelope signal. On the other hand, switching frequency of the $SMPS$ should be several times higher than the converter's roll-off frequency to reduce pulsation of the modulated supply voltage V_{CC}.

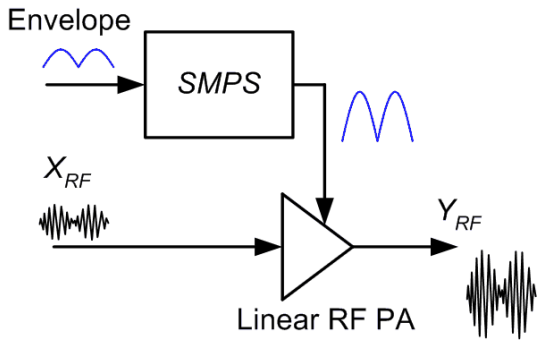

Figure 2.10: Power amplifier with envelope tracking.

As a consequence, the power losses in the RF PA with ET increase as the RF bandwidth increases. To alleviate the need for large switching frequency of the $SMPS$, the envelope amplifier can be designed as a combination of a narrowband and power efficient switching stage and low power, linear stage [109]. The ET can be simplified further by replacing the $SMPS$ with a simple circuit switching between two or more supply voltages as demonstrated in [115]. In practical realization the linearity of an amplifier with ET is affected by knee voltage and nonlinear capacitances causing AM-AM and AM-PM distortion [111, 114, 116].

The Class-AB RF amplifiers with ET have been reported to achieve PAE in a range of 30% to less than 50% for $5\,MHz$ to $20\,MHz$ LTE signals [109, 114].

2.2.2 Envelope elimination and restoration

The envelope elimination and restoration (EER) technique was proposed by Kahn [80] in 1952. In the EER transmitter the RF signal with varying envelope is divided into phase modulated and envelope signals. The phase signal is amplified by nonlinear RF amplifier, while the V_{CC} for the amplifier is supplied from a $SMPS$ or Class-D amplifier driven by a pulse-width-modulated envelope, similarly to the amplifier in ET. In contrast with the ET technique, the output RF amplitude in the EER is shaped by the supply voltage, and it is ideally a linear function $ENV(t) = kV_{CC}(t)$. Consequently, sufficient roll-off frequency of the $SMPS$ is necessary to avoid an amplitude modulation distortion caused by bandlimiting of the envelope signal. The concept of an EER transmitter is depicted in Fig.2.11.

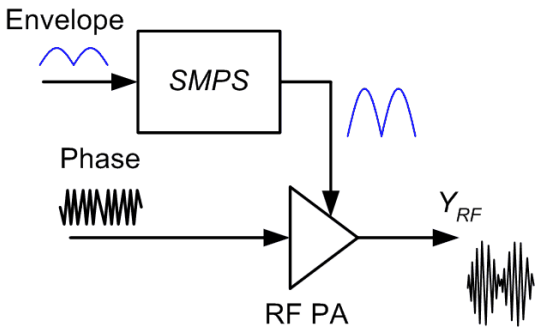

Figure 2.11: EER transmitter.

The RF output is restored after correcting the delay between phase and envelope signals, which occurs in the transmitter due to different group delays in the two branches. The amplifier system can be power efficient (a 100 % of efficiency in theory is possible) and linear. Practical implementations of an EER transmitter suffer power losses occurring in both, the $SMPS$ and the RF amplifier. Also, the EER transmitter exhibits an AM and PM distortion. The AM distortion is caused by a finite bandwidth of the $SMPS$ and by a nonlinear relation of amplifiers output amplitude to the supply voltage V_{CC} [88, 116]. The PM distortion is caused by nonlinear capacitances in the PA circuit. In modern wireless

communication systems, the EER PA is often referred to as a polar transmitter due to the use of polar coordinates - radius and angle - to express the RF signal composed of in-phase and quadrature components I and Q.

$$X_{RF}(t) = I(t)\cos(\omega_C t) + Q(t)\sin(\omega_C t) = ENV(t)\cos(\omega_C t + \phi(t))$$

A digitized polar transmitter (DPT) was proposed by Wang [73], as a sub-class of the EER transmitter. In the DPT a pulse-modulation of a phase signal allows incorporating both, envelope and phase in one signal. The pulse-modulated phase signal drives a nonlinear, RF PA which amplifies the phase signal-when the digitized envelope is 'one', and it remains idle when the digitized envelope is 'zero'. The amplified RF signal is reconstructed after band-pass filtering of the nonlinear PA's output. The DPT system employing a $LP\Sigma\Delta$ modulator for digitizing the envelope signal is shown in Fig.2.12.

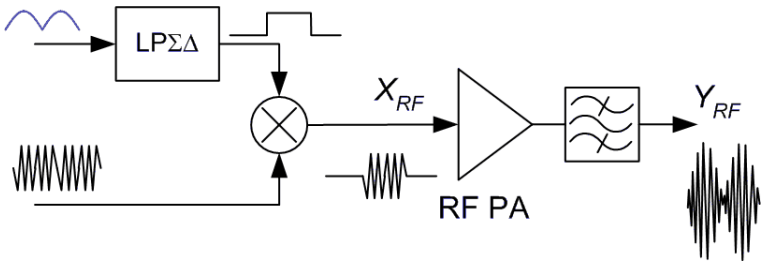

Figure 2.12: Polar transmitter with digitized envelope signal.

In theory, the amplitude and phase distortion of the DPT are eliminated due to binary operation (the amplifier is driven by the phase signal or it remains idle) of the amplifier, while maintaining good efficiency. In practice a large oversampling ratio is necessary when a 2-level $\Sigma\Delta$ modulation is used to encode the envelope signal in order to achieve sufficient $ACLR$. As the transitions between the idle state and switchmode operation are very short, the RF PA in DPT must operate over a much wider frequency range than the RF PA in the conventional EER transmitter. The finite bandwidth of a RF PA limits the sampling frequency of the $LP\Sigma\Delta$ modulator which in turn causes $ACLR$ degradation due to quantization noise present in the output of the transmitter.

2.2.3 Outphasing amplifier

The outphasing technique was introduced by Chireix in 1935 [13] and was studied in [14, 15]. The outphasing technique uses a sum of two constant-amplitude, phase modulated signals to create the RF, amplitude modulated signal.

$$X_{RF}(t) = ENV(t)\cos(\omega_C t + \phi(t)) = X_1 + X_2$$

where

$$X_1 = \tfrac{1}{2}\cos(\omega_C t + \phi(t) + \psi(t))$$

$$X_2 = \tfrac{1}{2}\cos(\omega_C t + \phi(t) - \psi(t))$$

$$\psi(t) = \arccos(ENV(t))$$

Consequently, the outphasing amplifier system employs two RF power amplifiers, whose outputs are summed creating the RF signal. The outphasing power amplifier system is shown in Fig.2.13.

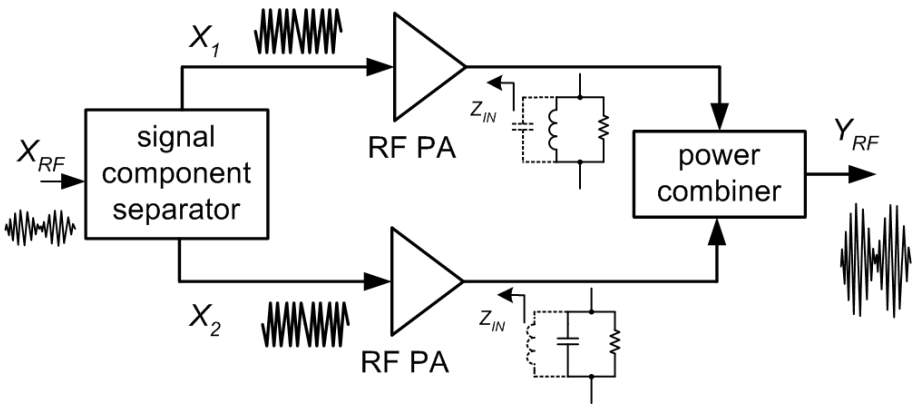

Figure 2.13: Outphasing power amplifier.

The advantage of the outphasing technique is that the two phase signals X_1, X_2 can be amplified by nonlinear devices offering high (theoretically up to 100%) efficiency. Despite the use of nonlinear amplifiers, the efficiency of the system is degraded in the course of power combination [15–18]. It is because the impedance seen by each of the RF amplifiers depends on the phase difference between the two signals X_1 and X_2 and has

imaginary parts for all angles except $\psi = 90^\circ$ when both signals are in-phase. When this condition occurs, the impedance seen by both amplifiers is real, and RF amplitude has its maximum value. As the phase difference decreases towards $\psi = 0$, the load impedance becomes a sum of real and imaginary parts, which is represented by shunt capacitance and inductance in Fig.2.13, and the amplitude of Y_{RF} decreases towards zero. The reactive components in load impedances contribute to power efficiency degradation in the RF amplifiers. An optimization of efficiency in the outphasing amplifier can be achieved by the addition of shunt susceptances in the inputs to the power combiner [15], which cancels the imaginary part of the impedance seen by the PA at some chosen angle ψ. The output of the amplifier is also affected by the nonlinearity of the Chireix-outphasing combiner and the imbalance between the two amplifiers branches, which makes the design of predistortion for the amplifier a challenging task [17].

2.2.4 Class-S power amplifier

The use of the *BP*ΣΔ modulator to drive an RF switchmode power amplifier had been suggested by Schreier in [96], and the power amplifier system was described by Jayaraman in 1998 [24]. The Class-S power amplifier uses a *BP*ΣΔ modulator to encode the RF input signal into a 2-level waveform which subsequently drives a Class-D amplifier. The band pass filter attenuates the quantization noise induced by the *BP*ΣΔ modulator, restoring the amplified RF signal at the antenna. The scheme of a Class-S power amplifier system is shown in Fig.2.14.

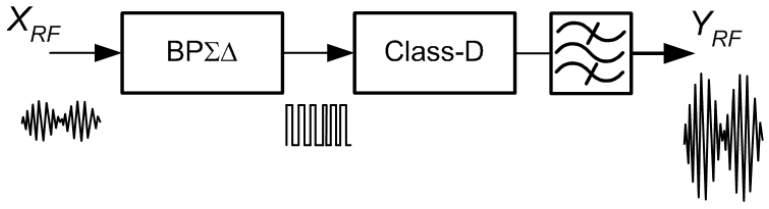

Figure 2.14: Class-S power amplifier.

The power amplifier in a Class-S amplifier can be either a voltage-switching Class-D ($VSCD$) or a current-switching Class-D (or $CSCD$). The $VSCD$ produces a 2-level voltage waveform while the $CSCD$ produces a 2-level current waveform. The band-pass-filter exhibits large impedance at frequencies below and above the amplified RF frequency, and is matched with a load impedance at the selected RF frequency when the $VSCD$ is used which is depicted in Fig.2.15(A). The output from the $BP\Sigma\Delta$ modulator is aperiodic, and switching transitions in a Class-D amplifier may occur when drain currents are zero or have positive or negative values. Subsequently, the transistors in a Class-D amplifier must operate as bidirectional switches. In theory the 2-level operation ensures that transistors operate in saturation or cut-off regions only, yielding 100 % efficiency and a linear relationship between the $BP\Sigma\Delta$ modulator's input and the BPF output. In practice a large oversampling ratio is needed to maintain low quantization noise power in adjacent channels. The $BP\Sigma\Delta$ modulator is typically assumed to operate at a sampling frequency two to four times higher than the carrier frequency of the RF signal. Such high sampling frequency for a GHz carrier results in pulse durations as short as a fraction of a nano second. The high sampling frequency becomes a problem for implementation of a $BP\Sigma\Delta$

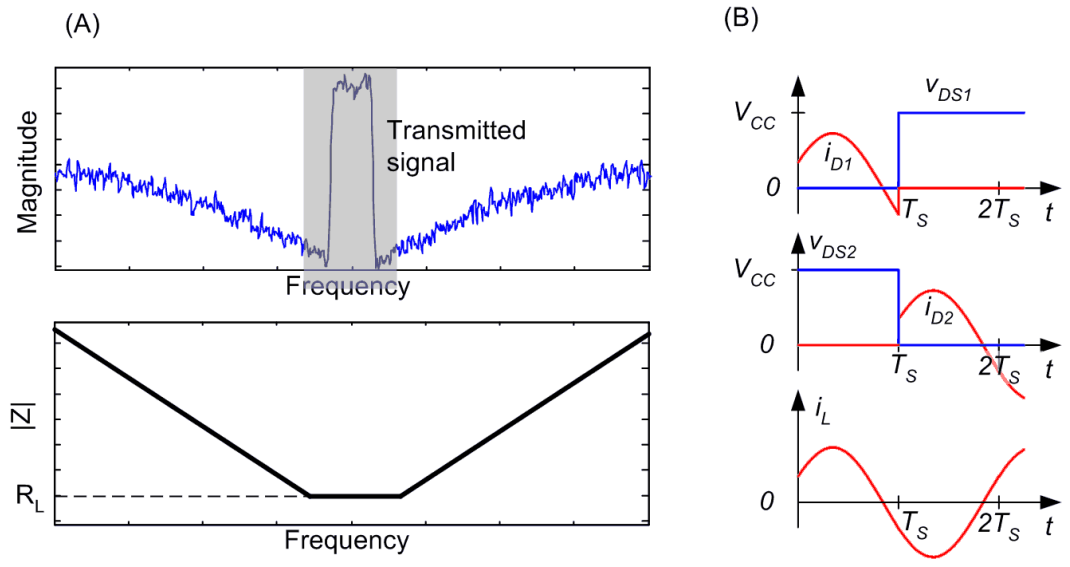

Figure 2.15: Class-S power amplifier with VSCD. (A) Band pass filtering. (B) Current and voltage waveforms.

modulator, but it also requires a very broadband Class-D amplifier. The efficiency and both, AM and PM distortion are influenced by the response of transistors in a Class-D amplifier to the broadband 2-level signal as well as by nonlinearity of the devices.

2.2.5 Dynamic load modulation

A dynamic load modulation (LM) technique was proposed by Raab [20]. The power delivered by a RF PA to the load, and subsequently the RF amplitude depend on the impedance seen by the RF PA. This relationship is used to modulate the RF amplitude by tuning an impedance matching network in the RF power amplifier.

In a practical circuit, LM in the RF power amplifier can be obtained by changing the voltage supplied to one or more varactors in the matching network. The appropriate selection of a matching network allows for reconstruction of the RF amplitude in the output of the power amplifier. Since the output amplitude variation depends on the tuning voltage(s), the RF amplifier can be nonlinear. The amplifier is similar to an EER in that both amplifiers require envelope-voltage signals. The advantage of the amplifier with dynamic load modulation over the EER transmitter however is that the envelope-voltage waveform in the former does not carry power, and therefore its generation is more power efficient than the use of a $SMPS$ in the EER transmitter.

The tuned matching network should be designed such that the impedance seen by the amplifier tracks the locus of the optimal load impedance of the selected RF PA over the entire dynamic range of the output amplitude. The accurate tracking of the optimal impedance locus requires simultaneous tuning of usually more than one element, which increases complexity of this power amplifier.

The amplitude and phase distortion in the amplifier are caused by a phase variation in the tuned matching-network and the nonlinear relation of the RF amplitude to the tuning voltage. Fig. 2.16 shows a Class-E amplifier with LM.

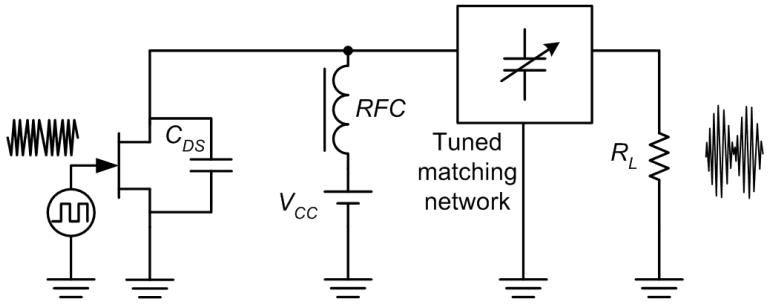

Figure 2.16: Class-E power amplifier with dynamic load modulation.

2.2.6 Conclusion

The techniques presented in this section offer an improvement in efficiency in comparison with a linear operation of power amplifiers of classes A, B or AB. The improvement is however achieved at the cost of increased complexity of amplifier systems. The brief summary of the described techniques is given in Tab.2.2.

The main interest of this work is in the two PA systems employing ΣΔ modulation for digitizing amplified signals, Class-S and *DPT*. The two amplifiers systems suffer the drawback of a very wideband requirement of the switchmode PA $(SMPA)$, but their strong advantage is relatively low complexity and reconfigurability. The digital power amplifiers allow for adaptation of transmitted signal's frequency and control over the noise in down link or adjacent channels, programmable by a *DSP* present in the transmitter.

This work focuses on problems associated with modulation of the RF signal and subsequently, the second part of this chapter describes principles of ΣΔ modulation.

Table 2.2: Summary.

Envelope tracking
Advantages
Efficiency improves while using linear PA
Drawbacks
Complexity
Some power is lost in *SMPS*
The maximum efficiency cannot reach 100 %
Envelope elimination and restoration
Advantages
Theoretically up to 100 % power efficient
No need for broadband impedance matching
Drawbacks
Complexity
Multiplication of efficiency figures of an *SMPS* and *SMPA*
Digitized polar transmitter
Advantages
Theoretically up to 100 % power efficient
Low complexity - only one, nonlinear PA is needed
Drawbacks
The PA must be very wideband
High sampling frequency of a *LP*ΣΔ modulator is needed for reducing noise in adjacent channels
Outphasing power amplifier
Advantages
PAs are driven by constant envelope signals
Drawbacks
Complexity of the PA system
Optimization of impedances is needed
Complexity of predistortion
Class-S
Advantages
Low complexity of signal processing, the RF signal is directly modulated by ΣΔ modulator
The use of digital modulation allows for control of transmitting frequency and noise in adjacent channels
Drawbacks
High sampling rate of ΣΔ modulator is needed
The PA must be very wideband
Dynamic load modulation
Advantages
The amplitude modulation is done by voltage signal
Drawbacks
Complexity of the matching network
Unsuitable for applications where the PA should be reconfigurable
Limited dynamic range

2.3 ΣΔ modulation

ΣΔ modulation plays an important role in *DPT* and Class-S amplifiers, providing a 2-level, noise shaped drive signal for switchmode power amplifiers. The signal to-noise-ratio and the maximum RF power in the output of a digital power amplifier depend on the modulator's sampling frequency and noise transfer function. This section describes the principles of ΣΔ modulation.

2.3.1 Quantization of an input signal

Quantization constrains the wordlength of an input to the quantizer to lower, multibit or a singlebit wordlength. Typically, the quantizer in a ΣΔ modulator is 1-bit due to robustness to distortion caused by displacement of the levels. For a zero-mean input the 2 levels of the quantizer are usually equidistant from zero, such as in the input-output transfer characteristic shown in Fig.2.17(B).

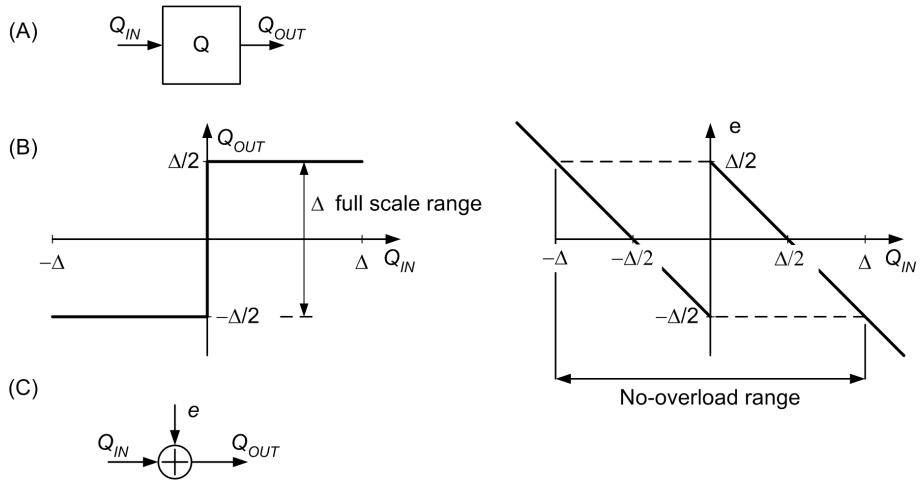

Figure 2.17: (A) Symbol of a quantizer. (B) Input-output characteristic and the resulting quantization error. (C) Linear model of the quantizer.

The amplitude of an input to the quantizer is mapped to the nearest level, producing quantization error in the output sequence. Subsequently the output of the quantizer can be expressed as a linear function of its input and the addition of the quantization error e,

$$Q_{OUT} = Q_{IN} + e \tag{2.13}$$

The range of the input signal, for which the absolute value of the error e does not exceed half of the quantization step $\Delta/2$ is called the no-overload range, and it is depicted in Fig.2.17(B) for the 1-bit quantizer. The full-scale range of a quantizer is defined as the difference between maximum and minimum levels of a quantizer.

The quantization error sequence e is often modeled as a white noise signal, independent of the quantizer's input Q_{IN} [69], and whose distribution in the range of $\langle -\Delta/2; \Delta/2 \rangle$ is uniform. When these conditions are met, the average power of the error sequence is,

$$e^2 = \frac{\Delta^2}{12} \tag{2.14}$$

When the white-noise error signal has power distributed uniformly between frequencies $-f_{\Sigma\Delta}/2; f_{\Sigma\Delta}/2$, where $f_{\Sigma\Delta}$ is a sampling frequency of the modulator, the in-band power of the white-noise quantization error is [71],

$$e_{INB}^2 = \frac{e^2}{OSR} \tag{2.15}$$

and OSR is an oversampling ratio, $OSR = \frac{f_{\Sigma\Delta}}{2BW}$. The above assumptions yield a linear model of a quantizer with the white-noise error signal e added as shown in Fig.2.17(C).

2.3.2 Single Feedback topology of ΣΔ modulator

The single feedback topology of a ΣΔ modulator is shown in Fig.2.18. It consists of a quantizer and a loop filter with a single feedback path. When the quantizer model described in the previous section is used to analyze the modulator, then its output becomes

$$Q(z) = X(z)\frac{H(z)}{1+H(z)} + E(z)\frac{1}{1+H(z)} = X(z)STF(z) + E(z)NTF(z) \tag{2.16}$$

The two transfer functions: STF and NTF are the signal transfer function and the noise

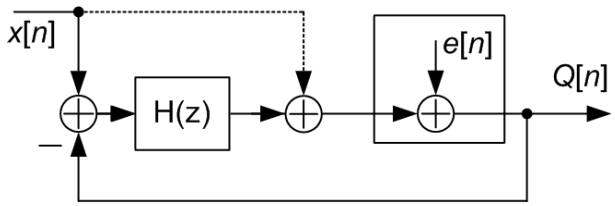

Figure 2.18: Single feedback topology.

transfer function of the ΣΔ modulator.

$$\begin{aligned} STF(z) &= \frac{H(z)}{1+H(z)} \\ NTF(z) &= \frac{1}{1+H(z)} \end{aligned} \tag{2.17}$$

The STF in the ΣΔ modulator should be characterized by a flat magnitude response, while the NTF is chosen such that it provides maximum suppression of the quantization noise in the selected band of interest. As a consequence, the quantization noise is shaped outside of the signal band yielding high inband SNR in the output of the modulator. A feedforward path in the single feedback topology can be added for ensuring unity STF, which is shown as a dashed line in Fig.2.18.

A first order, low-pass ΣΔ ($LP\Sigma\Delta$) is described by a noise transfer function having single zero at a zero frequency,

$$NTF(z) = 1 - z^{-1} \tag{2.18}$$

The first-order NTF suppresses quantization-noise at low frequencies shaping its power towards $f_{\Sigma\Delta}/2$. The noise transfer function in the single feedback topology also defines the signal transfer function in the modulator through (2.17), although this relationship is not the same in all ΣΔ structures. The transfer function of the loop filter becomes $H(z) = \frac{z^{-1}}{1-z^{-1}}$, and the input x is simply delayed in the modulator's output by one clock cycle by the signal transfer function $STF(z) = z^{-1}$. When such a modulator is supplied with an input signal of a low frequency, the inband quantization noise is of much lower magnitude than the modulator's input signal.

In general, the degree of noise shaping is controlled by placement of zeros in the noise transfer function. The numerator of an arbitrary order (ORD) noise transfer function with all zeros superimposed at DC becomes $\left(1-z^{-1}\right)^{ORD}$. In theory, such a $LP\Sigma\Delta$ modulator would be characterized by inband noise suppression expressed as a function of oversampling ratio and order of the NTF by [69]

$$e_{INB}^2 = \frac{\pi^{2\cdot ORD}\Delta^2}{12\cdot(2\cdot ORD+1)\,(OSR)^{2\cdot ORD+1}} \tag{2.19}$$

yielding excellent SNR for high order modulators also at low OSR. In practice, the inband noise power calculation in (2.15) assumes the linear quantizer model, which is not always true, since the error signal added in the quantizer depends on the input to the ΣΔ modulator. In practice, the inband error suppression, and therefore the SNR, are limited by the stable operation of a modulator with a 2-level quantizer. This is discussed in the next section.

2.3.3 Stability of a ΣΔ modulator with 2-level quantizer

A ΣΔ modulator is considered to be unstable, when oscillations occur in the quantizer-input Q_{IN}, whose amplitudes largely exceed the quantizer's no-overload range. Such large amplitude oscillations of Q_{IN} result in oscillations of a quantization error, whose spectral components can not be suppressed by zeros of NTF, and fall into band of interest causing severe degradation of SNR. This runaway behavior can be controlled by limiting the maximum absolute value of noise transfer function $||NTF||_\infty$ and amplitude of an input signal [97]. In order to prevent the unstable operation in modulators of order higher than two, the $||NTF||_\infty$ should be limited by the appropriate placement of poles in the denominator of NTF. Lee's criterion for stability of a 2-level ΣΔ modulator says that the modulator should be characterized by maximum gain $||NTF||_\infty < 2$ [102]. This criterion is not universally correct for modulators of different orders, but it can be used as an initial

indication when synthesizing the NTF. Empirical values of $||NTF||_\infty$ for stable, high order modulators can be found in [97], where it was controlled by applying Butterworth poles in the noise transfer function. The general expression for a noise transfer function for modulators of order higher than two becomes,

$$NTF(z) = \frac{1 + a_1 z^{-1} + ... + z^{-ORD}}{1 + b_1 z^{-1} + ... + b_{ORD} z^{-ORD}} \tag{2.20}$$

When Butterworth poles arrangement is used, the increase of the low pass cut-off frequency increases the $||NTF||_\infty$, improving suppression of the in-band quantization noise and SNR. The maximum gain of noise transfer function should be however limited to ensure stable operation of the modulator. The use of a low-pass Butterworth arrangement can be advantageous when the NTF and STF share the same poles. In such a scenario, the STF becomes a low-pass function, which can be useful when an input signal to the modulator is sampled at a rate much lower than the sampling frequency of a ΣΔ modulator, and interpolation of the signal is required.

2.3.4 Nonlinearity in multilevel ΣΔ modulators

According to equation (2.14), the quantization error power reduces as the quantization step Δ decreases or equivalently, as the number of levels in the quantizer increases. In theory, the use of a multilevel quantizer allows for reduction of quantization noise in the output of the modulator, and reduction of a sampling rate in comparison to the modulator with a 2-level quantizer. Despite these theoretical benefits, practical implementations of multilevel quantizers add nonlinearity problems to the modulator design.

Let us consider a ΣΔ modulator operating as a digital to analog converter (DAC). The modulator consists of the loop filter $H(z)$, the multilevel quantizer and the feedback loop. Subsequently, the output of the modulator is connected to the multilevel DAC and to the lowpass filter as shown in Fig.2.19(A). When the quantizer is M-level, and $M > 2$, a dis-

placement of one or more of the levels in the *DAC* causes an addition of an error $e_{DAC}(t)$ as shown in Fig.2.19(B). Since the addition of the $e_{DAC}(t)$ occurs outside the feedback loop of the modulator, this error remains unshaped and causes nonlinear operation of the ΣΔ digital to analog converter. This property applies to modulators having any number of levels higher than two, e.g. 4-level quantizer whose characteristic is shown in Fig.2.19(C).

The situation changes when the quantizer has two levels. When in such case one or both of the levels are displaced in the *DAC* by some constants a_1 and a_2 as shown in Fig.2.19(D), the subsequent output of the modulator is added a *DC* component and it is scaled by a constant gain, but the converter preserves linear relation between the digital input and the analog output. Very often both, the *DC* component and the scaling do not impose problems for zero-mean signals.

Due the above problems encountered in multilevel ΣΔ modulators, inherently linear 2-level ΣΔ modulation is assumed in this work.

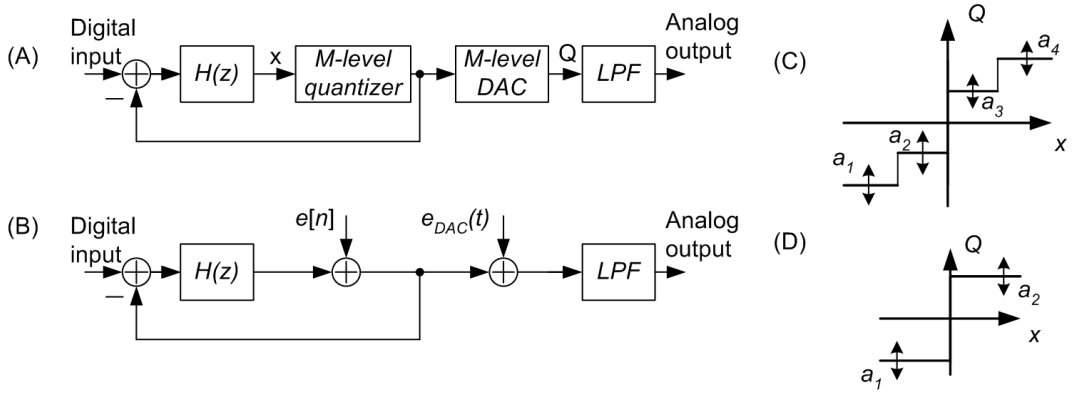

Figure 2.19: ΣΔ modulator operating as a digital to analog converter. (A) Modulator with a multilevel quantizer. (B) Model with additive errors. (C) 4-level *DAC*. (D) 2-level *DAC*.

2.3.5 ΣΔ modulator for a digital power amplifier

This section discusses properties of a *LP*ΣΔ modulator of order one to three. The structure under analysis is a modulator with distributed feedback. Being one of the most common structures, this *LP*ΣΔ modulator is feasible for digital implementation where high sampling frequency is of importance. Transfer functions are obtained in the course of linear

analysis and are discussed, providing insight into behavior of the modulator. The transfer functions for quantization errors $e_1 - e_4$ and signal transfer function are specific for this particular structure, but the discussion on the choice of noise transfer function is valid in any other ΣΔ modulator structure.

2.3.5.1 *LP*ΣΔ modulator with distributed feedback

The *LP*ΣΔ modulator is created by placing delaying integrators and distributed weighted feedback of the output of the quantizer. It is shown in Fig.2.20 for a third order modulator.

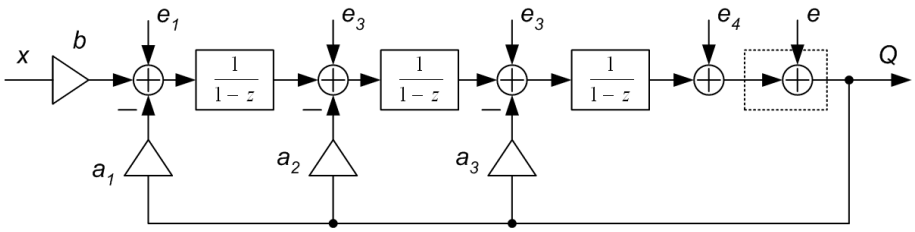

Figure 2.20: Third order *LP*ΣΔ modulator.

The error sequences e_{1-4} are added across the modulator in order to account for quantization of the signal done before the integrators blocks. The error e_1 represents quantization of the input signal x, while e_{2-4} represent quantization error induced by scaling of the signal between subsequent integrators stages. The linear analysis of the modulator of third order leads to expression for modulator output:

$$Q_3(z) = \frac{\left\{[b_1 X(z) + E_1(z)] + E_2(z)(1-z) + E_3(z)(1-z)^2 + [E_4(z) + E(z)](1-z)^3\right\}}{(1+a_1+a_2+a_3) - z(3+a_2+2a_3) + z^2(3+a_3) - z^3} \tag{2.21}$$

Using equation (2.21), STF, NTF and transfer functions for signals e_{1-4} are,

$$STF = \frac{b_1}{(1+a_1+a_2+a_3) - z(3+a_2+2a_3) + z^2(3+a_3) - z^3} \tag{2.22}$$

$$NTF = TF_{E_4} = \frac{(1-z)^3}{(1+a_1+a_2+a_3) - z(3+a_2+2a_3) + z^2(3+a_3) - z^3} \tag{2.23}$$

$$TF_{E_1} = \frac{1}{(1+a_1+a_2+a_3) - z(3+a_2+2a_3) + z^2(3+a_3) - z^3} \tag{2.24}$$

$$TF_{E_2} = \frac{(1-z)}{(1+a_1+a_2+a_3)-z(3+a_2+2a_3)+z^2(3+a_3)-z^3} \tag{2.25}$$

$$TF_{E_3} = \frac{(1-z)^2}{(1+a_1+a_2+a_3)-z(3+a_2+2a_3)+z^2(3+a_3)-z^3} \tag{2.26}$$

The transfer functions in the modulator are discussed in the following sections.

2.3.5.2 Noise transfer function selection

Two important criteria should be taken into consideration when choosing a modulator for a digital switchmode power amplifier: what is the needed signal to noise ratio, and what maximum power level should the digital power amplifier deliver to the load.

As it was discussed in Section 2.3.3, the suppression of a quantization noise improves when modulator order increases. While modulators of first and second orders maintain stable operation for noise transfer function in the form of $\left(1-z^{-1}\right)^n$, $n = 1, 2$, modulators of higher order require the maximum gain of the NTF to be limited by appropriately arranged poles. While increasing the $||NTF||_\infty$ norm improves the SNR , it also limits the stable input range in higher order ΣΔ modulators, subsequently limiting the maximum power reconstructed in the output of a digital power amplifier.

Simulated signal to noise ratios as a function of a normalized power of an input signal supplied to a third order $LP\Sigma\Delta$ modulator are shown in Fig.2.21 for $||NTF||_\infty$ of 1.25, 1.5 and 1.7. The input was a single tone signal of frequency $f_0 = 0.005 f_{\Sigma\Delta}$ and the oversampling ratio used for calculating SNR was $OSR = 50$. The modulator whose $||NTF||_\infty = 1.7$ yielded the highest peak SNR, but it also exhibited the lowest stable input amplitude range of 0.74, relative to full scale. The subsequent reduction of the $||NTF||_\infty$ allowed for higher input amplitude at the cost of reducing the peak SNR by $12\,dB$ when the $||NTF||_\infty = 1.25$. On the other hand, the maximum output power increased by $2.5\,dB$

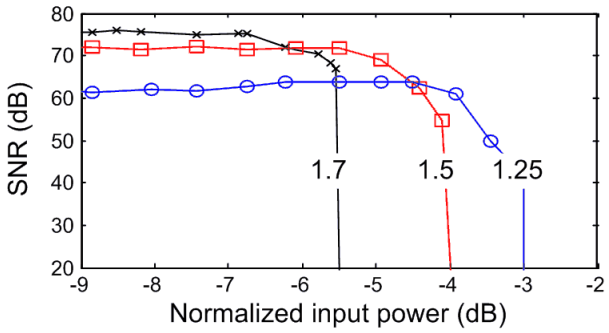

Figure 2.21: Simulated *SNR* vs. input signal's power for three, third order noise transfer functions, $||NTF||_\infty = 1.25$, $||NTF||_\infty = 1.5$ and $||NTF||_\infty = 1.7$.

while maintaining stable operation of the modulator.

From the perspective of an analog to digital (or digital to analog) conversion, the *SNR* in the output of an *ADC* (or *DAC*) employing a ΣΔ modulator is a crucial parameter determining the quality of the converter, and the effective number of bits (*ENOB*) in the converted signal. While high resolution is usually required, the maximum amplitude relative to full scale of the converter is not of first importance. In contrast, *SNR* requirement in wireless communication is not as critical for the transmitted signal as in *DAC* applications. The transmitter should be characterized by *ACLR* of $33\,dB$ in adjacent and $43\,dB$ in alternate channels to fulfill spectral mask requirements in UMTS. While $40dB$ of an *SNR* corresponds to a 1% of an EVM, an extensive increase of the *ACLR* will not yield significant improvement to the transmitted RF signal. Finally, the *SNR* of the output of an RF transmitter is often limited by nonlinearity of an amplifier, which questions the use of high order ΣΔ modulator characterized by an excellent *SNR*. For the above reasons first and second order ΣΔ modulators, offering moderate *SNR* performance, but being capable of delivering higher output power can be advantageous in a digital power amplifier system over high order modulators.

The modulators used across this work are of order one, two and three. The NTF for the modulators of order two and three have the same maximum gains $||NTF||_\infty = 1.5$. The magnitude responses of noise transfer functions for these modulators are shown

in Fig.2.22 while coefficients for the modulator with distributed feedback and NTF zeros/poles are listed in Tab.2.3. The simulated output spectra of the modulators in response to the single tone signal of frequency $f_0 = 0.005 f_{\Sigma\Delta}$, and of amplitudes $Amp = 0.7$ are shown in Fig.2.23(A) and the SNR calculated for the modulators are shown in Fig.2.23(B).

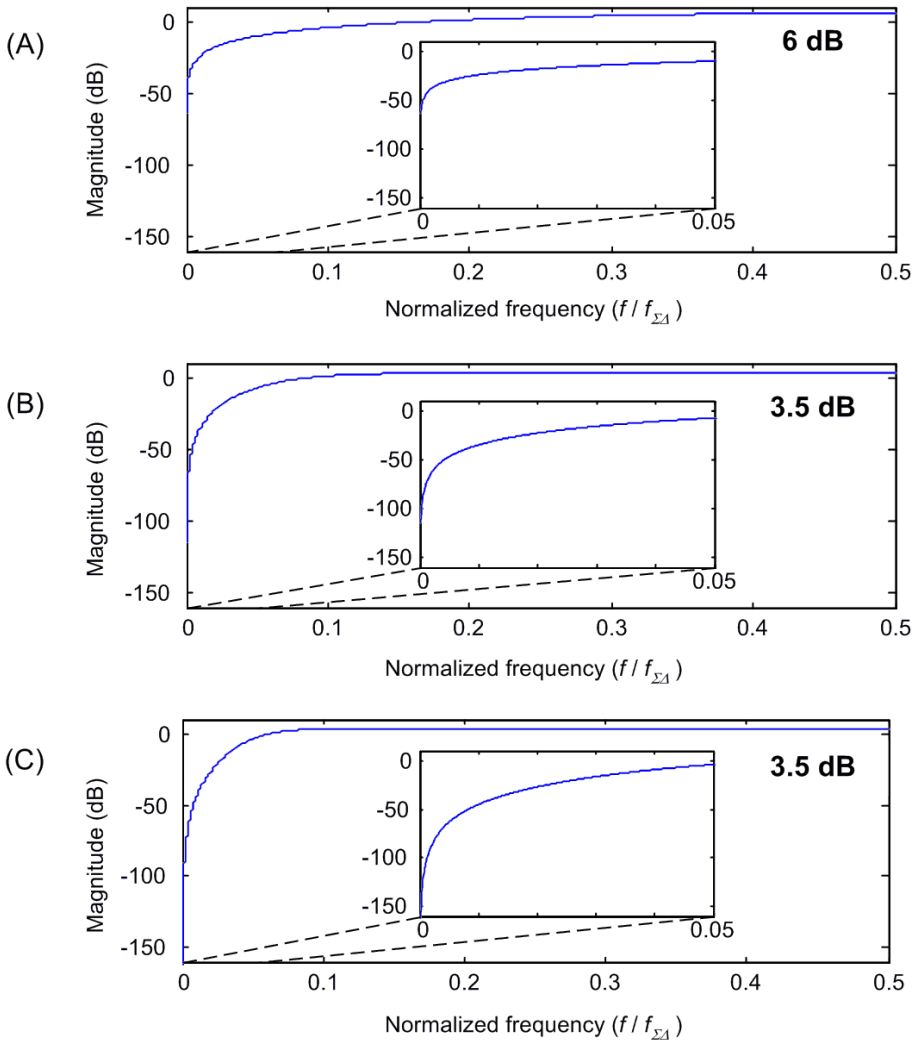

Figure 2.22: Noise transfer function used. (A) First order. (B) Second order. (C) Third order.

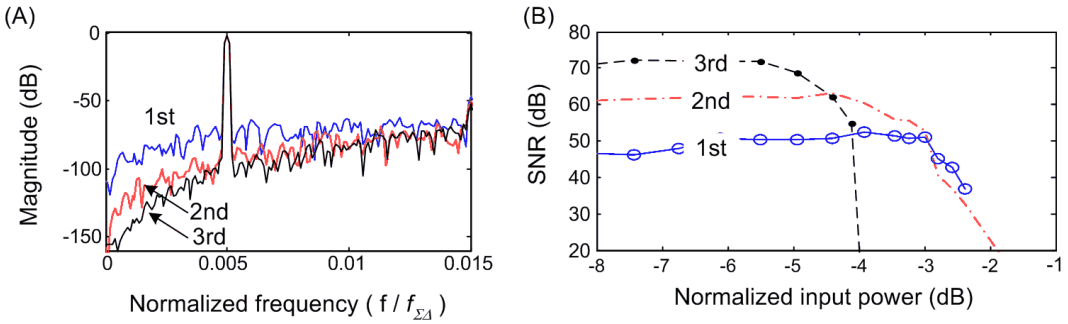

Figure 2.23: Simulated ΣΔ modulators. (A) Output spectra. (B) SNR vs. normalized input signal's power ($OSR = 50$).

Table 2.3: Coefficients for *CIFB LP*ΣΔ modulators.

Order	a_1, b_1	a_2, b_2	a_3, b_3	a_4, b_4	Zeros	Poles
1	1	-	-	-	1	0
2	0.216	0.775	$b_3 = 1$	-	1, 1	$0.6126 \pm j0.2574$
3	0.044	0.288	0.8	$b_4 = 1$	1, 1, 1	$0.7654 \pm j0.2793$; 0.6694;

Peak *SNR* values were $52.3\,dB$, $63.2\,dB$ and $71.3\,dB$ for first, second and third order modulators respectively. As observed from the figure, the third order modulator offers the highest *SNR*, but it also has the lowest stable input range and it becomes unstable when the input amplitude exceeds $Amp = 0.88$ normalized to the full scale range of the quantizer $(P_{IN} = -4.1\,dB)$. In contrast, modulators of first and second order maintained relatively high *SNR* for signal's with amplitudes reaching $Amp = 1$ $(P_{IN} = -3\,dB)$. Consequently, a Class-D power amplifier driven by the above third order modulator would offer 22.6 % less of the maximum output power than if a first or second order ΣΔ was used.

2.3.5.3 Signal transfer function

The signal and noise transfer functions of the ΣΔ modulator of Fig.2.20 share the same poles. When the NTF poles have Butterworth arrangement, then the resulting all-pole STF has properties of a low-pass filter, with cut-off frequency close to that of the Butterworth filter. Signal transfer functions for modulators of order 1-3 having poles listed in Tab.2.3 are shown in Fig.2.24. Only the first order modulator's STF has a flat magnitude response, and the second and third order modulator yield a low-pass transfer functions

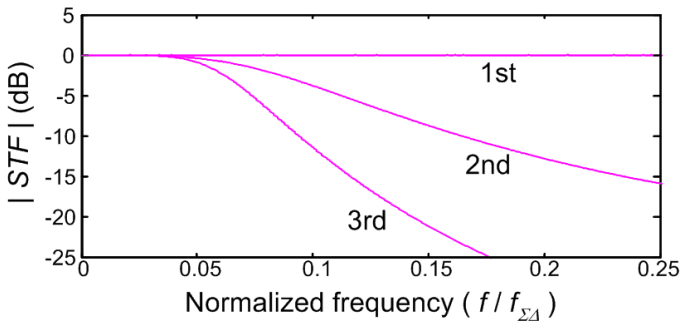

Figure 2.24: Signal transfer functions for CIFB *LP*ΣΔ modulators.

with $3\,dB$ cut-off frequencies at $f_{coff} \approx f_{\Sigma\Delta}/11$ and $f_{coff} \approx f_{\Sigma\Delta}/16$. This relatively low cut-off frequency can be useful when the digital hardware preceding the modulator should operate at a sampling frequency being a fraction of the frequency $f_{\Sigma\Delta}$. In such case, the low-pass STF can eliminate the need for an additional low-pass filter.

2.3.5.4 Noise shaping

A general property of the $LP\Sigma\Delta$ modulator with distributed feedback is that the in-band suppression of an error is stronger the closer its addition occurs to the quantizer's input, which is observed in equations (2.23)-(2.26). Errors e_{2-4} are high-pass filtered by first, second and third order functions respectively. The advantage can be taken of the suppression of e_{2-4} in a digitally implemented modulator for, e.g. reduction of wordlengths in integrators being placed nearer to the quantizer. The subsequent addition of error does not cause significant degradation of *SNR* due to the high-pass transfer function, while the reduced hardware count results in lower power consumption of the modulator. Also, in order to prevent limit-cycles and subsequent spurious components in a modulator's output, a pseudo-random dither signal can be added to e_4, which is shaped by the NTF [103]. While reducing the magnitude of spurious components in the output spectrum of a ΣΔ modulator, this pseudo-random signal is suppressed in the band of interest by the NTF, and therefore it has little effect on *SNR*.

2.3.6 Bandpass ΣΔ modulation

A band pass ΣΔ modulator is needed for encoding an RF signal for a Class-S power amplifier. In order to obtain a modulator whose NTF suppresses quantization noise at nonzero frequency, the NTF zeros and poles should be moved from $z = 1$ (DC) along the unit circle creating angle $0 < \Phi < \pi$, which corresponds to the desired frequency, $0 < f_0 < f_{\Sigma\Delta}/2$, where $f_{\Sigma\Delta}$ denotes the sampling frequency of the modulator. The band-

pass modulator should be of even order, which is needed to avoid unwanted NTF zeros at $z = +1$ or $z = -1$. Similarly as in the $LP\Sigma\Delta$ modulator, poles should be chosen such that the NTF is monotonic and its maximum absolute value limited in order to maintain stable operation [96]. An example of zero-pole placement and NTF of a $BP\Sigma\Delta$ modulator with $f_0 = f_{\Sigma\Delta}/3$ is shown in Fig.2.25.

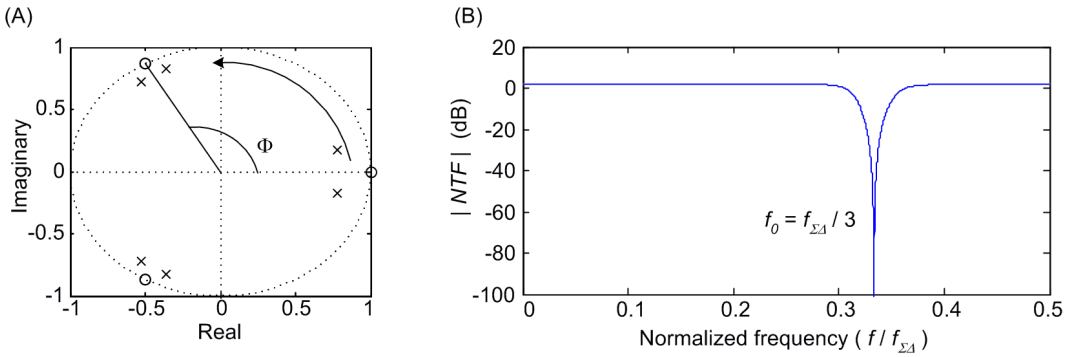

Figure 2.25: Bandpass ΣΔ modulator. (A) NTF pole-zero placement of lowpass and bandpass ΣΔ modulator. (B) Example of NTF of a $BP\Sigma\Delta$ modulator with $f_0 = f_{\Sigma\Delta}/3$.

Alternatively, a $BP\Sigma\Delta$ modulator can be obtained by transforming a $LP\Sigma\Delta$ by means of $z \to -z^2$, which has the effect of mapping zeros and poles at $z = \pm j$, and places the carrier frequency at $f_0 = f_{\Sigma\Delta}/4$. The advantages of this transformation are discussed in Chapter 3.

Another useful technique for obtaining a bandpass signal is similar to the modulation scheme of the in-phase and quadrature signals in an RF transmitter. This scheme employs a pair of $LP\Sigma\Delta$ modulators, whose inputs are baseband signals I and Q. Subsequent up-sampling, inversion and addition of the two $LP\Sigma\Delta$ modulators outputs places the RF signal at one fourth of the output sampling frequency. This method is described in more detail in Chapter 4.

2.3.7 Coding efficiency

The term coding efficiency was introduced for characterizing a ΣΔ modulator used in a digital power amplifier for its capability to encode the power of an input signal. It is

defined as a ratio of reconstructed signal power, i.e. after bandpass filtering applied in modulator's output, to the total power of the pulse stream in the output of the ΣΔ [26],

$$\eta_C = \frac{x_{rms}^2}{q^2} \tag{2.27}$$

Coding efficiency provides two useful bits of information: it describes how much power can be delivered to a load by a digital power amplifier, but also, what the percentage signal power is in the modulator's output, giving some insight into *SNR* performance of the modulator. The coding efficiency does not affect power efficiency of a switchmode amplifier only when it is ideal and 100 % power efficient. As the ideal condition does not exist for a real amplifier, it is desirable to maximize the output power and minimize the quantization noise power in the output of a modulator. There are several factors that impact coding efficiency of a ΣΔ modulator, which are discussed in the following sections. The coding efficiency is first considered in a discrete-time domain, and subsequently its explained for continuous time signals.

2.3.7.1 Discrete-time coding efficiency

The power of the quantization noise in the modulated signal q of equation (2.27) depends on a spacing between quantizer levels according to equation (2.14). The coding efficiency increases when the number of quantizer levels increases, however due to the nonlinearity encountered in multilevel quantizers, ΣΔ modulators are often restricted to two levels. When the two levels of quantizer described by input-output transfer characteristic of Fig.2.17(B) are $\pm A$, the quantizer's output power is constant and it does not depend on the modulator's input, $q^2 = A^2$. Subsequently, the coding efficiency of the modulator with 2-level quantizer expressed by (2.27) depends on the input power.

The coding efficiency for a zero-mean, bandlimited signal is always less than one since the quantization adds error to the input signal [26]. The maximum coding efficiency

occurs when the input signal to a quantizer is a sinewave of some frequency f_0 and the 2-level waveform is a 50 % duty cycle square wave as it is shown in Fig.2.26(A).

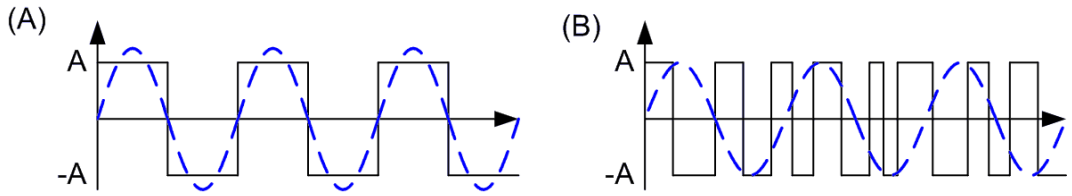

Figure 2.26: A single tone encoded into 2-level waveform. (A) Maximum amplitude. (B) Amplitude limited by a full scale range of a quantizer.

The amplitude of the first harmonic of the 2-level waveform is $Amp = \frac{4A}{\pi}$, producing a coding efficiency of $\eta_{2L_{MAX}} = \frac{0.5\left(\frac{4A}{\pi}\right)^2}{A^2} \approx 0.81$. However, when the same signal is supplied to the input of a ΣΔ modulator, the maximum amplitude of the single tone is limited by the modulator's stable input rage, being usually less or equal to the full scale range of a quantizer, i.e. $Amp_{MAX} = A$ yielding the waveforms shown in Fig.2.26(B). The maximum coding efficiency for a single tone input becomes $\eta_{\Sigma\Delta_{MAX}} = \frac{0.5A^2}{A^2} = 0.5$. The coding efficiency reduces when the stable input range of modulator reduces, e.g. third order ΣΔ chosen in Section 2.3.5.2 allows maximum input amplitude of approximately $0.88A$, yielding a coding efficiency of only $\eta_{\Sigma\Delta_{MAX}} = 0.387$. If the stable input range of the ΣΔ modulator was determined by a full scale range of a 2-level quantizer, i.e. $Amp_{MAX} \leqslant A = \Delta/2$, then the maximum power of the input signal calculated over one RF period would be the same as half the power of the 2-level waveform, i.e. $P_{PEAK} = 0.5A^2$. Consequently the input power can be calculated as a function of *PAPR* of the RF signal,

$$PAPR = \frac{P_{PEAK}}{x_{rms}^2} = \frac{0.5A^2}{x_{rms}^2} \Rightarrow x_{rms}^2 = \frac{0.5A^2}{PAPR}$$

substitution of the x_{rms}^2 calculated above in (2.27) yields the approximated expression for discrete time coding efficiency of a 2-level ΣΔ modulator,

$$\eta_{\Sigma\Delta_{FULL-SCALE}} = \frac{0.5}{PAPR} \tag{2.28}$$

Values of coding efficiency for a 2-level ΣΔ modulator for different signals, calculated

with assumption that the input signal's amplitude falls in the full-scale range of a quantizer are given in Tab.2.4. As read from Tab.2.4 for bandlimited signals whose *PAPR* is above $7\,dB$, the power of the 2-level waveform is dominated by quantization noise, and only less than $10\,\%$ of the total pulse train's power belongs to the input signal.

Table 2.4: Coding efficiency of a full scale, two level ΣΔ modulator.

Signal	$\eta_C \cdot 100\%$	$PAPR\ (dB)$
Single tone	50	0
Two tones	25	3
Four tones	12.6	6
4QAM	13.3	5.77
-	10	7
-	6.3	9

2.3.7.2 Continuous-time coding efficiency

In the last step of modulation of the RF signal, the discrete time output from a ΣΔ modulator undergoes digital to analog conversion according to the scheme of Fig.2.27(A). The *DAC* in a ΣΔ modulator for a digital PA is usually a NRZ type, yielding a *DAC* pulse of duration equal to the sampling step of the modulator $T_{\Sigma\Delta} = 1/f_{\Sigma\Delta}$ as shown in Fig.2.27(B). The output from the *DAC* is scaled in the frequency domain by the Fourier transform of the pulse which is shown in Fig.2.27(C). Subsequently, the reconstructed signal power

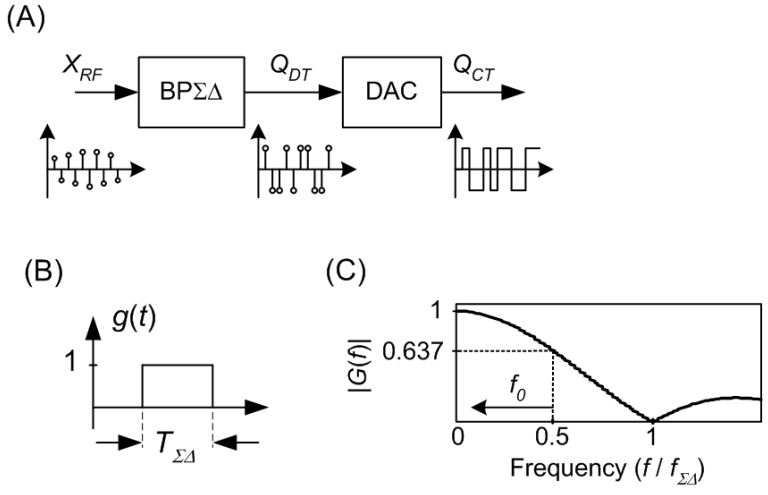

Figure 2.27: (A) Digital to analog conversion of a *BP*ΣΔ modulator output. (B) DAC pulse. (C) Fourier transform of the DAC pulse $|G(f)|$.

depends on the carrier frequency f_0 and the sampling frequency $f_{\Sigma\Delta}$ [28],

$$\eta_{CT} = |G(f_0/f_{\Sigma\Delta})|^2 \eta_{DT} \tag{2.29}$$

The η_{DT} in (2.29) denotes the discrete time coding efficiency of the modulator i.e. the coding efficiency calculated for the output Q_{DT}, and η_{CT} is the continuous time coding efficiency, i.e. coding efficiency calculated in the output Q_{CT} in Fig.2.27(A). The continuous time coding efficiency is less than or equal the discrete time coding efficiency due to the magnitude response of the sinc function as seen in Fig.2.27(C). The η_{CT} is nearly the same as η_{DT} when $f_0 \ll f_{\Sigma\Delta}$, and it reduces to approximately $0.81\eta_{DT}$ when $f_0 = f_{\Sigma\Delta}/4$, to $0.69\eta_{DT}$ when $f_0 = f_{\Sigma\Delta}/3$ and to $0.41\eta_{DT}$ when $f_0 = f_{\Sigma\Delta}/2$. Typically Class-S PA places the carrier frequency in a range of $f_{\Sigma\Delta}/4 \leqslant f_0 < f_{\Sigma\Delta}/2$. Despite the reduction of the reconstructed signal's amplitude accompanied by increase of the frequency f_0 towards $f_{\Sigma\Delta}/2$, there is an argument for doing so. As f_0 increases, the average frequency of transitions in the 2-level output reduces, reducing switching losses in a Class-D stage. A carrier frequency $f_0 = f_{\Sigma\Delta}/3$ was indicated by Johnson as an optimal tradeoff between coding efficiency and power efficiency caused by switching losses in Class-D stage [28]. In contrast, the attractiveness of modulator with $f_0 = f_{\Sigma\Delta}/4$ is in lower complexity of the modulator, i.e. the modulator can be obtained by a simple transformation of a $LP\Sigma\Delta$ modulator, which allows for achieving higher clock frequency than in a $BP\Sigma\Delta$ modulator whose frequency f_0 is either lower or higher than $f_{\Sigma\Delta}/4$.

2.4 Conclusion

This chapter focused on the efficiency and linearity of power amplifiers. The demand for linear RF amplification appears when a bandlimited RF signal has a modulated amplitude. Although linear classes of amplifier can be used in an RF transmitter, they are character-

ized by low power efficiency due to operation in the active region. Switchmode operation, on the other hand, allows for significant improvement of efficiency when the RF signal has a constant amplitude. In order to obtain a linear amplifier system, an appropriate conversion of the RF signal is necessary. Among the reviewed techniques, Class-S and polar transmitter with ΣΔ digitized envelope signal are chosen due to their potential for reconfigurability and high efficiency. The use of ΣΔ modulation allows for the conversion of an RF input with varying envelope into a noise shaped, 2-level waveform, which can be used to drive a broadband Class-D power amplifier. Although ΣΔ modulators are well known and are widely used in *ADC* or *DAC*, their use is slightly different in an RF SMPA. In contrast with a *DAC* or *ADC*, the priority for the modulator in SMPA is encoding the maximum possible RF power, while accepting an *SNR* that can be much lower than normally used in *ADC*s or *DAC*s. Low order ΣΔ modulators seem to be a rational choice for the use in digital PAs due to providing the highest stable input range and offering a low complexity.

Chapter 3

Time-interleaved ΣΔ modulators

3.1 Introduction

The need for a high sampling frequency for a 2-level ΣΔ modulator appears in a digital power amplifier due to the wide bandwidth of the modulated RF signal. A minimum value of oversampling ratio of approximately $OSR = 50$ can be assumed [97] as needed for suppressing quantization noise in a passband of a band pass filter in a DPT shown in Fig.2.12 or in a Class-S PA of Fig.2.14. It is easily calculated that for a $20MHz$ LTE signal, the required clock frequency of the digital logic is $f_S = 2GHz$ when $OSR = 50$. While $FPGAs$ allow for reconfigurability of implemented modulators, currently the clock frequencies are limited to less than $700MHz$, being often insufficient for achieving $43dB$ of $ACLR$ in the output of a digital power amplifier. Taking into account the above sampling rate limitation, the scope of this chapter is a design of time-interleaved ΣΔ modulators operating at sampling rates higher than the frequency of the system clock. The increase in the sampling rate is achieved by processing of a number of input samples in parallel ΣΔ sections. Concepts of parallel expansion of ΣΔ modulators are introduced and verified in the course of simulations and experimental results.

3.2 Parallel ΣΔ modulation

An increase in the sampling rate of a ΣΔ modulator can be achieved by concurrent processing of a number of consecutive input samples. The increase in the sampling rate, hardware count and finally *SNR* depend on the method used for expanding the modulator into a time-interleaved system. Subsequently, three known approaches to parallel modulation are reviewed in this section.

3.2.1 Direct method

A simple method of utilizing ΣΔ modulators in parallel is shown in Fig.3.1(A, B). The modulator operating at low sampling rate f_S is replicated N times, and each of the parallel blocks is fed with consecutive input sample at time indexes Nn, $Nn+1$, $Nn+2$...$Nn+N-1$. The outputs of the parallel blocks are next up-sampled and added, creating output sequence sampled at increased rate Nf_S. Since the arithmetic operations in each of the parallel blocks are processed independently, large N can be used without causing problems with propagation delay in the digital circuit. The drawback of the direct technique is that, despite the increased sampling rate, the NTF of the modulator of Fig.3.1(B) is the

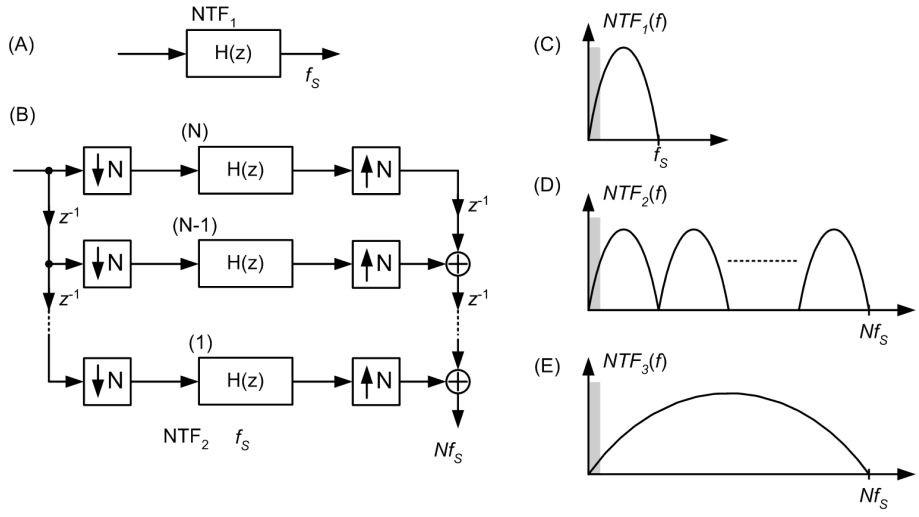

Figure 3.1: Parallel modulator. (A) Basic structure. (B) N blocks in parallel. (C) NTF of the modulator operating at low sampling rate f_S. (D) NTF of the parallel modulator. (E) desired NTF.

same as the NTF of the modulator operating at low sampling rate, repeated in frequency domain every f_S as it is depicted in Fig.3.1(D) [61, 66]. Consequently, the parallel modulator exhibits only $3\,dB$ of SNR improvement per every doubling of N. In order to avoid the undesired repeating of NTF zeros at multiples of f_S and to obtain the NTF shown in Fig.3.1(E), cross-connections between the blocks in parallel are necessary.

3.2.2 Block digital filter

A time-interleaved ΣΔ $(TI-\Sigma\Delta)$ modulator using a block digital filter technique was proposed in 1993 by Poorfard et al [51–53]. Poorfard used a multirate system shown in Fig.3.2(A) for replacing loop filters $H(z)$ in a ΣΔ modulator, which in consequence reduced the sampling rate of the digital hardware N times. Since the transfer function of the multirate system was the same as that of the replaced loop filter, the $TI-\Sigma\Delta$ modulator had the same NTF and STF as the original modulator while using N times lower clock frequency. The transfer function matrix $P(z)$ for the $TI-\Sigma\Delta$ is realized in two steps. First, the loop filters in ΣΔ modulator structure are expanded to type 1 polyphase,

$$H(z)=\sum_{n=0}^{N-1} z^{-n} P_n\left(z^N\right) \tag{3.1}$$

e.g. when loop filter is a non delaying integrator and $N=2$ then $H(z)$ becomes,

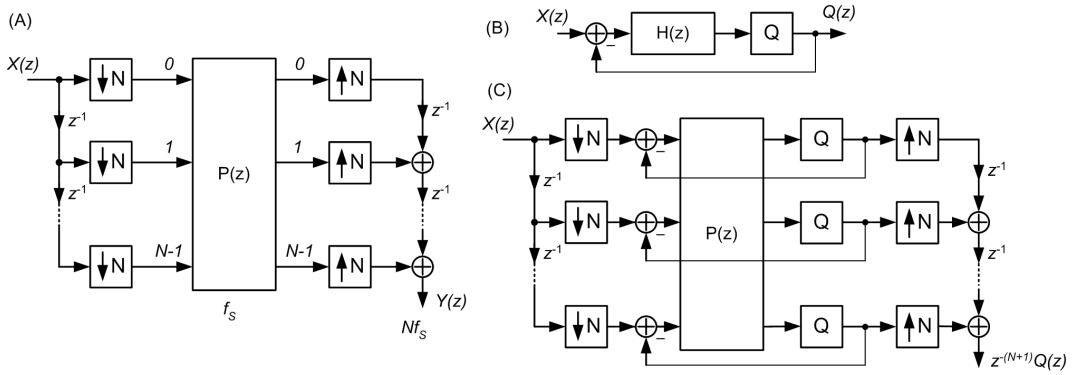

Figure 3.2: (A) Multirate system used to represent a loop filter in a ΣΔ modulator. (B) Single feedback topology of ΣΔ modulator. (C) $TI-\Sigma\Delta$ modulator obtained using block digital filter technique.

$$H(z) = \frac{1}{1-z^{-1}} = \frac{1}{1-z^{-2}} + z^{-1}\frac{1}{1-z^{-2}} = P_0\left(z^2\right) + z^{-1}P_1\left(z^2\right)$$

Next, an $N \times N$ transfer matrix $P(z)$ is obtained using P_n components of equation (3.1) according to (3.2), with $P_{i,j}$ describing transfer function of i-th input to j-th output.

$$P(z) = \begin{bmatrix} P_0(z) & P_1(z) & \cdots & P_{N-1}(z) \\ z^{-1}P_{N-1}(z) & P_0(z) & \cdots & P_{N-2}(z) \\ \vdots & \vdots & \ddots & \vdots \\ z^{-1}P_1(z) & z^{-1}P_2^{-1}(z) & \cdots & P_0(z) \end{bmatrix} \tag{3.2}$$

The transfer matrix $P(z)$ is pseudo-circulant, and subsequently alias terms $X\left(e^{(j\omega+2\pi k)/N}\right)$ created in the course of the decimation of the input $X\left(e^{j\omega}\right)$ are canceled [67], yielding a time-invariant system whose transfer function is,

$$\overline{H(z)} = \frac{Y(z)}{X(z)} = z^{-N+1}H(z) \tag{3.3}$$

The resulting multirate system has the same transfer function as the original loop filter with additional delay z^{-N+1}. In the last step, quantizers and feedback paths of a ΣΔ modulator are included in the low sampling rate section creating the $TI-\Sigma\Delta$ as seen in Fig.3.2(B, C) for a single feedback topology.

One of drawbacks of the $TI-\Sigma\Delta$ implemented as a switched capacitor (SC) circuit is an imperfect cancellation of aliasing terms caused by modulator's coefficients mismatch, i.e. the ideal pseudo-circulant transfer matrix cannot be created using analog components, and subsequently aliasing appears in the system. The problem of increasing noise-floor can be partially solved by using a zero in NTF at frequency $f_S/2$. Due to the mismatch problem, N was suggested to be not higher than 2.

In contrast to the above, the use of digital logic to implement the $TI-\Sigma\Delta$ avoids the coefficients mismatch effect and finite gains problems encountered in SC integrators.

Subsequently the expansion of the modulator to $N > 2$ is possible without degradation of the *SNR*. The limitation of N is however imposed by complexity of the time interleaved structure - the number of adders and multipliers in the $TI-\Sigma\Delta$ based on the block digital filter approach is a quadratic function of N due to the cross-connections needed between each of parallel sections, which results in a rapid increase of a hardware in $TI-\Sigma\Delta$ modulators with higher N.

Despite the large complexity of loop filters, the block digital filter technique proposed by Poorfard was successfully employed to implement high-sampling rate $TI-\Sigma\Delta$ modulators in an *FPGA* (Stratix II GX from Altera) [59]. A sampling rate of 640MHz and 800MHz were reported for 2nd order ΣΔ modulator, which yield good results when compared with earlier *FPGA*-ΣΔ: $f_S = 109MHz$ using CRFF ΣΔ and implemented in Virtex 6 FPGA [45], $f_S = 100MHz$ using a bandpass ΣΔ and implemented in Virtex II FPGA [29, 95], $f_S = 215MHz$ implemented in Virtex II FPGA [94].

3.2.3 $TI-\Sigma\Delta$ based on time domain equations

In 1999 Kozak presented a $TI-\Sigma\Delta$ modulator derived from the discrete time domain equations of a ΣΔ modulator [54]. The technique uses a system of discrete time-domain equations to describe a ΣΔ modulator, which are next written for N consecutive time slots, i.e. $Nn, Nn+1...$ etc. After combining them into a one system at $n-th$ time slot, one arrives at a time-domain description of the $TI-\Sigma\Delta$ modulator [55].

Similar to Poorfard's $TI-\Sigma\Delta$, the modulator suffers a noise-floor increase caused by coefficients mismatch when implemented using a SC circuit, which however does not affect *SNR* when digital logic is used to implement the modulator. When comparing $TI-\Sigma\Delta$ modulators derived using Poorfard and Kozak techniques, the latter results in lower complexity of the TI system, although both techniques yield functionally equivalent modulators. A $TI-\Sigma\Delta$ derived from the transfer matrix in the block digital filter

technique uses $N-1$ cross-connections between each of the parallel branches, which is a direct reason for the large hardware count, i.e. each cross-connection requires the use of at least one adder in the time-interleaved modulator. Conversely, a manipulation of the time-domain equations in the $TI-\Sigma\Delta$ described by Kozak leads to a simplification of computed functions, and subsequent reduction of the hardware. Despite this advantage, to our knowledge no implementations in $FPGA$ of $TI-\Sigma\Delta$ modulator based on the time-domain technique have yet been reported.

3.2.4 Conclusion

Increasing the sampling rate of a ΣΔ modulator can be straight forward, such as in the case of the direct implementation of ΣΔ sections in parallel. However, in order to avoid the unnecessary NTF zeros repeated at frequencies $m\frac{f_S}{N}$, the blocks in parallel should be cross-connected. The $TI-\Sigma\Delta$ modulator can be obtained using an NxN pseudo-circulant transfer matrix to represent modulator's loop filter, or equivalently, by exploiting time domain equations of a ΣΔ modulator. The latter technique requires less hardware, and has the potential for achieving higher sampling rates due to the shorter critical path in the time-interleaved system.

3.3 Low pass and band pass ΣΔ modulators' structures

This section addresses the problem of critical path in low pass and band pass ΣΔ modulators structures. The critical paths are studied in two common structures of ΣΔ modulator: a cascaded integrators with distributed feedback $(CIFB)$ and cascade of resonators with distributed feedback $(CRFB)$ [69]. In the second part of this section, the problem of the long critical path in a $BP\Sigma\Delta$ modulator is addressed and a new structure employing low-order, delaying loop-filter sections is proposed.

3.3.1 Critical path in *LP*ΣΔ and *BP*ΣΔ modulators

Every gate in a combinational circuit induces a propagation delay between its input and output caused by response time of transistors to changing voltage levels. As the chain of gates expands, the total time needed for the signal to propagate from the input to the output increases. Digital filters, IIR or FIR usually process more than one discrete time equation at a time. Before a consecutive clock cycle begins, all computations must be completed to avoid incorrect output values. The longest propagation time in the circuit determines the critical path in the filter structure, and it limits the maximum clock frequency that the filter can operate at.

Fig.3.3(A) shows a generalized, distributed feedback topology of a ΣΔ modulator that can be used to derive second order *CIFB* or *CRFB* structures. Using the linear model of quantizer of Fig.2.17, one can express the output of the ΣΔ modulator by,

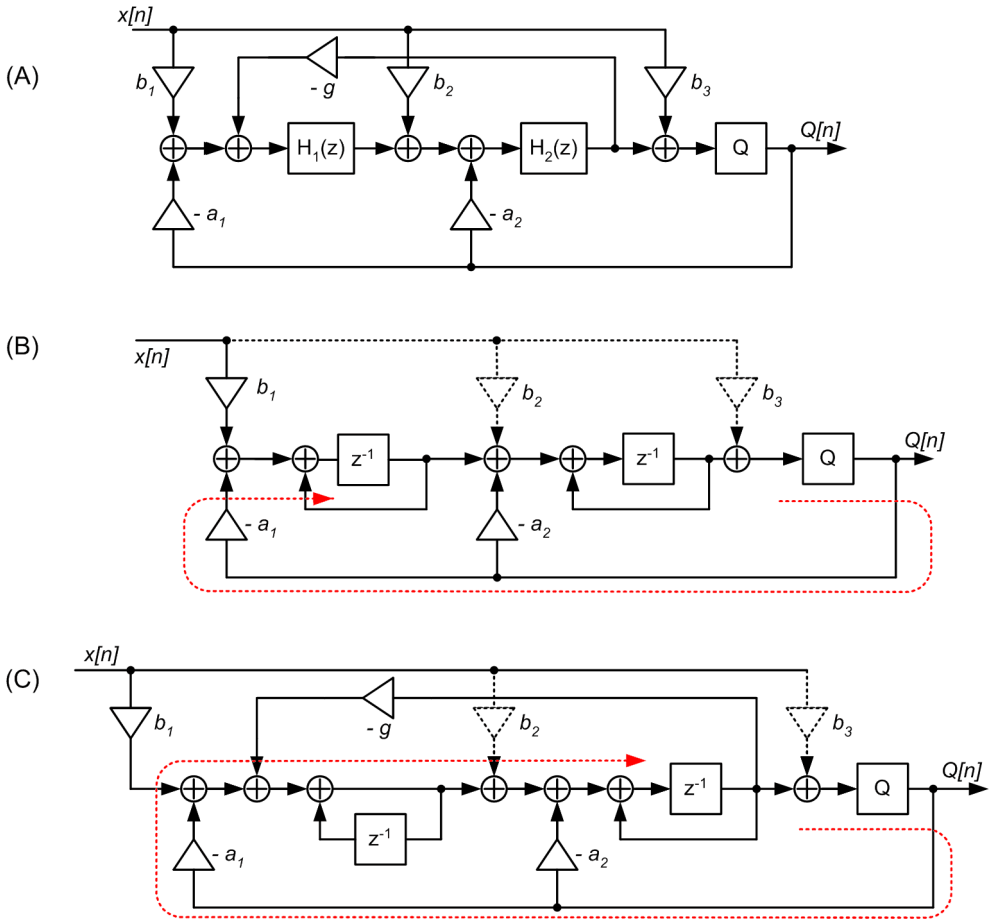

Figure 3.3: (A) Generalized scheme of CIFB/CRFB modulator. (B) 2nd order CIFB. (C) 2nd order CRFB.

$$Q(z) = X(z)\frac{b_3+(b_1+b_3g)H_1(z)H_2(z)+b_2H_2(z)}{1+(a_1+g)H_1(z)H_2(z)+a_2H_2(z)}+ \\ +E(z)\frac{1+gH_1(z)H_2(z)}{1+(a_1+g)H_1(z)H_2(z)+a_2H_2(z)} \tag{3.4}$$

In a $CIFB$ structure, all loop filters are delaying integrators, i.e. $H_{1,2,...}(z) = \frac{z^{-1}}{1-z^{-1}}$, which substituted in (3.4) yield a second order noise transfer function. Subsequently the numerator of the NTF becomes,

$$N_{CIFB} = 1 - 2z^{-1} + (1+g)z^{-2} \tag{3.5}$$

The complex conjugate zeros of N_{CIFB} should be placed in a complex plane on the unit circle in order to obtain maximum quantization noise suppression at the selected frequency. This is achieved only when $g = 0$ in (3.5). Subsequently the NTF zeros of the $CIFB$ modulator are superimposed at $z = 1$ (or $z = -1$) yielding a lowpass (or highpass) modulator whose structure is shown in Fig.3.3(B). By omitting coefficients $b_n, n = 2,3...$ as having no impact on a noise transfer function, the complexity of the low-pass $CIFB$ structure is reduced further. The critical path marked by the dashed line in Fig.3.3(B) consists now of one quantizer, one multiplier and two adders only. It is noticed that any expansion to higher order modulator by adding more integrators will have no effect on the length of the critical path, making this structure suitable for operating at high clock rates. Despite the advantage of short critical path, the $CIFB$ structure restrains the modulator to low pass or high pass operation only, i.e. NTF zeros can be either $z = 1$ or $z = -1$ for $g = 0$.

Band-pass operation requires that the zeros in the NTF are located at some positive frequency $0 < f < f_{\Sigma\Delta}/2$ which corresponds with the zero locus shown in Fig.3.4 with $0 < \Phi < \pi$ and $r = 1$. Such zeros can be obtained in a $CRFB$ modulator, when one of the integrators in the generalized structure of Fig.3.3(A) is of non-delaying type, $H_1 = \frac{1}{1-z^{-1}}$ while the other remains $H_2(z) = \frac{z^{-1}}{1-z^{-1}}$. When H_1, H_2 are substituted into (3.4), the numerator of the NTF becomes,

$$N_{CRFB}(z) = 1 - z^{-1}(2-g) + z^{-2}$$

Inspection of the *CRFB* structure reveals that the change of the first integrator coupled with the addition of the feedback consisting of multiplier g increases the critical path of the modulator in comparison with the *CIFB* structure, as seen in Fig.3.3(C).

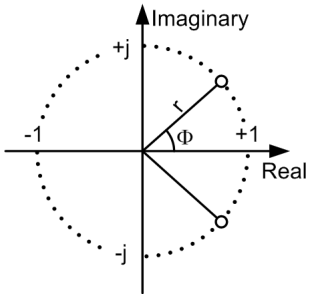

Figure 3.4: Zero location for second order function.

The *CRFB* has a critical path consisting of 5 adders (similarly as in *CIFB* coefficients b_2 and b_3 can be omitted as they impact STF only), multiplier and a quantizer in cascade. Consequently, a longer computation time than in the case of the *CIFB* ΣΔ is expected.

The property of longer critical path in band-pass over low-pass modulators having zero(s) at $z = 1$ is common in other ΣΔ modulators structures. It is because bandpass operation requires at least second order loop filter sections, in contrast with lowpass modulators which can be realized with delaying integrators. Some reduction of a critical path in a *BP*ΣΔ structures can be however attained which is demonstrated later in Sections 3.3.3 and 3.3.4 of this chapter.

3.3.2 Effect of quantized coefficients on noise transfer function

Implementation of high precision, multibit coefficients for a digital filter often causes undesired increase of propagation delay in a critical path, and a subsequent limitation of the sampling rate. When however the change in the filter's transfer function caused by approximation of its coefficient to the nearest 2^n number is small, then the multiplica-

tion can be replaced by simple right or left shift operation by n bits, resulting in shorter computation time and less hardware needed for the implementation of the coefficient.

Some robustness to the coefficients quantization effect can be gained, when a transfer function of a high order is broken into cascade of lower order sections. Let us consider a numerator of a noise transfer function expressed by a product of quadratic equations, and by polynomial, as shown below,

$$N_{BP} = \left(1 + a_1 z^{-1} + z^{-2}\right)\left(1 + a_2 z^{-1} + z^{-2}\right)\cdots \tag{3.6}$$

$$N_{BP} = a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + \cdots \tag{3.7}$$

The transfer function (3.6) is equivalent to the use of a cascade of second order filter sections, while (3.7) can be realized by a single, high order direct form filter. In the former case of equation (3.6), the locus of any pair of conjugate zeros depends on one single coefficient only, and it is unaffected by any change of other coefficients values. Also, and this is important for efficient noise shaping, the zeros of the transfer function always remain on the unit circle when $-2 \leqslant a_k \leqslant 2$. The representation of coefficients a_k by 2^n numbers in (3.6) yields however a finite set of possible angles Φ, and subsequently the number of possible frequencies f_0 of the input signal is also limited. Despite this drawback, the quantization noise suppression at those frequencies can be close to that of the ideal modulator since the NTF zeros are guaranteed to be on the unit circle, while avoiding the use of multibit multipliers. This is in contrast with the high order polynomial of equation (3.7) which often requires higher precision of coefficients approximation in order to preserve desired transfer function [66].

Let us consider the following example, where the NTF has zeros superimposed at the frequency $f_0 = 0.29 f_{\Sigma\Delta}$. When a fourth order modulator is implemented, then the coefficients for cascaded loop filter of equation (3.6) become $a_{1,2} = 2^{-1}$, which corresponds to a right shift operation of the multiplied number by 1 bit. The equivalent direct form

implementation of the loop filter on the other hand has following coefficients:$a_{0,1,3,4} = 1$ and $a_2 = 2.25 = 2^1 + 2^{-2}$, i.e. the approximation of the a_2 requires now the use of two shift operations and an adder, which in turn increases complexity and propagation delay in the modulator's structure. When the modulator is of sixth order, the coefficients for the cascaded loop filter remain unchanged, i.e. $a_{1,2,3} = 2^{-1}$ (3.6), but the complexity of coefficients approximation for the direct form increases further: $a_{0,6} = 1$, $a_{1,5} = 1.5 = 2^0 + 2^{-1}$, $a_{2,4} = 3.75 = 2^2 - 2^{-2}$, $a_3 = 3.125 = 2^1 + 2^0 + 2^{-3}$.

It is therefore desirable that for a fast operation, a ΣΔ modulator should be composed of low order sections rather than single, high order loop filter.

3.3.3 *BP*ΣΔ using a single feedback topology

An arbitrary order ΣΔ modulator can be realized using a single feedback (*SF*) topology shown in Fig.2.18. The loop filter (*LF*) is broken into 2nd order sections to ensure that *NTF* zeros of a *BP*ΣΔ modulator are on the unit circle. The *LF* transfer function becomes,

$$H(z) = \frac{\left(d_1 z^{-1} + d_2 z^{-2}\right)}{\left(1 + a_1 z^{-1} + z^{-2}\right)} \frac{\left(d_3 + d_4 z^{-1} + d_5 z^{-2}\right)}{\left(1 + a_2 z^{-1} + z^{-2}\right)} \cdots \tag{3.8}$$

The noise transfer function calculated from (2.17) has the numerator expressed by a product of quadratic equations as was desired,

$$NTF(z) = \frac{\left(1 + a_1 z^{-1} + z^{-2}\right)\left(1 + a_2 z^{-1} + z^{-2}\right) \cdots}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + \cdots} \tag{3.9}$$

Note that the numerator and denominator in *NTF* of a single feedback topology cannot be expressed by products of second order functions simultaneously because they are not created directly from loop filter coefficients, and the denominator remains in a polynomial form, which is common in all ΣΔ structures cited in this work.

Because only one block in the cascaded transfer function of equation (3.8) is of delaying type, the critical path of the loop filter will expand proportionally to the modulator's

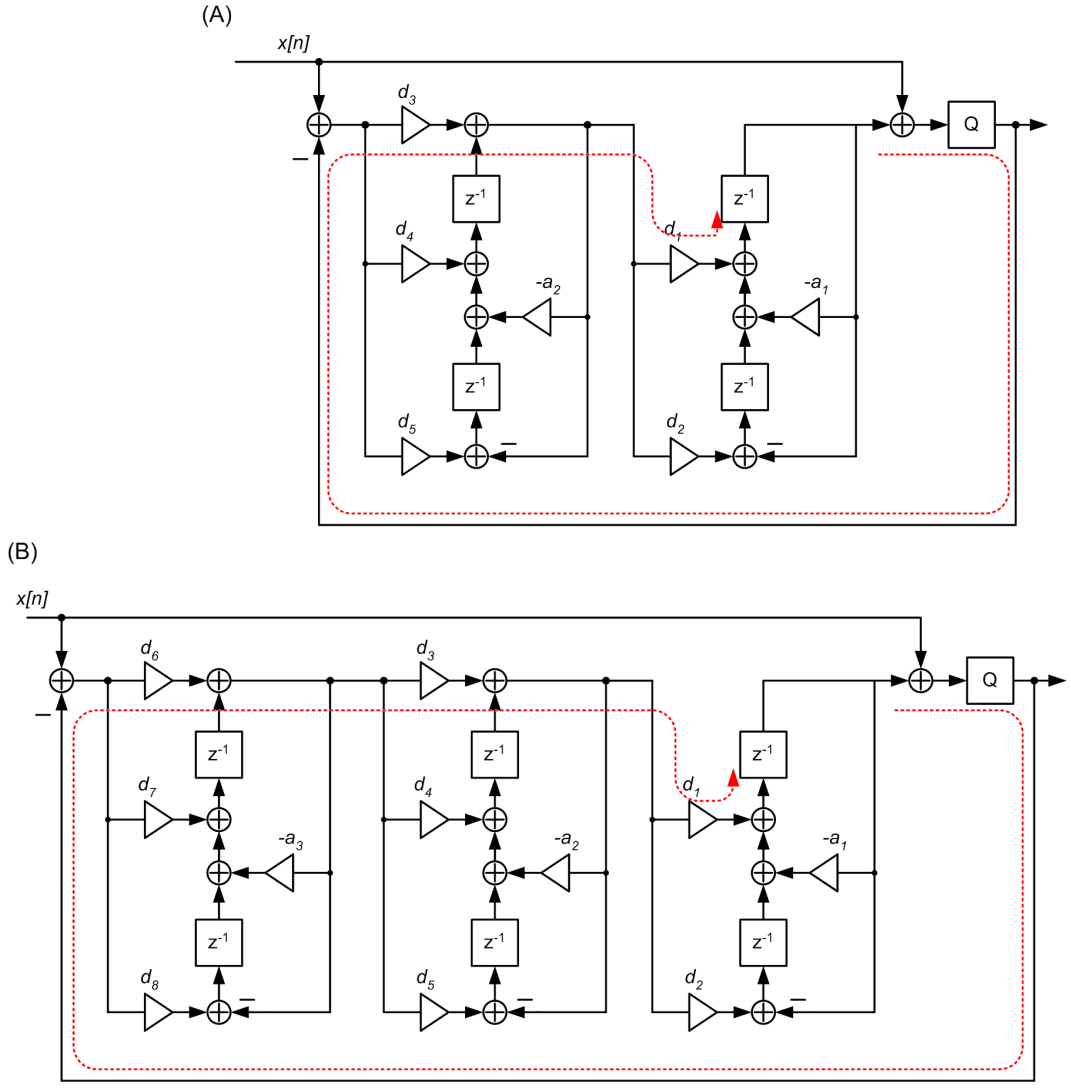

Figure 3.5: Single Feedback (SF) ΣΔ modulators with marked critical paths. (A) Fourth order. (B) Sixth order.

order. Modulators of order fourth and sixth, using a direct form II-transposed $(DF-II_t)$ IIR for loop filter sections are shown in Fig.3.5(A, B). The critical paths in the fourth and sixth order modulators are marked in the figure and they consist of: a quantizer, two multipliers and four adders in fourth order modulator and; a quantizer, three multipliers and five adders in the sixth order modulator. Although the fourth order modulator has a shorter critical path than the $CRFB$ of the same order, the sixth order modulator has a longer critical path comparable with that of $CRFB$ structure.

A method that allows further reduction of a critical path is through pipelining i.e. a long critical path can be broken into smaller paths by insertion of delay blocks be-

tween the subsequent second order sections. The use of delaying, second-order sections is demonstrated next for a distributed feedback topology.

3.3.4 ΣΔ structure based on distributed feedback topology

This section proposes a structure for a band-pass ΣΔ modulator with a reduced critical path length when compared to the band-pass structures presented earlier in this chapter. The reduction of the critical path is achieved through the use of delaying-type loop filters in a distributed feedback (DF) topology.

The ΣΔ modulator with distributed feedback shown in Fig.3.6 has NTF obtained for linear quantizer model given by (3.10), and an unity STF,

$$NTF(z) = \frac{1}{1 + H_1(z) + H_1(z)H_2(z)H_3(z) + \cdots + H_1(z)H_2(z)H_3(z)\cdots H_N(z)} \tag{3.10}$$

$$STF(z) = 1 \tag{3.11}$$

The transfer functions of loop filters $H_k(z)$ should be of minimum second order to obtain band pass modulator. When the loop filters have transfer functions of the form,

$$H_k(z) = \frac{P_k(z)}{L_k(z)} \tag{3.12}$$

then the NTF becomes

$$NTF(z) = \frac{L_1L_2L_3\cdots L_W}{(L_1L_2L_3\cdots\cdots L_W) + (P_1L_2L_3\cdots\cdots L_W) + (P_1P_2\cdot L_3\cdots\cdots L_W) + \cdots + (P_1P_2P_3\cdots P_W)} \tag{3.13}$$

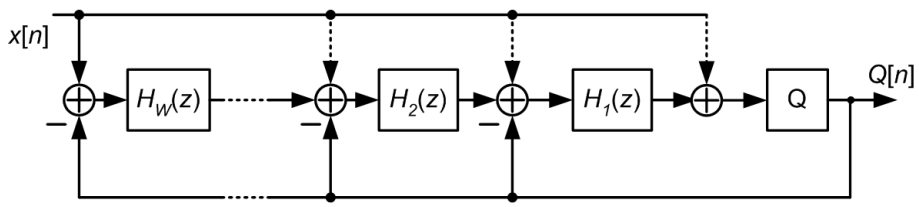

Figure 3.6: ΣΔ modulator, distributed feedback (DF) topology.

where W is the number of loop filters in the modulator. In order to obtain such a structure, whose critical path does not depend on modulator's order, each loop filter section H_k should be of delaying type which implies that each P_k should introduce at least one delay. It is observed that when numerators of the loop filters are,

$$P_k = d_k z^{-1},\ k = 1, 2, ..(W-1) \tag{3.14}$$

and only the numerator of last loop filter section is in the polynomial form

$$P_W = d_{k+1} z^{-1} + d_{k+2} z^{-2} + ... \tag{3.15}$$

then the resulting denominator of the NTF (3.13) becomes a polynomial where every coefficient b_i is independently controlled by one coefficient d of the loop filter.

$$D_N(z) = 1 + b_1 z^{-1} + b_2 z^{-2} + \cdots b_{ORD} z^{-ORD}$$

where D_N denotes denominator of NTF. Also, each loop filter section $H_k(z)$ provides a single clock delay due to the z^{-1} in (3.14) and (3.15). Additionally, when numerator of $H_k(z)$ is an equation of the second degree,

$$L_k = 1 + a_k z^{-1} + z^{-2}$$

then the NTF expressed by (3.13) has zeros on the unit circle for $-2 \leqslant a_k \leqslant 2$. In other words, a stable $BP\Sigma\Delta$ modulator whose loop-filter sections provide the desired delay between their inputs and outputs can be obtained. Example structures of modulators of order fourth and sixth are presented in following sections.

3.3.4.1 Fourth order ΣΔ modulator

Reading from equations (3.12) and (3.13), the zeros of fourth order noise transfer function are defined by denominators of loop-filters transfer functions, $H_1(z)$ and $H_2(z)$, which are equations of the second degree as explained in the previous section,

$$\begin{aligned} L_1 &= 1 + a_1 z^{-1} + z^{-2} \\ L_2 &= 1 + a_2 z^{-1} + z^{-2} \end{aligned} \tag{3.16}$$

Numerators P_1 and P_2 are of delaying type, and are obtained from (3.13)-(3.15),

$$\begin{aligned} P_1 &= d_1 z^{-1} \\ P_2 &= d_2 z^{-1} + d_3 z^{-2} + d_4 z^{-3} \end{aligned} \tag{3.17}$$

Consequently, $L_{1,2}$ and $P_{1,2}$ define transfer functions of the loop filters,

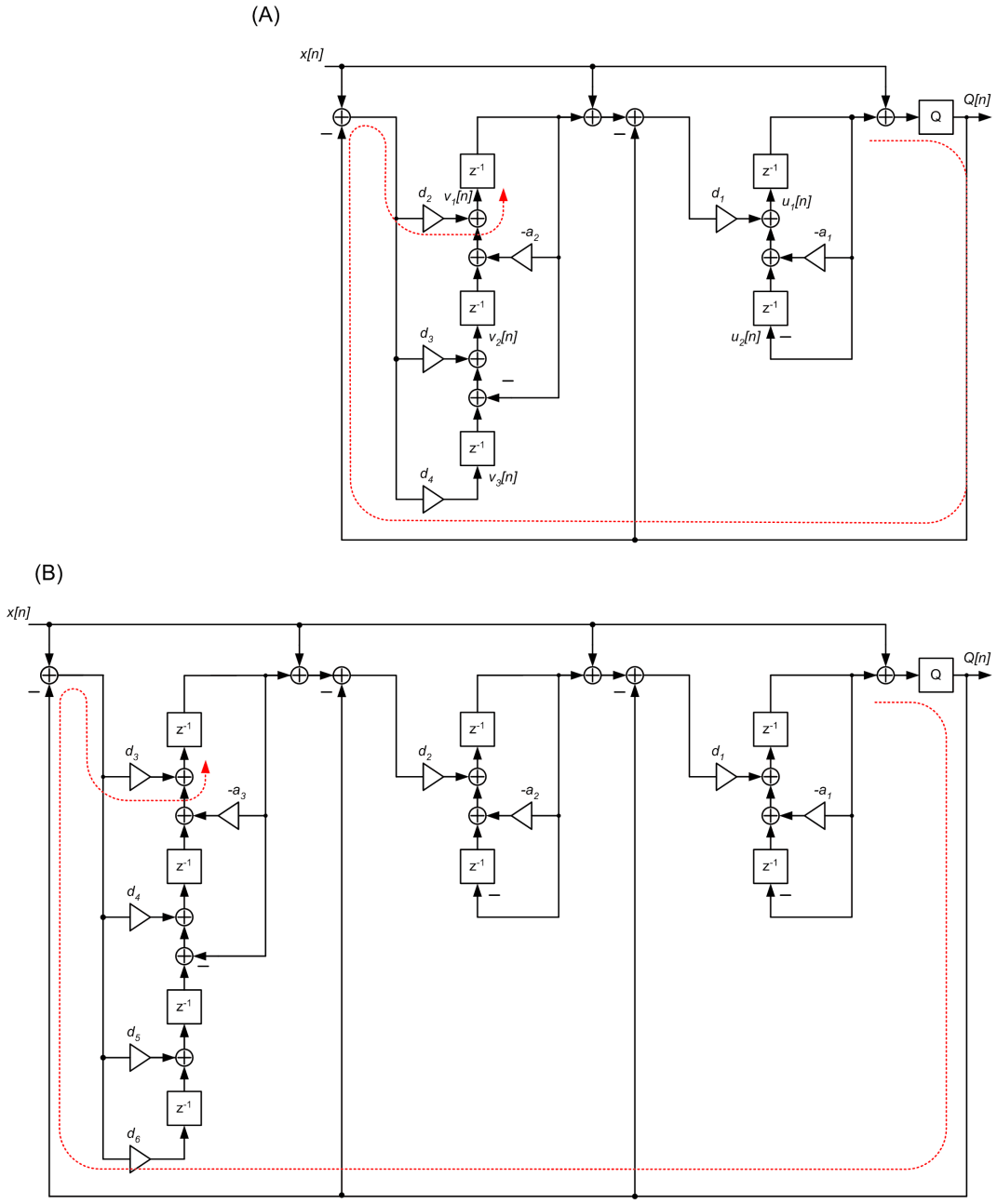

Figure 3.7: Distributed Feedback ΣΔ modulators with delaying loop filters, the dashed lines indicate critical paths. (A) Fourth order modulator. (B) Sixth order modulator.

$$\begin{aligned} H_1(z) &= \frac{P_1(z)}{L_1(z)} = \frac{d_1 z^{-1}}{1+a_1 z^{-1}+z^{-2}} \\ H_2(z) &= \frac{P_2(z)}{L_2(z)} = \frac{d_2 z^{-1}+d_3 z^{-2}+d_4 z^{-3}}{1+a_2 z^{-1}+z^{-2}} \end{aligned} \tag{3.18}$$

After substituting (3.16) and (3.17) in (3.13) the fourth order NTF becomes,

$$NTF_4(z) = \frac{\left(1+a_1 z^{-1}+z^{-2}\right)\left(1+a_2 z^{-1}+z^{-2}\right)}{1+b_1 z^{-1}+b_2 z^{-2}+b_3 z^{-3}+b_4 z^{-4}} \tag{3.19}$$

The coefficients d_i of the loop filter can be calculated from,

$$\begin{aligned} d_1 &= b_1 - (a_1 + a_2) \\ d_2 &= \left[b_2 - (2 + a_1 a_2)\right]/d_1 - a_2 \\ d_3 &= \left[b_3 - a_1 - a_2\right] d_1 - 1 \\ d_4 &= (d_4 - 1)/d_1 \end{aligned} \tag{3.20}$$

The ΣΔ structure based on distributed feedback topology and loop filters $H_1(z)$ and $H_2(z)$ implemented as the $DF-II_t$ IIR is shown in Fig.3.7(A). The critical path in the modulator reduces to one quantizer, one multiplier and three adders. The critical path is now shorter than that in the $CRFB$ or in the single feedback topology structure of Fig.3.5(A).

3.3.4.2 Sixth order ΣΔ modulator

The sixth order ΣΔ structure is obtained in a similar fashion as the fourth order structure. Let the denominators of loop filters transfers functions be expressed by quadratic equations,

$$\begin{aligned} L_1 &= 1 + a_1 z^{-1} + z^{-2} \\ L_2 &= 1 + a_2 z^{-1} + z^{-2} \\ L_3 &= 1 + a_3 z^{-1} + z^{-2} \end{aligned} \tag{3.21}$$

From (3.14) and (3.15) the numerators of transfer functions H_k are,

$$\begin{aligned} P_1 &= d_1 z^{-1} \\ P_2 &= d_2 z^{-1} \\ P_3 &= d_3 z^{-1} + d_4 z^{-2} + d_5 z^{-3} + d_6 z^{-4} \end{aligned} \tag{3.22}$$

then noise transfer function becomes,

$$NTF_6(z) = \frac{\left(1+a_1z^{-1}+z^{-2}\right)\left(1+a_2z^{-1}+z^{-2}\right)\left(1+a_3z^{-1}+z^{-2}\right)}{1+b_1z^{-1}+b_2z^{-2}+b_3z^{-3}+b_4z^{-4}+b_5z^{-5}+b_6z^{-6}} \tag{3.23}$$

where coefficients d_i are calculated for a given NTF,

$$\begin{array}{l} d_1 = b_1-(a_1+a_2+a_3) \\ d_2 = [b_2-(a_1a_3+a_2a_3+a_1a_2+2)]/d_1-(a_2+a_3) \\ d_3 = [b_3-(2a_1+2a_2+2a_3+a_1a_2a_3)-d_1(2+a_2a_3)]/(d_1d_2)-a_3 \\ d_4 = [b_4-(3+a_1a_2+a_1a_3+a_2a_3)-d_1(a_2+a_3)]/(d_1d_2)-1 \\ d_5 = [b_5-(a_1+a_2+a_3)-d_1]/(d_1d_2) \\ d_6 = (b_6-1)/(d_1d_2) \end{array} \tag{3.24}$$

6th order $BP\Sigma\Delta$ structure is shown in Fig.3.7(B). It is observed that the sixth order structure has the same critical path as the fourth order modulator of Fig.3.7(A): one quantizer, one multiplier and three adders.

3.3.5 Digital design

Although the primary goal for reduction of critical path in the structures for $BP\Sigma\Delta$ modulator has been achieved, the multiplication operations in the $BP\Sigma\Delta$ modulators can be still troublesome in terms of computation time. The problem is observed when analyzing the time-domain equations of fourth order modulator of Fig.3.7(A),

$$\begin{array}{l} Q[n] = Sgn\{x[n]+u_1[n-1]\} \\ u_1[n] = x[n]d_1+\underline{v_1[n-1]d_1}-Q[n]d_1-\underline{u_1[n-1]a_1}+u_2[n-1] \\ u_2[n] = \quad -u_1[n-1]_1 \\ v_1[n] = x[n]d_2 \quad -Q[n]d_2-\underline{v_1[n-1]a_2}+v_2[n-1] \\ v_2[n] = x[n]d_3 \quad -Q[n]d_3-\underline{v_1[n-1]}\ +v_3[n-1] \\ v_3[n] = x[n]d_4d_3 \quad -Q[n]d_4 \end{array} \tag{3.25}$$

All multiplications of input samples, i.e. products $x[n]d_i$ in (3.25) are in feedforward paths and subsequently pipelining can be applied in the arithmetic operations. This allows us to achieve a good approximation of coefficients while operating at a high clock rate. Also, when a ΣΔ output is a single-bit, the products $Q[n]d_i$ do not require the use of multipliers since the result of any of the multiplications has only two possible values. In

contrast, products: $v[n]\,a_i$, $v[n]\,d_i$, $u[n]\,a_i$; are done in feedback branches of the modulator and the pipelining cannot be used as it would affect an NTF of a modulator. These products require the use of multipliers, or at least right/left shift operations which will approximate loop filters coefficients by 2^n numbers. When a more accurate approximation of the coefficient is needed, the multiplication can be broken into a sum (or difference) of two or more different powers of two. The higher approximation accuracy however costs a more hardware and a longer computation time. In contrast, a $CIFB$ structure of the $LP\Sigma\Delta$ modulator shown in Fig.3.3(B) has a shorter critical path than any of the reviewed $BP\Sigma\Delta$ structures, while its 1 *bit* output additionally alleviates the need for the use of multipliers in the feedback paths. Although some improvement in $BP\Sigma\Delta$ modulator's structures towards reduction of a critical path has been achieved, $LP\Sigma\Delta$ have still more potential for shorter computation time and consequently for an operation at higher clock frequencies than $BP\Sigma\Delta$ modulators.

3.3.6 Conclusion

A $BP\Sigma\Delta$ modulator is needed in a Class-S amplifier for encoding the input RF signal into a binary waveform. As observed, the $BP\Sigma\Delta$ modulators are characterized by higher complexity and longer critical paths due to the use of second order loop filter sections than $LP\Sigma\Delta$ modulators, which can use loop filter sections of first order.

Some reduction of critical path has been achieved in the proposed $BP\Sigma\Delta$ modulators structures by employing delaying loop filters. The computation time in the critical path however still remains higher than in $LP\Sigma\Delta$ modulators. The critical path and hardware count are summarized in Tab.3.1 for the modulators reviewed in this section. Further reduction of a critical path and subsequent increase of a sampling rate can be achieved in $BP\Sigma\Delta$ modulators obtained in the course of $z- > -z^2$ transformation from $LP\Sigma\Delta$ modulators. This technique is explained in the following section.

Table 3.1: Comparison of ΣΔ structures.

Structure	Critical path	Hardware	Modulator
CIFB, 4th order	quantizer, multiplier, 2 adders	5 multipliers, 4 delays, 8 adders, 1 quantizer	low-pass
CRFB, 4th order	quantizer, multiplier, 5 adders	11 multipliers, 4 delays, 14 adders, 1 quantizer	low-pass, band-pass
Single feedback 4th order	quantizer, 2 multipliers, 4 adders	11 multipliers, 4 delays, 9 adders, 1 quantizer	low-pass, band-pass
Single feedback 6th order	quantizer, 3 multipliers, 5 adders	11 multipliers, 6 delays, 13 adders, 1 quantizer	low-pass, band-pass
Distributed feedback 4th order	quantizer, multiplier, 3 adders	6 multipliers, 5 delays, 10 adders, 1 quantizer	low-pass, band-pass
Distributed feedback 6th order	quantizer, multiplier, 3 adders	9 multipliers, 8 delays, 15 adders, 1 quantizer	low-pass, band-pass

3.4 Time-interleaved bandpass ΣΔ modulators

The problem of critical path in ΣΔ modulators was studied in the previous section. Despite enhancements, the proposed structures for *BP*ΣΔ are still characterized by higher complexity than *LP*ΣΔ modulators. A method that allows alleviating the problem of long critical path while offering bandpass operation is the $z \rightarrow -z^2$ transformation of a *LP*ΣΔ modulator. This section demonstrates that the *BP*ΣΔ modulator can be realized as a pair of highpass ΣΔ modulators operating in parallel, which increases the sampling rate of the system by two [50].

3.4.1 Lowpass to bandpass time-interleaved transformation

The result of the $z \rightarrow -z^2$ transformation is doubling all delay blocks in a *BP*ΣΔ modulator. In a consequence all arithmetic operations realized by the modulator at a time index n are describable by functions of variables at the same time index n or M-clock cycles delayed, where M is an even and greater than zero number. For instance, a function calculated at at time index n can use variables at time indexes $n, n-2, n-4 ... etc$ but it will not

use time indexes $n-1, n-3, n-5...etc$. It is observed that due to the independence of modulator states at even and odd time indexes, the $z \rightarrow -z^2$ transformed $LP\Sigma\Delta$ modulator is equivalent to two independent, sub-systems, each operating at odd $(n = 1,3,5...)$ and even time indexes $(n = 2,4,6...)$. These two sub-systems can operate in parallel, increasing the effective sampling rate of the bandpass modulator by two. In order to demonstrate this effect, let us consider the first order ΣΔ modulator shown in Fig.3.8(A) and its bandpass transformation of Fig.3.8(B). The $BP\Sigma\Delta$ modulator is described in the time domain at two subsequent time indexes by,

$$\begin{aligned} u[n] &= -x[n] + Sgn\{u[n-2]\} - u[n-2] \\ u[n+1] &= -x[n+1] + Sgn\{u[n-1]\} - u[n-1] \end{aligned} \tag{3.26}$$

It is observed that values of u at odd time indexes $(n = 1,3,5,7...)$ do not depend on values of u at even time indexes $(n = 2,4,6,8...)$, and conversely, u at even time indexes do not depend on u at odd time indexes, which is seen in (3.26). Also, when one delay block in the modulator in Fig.3.8(B) is omitted, and the modulator is supplied with an input at odd (or even) time indexes, the output of the modulator is the same as that of the $BP\Sigma\Delta$

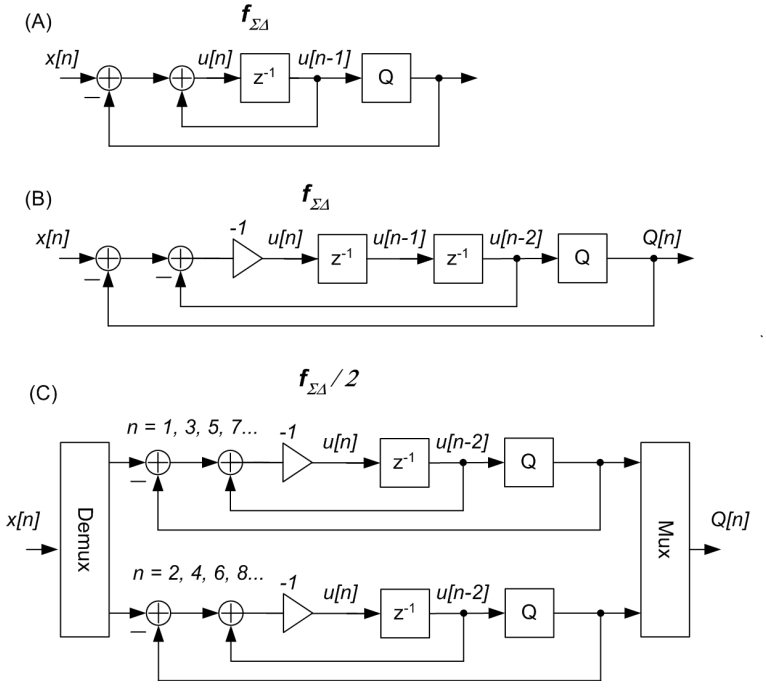

Figure 3.8: First order ΣΔ modulator. (A) Low-pass (B) $z \rightarrow -z^2$ transformed $LP\Sigma\Delta$. (C) Two $z \rightarrow -z$ transformed $LP\Sigma\Delta$ modulators in parallel.

modulator of Fig.3.8(B) at odd (or even) time indexes. Thus let us next divide the modulator into two digital sub-systems shown in Fig.3.8(C), each being the $z \rightarrow -z$, i.e. the lowpass-to-highpass transformation of the *LP*ΣΔ modulator. Each of the sub-systems operates at half of the input/output sampling rate, i.e. $f_{\Sigma\Delta}/2$, and is supplied with odd and even input samples, yielding the same output as a $z \rightarrow -z^2$ transformed *LP*ΣΔ modulator operating at two times higher sampling rate, i.e. $f_{\Sigma\Delta}$.

In general, any bandpass modulator obtained through $z \rightarrow -z^2$ transformation can be divided into two parallel sub-systems operating at half of the sampling rate regardless of topology or order by using two highpass modulators (i.e. $z \rightarrow -z$ transformed *LP*ΣΔ modulators) in parallel, as is concluded from the above example. The transformation scheme to time interleaved *BP*ΣΔ ($TI-BP\Sigma\Delta$) modulator with downsamplers and upsamplers used for decomposition of the input and output signals is depicted in Fig.3.9.

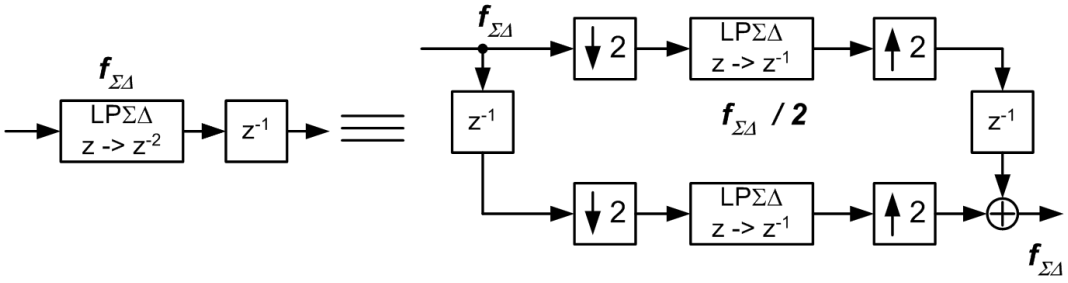

Figure 3.9: Time-interleaved *BP*ΣΔ modulator with $f_0 = f_{\Sigma\Delta}/4$.

To prove correctness of the above transformation, let us consider an arbitrary order, single feedback *BP*ΣΔ modulator obtained in the course of $z \rightarrow -z^2$ transformation as shown in Fig.3.10(A). The modulator is next transformed to $TI-BP\Sigma\Delta$ as shown in Fig.3.10(B). In order to calculate noise transfer function of the parallel modulator, three modifications in the digital circuit are done. The purpose of the modifications is to exclude quantizers from the multirate system and subsequently avoid nonlinear analysis. Similar but reverse manipulation of a multirate system was used by Poorfard to obtain a block digital filter $TI-\Sigma\Delta$ [53].

1. The advancer block z is added in order to compensate for the delay introduced by the parallel ΣΔ modulator in Fig.3.10(B),

2. Feedback paths $Q_1 - S_1$, $Q_2 - S_2$ are expanded to include input and output from the parallel modulator as shown in Fig.3.10(C). It is noticed that the inputs to loop filters remain the same, i.e. $u_1 = x[2n] - Q[2n]$ and $u_2 = x[2n-1] - Q[2n-1]$

3. Two quantizers are replaced by single quantizer sampled at the higher rate $f_{\Sigma\Delta}$ as depicted in Fig.3.10(D).

Because the three modifications above do not change the input-output relationship of the

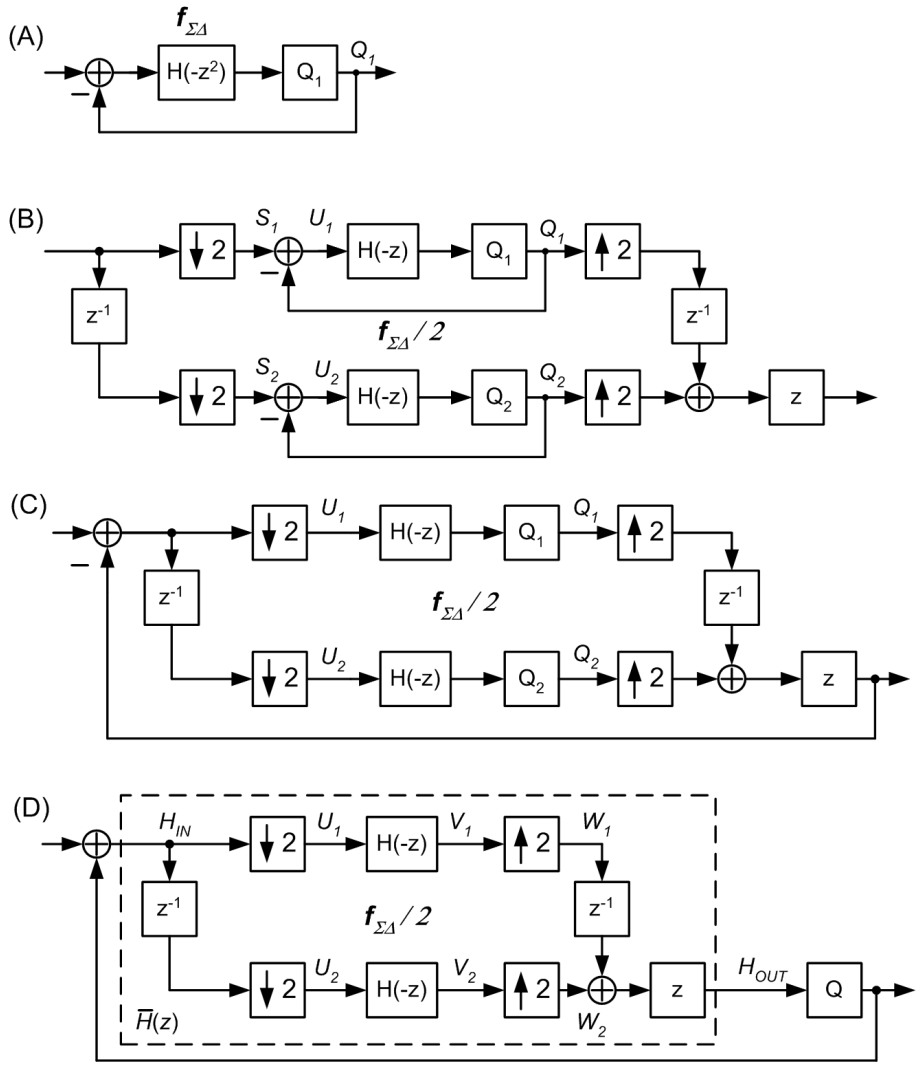

Figure 3.10: Time-interleaved single feedback ΣΔ modulator. (A) Single feedback $BP\Sigma\Delta$. (B) $TI - BP\Sigma\Delta$ with advancer. (C) Replacement of two feedback paths with single feedback path. (D) Structure with single quantizer.

modulator, the two systems shown in Fig.3.10(B) and in Fig.3.10(D) have the same signal and noise transfer functions. Moreover, the $TI-BP\Sigma\Delta$ modulator of Fig.3.10(D) can be analyzed as a single feedback topology ΣΔ, whose NTF and STF depend on $\overline{H}(z)$ by (2.17). The transfer function $\overline{H}(z)$ for the single feedback topology is found below,

$$\begin{aligned} U_1(z) &= \tfrac{1}{2}\left\{H_{IN}\left(z^{\frac{1}{2}}\right)+H_{IN}\left(-z^{\frac{1}{2}}\right)\right\} \\ U_2(z) &= \tfrac{1}{2}\left\{z^{-\frac{1}{2}}H_{IN}\left(z^{\frac{1}{2}}\right)-z^{-\frac{1}{2}}H_{IN}\left(-z^{\frac{1}{2}}\right)\right\} \end{aligned} \tag{3.27}$$

and

$$\begin{aligned} W_1(z) &= V_1\left(z^2\right),\ \textit{where } V_1(z) = H(-z)U_1(z) \\ W_2(z) &= V_2\left(z^2\right),\ \textit{where } V_2(z) = H(-z)U_2(z) \end{aligned} \tag{3.28}$$

finally

$$\overline{H}(z) = \frac{\left[z^{-1}W_1(z)+W_2(z)\right]z}{H_{IN}(z)} = H\left(-z^2\right) \tag{3.29}$$

This proves the equivalence of the $BP\Sigma\Delta$ modulator of Fig.3.10(A) with the single feedback $TI-BP\Sigma\Delta$ modulator of Fig.3.10(B), and it confirms the general transformation scheme of Fig.3.9.

3.4.2 Simulation

A Matlab simulation is carried out to verify the $TI-BP\Sigma\Delta$ modulator. A second order, single feedback $LP\Sigma\Delta$ modulator having NTF described by (3.30) is transformed to a time-interleaved system according to the scheme of Fig.3.9. The output spectrum of the time-interleaved modulator is compared against the spectrum of the conventional, $z \to -z^2$ transformed modulator operating at twice the original sampling rate. As expected, the two modulators show the same output spectra.

$$NTF_2(z) = \frac{1-1.999z^{-1}+z^{-2}}{1-1.225z^{-1}+0.4413z^{-2}} \tag{3.30}$$

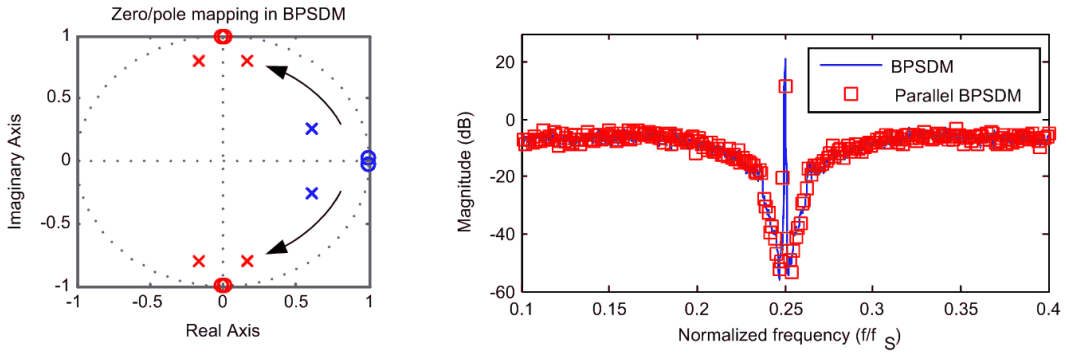

Figure 3.11: Pole/zero mapping in $z \rightarrow -z^2$ transformed $LP\Sigma\Delta$ and frequency responses of conventional and time-interleaved modulators.

3.4.3 Conclusion

The $z \rightarrow -z^2$ transformation enables a $BP\Sigma\Delta$ modulator to be obtained, while preserving short critical path of the $LP\Sigma\Delta$ modulator. The critical path in the $TI-BP\Sigma\Delta$ modulator is shorter than in a $BP\Sigma\Delta$ modulator whose zeros can be placed along the unit circle with angle $0 < \Phi < \pi$, such as the $CRFB$ structure of the distributed feedback derived in Section 3.3.4. Furthermore, the $BP\Sigma\Delta$ modulator can be implemented in a time-interleaved fashion which reduces the clock frequency of the digital hardware by a factor of two. The $TI-BP\Sigma\Delta$ modulator is obtained at the cost of doubling the hardware used for implementing an equivalent $LP\Sigma\Delta$ modulator. The other drawback of the method is that the parallel modulator maps NTF zeros/poles of a $LP\Sigma\Delta$ at $\pm j$ in the complex plane, which corresponds to a fixed frequency $f_0 = f_{\Sigma\Delta}/4$.

3.5 Time-interleaved ΣΔ based on time domain equations

The time interleaved expansion described in the previous section is applicable to $z \rightarrow -z^2$ transformed $LP\Sigma\Delta$ and it allows for increase of the modulator sampling rate by a factor of two only. This section describes a method of a parallel expansion based on discrete time domain equations of a ΣΔ modulator. In contrast with the earlier technique, the presented

$TI-\Sigma\Delta$ can be lowpass, bandpass or highpass, while the number of parallel sections is limited only by the available hardware, consequently $N > 2$ is possible.

The technique described in this section aims at increasing a sampling frequency of a $LP\Sigma\Delta$ modulator, although it is not limited to lowpass operation only. It can be coupled with the transformation to $TI-BP\Sigma\Delta$ described in the previous section, yielding a bandpass modulator for the Class-S amplifier.

3.5.1 Time-interleaved modulator

A digital filter can be described at a current time index n by its state variables being a function(s) of a current and delayed variables at discrete times $n; n-1; n-2....$ When the circuit is time-invariant, then the variables at subsequent time steps can be found by increasing n in the equations. For instance, a second order FIR filter shown in Fig.3.12(A) can be described at time index n by the following system of equations,

$$\begin{aligned} u_1[n] &= a_1 x[n] \\ u_2[n] &= a_2 x[n] + u_1[n-1] \\ y[n] &= a_3 x[n] + u_2[n-1] \end{aligned} \tag{3.31}$$

the next state is found by transforming $n \to n+1$ in (3.31),

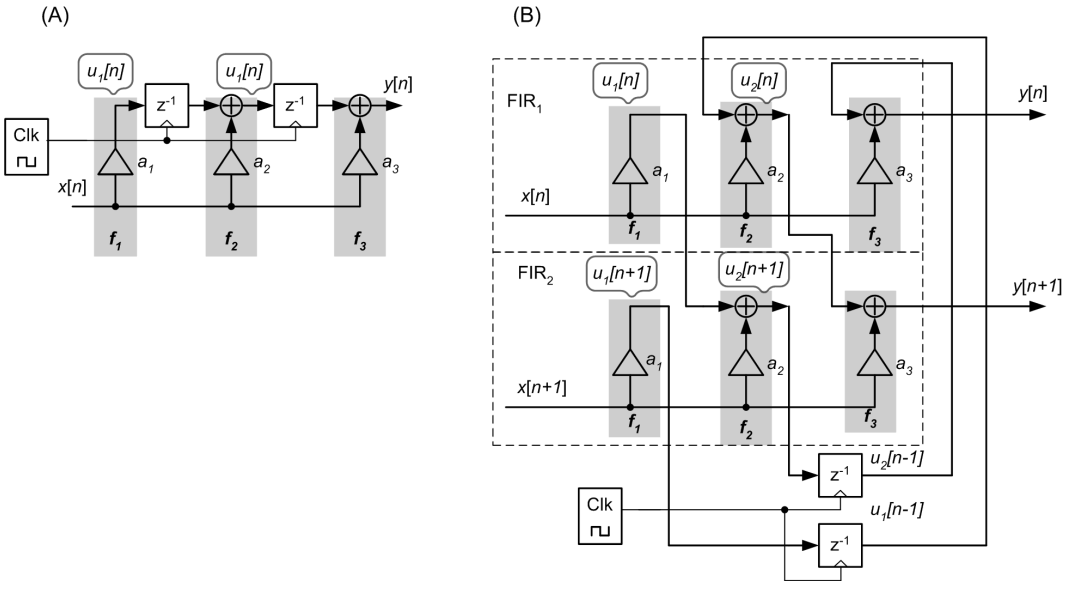

Figure 3.12: Parallel expansion of a second order FIR filter. (A) Basic structure. (B) Two FIR filters in parallel.

$$\begin{aligned} u_1[n+1] &= a_1 x[n+1] \\ u_2[n+1] &= a_2 x[n+1] + u_1[n] \\ y[n+1] &= a_3 x[n+1] + u_2[n] \end{aligned} \tag{3.32}$$

The two systems of equations (3.31), (3.32) are used to derive the block diagram of two *FIR* filters in parallel, computing consecutive filter outputs at times n and $n+1$ as shown in Fig.3.12(B). The first section marked as FIR_1 computes variables u_1, u_2, y at discrete time n, i.e. it implements system of equations (3.31). Subsequently $u_1[n]$, and $u_2[n]$ computed by FIR_1 are fed to FIR_2 and used to compute variables at discrete time $n+1$, implementing (3.32). If the propagation delays in the expanded system are sufficiently short to compute u_1, u_2 and y at both time indexes n, and $n+1$ before the end of clock period $T_S = \frac{1}{f_S}$, then the sampling rate of the expanded system can be increased two times in comparison with the basic structure of the filter shown in Fig.3.12(A).

In a general case, a discrete time ΣΔ modulator can be described at time n by a system of a discrete time equations, being functions of variables at discrete times n, $n-1$, $n-2$,...etc as written below,

$$\begin{aligned} y[n] &= f_1(x[n]\, u_1[n-1], u_2[n-1]\ldots) \\ u_1[n] &= f_2(x[n]\, u_1[n-1], u_2[n-1]\ldots) \\ u_2[n] &= f_3(x[n]\, u_1[n-1], u_2[n-1]\ldots) \\ &\ldots \end{aligned} \tag{3.33}$$

The expansion into the time-interleaved circuit is done in three steps. First the system of discrete time equations is written for N consecutive time indexes:

$N \cdot n, N \cdot n+1; N \cdot n+2; \ldots N \cdot n+N-1$. In the second step, the N systems of equations are used to create N digital sub-systems. In the third step the sub-systems are cross-connected according to the discrete time domain equations. The resulting time-interleaved circuit supplied with N consecutive inputs returns N consecutive outputs during a single clock cycle, increasing the effective sampling rate of the modulator N times. After the Nth computation, the variables are fed back in the circuit through delays blocks. Consequently, a modulator described by system of time domain equations (3.33) and shown in

Fig.3.13(A), expands to time interleaved system shown in Fig.3.13(B).

In theory the discrete time ΣΔ modulator can be expanded to any number N of blocks in parallel using the method described above. In practice, the parallel sections create a cascade of consecutively executed functions, increasing propagation delay in the digital circuit linearly with the increase of N. Consequently, the maximum number of blocks in parallel N becomes $N_{MAX} \leqslant T_S/T_C$, where T_S is the clock period of the TI system and T_C is the computation time in the critical path of the original structure.

This method can be applied to a ΣΔ modulator or a digital filter having low-pass, band-pass, or a high pass transfer function. The $TI-\Sigma\Delta$ modulators based on first order, $CIFB$, $CRFB$ and presented earlier distributed feedback structures are demonstrated in the following sections.

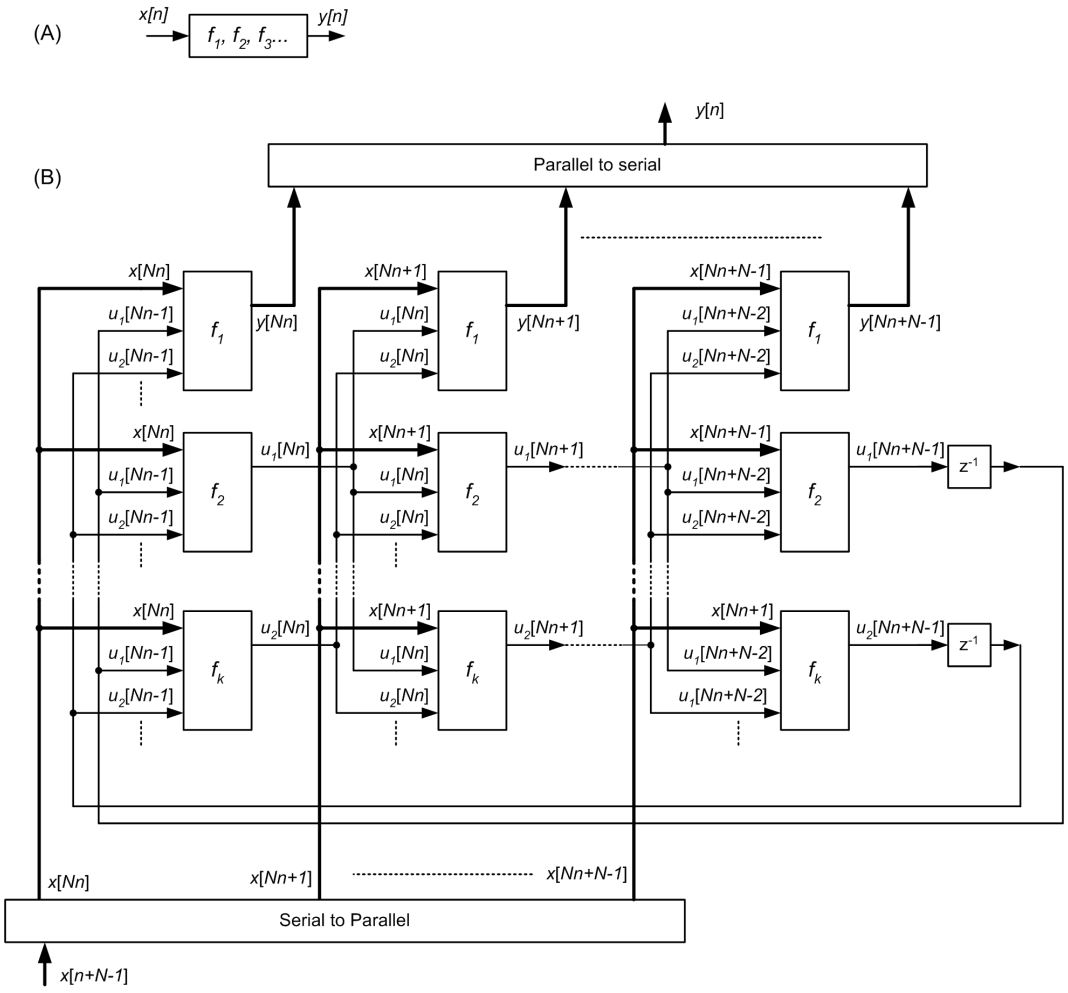

Figure 3.13: Parallel expansion of a digital system. (A) Original. (B) Time-interleaved.

3.5.2 First order $TI-LP\Sigma\Delta$ modulator

The first order modulator shown in Fig.3.14(A) can be described by the following discrete time domain equations at time n,

$$\begin{aligned} q[n] &= Sgn\{u[n-1]\} \\ u[n] &= x[n]-q[n]+u[n-1] \end{aligned} \tag{3.34}$$

In order to create a time-interleaved system, the equations are repeated at N subsequent time indexes. When $N=4$, the system of equations describing the modulator becomes,

$$\begin{aligned} q[Nn] &= Sgn\{u[Nn-1]\} \\ u[Nn] &= x[Nn]-q[Nn]+u[Nn-1] \ _{(I)} \\ q[Nn+1] &= Sgn\{u[Nn]\} \\ u[Nn+1] &= x[Nn+1]-q[Nn+1]+u[Nn] \ _{(II)} \\ q[Nn+2] &= Sgn\{u[Nn+1]\} \\ u[Nn+2] &= x[Nn+2]-q[Nn+2]+u[Nn+1] \ _{(III)} \\ q[Nn+3] &= Sgn\{u[Nn+2]\} \\ u[Nn+3] &= x[Nn+3]-q[Nn+3]+u[Nn+2] \ _{(IV)} \end{aligned} \tag{3.35}$$

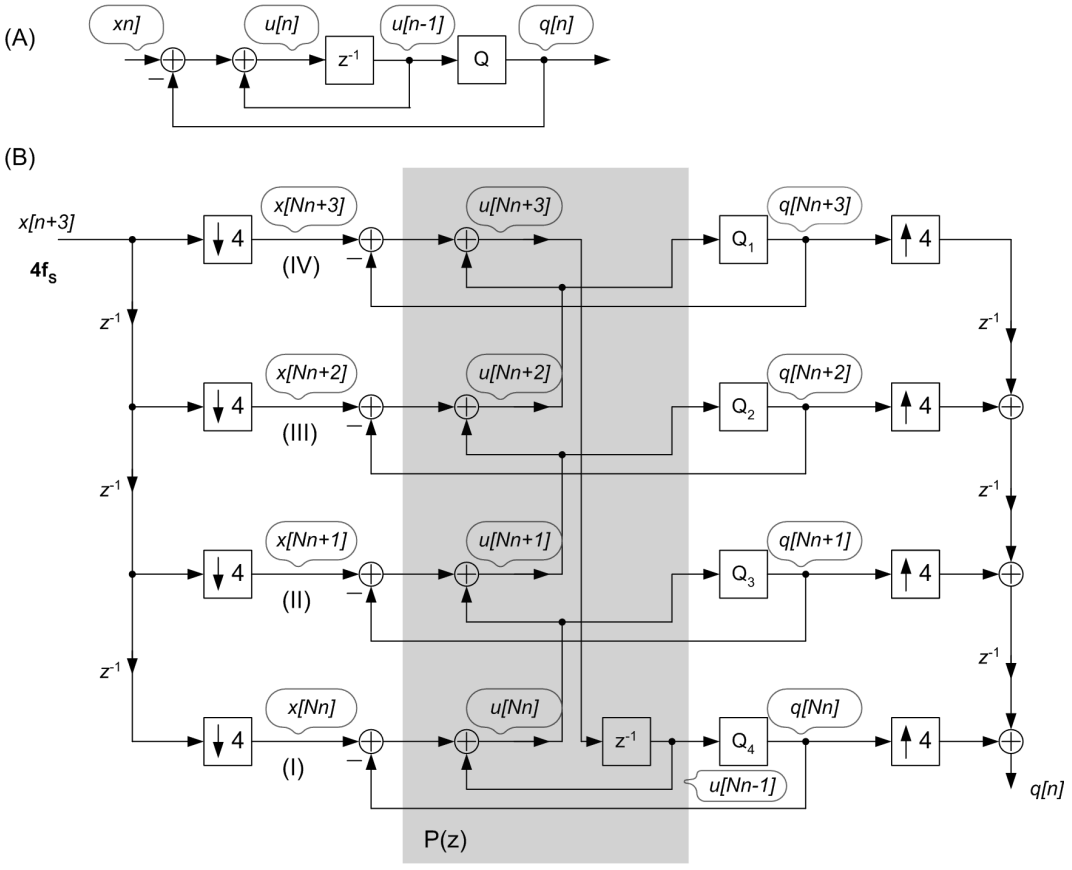

Figure 3.14: Parallel expansion of a first order ΣΔ modulator. (A) First order $LP\Sigma\Delta$. (B) $TI-LP\Sigma\Delta$ expanded by factor of 4.

The sub-systems that implement arithmetic operations of (3.35) are drawn in Fig.3.14(B). The cross-connections between the successive sub-systems are placed in the digital system by following steps $I-IV$ in the system of equations (3.35): variable $u[Nn]$ needed to compute $u[Nn+1]$ in the second sub-section is supplied from the first sub-section, subsequently $u[Nn+1]$ needed to compute $u[Nn+2]$ in the third sub-section is supplied from the second sub-section etc. The last variable $u[Nn+3]$ is supplied to the input of the delay. Note, that due to the change of time indexes in each of the sub-systems by $N=4$, which occurs every new clock period, the z^{-1} block has its output delayed by $N=4$ time steps to its input, and it acts as four delays in cascade, i.e. z^{-4}, which is correct in the multirate system.

The $TI-LP\Sigma\Delta$ modulator processes exactly the same arithmetic operations as the first order ΣΔ of Fig.3.14(A) sampled at four times higher rate. Subsequently, both modulators yield the same outputs in response to the same input sequence, with the only difference being the additional z^{1-N} delay of the $TI-LP\Sigma\Delta$ modulator's output. It should be noted that the new $TI-LP\Sigma\Delta$ derived above has the same functionality and the hardware-count as if the $TI-\Sigma\Delta$ was obtained using the method described in [54]. This is because both methods, albeit derived differently, are based on discrete time domain equations of a modulator. Consequently both of the resulting TI systems realize the same arithmetic operations and can be similar or the same. Also, the new $TI-\Sigma\Delta$ modulator has the advantage of lower complexity over the equivalent modulator obtained using the block digital filter method, which is seen when comparing both systems.

In order to obtain the transfer matrix for the modulator based on the block digital filter method, the loop filter $H(z)=\frac{z^{-1}}{1-z^{-1}}$ of the first order ΣΔ shown in Fig.3.14(A) is first expressed as type 1 polyphase. Using (3.1) and $N=4$ yields,

$$H(z) = \frac{z^{-1}}{1-z^{-1}} = \frac{z^{-4}}{1-z^{-4}} + z^{-1}\frac{1}{1-z^{-4}} + z^{-2}\frac{1}{1-z^{-4}} + z^{-3}\frac{1}{1-z^{-4}} =$$
$$= P_0\left(z^4\right) + z^{-1}P_1\left(z^4\right) + z^{-2}P_2\left(z^4\right) + z^{-3}P_3\left(z^4\right)$$

Using (3.2) the transfer matrix becomes,

$$P(z) = \frac{1}{1-z^{-1}}\begin{bmatrix} z^{-1} & 1 & 1 & 1 \\ z^{-1} & z^{-1} & 1 & 1 \\ z^{-1} & z^{-1} & z^{-1} & 1 \\ z^{-1} & z^{-1} & z^{-1} & z^{-1} \end{bmatrix} \tag{3.36}$$

The transfer matrix $P(z)$ is used to obtain the time-interleaved modulator shown in Fig.3.15.

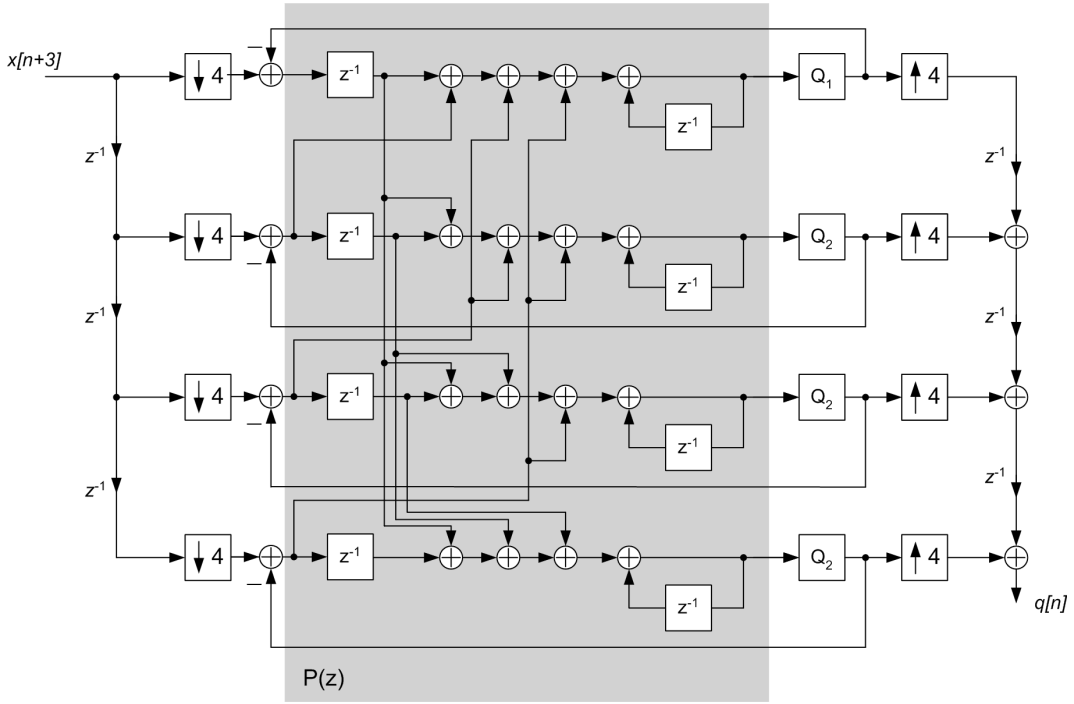

Figure 3.15: Parallel expansion of a first order ΣΔ modulator: block digital filter method.

The important difference between the new modulator of Fig.3.14(B) and the modulator based on the block digital filter (BDF) technique shown in Fig.3.15 is a shorter critical path and a lower hardware count of the former. The hardware count in the proposed TI modulator increases linearly with N due to a simple repetition of arithmetic operations, i.e. the first order $TI-LP\Sigma\Delta$ consists of a single delay, N quantizers and $2N$ adders when the input and output multiplexer/demultiplexer are not taken into account. The system based on the BDF method on the other hand is less hardware-efficient due to the cross-connections between the parallel sections, and subsequent increase of adders. The

number of adders in first order, *BDF* modulator becomes $[2+(N-1)]N$, the number of delays is $2N$ and number of quantizers N. The hardware comparison between the two approaches for a first order modulator is given in Tab.3.2, and it shows that the increase of N is accompanied by much faster increase of the hardware count in TI structure based on *BDF* approach. Despite the lower complexity, it can be shown that the new TI modulator of Fig.3.14(B) has the same transfer-matrix as the modulator of Fig.3.15 expressed by (3.36), which proves their equivalence and thus equal performance.

Table 3.2: Hardware count comparison.

N	TI - proposed			TI - block digital filter		
	adders	delays	quantizers	adders	delays	quantizers
2	4	1	2	6	4	2
3	6	1	3	12	6	3
4	8	1	4	20	8	4

3.5.3 Higher order $TI-LP\Sigma\Delta$ modulator based on $CIFB$ structure

This section describes a time-interleaved expansion of an arbitrary order $LP\Sigma\Delta$ modulator. The property of the input signal being in a low-frequency range, and a large oversampling ratio typical for 2-level modulators is exploited for reducing complexity of the $TI-\Sigma\Delta$ structure. The concept of hardware reduction is based on the zero-insertion technique described in [71], but it uses a more efficient method for suppression of the input signal's images. As will be demonstrated, the use of a lowpass STF offers some important advantages in the $TI-LP\Sigma\Delta$ modulation.

3.5.3.1 Sample-hold $TI-LP\Sigma\Delta$ modulator

The $CIFB$ ΣΔ modulator is shown in Fig.3.16, and it can be described by the following set of equations,

$$\begin{aligned} q[n] &= Sgn\{u_m[n-1]\} \\ u_1[n] &= b_1 x[n] - a_1 q[n] + u_1[n-1] \\ u_m[n] &= u_{m-1}[n-1] - a_m q[n] + u_m[n-1],\ m = 2,3,4,...,ORD \end{aligned} \tag{3.37}$$

Applying the $n \to Nn+1$ transformation in (3.37), the time domain equations at consecutive n are obtained and subsequently the $TI-LP\Sigma\Delta$ modulator. Instead of using a demultiplexer composed of delays and downsamplers for distributing the input samples, the same input sampled at the low rate $f_S = f_{\Sigma\Delta}/N$ can be supplied to all parallel blocks as is shown in Fig.3.17. Consequently, the input demultiplexer operating at the high

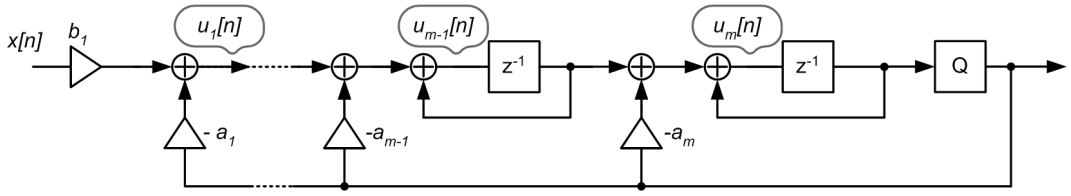

Figure 3.16: Higher order $CIFB$ $LP\Sigma\Delta$ modulator.

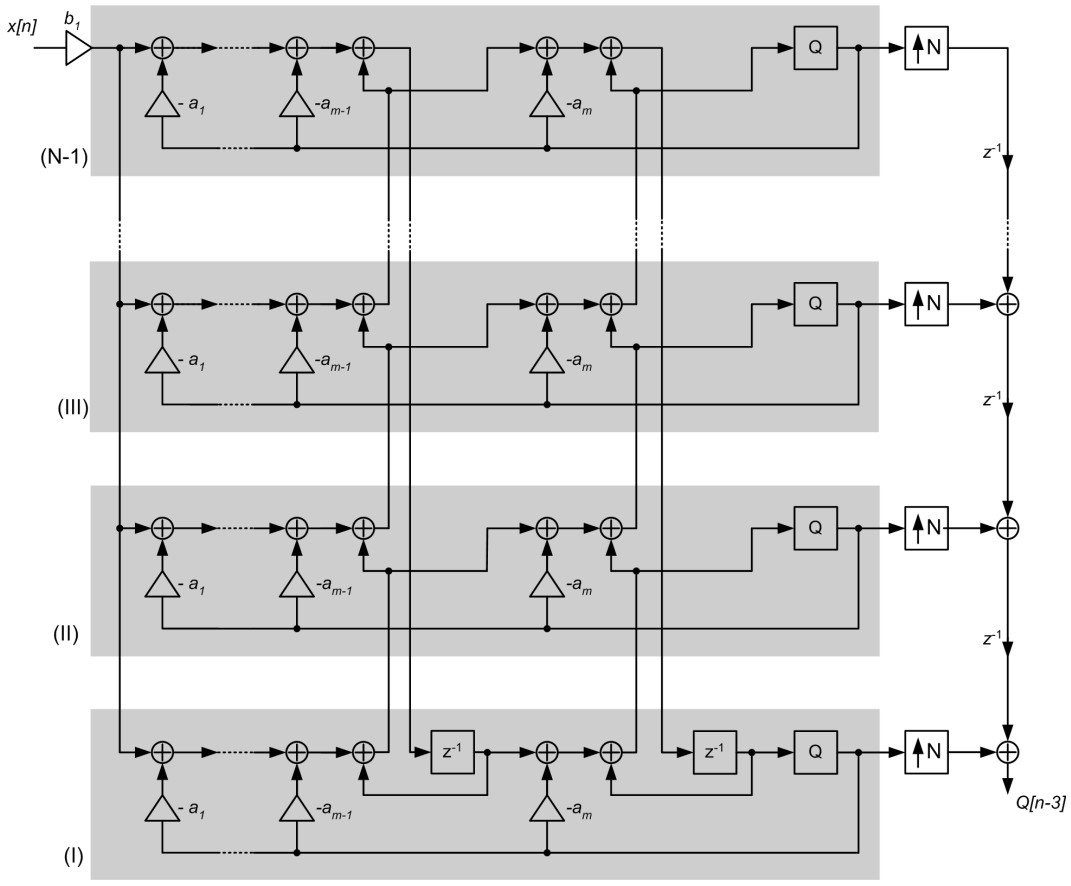

Figure 3.17: General scheme of $TI-LP\Sigma\Delta$ modulator based on high order $CIFB$ structure with sample-hold.

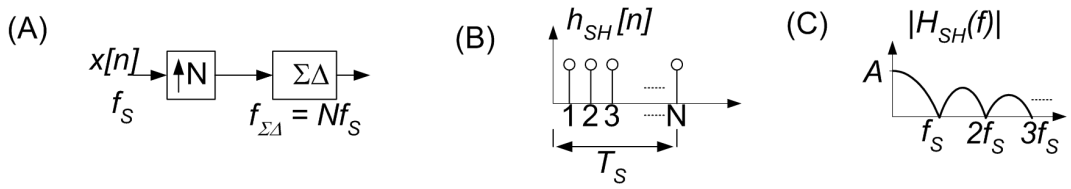

Figure 3.18: (A) Equivalent system for $TI-LP\Sigma\Delta$ with sample-hold. (B) Impulse response of the upsampler. (C) Magnitude response of the upsampler.

sampling rate is removed from the $TI-LP\Sigma\Delta$ modulator.

The above simplification is equivalent to the upsampling of the input signal by a factor of N with repetition of the input samples which is shown in Fig.3.18(A, B). As a result of the reduced input sampling rate, replicas of the input signal occur at frequencies $m\frac{f_{\Sigma\Delta}}{N}$, $m=\pm1, \pm2...$, where $f_{\Sigma\Delta}$ denotes the effective sampling rate of the time-interleaved modulator. The sample-hold has unity magnitude response at DC, and provides suppression

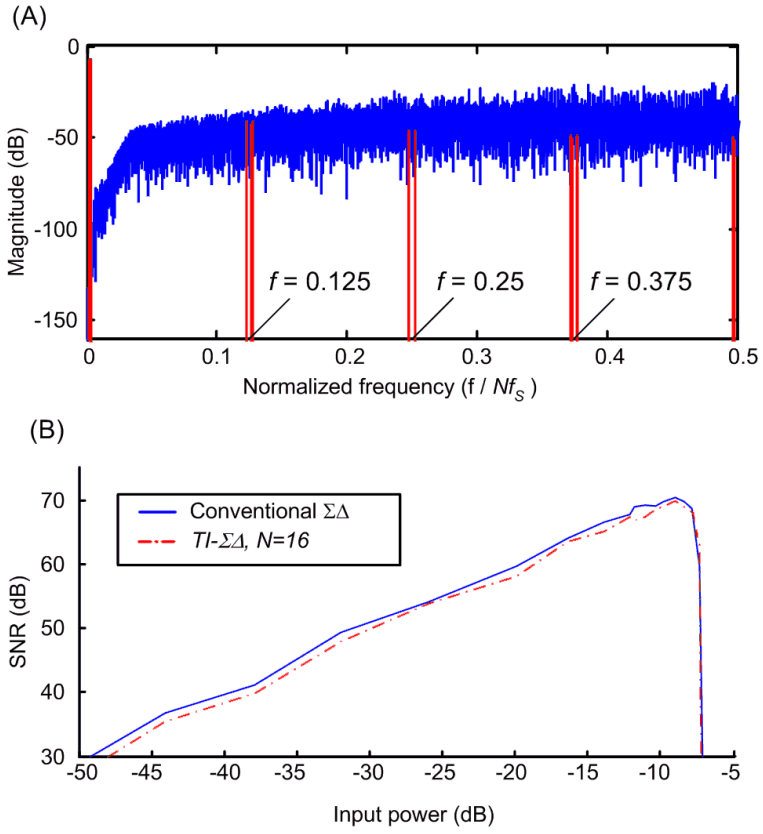

Figure 3.19: Simulated third order $TI-LP\Sigma\Delta$ modulator with the same input supplied to all parallel sections: $STF=1$ and $OSR=\frac{f_{\Sigma\Delta}}{BW}=50$. (A) Output spectrum for two tone input $Amp_1=Amp_2=0.42$, $f_1=0.002Nf_S$, $f_2=0.0025Nf_S$, $N=8$.
(B) SNR comparison for $LP\Sigma\Delta$ and $TI-LP\Sigma\Delta$ operating at the same effective sampling rates $f_{\Sigma\Delta}=Nf_S$, $N=16$.

of the input signal replicas by zeros of a sinc function at the frequencies $m\frac{f_{\Sigma\Delta}}{N}$. As a result, the total power of the spectral copies is often many dB below the quantization noise power and it is negligible for modulator's stability and *SNR*. Fig.3.19(A) shows an example of the output spectrum for a third order $TI-LP\Sigma\Delta$ for $N=8$ based on a $CIFB$ structure, whose NTF zeros and poles are provided in Tab.2.3. Also, the comparison of *SNR* for conventional and TI modulators shows only small performance degradation of the latter for relatively large number of the up-sampling factor, $N=16$. It is observed, that both modulators have nearly the same stable input ranges.

3.5.3.2 Zero-insertion in $TI-LP\Sigma\Delta$ modulator

Further simplification to the $TI-\Sigma\Delta$ can be achieved when the zero-insertion technique proposed in [55, 56, 71] is used. The $TI-LP\Sigma\Delta$ modulator with zero-insertion is created by providing an input at low sampling rate $f_S=f_{\Sigma\Delta}/N$ to one parallel section only, and by setting zero inputs for remaining ones as shown in Fig.3.20 for the $CIFB$ modulator. This technique allows for reducing the hardware count of the $TI-LP\Sigma\Delta$ modulator by $N-1$ of a multibit adders, but it has also some implications that need to be taken into consideration. In [56] the occurrence of aliases was explained as having a negligible impact on the *SNR* of a TI modulator, because their magnitudes should be well below a ΣΔ quantization noise. As it will be shown, the above explanation can be true for low N, and only for some modulators structures, e.g. a second order modulator with $N=2$, while the zero-insertion causes severe degradation of *SNR* in other structures.

3.5.3.3 The effect of high N on *SNR* in zero-insertion $TI-LP\Sigma\Delta$

The TI modulator with zero-insertion can be considered as an equivalent ΣΔ modulator operating at the same, effective sampling rate, $f_{\Sigma\Delta}$. The input signal for the ΣΔ modulator is sampled at the low rate $f_S=f_{\Sigma\Delta}/N$ and it is supplied the modulator through the

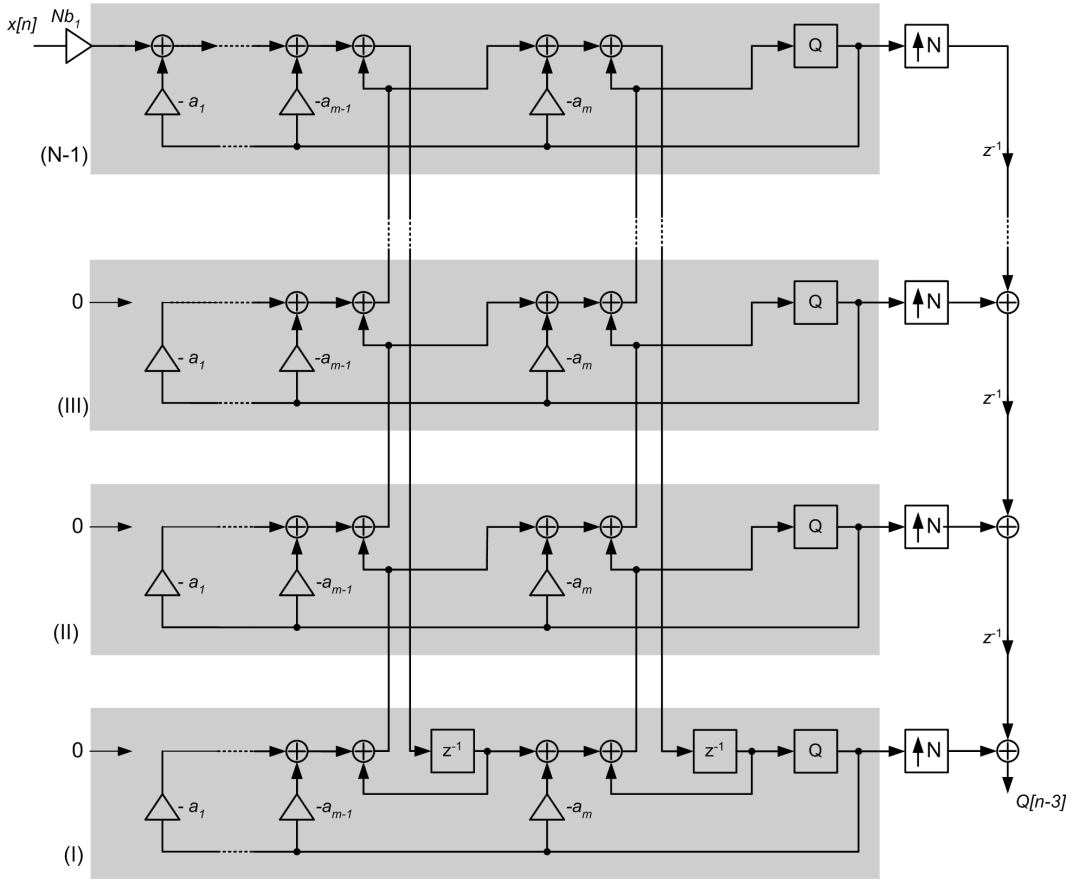

Figure 3.20: $TI-LP\Sigma\Delta$ modulator based on $CIFB$ structure with the input supplied to one of the parallel blocks.

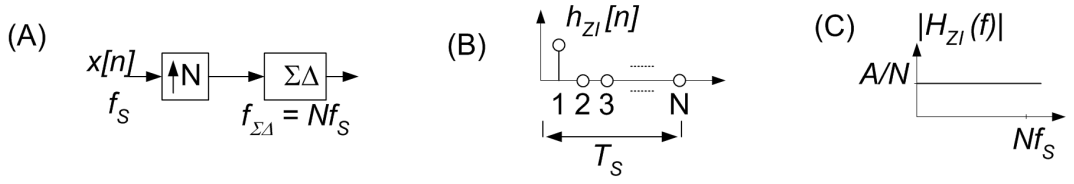

Figure 3.21: (A) Equivalent system for zero-insertion $TI-LP\Sigma\Delta$. (B) Impulse response of the upsampler. (C) Magnitude response of the upsampler.

upsampler as shown in Fig.3.21(A), whose impulse and magnitude responses are depicted in Fig.3.21(B, C). In the frequency domain, the output of the upsampler consists of a baseband portion of the input signal and aliases at frequencies $m\frac{f_{\Sigma\Delta}}{N}$, similar to the sample-hold technique explained before. The difference is that now the baseband, and each of the aliases have the same magnitudes due to a flat magnitude response $|H_{ZI}(f)|$ of the upsampler. The magnitudes of baseband portion of the signal and of the aliases equal $\frac{1}{N}$ of the upsampler's input signal magnitude. Consequently, the magnitude reduction in the

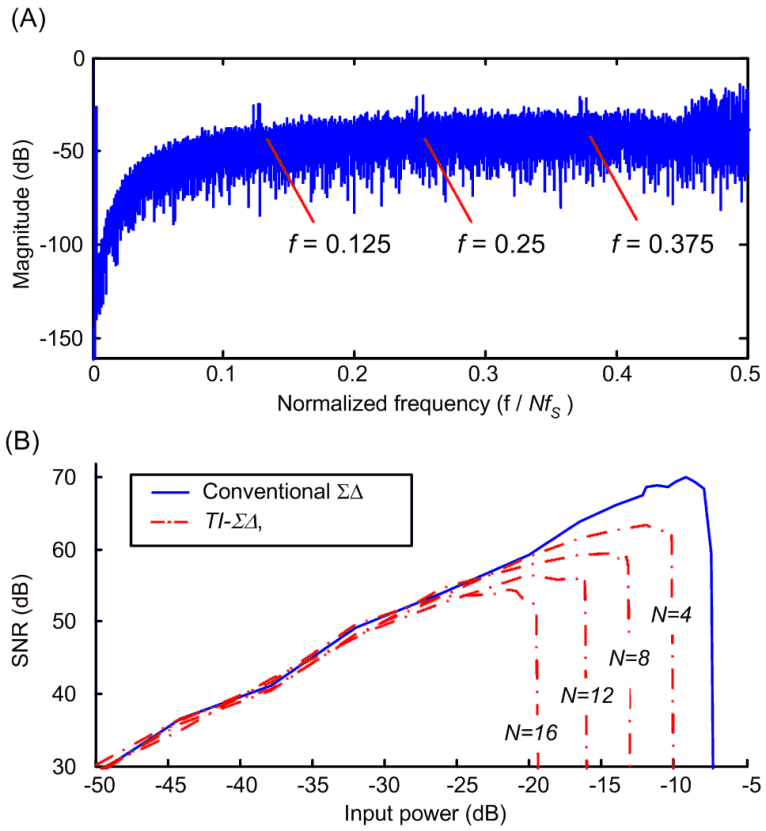

Figure 3.22: Simulated third order $TI-LP\Sigma\Delta$ with the same input supplied to one parallel block only, the input to the modulator is two tone signal: $Amp_1 = Amp_2 = 0.1$, $f_1 = 0.002Nf_S$, $f_2 = 0.0025Nf_S$, $|STF = 1|$. (A) Output spectrum for $N = 8$. (B) Comparison of SNR for $TI-LP\Sigma\Delta$ with equivalent modulator operating at sampling rate $f_{\Sigma\Delta} = Nf_S$, $OSR = \frac{f_{\Sigma\Delta}}{BW} = 50$.

output of the upsampler should be compensated by increasing input gain to the $TI-LP\Sigma\Delta$ N times, as seen in Fig.3.20. Now that the total input power to the $TI-LP\Sigma\Delta$ modulator is a sum of the baseband portion of the input signal and of the aliases, an overloading of the quantizer and subsequent unstable operation of the modulator may occur.

The impact of the aliases on the output of a $TI-LP\Sigma\Delta$ modulator can be seen in the following example: let us consider a third order modulator having the NTF zeros listed in Tab.2.3, and an $STF = 1$. The modulator is expanded to the time-interleaved system with only one parallel section supplied with the scaled input similar to the $TI-LP\Sigma\Delta$ of Fig.3.20. The simulated output spectrum of the TI modulator for $N = 8$ is shown in Fig.3.22(A). Apart from the baseband portion of the input signal, aliases at frequencies $f = \frac{1}{8}f_{\Sigma\Delta}$, $f = \frac{2}{8}f_{\Sigma\Delta}$, $f = \frac{3}{8}f_{\Sigma\Delta}$ and $f = \frac{4}{8}f_{\Sigma\Delta}$ are observed above the quantization noise.

It is concluded, that when the scaled input is supplied to the modulator, the total input power (power of baseband and aliases) increases as N increases and subsequently, the effective stable range of the $TI-\Sigma\Delta$ decreases. This effect is observed for simulated SNR vs. input power for the two tone input and $N = 4, 8, 12, 16$ shown in Fig.3.22(B). Note that all simulated modulators are characterized by the same NTF, and their effective sampling rates are also the same, i.e. $Nf_S = const = f_{\Sigma\Delta}$.

3.5.3.4 Zero-insertion in $TI-LP\Sigma\Delta$ modulator with lowpass STF

To take full-advantage of the reduced hardware complexity in the modulator with the zero-insertion, the aliases of the input signal should be suppressed prior to supplying the input to the TI modulator, or alternately in the course of the ΣΔ modulation, which can be achieved by utilizing a lowpass signal transfer function.

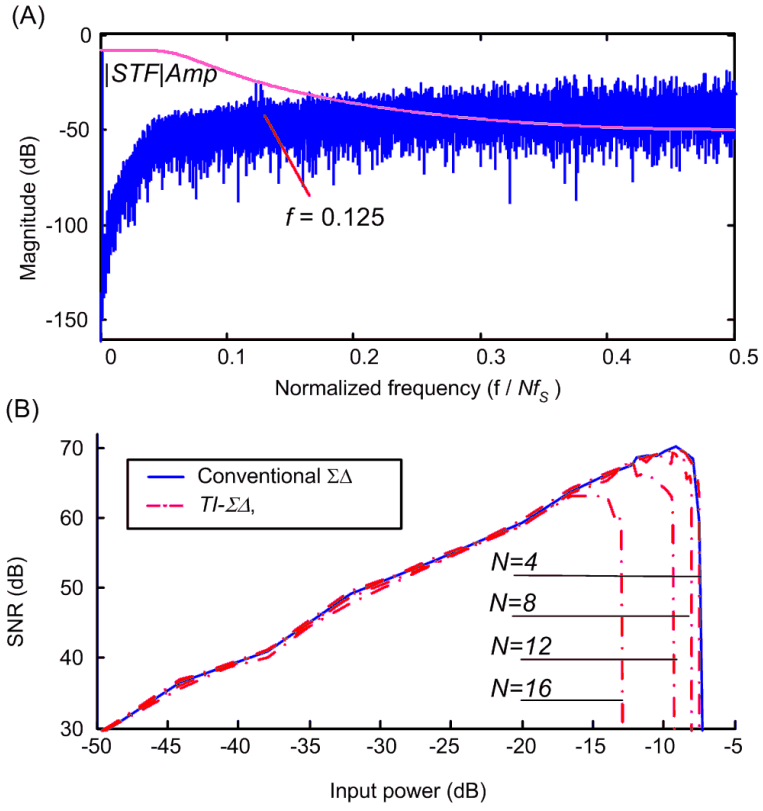

Figure 3.23: Simulated third order $TI-LP\Sigma\Delta$ modulator with the same input supplied to all parallel inputs. (A) Output spectrum for two tone input $Amp_1 = Amp_2 = 0.39$, $f_1 = 0.002Nf_S$, $f_2 = 0.0025Nf_S$, $N = 8$. (B) SNR comparison of $TI-LP\Sigma\Delta$ with equivalent modulator operating at sampling rate $f_{\Sigma\Delta} = Nf_S$.

This transfer function is provided by a $CIFB$ modulator, or other structures whose NTF and STF share the same poles as has been discussed in Section 2.3.5.3.

Let us consider the third order modulator whose NTF zeros and poles are listed in Tab.2.3. The modulator has lowpass STF shown in Fig.2.24 characterized by $3\,dB$ cut-off frequency $f_{coff} = f_{\Sigma\Delta}/16$. Simulation of the $TI-\Sigma\Delta$ modulator of Fig.3.20(A) done for $N = 8$ shows the expected suppression of the aliases by the lowpass STF in Fig.3.23(A) - only the first alias at frequency $Nf_S/8$ has magnitude higher than a quantization noise. The subsequent improvement of the stable input range is observed when comparing simulated SNR for different N of Fig.3.22(B) and Fig.3.23(B). Due to suppression of aliases, the third order $TI-LP\Sigma\Delta$ with the zero-insertion offers nearly the same stable range and SNR as equivalent modulator operating at four times higher sampling rate $(N = 4)$, having only $0.1\,dB$ lower stable input range. The stable input range reduces now by $0.63\,dB$ for $N = 8$, by $1.9\,dB$ for $N = 12$ and by $5.5\,dB$ when $N = 16$, which enables the use of higher amplitudes of an input signal than when the magnitude of STF is unity. The stable range of the $TI-\Sigma\Delta$ with zero-insertion can be increased further by reducing the Butterworth cut-off frequency, or by increasing the order of the NTF.

3.5.4 Band pass TI modulators

This section describes time-interleaved expansion of two $BP\Sigma\Delta$ modulators, $CRFB$ and direct feedback topology with delaying loop filter sections described earlier in this chapter. Also, the use of the parallel transformation for modulators with sample-hold and zero insertion is explained.

The design of the TI modulators based on $CRFB$ and distributed feedback structures is carried out using discrete time domain equations at N consecutive time indexes. The $CRFB$ for $N = 4$ and the distributed feedback topology for $N = 2$ are shown in Fig.3.24 Fig.3.25.

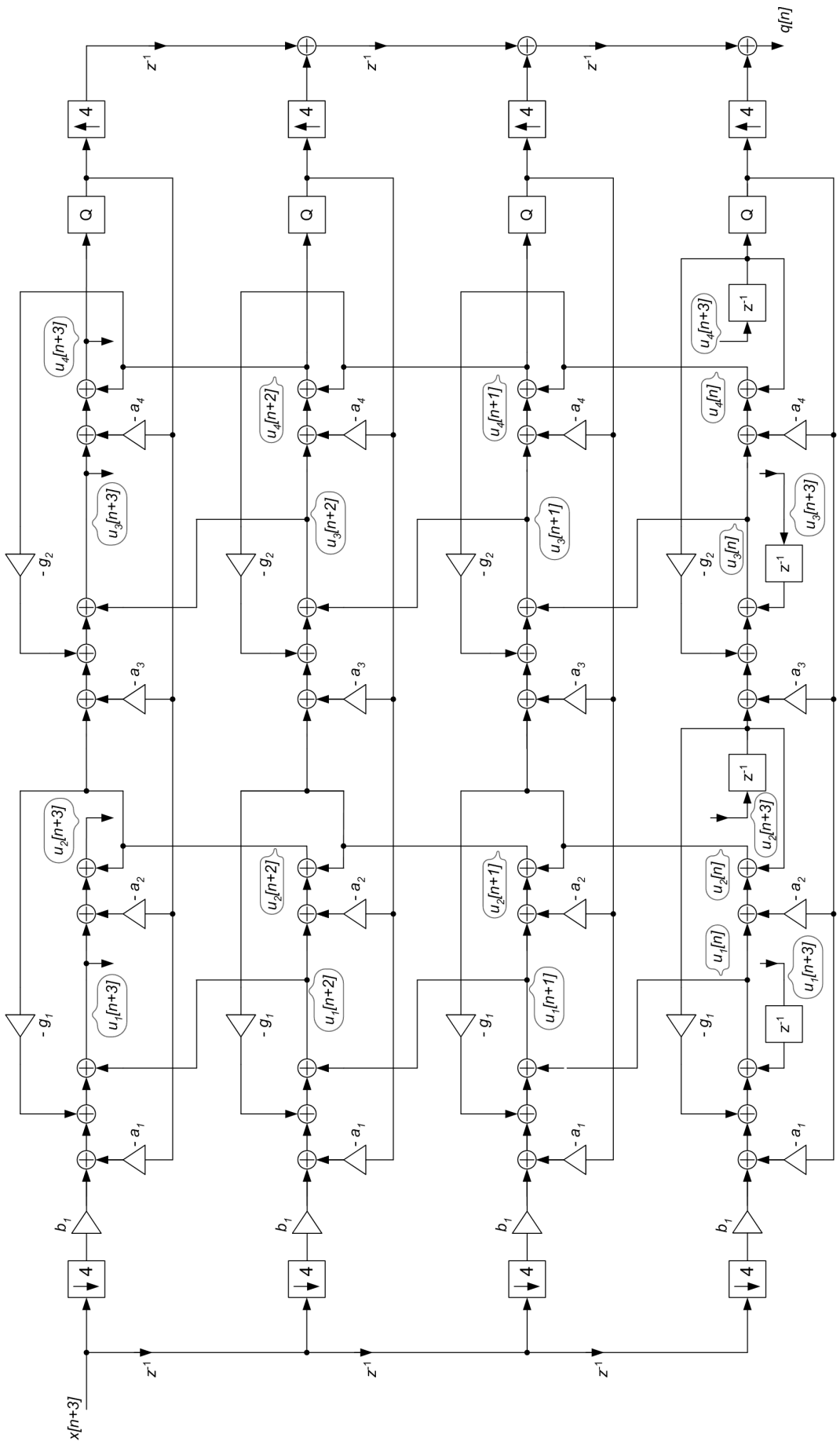

Figure 3.24: $TI-\Sigma\Delta$ based on fourth order $CRFB$ structure.

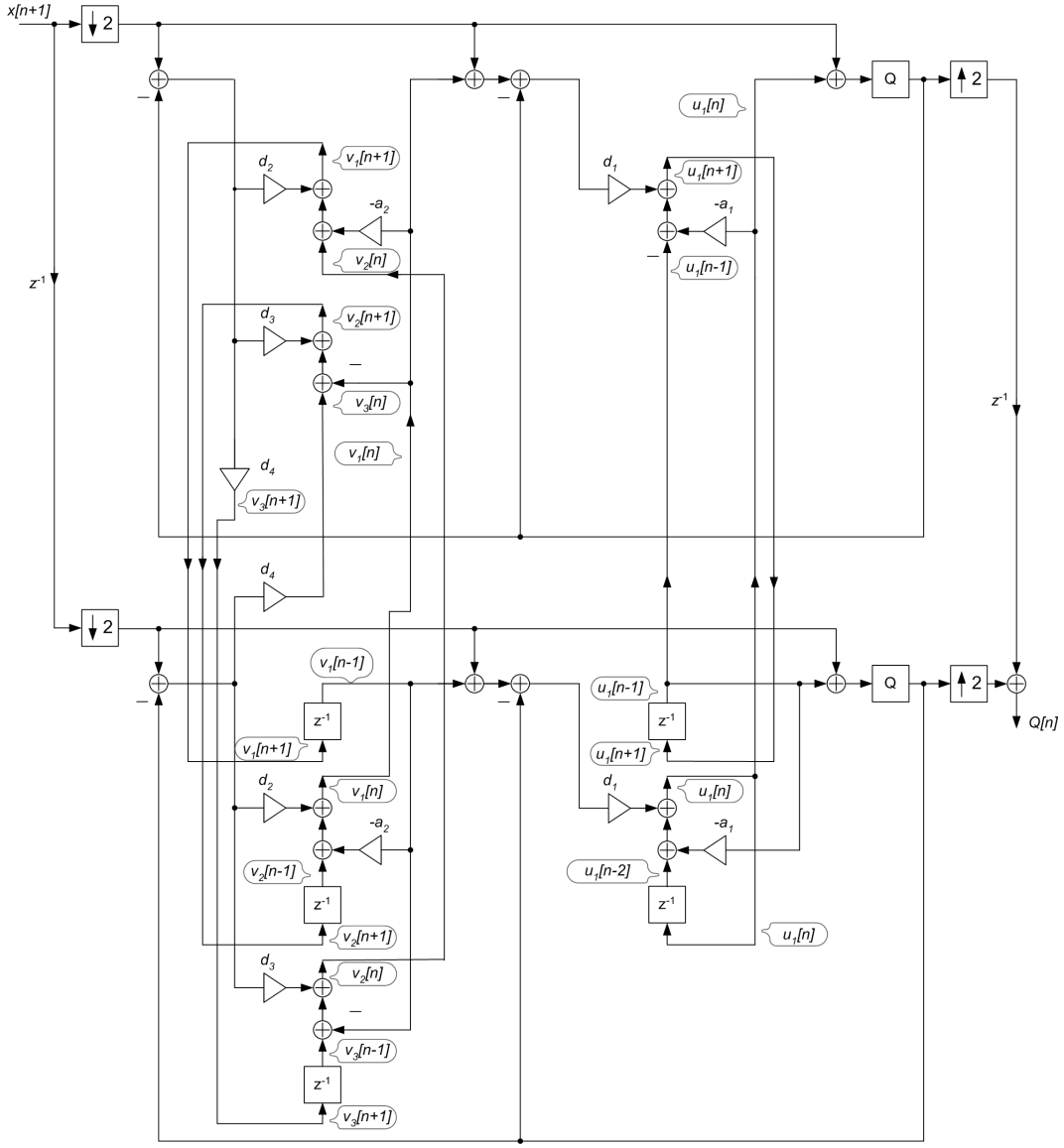

Figure 3.25: $TI-\Sigma\Delta$ based on fourth order modulator with delaying loop filters.

As the inputs signal to the modulators are bandpass, they should be sampled at the same rate as the $TI-\Sigma\Delta$ modulators, i.e. $f_{\Sigma\Delta} = Nf_S$ to avoid distortion caused by aliasing. Subsequently, both structures use input multiplexers in contrast with the sample-hold or zero-insertion used in $TI-LP\Sigma\Delta$ modulators.

Both of the structures can be employed for encoding input signal at any frequency in the range of $0 \leqslant f_0 \leqslant f_{\Sigma\Delta}/2$ using appropriate loop filters coefficients. Also, both of the $TI-BP\Sigma\Delta$ modulators are characterized by similar hardware count: every parallel section consists of 6 multipliers, 10 adders, 1 quantizer which is observed from Fig.3.24 and Fig.3.25. The drawback of the structure based on the new, distributed feedback topology

against the *CRFB* is that it uses an additional delay block. The disadvantage is however compensated by the shorter critical path, and expected higher maximum sampling rate than the *CRFB* structure. The maximum N in both $TI-BP\Sigma\Delta$ modulators shown above is however expected to be lower than in the case of $TI-BP\Sigma\Delta$ modulator based on the parallel, $z \to -z$ transformation described in Section 3.4.

When the modulator has its center frequency at one fourth of its effective sampling rate, i.e. $f_0 = f_{\Sigma\Delta}/4$, then the lowpass to parallel transformation described in Section 3.4 can be used. In such case, the $TI-\Sigma\Delta$ based on a *CIFB* or other lowpass structure increases sampling rate by N, and the sampling rate of the bandpass system increases again by a factor of two after transforming the pair of the $TI-LP\Sigma\Delta$ by means of $z \to -z^{-1}$ and placing them in parallel as it is shown in Fig.3.26. There are some possibilities for supplying the input to the $TI-BP\Sigma\Delta$ modulator, which depend on the modulator's structure.

When the $TI-LP\Sigma\Delta$ modulator uses the input demultiplexer operating at a high sampling rate, such as the first order system shown in Fig.3.14(B), then the $TI-BP\Sigma\Delta$ modulator is obtained by applying directly the scheme of Fig.3.26. This modulator should be supplied with a bandpass input signal sampled at the same rate as the TI system, $f_{\Sigma\Delta}$, and whose center frequency equals $f_0 = f_{\Sigma\Delta}/4$, similar to conventional $BP\Sigma\Delta$ modulator obtained in the course of $z \to -z^2$ transformation. In contrast, the sample-hold and zero-insertion methods use baseband inputs sampled at low rate $f_S = f_{\Sigma\Delta}/(2N)$, which requires modification of the distribution of input samples.

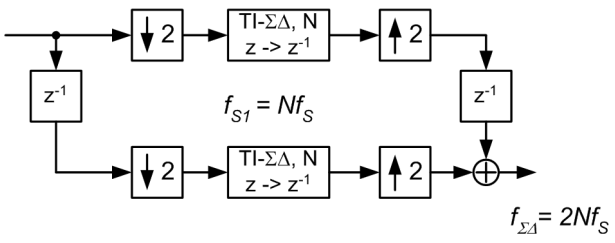

Figure 3.26: Parallel $BP\Sigma\Delta$ modulator.

In the case of the sample-hold technique, the parallel TI sections in Fig.3.26 are equivalent to highpass ΣΔ modulators. Subsequently the inputs to each of the two parallel sections should be shifted in a frequency domain at $Nf_S/2$, i.e. half of the sampling rate of the $TI-LP\Sigma\Delta$. This is achieved by multiplying by -1 every second input to the time-interleaved section as shown in Fig.3.27, which allows complexity reduction of the TI modulator by the input demultiplexer.

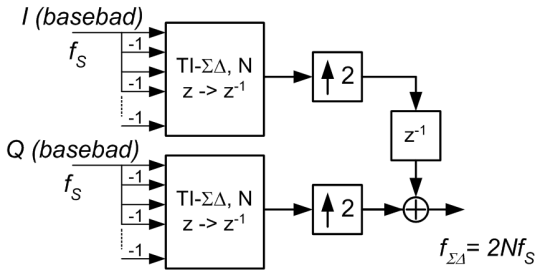

Figure 3.27: Bandpass $TI-\Sigma\Delta$ modulator with sample-hold.

The zero-insertion technique uses one input sample per N clock cycles, which makes the conversion of the baseband input signal for the highpass $TI-\Sigma\Delta$ modulator somewhat unclear. In fact, the zero insertion simplifies the process of TI modulation again. Let us notice, that the expander's output in $TI-LP\Sigma\Delta$ modulator with zero-insertion consists of the baseband portion of an input signal and its aliases of the same magnitudes at integer multiples of sampling rate f_S. Subsequently, one spectral copy of the baseband occurs at frequency $Nf_S/2$. The $z \rightarrow -z$ highpass transformation of the $TI-LP\Sigma\Delta$ modulator changes the NTF and the STF of the modulator, as is shown in Fig.3.28(A). The subsequent highpass STF suppresses now all spectral copies of the input signal apart from

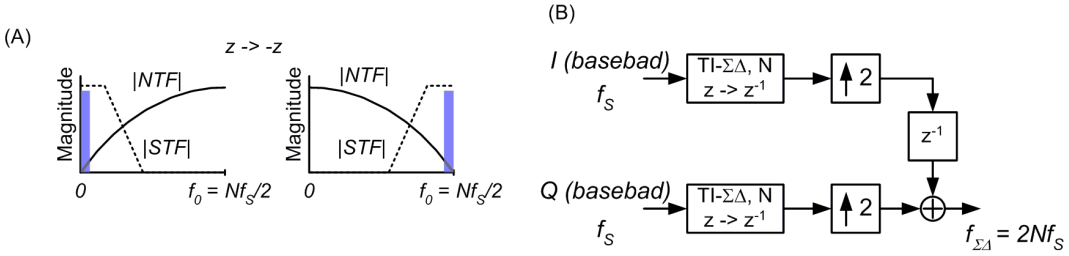

Figure 3.28: Bandpass $TI-\Sigma\Delta$ modulator with zero-insertion. (A) NTF and STF for $LP-TI\Sigma\Delta$ and $HP-TI\Sigma\Delta$. (B) Scheme of the $TI-BP\Sigma\Delta$ with zero-insertion.

the $X\left(e^{j(\omega\pm\omega_0)}\right)$ i.e. the copy at frequency $Nf_S/2$, which is the same as the signal encoded by highpass modulators of Fig.3.26. In consequence, the $TI-BP\Sigma\Delta$ modulator with zero-insertion simplifies to the scheme shown in Fig.3.28(B).

3.5.5 Conclusion

This section introduced new concept of parallel $\Sigma\Delta$ modulator based on discrete time domain equations. The design of the TI system is intended for programmable logic such as $FPGA$ rather than for SC circuit and subsequently, $\Sigma\Delta$ structures offering short critical paths were considered. As observed, the $TI-\Sigma\Delta$ based on discrete-time domain equations is a more hardware efficient method than the equivalent, block digital filter approach [53] caused by multiple cross-connections between the parallel blocks in the latter.

As demonstrated, the time-interleaved modulators used with $LP\Sigma\Delta$ allow for simplification of modulator structure by sample-hold or zero-insertion techniques. The utilization of a modulator with poles shared by STF and NTF allows for suppression of aliases caused by low sampling rate of the input to the modulator. The expansion to time-interleaved system of $BP\Sigma\Delta$ structures is possible, and it offers best results for modulators having NTF zeros at $f_0 = f_{\Sigma\Delta}/4$, i.e. the effective sampling rate of the modulator increases by factor of $2N$.

3.6 Experimental results

This section validates the technique of expansion to time-interleaved $\Sigma\Delta$ modulator, providing simulated and measured results for modulators implemented in $Virtex$ 2 Pro $FPGA$ of Xilinx.

3.6.1 Testbench

The tested modulators were supplied with a baseband signal having a bandwidth $1.25\,MHz$. The input signal was generated in the $FPGA$ using a pseudo random generator, whose binary output was fed to a raised cosine filter. The input sequence was sampled at the rate of $f_S = 50MHz$ and simple, sample-hold method described in Section 3.5.3.1 was used for increasing the sampling rate to the rate of $\Sigma\Delta$ modulators. The $FPGA$ used $100\,MHz$ clock signal. The output multiplexer was implemented with the use of *Rocket IO* transceiver operating as a $20\,bit$, parallel to serial register. The serial output from $FPGA$ board was connected to digital spectrum analyzer FSL of *Rohde & Schwarz*. The scheme of the testbench and simulated input signal are shown in Fig.3.29.

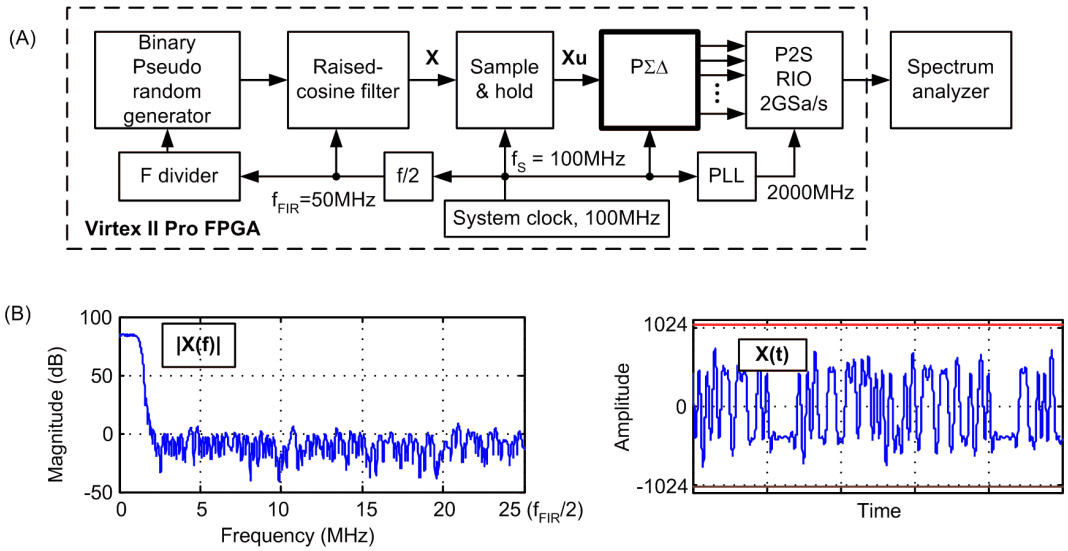

Figure 3.29: $FPGA$ test bench for $TI-\Sigma\Delta$ modulators. (A) Block diagram. (B) Simulation of an input signal in time and frequency domains.

3.6.2 Implemented modulators

The implemented structures were first order and second order $CIFB$, $LP\Sigma\Delta$ modulators for $N = 1$ $(100\,MHz)$, $N = 2$ $(200\,MHz)$ and $N = 4$ $(400\,MHz)$.

The simulated outputs of first order $TI-LP\Sigma\Delta$ modulators show a dynamic range improvement by approximately $9\,dB$ per every doubling of the sampling rate as seen in

Fig.3.30(A-C), which is in agreement with the theoretical expectation [69]. The graphs on the right hand side show measured spectra from the output of the Virtex II Pro $FPGA$ board. The measured results resemble the simulated modulators outputs for $f_{\Sigma\Delta} = 100MHz$ and $f_{\Sigma\Delta} = 200MHz$. Some degradation in dynamic range to the simulated spectrum is observed at low frequencies when $N = 4$ and $f_{\Sigma\Delta} = 400MHz$. The distortion has been caused by a jitter added by PLL in Rocket IO of the $FPGA$, and by memory effect in the output, $1\,bit$ digital to analog converter (DAC).

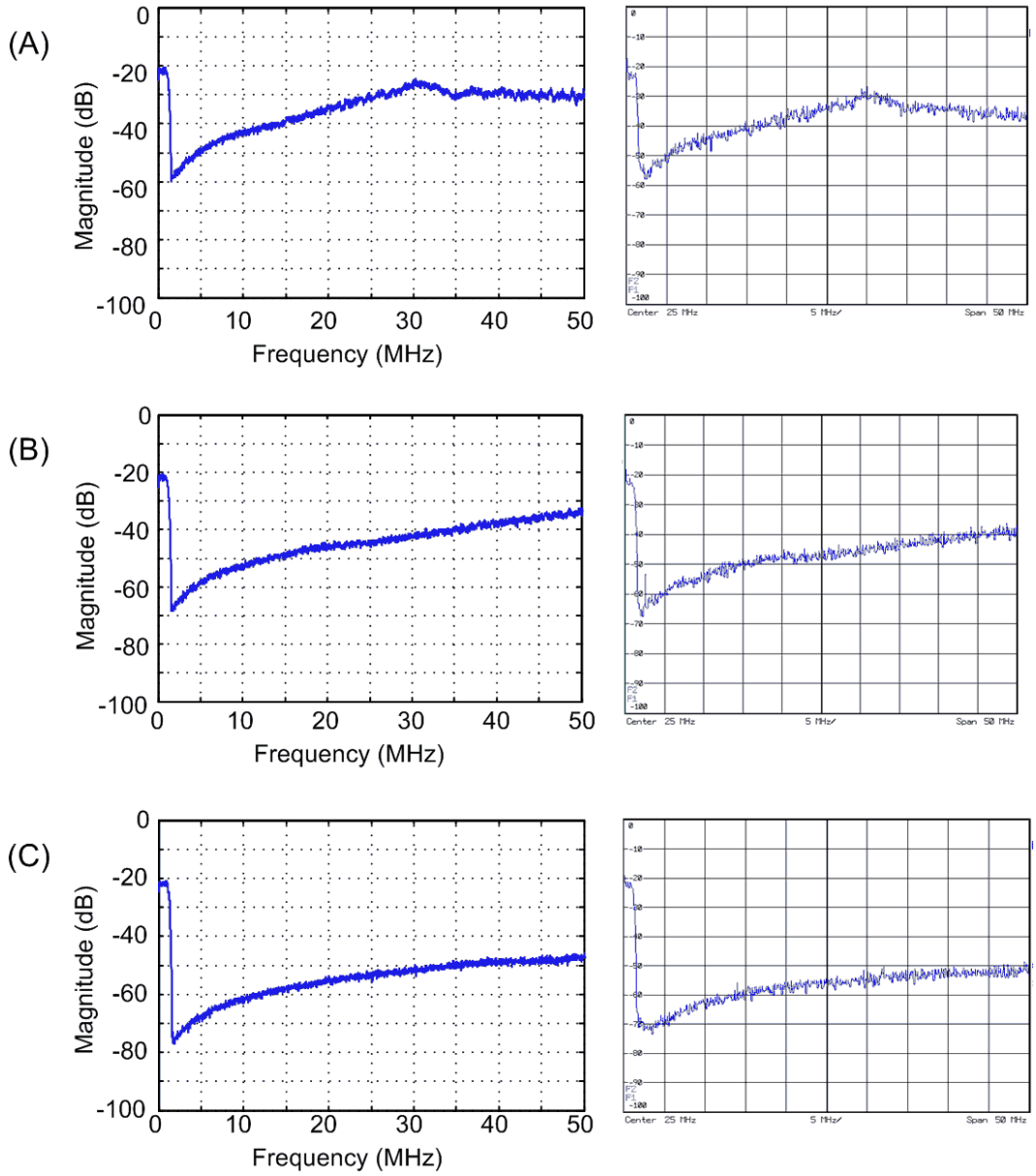

Figure 3.30: First order ΣΔ modulator, simulated-left and measured-right.
(A) $f_S = 100MHz$. (B) $N = 2$, $f_S = 200MHz$. (C) $N = 4$, $f_S = 400MHz$.

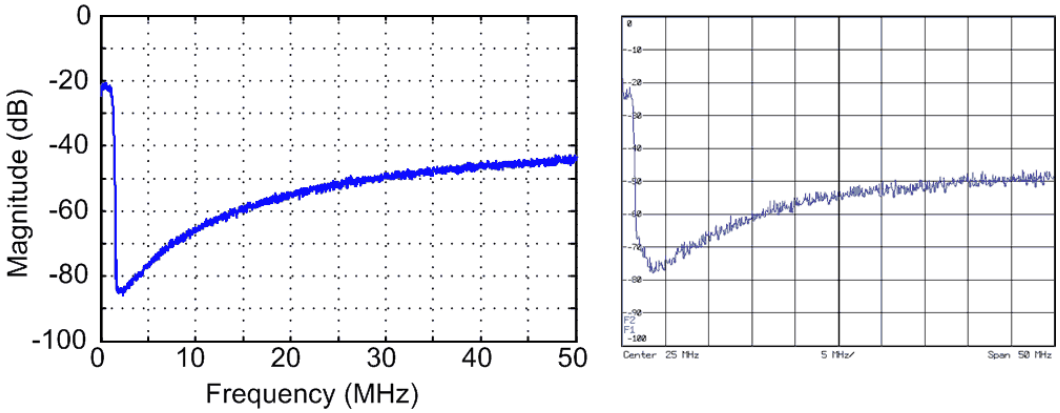

Figure 3.31: Second order $TI-LP\Sigma\Delta$ modulator, simulated-left and measured-right for $N=4$, $f_S=400MHz$.

Fig.3.31 shows simulated and measured output of the $TI-LP\Sigma\Delta$ modulator based on second order $CIFB$ structure for $f_{\Sigma\Delta}=400MHz$ $(N=4)$. The dynamic range in the simulated output of the second order modulator improves in comparison with first order $TI-LP\Sigma\Delta$ output shown in Fig.3.31(C) due to increase of modulator's order. Also, some increase of a noise floor in the proximity of the baseband signal is seen in the output of the second order modulator shown Fig.3.31. This performance degradation has been caused by the effect of a finite, 11 *bit* precision used in the simulated modulator. The measured output spectrum resembles the simulated one, with some performance degradation caused by jitter and nonlinearity of the DAC. The implemented modulators prove the concept of the parallel expansion technique presented in this chapter, and show increase of sampling rate of a $\Sigma\Delta$ modulators in comparison with conventional modulators implemented in the same, or newer generations of $FPGA$s: $f_{\Sigma\Delta}=100MHz$ for error feedback topology [95] in Virtex II Pro, $f_{\Sigma\Delta}=215MHz$ for second order $CRFB$ structure implemented in Virtex II Pro [94], $f_{\Sigma\Delta}=219MHz$ for second order $CRFF$ structure implemented in Virtex 6 [45].

3.7 Conclusion

The TI expansion is aimed at increasing the sampling rate of the modulator, being critical to the SNR of the output signal, but also allowing latter reconstruction of the modulated, bandpass signal by analog filtering. This chapter introduced two new techniques of parallelizing $\Sigma\Delta$ modulators, one transforming $LP\Sigma\Delta$ to $BP\Sigma\Delta$, and one based on computation of subsequent states of the modulator.

The sampling rate of a $TI-\Sigma\Delta$ increases N times, where N denotes the number of modulator blocks in parallel. The maximum possible expansion factor N depends on the number of multibit adders and multipliers in cascade in the critical path of the $TI-\Sigma\Delta$ modulator. The shortest critical path can be obtained in lowpass modulators whose NTF zeros are superimposed at $z=1$. The optimization of the zeros or bandpass operation requires that loop filters sections are of at least second order, which in turn has the effect of increasing the critical path. In order to prevent this increase, the loop filters in a modulator's topology should be of possibly low order - first or second - and of delaying type.

The hardware count reduction in a $TI-LP\Sigma\Delta$ modulator can be achieved by using the zero-insertion technique, which allows for removing the first adder in each but one of the parallel $\Sigma\Delta$ sections. While the simplification creates input signal aliases at frequencies $m\frac{f_{\Sigma\Delta}}{N}$, their suppression is possible when the modulator has lowpass STF. Such STF is common in $LP\Sigma\Delta$ modulators whose STF and NTF share the same set of poles as discussed in Section 2.3.5.3.

The problem of extended critical path in a $BP\Sigma\Delta$ modulator can be avoided when a pair of $z\rightarrow -z$ transformed $LP\Sigma\Delta$ modulators are used in parallel. The resulting $BP\Sigma\Delta$ modulator has its NTF zeros at $z=\pm j$, and increases the sampling rate by factor of two.

The contributions of this chapter are:

1. New structure of a bandpass ΣΔ modulator using delaying loop filters has been designed

2. New technique for expansion to a $TI-\Sigma\Delta$ based on discrete time domain equations of the modulator has been presented

3. The effect of up-sampling in the TI modulator with zero-insertion on modulator's stability and its SNR has been explained, and the suppression of aliases in the input spectrum has been achieved through the use of lowpass STF

4. The use of two TI modulators in parallel for obtaining $TI-BP\Sigma\Delta$ modulator operating at increased sampling rate has been proposed

Chapter 4

Improved coding efficiency $BP\Sigma\Delta$ modulator

This chapter describes a new method of 2-level modulation of a band-pass signal. The new modulation is based on 3-level $\Sigma\Delta$ modulation and error pulses shaping. While the output of the new modulator has only 2 levels, it can perform nearly as good as a 3-level $BP\Sigma\Delta$ modulator, and it generates less quantization noise than a conventional 2-level $BP\Sigma\Delta$ modulator. One of the uses for the new modulator is in a Class-S power amplifier, where a 2-level signal drives an RF switchmode power amplifier $(SMPA)$.

The concept of error pulse shaping and 3-level to 2-level conversion is introduced in the first part of the chapter. The analysis of the noise performance is followed by a description of a linearization technique developed for the new modulator. Subsequently experimental results and comparison against 3-level and conventional 2-level modulators are provided.

4.1 3-level ΣΔ modulation

The advantage of a multilevel over a 2-level quantization is less quantization-noise in the output of the former. While in theory the use of a multilevel quantizer improves *SNR* in comparison with 2-level quantizer, in practice a displacement of any of the levels induces nonlinear distortion in the multilevel output. This section presents an exception to this rule when applied in the output of a 3-level, *BP*ΣΔ modulator. A technique of shaping error pulses in the output of 3-level *BP*ΣΔ is explained and demonstrated.

4.1.1 3-level quantizer with zero-level offset

The use of 3-level quantizer reduces quantization-error power by $6\,dB$ in comparison with a 2-level quantizer. The problem arises when the stage that follows the 3-level modulator exhibits unequal spacings between the levels. The effect of displacement of one of the levels has been explained in Section 2.3.4 and can be demonstrated when a 3-level, *LP*ΣΔ modulator is followed by a 3-level *SMPA* as it is shown in Fig.4.1(A, B). The consequence of the zero-level displacement is the increased error power in the output spectrum.

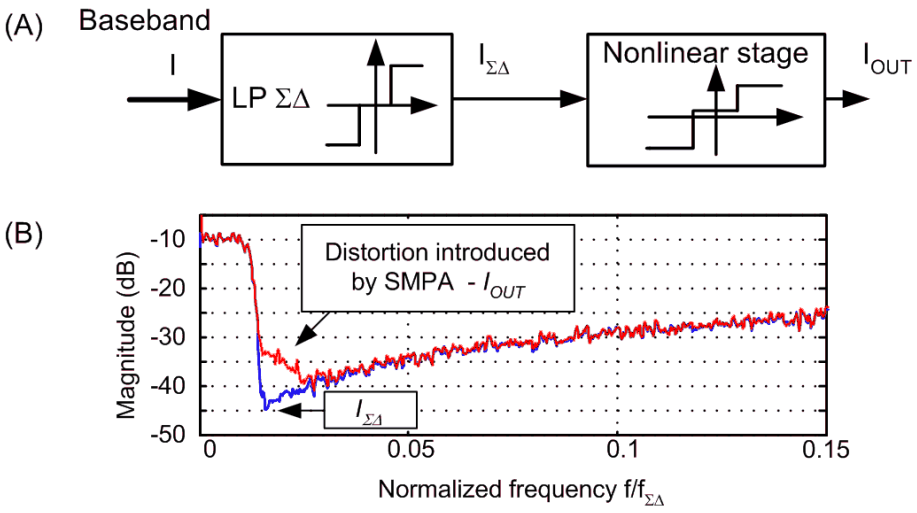

Figure 4.1: ΣΔ driving 3-level *SMPA*. (A) Zero level displacement in the *SMPA*. (B) Distortion in the output spectrum.

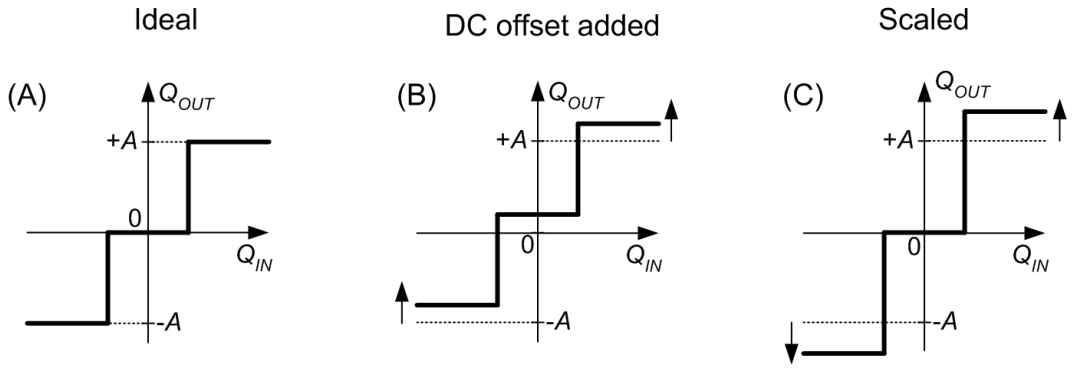

Figure 4.2: 3-level quantizer's input output characteristic. (A) Ideal. (B) DC offset added. (C) Scaled.

The 3-level quantizer in a *LP*ΣΔ modulator has the input-output characteristic shown in Fig.4.2(A). In an ideal case and when the gain of the 3-level *SMPA* in Fig.4.1(A) is unity, the *SMPA* has the same output levels as the *LP*ΣΔ, i.e. $-A, 0, +A$. In contrast to this situation, a real device's characteristic can stray from the ideal case. Three possible types of alteration of the input-output characteristic are,

1. All three levels are offset by a constant, positive or negative value A_1, but the distance A between the levels is preserved, i.e. $Q = \{-A+A_1; 0+A_1; +A+A_1\}$ as it is depicted in Fig.4.2(B)

2. The output characteristic is scaled, i.e. $Q = \{-Ag; 0; +Ag\}$, and g is a real number, as shown in Fig.4.2(C)

3. Only one of the levels shifts, while the other two remain unchanged,

   (a) $Q = \{-A; 0+A_1; +A\}$, example of which is shown in Fig.4.3(A)

   (b) $Q = \{-A+A_1; 0; +A\}$ or $Q = \{-A; 0; +A+A_1\}$, example of which is shown in Fig.4.3(B)

The change in 3-level characteristic described in point 1. adds a DC offset to the output, while the change of point 2. scales the output signal. None of the two causes nonlinear

distortion in the output. In contrast, the offsetting of only one of the levels described in point 3. adds nonlinear distortion in the output of the *SMPA*.

Both types of displacement described in point 3. can be represented by a quantizer whose zero level is offset by some value A_1 as it is shown in Fig.4.3(A). The equivalence of upper or lower level shift of point 3.(b) with the scaled characteristic having displaced zero-level of point 3.(a) is depicted in Fig.4.3(B). Consequently, the displacement of the quantizer's level will be represented in the following sections by a zero-level offset depicted in Fig.4.3(A). It is also assumed that the quantizer's characteristic does not change over time, or the period of changes is much longer than a sampling period of the *LP*ΣΔ modulator.

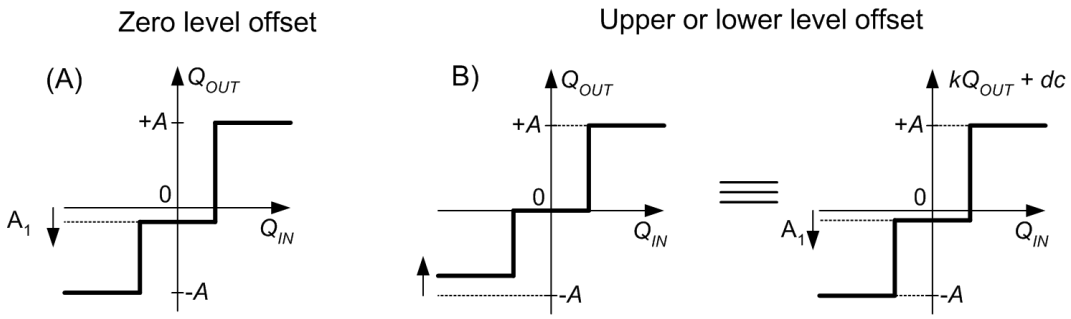

Figure 4.3: Input-output characteristic of 3-level quantizer. (A) Zero level is displaced. (B) Lower (or upper) level is displaced and equivalent transfer-function.

4.1.2 Error pulses

The zero-level displacement in the 3-level characteristic of Fig.4.3(A) causes an addition of a constant value A_1 to the quantizer's output each time the quantizer's input is zero. An example of where $I_{\Sigma\Delta}$ and I_{OUT} are input and output waveforms of the quantizer is shown in Fig.4.4. The quantizer's output I_{OUT} becomes a sum of a linear output and pulses $g_e(t)$ corresponding to zero-inputs. The time $T_{\Sigma\Delta} = \frac{1}{f_{\Sigma\Delta}}$ denotes sampling period of the ΣΔ modulator. If the error $g_e(t)$ is an ideal square pulse, then its Fourier transform $G_e(f)$ given by (4.1) has zeros at integer multiples of frequency $f_{\Sigma\Delta}$ as shown in Fig.4.5.

$$G_e(f) = T_{\Sigma\Delta} A_1 sinc\left(\frac{\omega T_{\Sigma\Delta}}{2}\right) e^{-j\omega T_{\Sigma\Delta}(n+1/2)} \tag{4.1}$$

The zero-level offset in the 3-level quantizer causes distortion in the modulator's output at low frequencies, but the distortion products are suppressed by the zeros of $G_e(f)$ at frequencies $Mf_{\Sigma\Delta}, M = 1,2,3...$ as seen from the magnitude response drawn in Fig.4.5. This property of function $G_e(f)$ can be used for suppressing the effect of the nonlinear distortion in the output from a 3-level $BP\Sigma\Delta$ modulator.

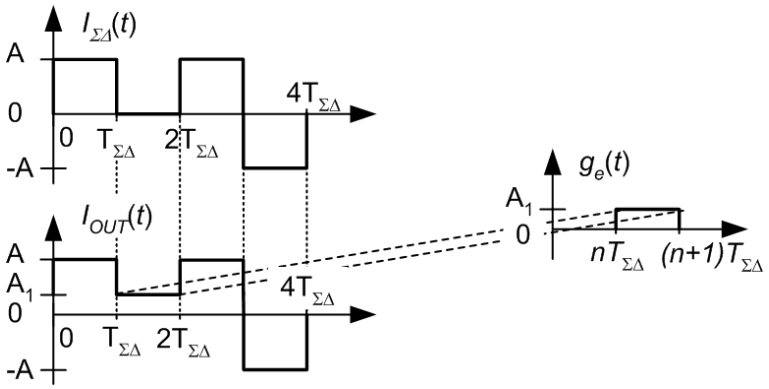

Figure 4.4: Input and output waveforms of the nonlinear stage.

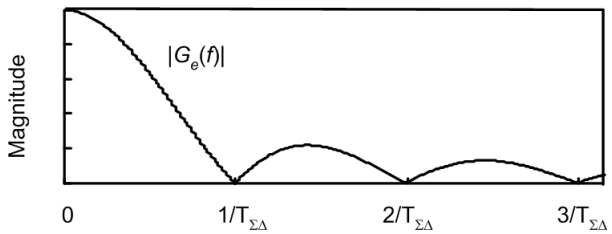

Figure 4.5: Fourier transform of the error pulse.

4.1.3 3-level $BP\Sigma\Delta$ modulator with zero-level offset

One of the existing modulation schemes for a digital *RF* transmitter utilizes a pair of $LP\Sigma\Delta$ modulators. Each of the modulators encodes low-frequency, baseband signal *I* or *Q*. $LP\Sigma\Delta$ modulators outputs are consequently mixed with a carrier and added [47].

Let us assume that the pair of $LP\Sigma\Delta$ modulators supply 3-level output signals $I_{\Sigma\Delta}$, $Q_{\Sigma\Delta}$ to a quadrature mixer. Subsequently, the quadrature mixer is followed by a 3-level quantizer with zero-level offset as it is shown in Fig.4.6. The blocks $c(t)$ and $s(t)$ in

the quadrature-mixer of Fig.4.6 have the same fundamental frequency f_C but are shifted in phase by 90° as depicted in Fig.4.7. The quadrature mixer's output yields band-pass signal at the carrier frequency f_C similar to the spectrum shown in Fig.4.9(B).

Let us consider two different input conditions for the quadrature-mixer. In the first case both inputs, $I_{\Sigma\Delta}$ and $Q_{\Sigma\Delta}$ are zero, and in the second case only one input is zero. When both inputs are zero, $I_{\Sigma\Delta} = Q_{\Sigma\Delta} = 0$, the quadrature mixer produces zero output, yielding the error pulse $g_e(t)$ of amplitude A_1 in the output of the nonlinear quantizer as it is depicted in Fig.4.8 for the time interval $0 \leqslant t \leqslant T_{\Sigma\Delta}$. As explained earlier, the magnitude response of $G_e(f)$ has a zero at a frequency $Mf_{\Sigma\Delta}$. When only one input to the quadrature-mixer is zero, i.e. $I_{\Sigma\Delta} \neq 0$, $Q_{\Sigma\Delta} = 0$ or $I_{\Sigma\Delta} = 0$, $Q_{\Sigma\Delta} \neq 0$, the error pulse in the output of the nonlinear quantizer no longer has the shape of the pulse $g_e(t)$. This error pulse, denoted here as $h_e(t)$, is found by offsetting zero valued intervals in the

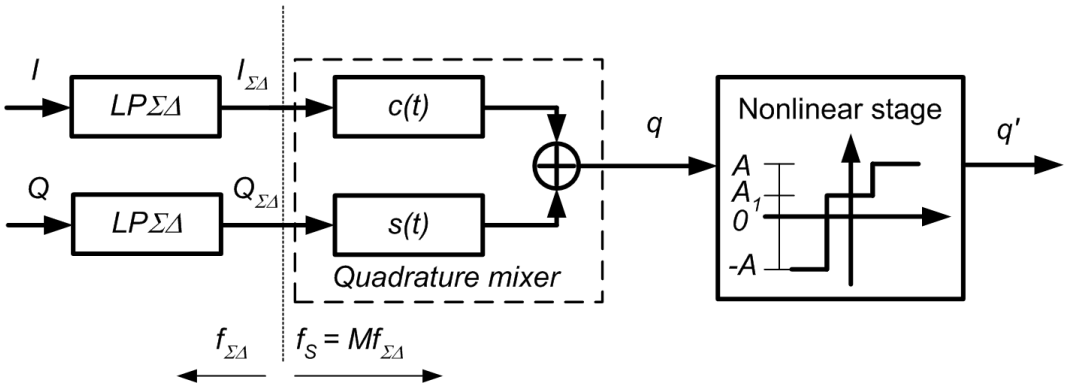

Figure 4.6: Quadrature mixer followed by SMPS with zero-level offset.

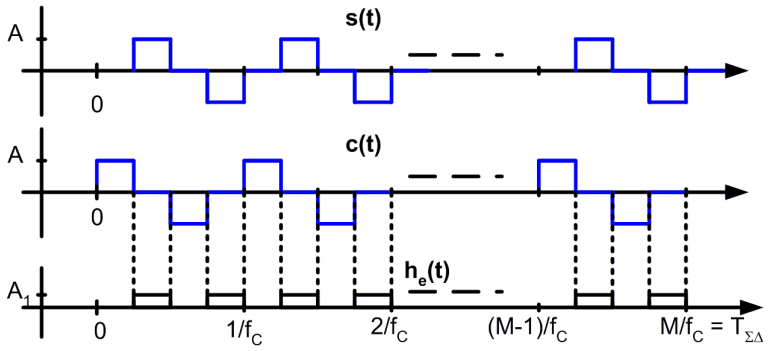

Figure 4.7: Impulse responses of $c(t)$ and $s(t)$ blocks and error pulse $h_e(t)$ corresponding to $I_{\Sigma\Delta} \neq 0$, $Q_{\Sigma\Delta} = 0$.

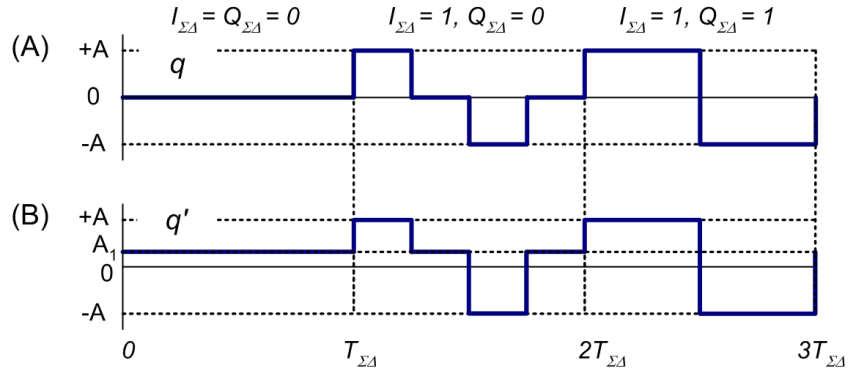

Figure 4.8: Error signal introduced by the zero-level offset in the quantizer for $M = 1$, $f_C = f_{\Sigma\Delta}$. (A) 3-level output $q(t)$. (B) Output $q'(t)$ for a positive A_1.

impulse response of a sine or a cosine blocks by the constant A_1 as seen in the example waveform of Fig.4.8 for $M = 1$ at the time $T_{\Sigma\Delta} \leqslant t \leqslant 2T_{\Sigma\Delta}$. In a more general case, $h_e(t)$ becomes a sequence of pulses of duration $\frac{T_{\Sigma\Delta}}{4M}$ as depicted in Fig.4.7 for positive A_1. The initial time offset of the pulses depends on whether $I_{\Sigma\Delta} \neq 0$ or $Q_{\Sigma\Delta} \neq 0$, and their amplitude may be positive or negative, depending on A_1 and the input to the quadrature mixer. Regardless of the time offset and polarity, the magnitude response $|H_e(f)|$ remains the same, and depends only on parameter M. A Fourier transform of the pulse $h_e(t)$ depicted in Fig.4.7 yields (4.2), a function that has also a zero at the frequency $Mf_{\Sigma\Delta}$.

$$\begin{cases} H_e(f) = 2A_1 \cdot \frac{T_{\Sigma\Delta}}{8M} \cdot sinc\left(\omega \frac{T_{\Sigma\Delta}}{8M}\right) \sum_{m=1}^{2M} e^{-j\omega t_m} \\ t_m = \frac{T_{\Sigma\Delta}}{8M}\left[1 + 4(m-1)\right] \end{cases} \tag{4.2}$$

Next, let us express the output of the quadrature-mixer by,

$$q(t) = I_{\Sigma\Delta} \cdot cos(2\pi f_C t) + Q_{\Sigma\Delta} \cdot sin(2\pi f_C t) \tag{4.3}$$

If a carrier frequency f_C such that

$$f_C = Mf_{\Sigma\Delta} \tag{4.4}$$

is chosen with M being a positive integer number, then by property of (4.1) and (4.2) the carrier frequency f_C will coincide with a zero of $G_e(f)$ and $H_e(f)$.

The occurrences of the error pulses can be written as a convolution of discrete time

error signals $e_1[n]$, $e_2[n]$ with error pulses $g_e(t)$, $h_e(t)$, and added to the 3-level output $q(t)$, resulting in the distorted output $q'(t)$,

$$q'(t) = q(t) + e_1[n] \star g_e(t) + e_2[n] \star h_e(t) \tag{4.5}$$

Note that $e_1[n]$ and $e_2[n]$ denote error signals, in contrast to a single occurrence of either error pulse. When (4.5) is rewritten in the frequency domain it yields,

$$Q'(f) = Q(f) + E_1(f) G_e(f) + E_2(f) H_e(f) \tag{4.6}$$

since

$$G_e(f_C = Mf_{\Sigma\Delta}) = H_e(f_C = Mf_{\Sigma\Delta}) = 0 \tag{4.7}$$

then

$$Q'(f_C) = Q(f_C) \tag{4.8}$$

which concludes that the quadrature mixer described above for $M = 1, 2, 3...$ and coupled with the nonlinear 3-level quantizer suppresses the error at the frequency f_C. It should be noted that the perfect suppression of the error added in the nonlinear quantizer occurs only at the carrier frequency f_C, and it worsens as the signal bandwidth widens. Because the error suppression follows similar rules as the suppression of a quantization noise by a NTF zeros in a ΣΔ modulator, high oversampling ratio should be used to ensure its maximum suppression by zeros of G_e and H_e. Also, the above analysis assumes that the error pulses have zero rise/fall times, which cannot be achieved in real systems.

4.1.4 Simulated output for $M = 1$, $A_1 = 0.2$

In order to verify the effect of the inband error suppression described in the previous section, a Matlab simulation of the modulator of Fig.4.6 is performed. Let the modulator be supplied with some bandlimited baseband signals I and Q $\left(BW_{I,Q} = f_{\Sigma\Delta}/160\right)$ and the

quadrature-mixer have the up-conversion factor of $M = 1$. A first order noise-transfer-function of the 3-level $LP\Sigma\Delta$ modulators $\left(NTF = 1 - z^{-1}\right)$ and magnitude responses of $G_e(f)$ and $H_e(f)$ are shown in Fig.4.9(A). The output $Q(f)$ and the error spectrum found by computing the FFT of $err(t) = e_1[n] \star g_e(t) + e_2[n] \star h_e(t)$ are shown in Fig.4.9(B, C) for quantizer levels $A = 1$ and zero-level offset $A_1 = 0.2$. It is observed that the error induced by the offset A_1 has a maximum magnitude $15dB$ below the quantization-error magnitude of the 3-level ΣΔ modulators in the proximity of frequency $f_C = 1$. This indicates only a small degradation of the performance in the output $Q'(f)$ to the ideal 3-level output $Q(f)$ and it proves the suppression of the error stated in the previous section. It can be observed from the frequency domain plots that both error shaping functions $|G_e(f)|$, $|H_e(f)|$ have maxima at frequency $f = 0$, while $H_e(f)$ has also a maximum in the proximity of frequency $f = 2f_C$. The maxima at frequencies 0 and in the proximity of frequency $2f_C$ of the two functions occur also for higher values of parameter M, and cause subsequent increase of the error magnitude at these frequencies, which is seen in Fig.4.9(C).

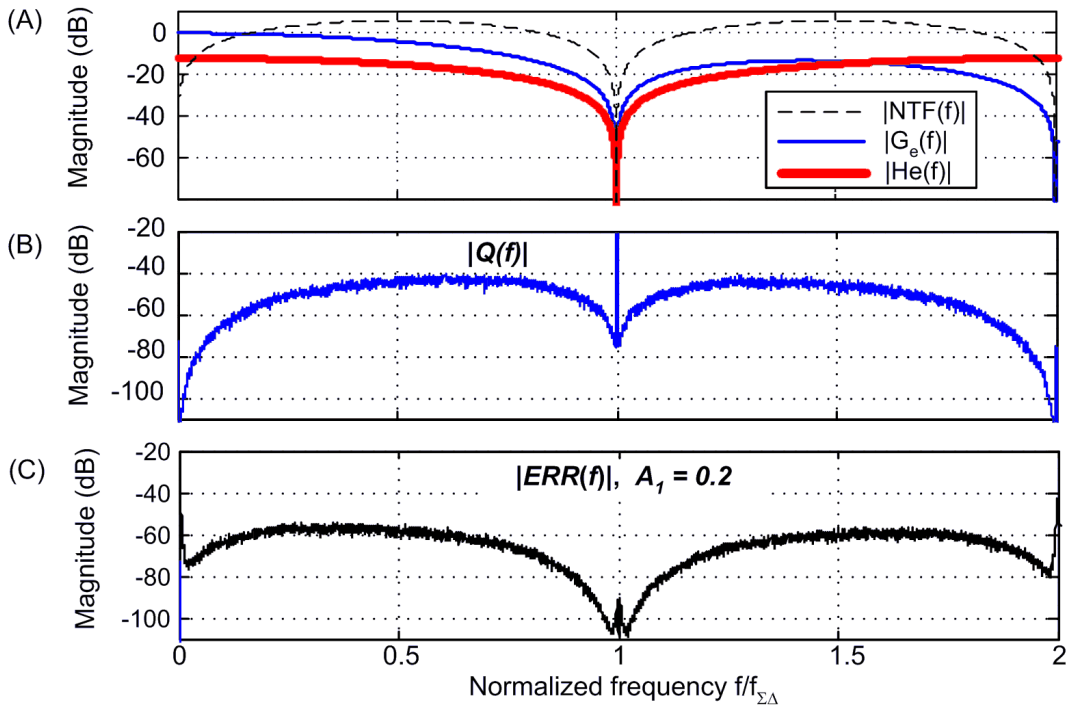

Figure 4.9: (A) First order noise transfer function, $|G_e(f)|$, $|H_e(f)|$. (B) Output spectrum of 3-level modulator$|Q(f)|$. (C) Spectrum of error $|ERR(f)|$ for $A_1 = 0.2A$.

4.1.5 Conclusion

This section described the effect of an uneven spacing between quantizer levels in a 3-level ΣΔ modulator. It was demonstrated that a linearity of the 3-level *BP*ΣΔ modulator can be robust to the zero-level offset when the output signal is centered at an integer multiple of the sampling frequency $f_{\Sigma\Delta}$. When the condition of $f_C = Mf_{\Sigma\Delta}$ is met, the magnitude responses of the error pulses have zeros that coincide with the signal frequency f_C, suppressing the error.

4.2 Modified 2-level modulator

This section describes a new technique of 2-level modulation of a band pass signal. The new modulation method is based on the shaping of the error pulses explained in Section 4.1. The obtained modulator offers noise performance close to that of a 3-level *BP*ΣΔ modulator, while generating only a 2-level output.

4.2.1 Conventional modulator

A 2-level ΣΔ modulator's output switches between zero and some non zero-valued amplitude, e.g. $0, +2A$ such as the waveform shown in Fig.4.12(B). This pulse stream can be used in a Class-S power amplifier to drive a 2-level, Class-D stage [24,25,28,41,42]. The drive signal can be generated with the use of the conventional modulator, employing a pair of 2-level *LP*ΣΔ modulators as shown in Fig.4.10. The coding efficiency in this case is however poor and the subsequent output is dominated by quantization noise power. The conventional modulator whose two output levels are $0, +2A$, supplied with an input of a mean value of $+A$ will be delivering an output level of $+2A$ for half of the operation time regardless of the input signal's amplitude. Consequently, the power of such output pulse stream is given by (4.9),

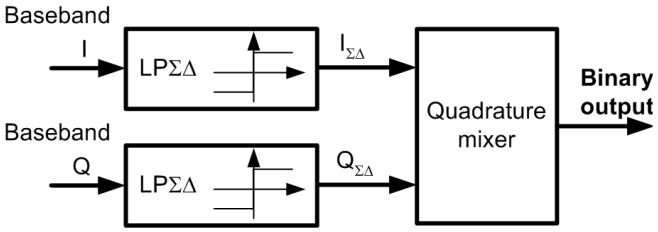

Figure 4.10: Conventional 2-level signal modulator.

$$q_{2L}^2 = 2A^2 = const \tag{4.9}$$

The quantization noise in the output of the 2-level signal can be reduced by modifying the modulator as it is described in next section.

4.2.2 Modified modulator

The scheme of the modified modulator is shown in Fig.4.11. It is created by replacing the pair of 2-level quantizers with a pair of 3-level quantizers in the conventional modulator. Subsequently, the quadrature mixer is followed by 3-level quantizer with the zero-level offset, similar as described in Section 4.1.3. The middle level of the quantizer is however offset exactly by $A_1 = -A$ (or $A_1 = +A$), which forces every middle-zero level in the output of the modulator to the same value as lower quantizer level (or upper level). In result, the 3-level signal $q(t)$ transforms to a 2-level signal. The example waveforms for $M = 1$ are shown in Fig.4.12(A, B), where the output of the output quantizer is added a constant A yielding the signal $q''(t)$. Similarly as described in Section 4.1, the zero-level offset in the quantizer causes appearance of two types of the error pulses, $g_e(t)$ and $h_e(t)$

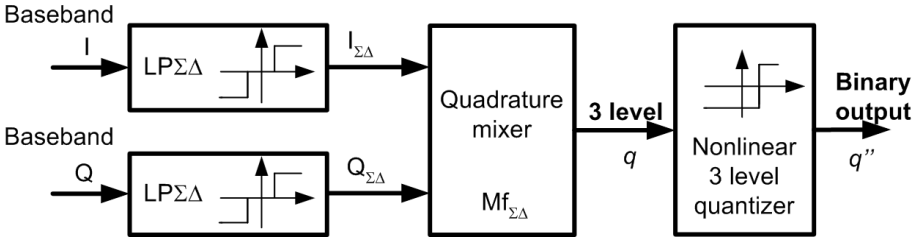

Figure 4.11: Modified 2-level signal modulator.

which are added to the output of the modulator. By meeting the condition of positive integer M in the quadrature-mixer, the distortion products in the output spectrum are suppressed at the carrier frequency $f_C = Mf_{\Sigma\Delta}$ by zeros of $G_e(f)$ and $H_e(f)$. Consequently, the resulting 2-level output of the modulator has quantization-noise power close to the quantization-noise power of the 3-level modulator, slightly degraded by the final quantization. Also, as this will be demonstrated in Section 4.3, the total power of the modified 2-level output is lower than that of conventional, 2-level modulator being described by (4.9), which proves better coding efficiency of the former.

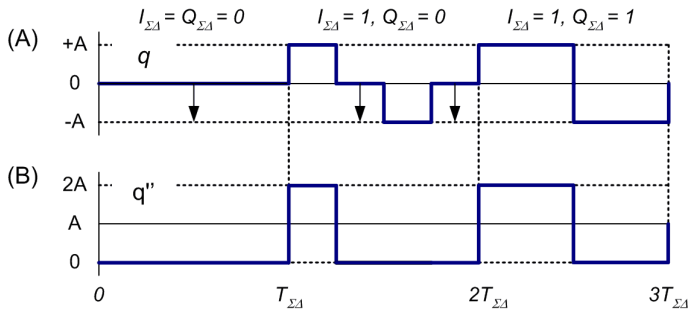

Figure 4.12: Error signal introduced by non-linear quantizer for $M = 1$, $f_C = f_{\Sigma\Delta}$. (A) 3-level quantizer output $q(t)$. (B) 2-level output $q''(t)$ for $A_1 = -A$ with a DC offset A.

4.2.3 Simulated output for $M = 1, A_1 = -1$

To validate the error shaping technique in the modified 2-level modulator, a simulation for the zero-level offset $A_1 = -A = -1$ and a bandlimited input signals I and Q, $\left(BW_{I,Q} = f_{\Sigma\Delta}/160\right)$ is carried out. The $\Sigma\Delta$ modulators used in the simulation are of first order, i.e. $NTF(z) = 1 - z^{-1}$, and $M = 1$ in the quadrature mixer.

Simulated output spectra of both, conventional and modified 2-level modulators are shown in Fig.4.13. The reduction of the quantization-noise in adjacent channels can be seen in the output of the modified 2-level against the output of the conventional 2-level modulator. Also, the 2-level waveforms exhibit less of the total signal power in the output of the modified modulator, showing an improvement in the coding efficiency.

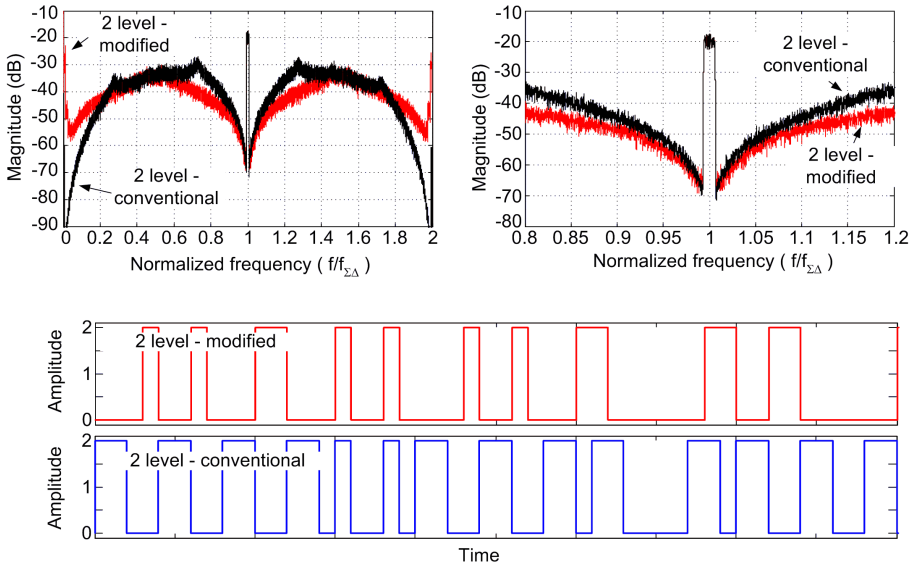

Figure 4.13: Simulated output spectra and output waveforms of conventional and modified modulators, $M = 1$, $OSR = 80$, $NTF = 1 - z^{-1}$.

4.2.4 Conclusion

This section demonstrated a new approach to the 2-level modulation of a band pass signal. As it was demonstrated, the 2-level signal can be obtained by offsetting every zero-level in a 3-level output from a quantizer. By ensuring that $f_C = Mf_{\Sigma\Delta}$, the effect of distortion caused by the second quantization can be minimized. The modified modulator is characterized by less quantization-noise and lower power of the output waveform when compared with equivalent, conventional 2-level modulator.

4.3 Analysis of the modified 2-level modulator

This section analyzes the modified, 2-level modulator, modeling the quantization of 3-level signal as the addition of two error signals; one directly related to an input signal, and one being considered as a quantization-noise. The obtained model provides an insight into the coding efficiency and noise performance of the new modulator, being a function of the input signal, the order of $LP\Sigma\Delta$ modulator and the upconversion factor M.

4.3.1 Coding efficiency of the modulator

In the general case, when a $LP\Sigma\Delta$ modulator is supplied with a constant input whose amplitude is bounded by the stable range of the modulator, the subsequent modulator's output has an average value calculated over a large number of samples close to that of the DC input.

Let us assume that a 3-level $LP\Sigma\Delta$ modulator responds to any positive, constant input IN, $0 < IN \leqslant +A$, with a 2-level output $+A; 0$. Similarly the modulator's response to a negative input, $-A \leqslant IN < 0$ is 2-level output having values $-A; 0$. The probability that the output of such $LP\Sigma\Delta$ modulator is either $+A$ or $-A$ is closely approximated by,

$$p_{\pm A} \approx |IN_{DC}| / A \tag{4.10}$$

where A denotes maximum quantizer level and is always positive. Consequently, when the same 3-level $LP\Sigma\Delta$ modulator is supplied with a not-constant, zero-mean input IN, $(-A \leqslant IN \leqslant A)$, the probability of the modulator's output taking a positive value of $+A$ is related to its input by,

$$p_A \approx 0.5\overline{|IN|}/A \tag{4.11}$$

When both inputs to the proposed modulator of Fig.4.11 are of the same mean-absolute values, $\overline{|I|} = \overline{|Q|} = \overline{|IN|}$, and have zero mean values, $\overline{I} = \overline{Q} = 0$, then the probability of the mixer's output being $+A$ is also expressed by equation (4.11). After the quantization of the 3-level waveform $q(t)$ and addition of the DC offset as it is depicted in Fig.4.12, the power of the resulting signal $q''(t)$ can be estimated from,

$$q^2_{MOD} = p_A (2A)^2 \approx 2A\overline{|IN|} \tag{4.12}$$

Subsequently the coding efficiency of the modified 2-level modulator is found by substituting (4.12) in (2.27),

$$\eta_{MOD} \approx \frac{x_{rms}^2}{2A\left(\overline{|IN|}\right)} \tag{4.13}$$

Since bandlimited signals used in digital communications are characterized by $\overline{|IN|} < A$ when $-A \leqslant IN \leqslant A$, then by comparison of (4.12) and (4.9), we can say that the modified 2-level modulator of Fig.4.11 has higher coding efficiency than the conventional, 2-level modulator of Fig.4.10, provided that both modulators are supplied with the same input.

As it has been demonstrated in Section 2.3.7.1, the discrete time coding efficiency of a 2-level ΣΔ modulator can be expressed as a function of the *PAPR* of an input signal to the modulator. Although the coding efficiency has been derived for the modified modulator as a function of an absolute-mean value, the use of *PAPR* can be more convenient for when the modulator encodes an RF signal. Subsequently, Fig.4.14 compares simulated coding efficiency of a 3-level, modified 2-level and conventional 2-level modulators as a function of *PAPR* of an input, bandlimited signal.

It is observed that the coding efficiency of the conventional 2-level modulator decreases towards zero as the *PAPR* increases. This is because the RF signal power x_{rms}^2 in equation (2.27) is inversely proportional to its *PAPR* when the amplitude is bounded by the stable range of the ΣΔ modulator. On the other hand, the output power of the conventional 2-level modulator, q_{2L}^2 remains constant according to (4.9). In contrast, the power of the modified modulator's output, q_{MOD}^2 decreases as the *PAPR* increases.

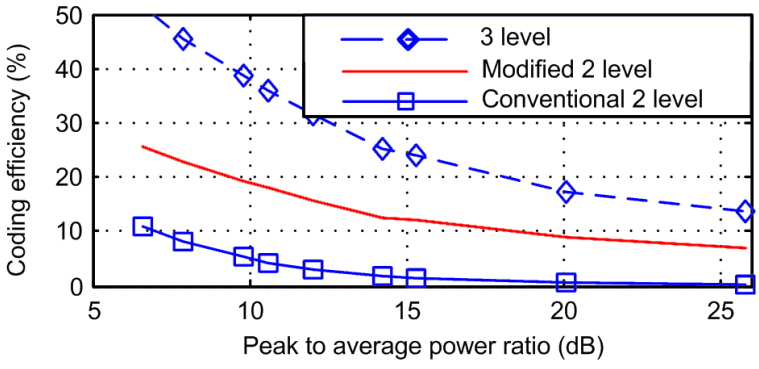

Figure 4.14: Simulated discrete time coding efficiency, $OSR = 80$, $M = 1$, $NTF = 1 - z^{-1}$.

Subsequently, the modified 2-level modulator maintains higher coding efficiency than the conventional 2-level modulator. It is also observed that the modified modulator exhibits coding efficiency which is equal to half the coding efficiency of the 3-level modulator whose quantizer levels are $A, -A, 0$. This is in agreement with the expected value, i.e. 3-level modulator yields half the output power of the modified 2-level modulator, $q_{3L}^2 = p_{\pm A}A^2 = q_{MOD}^2/2$.

It should be noted that the coding efficiency of the modified 2-level modulator does not depend on the M parameter, and there is only a small dependence on the order of the $\Sigma\Delta$ modulator used, which will be discussed in Section 4.3.7.

4.3.2 Transfer characteristic of the modulator

For the purpose of analysis it is convenient to consider the modified 2-level modulator independently for I and Q signals. Such division into two sub-systems allows for calculating the transfer-characteristics of the modulator and estimating the magnitude of an error added in its output.

Accordingly, let us assume that only one of the two input signals is supplied to the modulator of Fig.4.6, and the other one is zero. Also, without affecting the output of the modulator, the quantizer with zero-level offset can be placed ahead of the mixer as it is depicted in Fig.4.15. The quantizer in the rearranged modulator scheme adds a DC offset A_1 to its output OUT every time the 3-level input $IN_{\Sigma\Delta}$ is zero. For a DC excitation, the average output of the quantizer becomes,

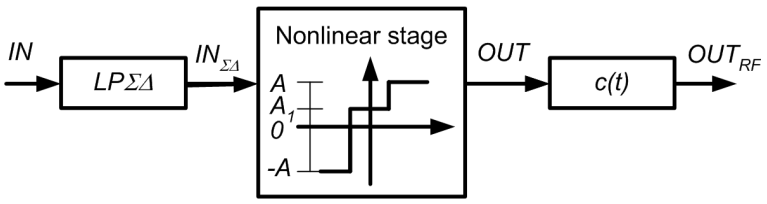

Figure 4.15: Rearranged modulator used for calculating the input-output transfer characteristic.

$$OUT_{DC} = IN_{DC} + p_0 A_1 \tag{4.14}$$

where p_0 denotes the probability of zero in the output of the $LP\Sigma\Delta$ modulator. As explained in the previous section, the probability of a 3-level, $LP\Sigma\Delta$ modulator's output taking the value of $+A$ depends on the mean-absolute value of the input by (4.10), which also defines p_0,

$$p_0 = 1 - p_{\pm A} \approx 1 - |IN_{DC}|/A \tag{4.15}$$

Substitution of (4.15) in (4.14) yields an expression for the output of the quantizer,

$$OUT_{DC} \approx IN_{DC} - |IN_{DC}| A_1/A + A_1 \tag{4.16}$$

Equation (4.16) is next used to draw the input-output transfer characteristics for the $LP\Sigma\Delta$ modulator followed by the quantizer. The characteristics are drawn for $A = 1$ in Fig.4.16.

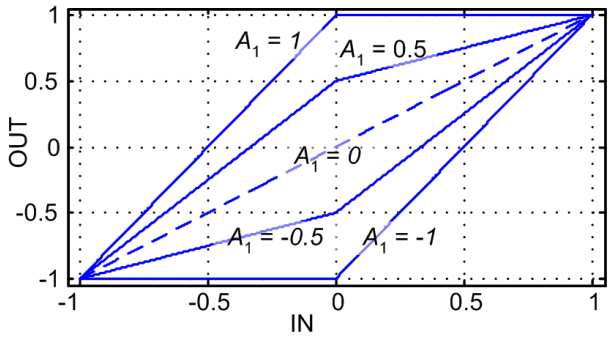

Figure 4.16: Transfer characteristics for $A = 1$.

Although the above characteristics are calculated for DC signals, they also hold true for AC signals whose maximum frequency is much lower than the sampling rate of a modulator, showing an average error added in the output of the quantizer.

4.3.3 Linear model

The output of the quantizer in Fig.4.15 has been described as the linear addition of an input-dependent error by equation (4.16). This error signal can be denoted as E_{IN} and

expressed by,

$$E_{IN} = A_1 - |IN_{DC}|A_1/A \tag{4.17}$$

E_{IN} is the average value of the 2-level error signal added in the quantizer as a result of offsetting the zero-input signal by A_1. Consequently, apart from E_{IN}, the quantizer's output consists of a quantization error, E_Q. The power of this quantization-error is proportional to the probability of zero output of a $LP\Sigma\Delta$ in the modulator of Fig.4.15. It follows from equation (4.15), that the quantization-error power is largest when the zero-mean input signal IN has its lowest amplitude. The two error signals, E_{IN} and E_Q are subsequently suppressed at the carrier frequency f_C by function $H_e(f)$ as a result of mixing with the carrier.

$$OUT_{RF}(f) = IN_{\Sigma\Delta}(f) + (E_{IN} + E_Q) H_e(f) \tag{4.18}$$

The total power of the error signal added by E_{IN} and E_Q can be expressed by,

$$E^2 = p_0 A_1^2 = (1 - |IN_{DC}|/A) A_1^2 \tag{4.19}$$

Instantaneous power of both error signals E_{IN} and E_Q in the output of the quantizer can be found as a function of the input to the 3-level $LP\Sigma\Delta$ modulator. Let us express the power of E_{IN} in the output of the modulator a a function of a DC input, which is obtained by raising both sides of equation (4.17) to power of two,

$$E_{IN}^2 = (A_1 - |IN_{DC}|(A_1/A))^2 \tag{4.20}$$

The quantization error E_Q is created as a difference between the total error E, and the average error E_{IN} over some period of time $T \gg T_{\Sigma\Delta}$. The creation of both errors in the rearranged modulator of Fig.4.15 is depicted in Fig.4.17(A, B). The quantization error E_Q has the amplitude equal to A_1 for the time $p_0 T$, and amplitude equal to the difference $A_1 - E_{IN}$ during the remaining time, i.e. $T_2 = (1 - p0) T$. Consequently the error power

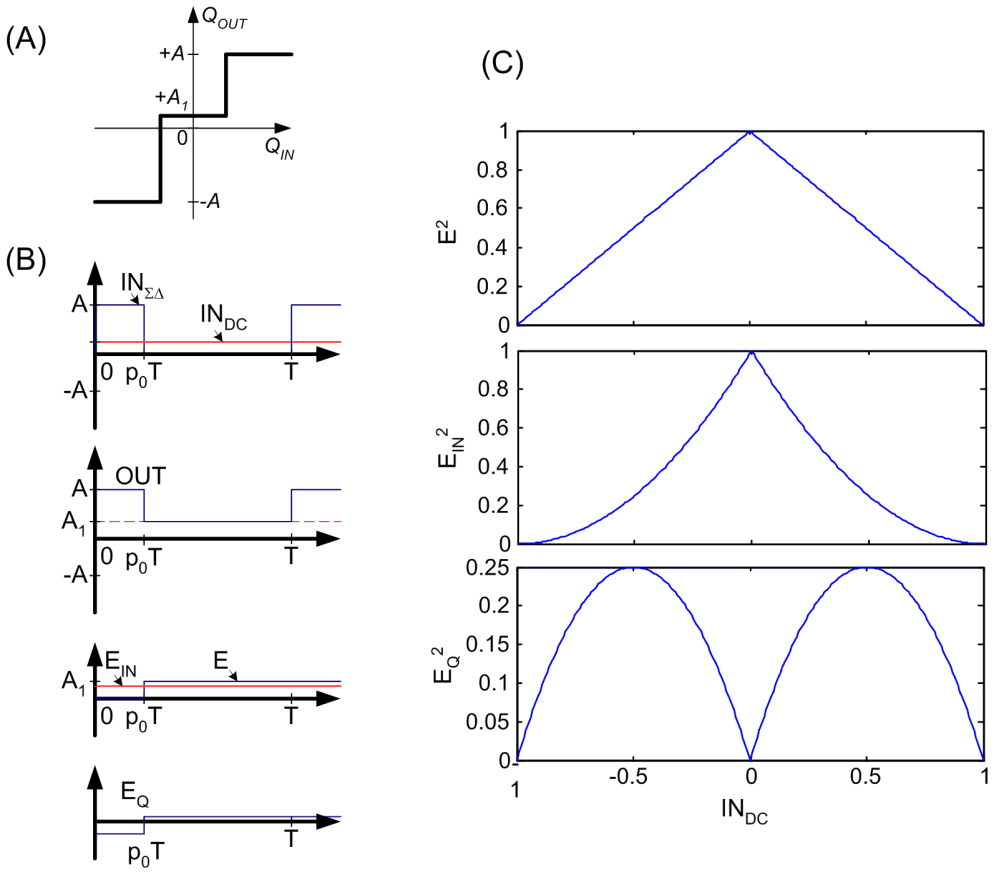

Figure 4.17: Error E_{IN} and E_Q added in the quantizer with zero-level offset. (A) Transfer function of the quantizer. (B) Waveforms in the rearranged modulator. (C) Power of the error added in the quantizer versus *DC* input applied a 3-level *LP*ΣΔ modulator.

E_Q^2 during the time T can be calculated as,

$$E_Q^2 = p_0 (A_1 - E_{IN})^2 + (1 - p_0) E_{IN}^2 \tag{4.21}$$

using equations (4.15), (4.17) in (4.21) we arrive at the expression for E_Q^2,

$$E_Q^2 = \left(A_1^2/A\right) \left(|IN_{DC}| - |IN_{DC}|^2 / A \right) \tag{4.22}$$

Equations (4.19), (4.20), (4.22) are next used to calculate error power added in the quantizer, shown in Fig.4.17(C) as a function of the *DC* input amplitude for $A = -A_1 = 1$. It is observed that the total error power E^2 is a linear function of the average input supplied to the 3-level *LP*ΣΔ modulator, and it has maximum value when the input amplitude is zero. The quantization error power E_Q^2 is a quadratic function with maxima corresponding to the input amplitude equal to half the quantizer full scale. The power of the error E_{IN}

increases as the *DC* input decreases. This error becomes dominant when a 3-level *LP*ΣΔ modulator is supplied with an input characterized by large *PAPR*. The linear model of the modified 2-level modulator based on the above analysis is shown in Fig.4.18.

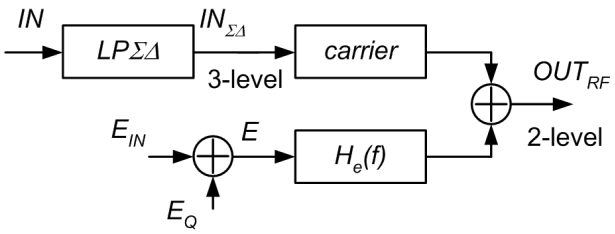

Figure 4.18: Linear model of the modulator.

4.3.4 Harmonic distortion

The linear model derived in the previous sections can be used for estimating noise performance in the output of the 2-level modulator as a function of an input signal's amplitude. A single tone waveform is a useful test-signal for demonstrating the effect of the nonlinear distortion and the addition of the quantization-error E_Q in the modulator's output.

Let the modified, 2-level modulator be obtained by offsetting nonlinear-quantizer zero-level by $A_1 = -A$, and $A = 1$. The obtained characteristic is shown in Fig.4.19, and is valid when the oversampling ratio of a *LP*ΣΔ modulator is large. The single tone signal is supplied to the one of the inputs of the modulator of Fig.4.11, while the other input is supplied with zero signal and has no effect on the modulator's output.

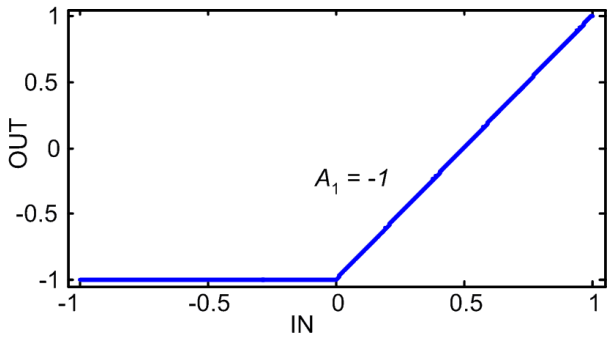

Figure 4.19: Transfer characteristic for $A_1 = -A = -1$.

The input signal is expressed by,

$$IN = Amp \cdot sin(\omega_0 t) \tag{4.23}$$

where amplitude Amp is bounded by the full scale of a quantizer, $Amp \leqslant 1$, $f_0 = \frac{\omega_0}{2\pi}$ and $f_0 \ll f_{\Sigma\Delta}$. When the sine-wave is passed through a nonlinear system described by the transfer characteristic of Fig.4.19, the output becomes a half-wave rectified sine as it is depicted in Fig.4.20. Note that the output waveform is obtained by adding a DC offset 1.

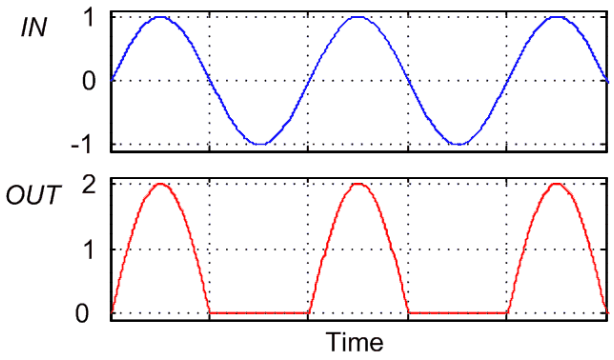

Figure 4.20: Input-output waveforms.

The output signal is described by Fourier series and consists of a DC component, first and even harmonics,

$$OUT = \frac{2 \cdot Amp}{\pi} + Amp \cdot sin(\omega_0 t) - Amp \frac{4}{\pi} \sum_{n=2,4,6...}^{\infty} \frac{cos(n\omega_0 t)}{n^2 - 1} \tag{4.24}$$

Although in theory a large number of harmonics could be considered in the output of the modified 2-level modulator, due to the tonal behavior of a $LP\Sigma\Delta$ modulator supplied with a single tone input and the rise of quantization noise at higher frequencies, the analysis of the output will be narrowed to the first and second harmonic only. The second harmonic component in the output of the modulator before and after the mixing with a carrier are,

$$\begin{aligned} H_2 &= \tfrac{4Amp}{3\pi} \\ H_{2C} &= \tfrac{4Amp}{3\pi} |H_e(f_C + 2f_0)| \end{aligned} \tag{4.25}$$

where H_2 is the amplitude of second harmonic in the output OUT, and H_{2C} is the amplitude of second harmonic after mixing with the carrier, i.e. in the output QUT_{RF} as shown in the modulator scheme in Fig.4.15. $H_e(f)$ is defined by (4.2). To reduce the tonal behavior of the modulator, a dither signal is added in the input to the $3-level$ quantizer.

4.3.4.1 First and third order modulator

It follows from the discussion carried out in Sections 4.3.1-4.3.3 that the two error signals E_{IN} and E_Q added in the quantizer with the zero-level offset are independent of the noise-transfer-function [1] of the $LP\Sigma\Delta$ modulator, but are functions of the input signal IN and $H_e(f)$. It means that the SNR improvement expected from an increase in the order of a $LP\Sigma\Delta$ may not occur due to the presence of the error added by the quantizer. This property is confirmed in the course of simulations of first and third order $LP\Sigma\Delta$ modulators.

Let the single-tone input signal have the amplitude $Amp = 0.8A$ and frequency $f_1 = 0.005 f_{\Sigma\Delta}$. The carrier frequency is $f_C = f_{\Sigma\Delta}$ when $M = 1$. After passing the signal through the quantizer with zero-level offset, the amplitude of the second harmonic is calculated from equation (4.25), $H_2 = 0.34$ $(-9.37\,dB)$, which appears at frequency $2f_1 = 0.01 f_{\Sigma\Delta}$. The effect of the addition of the quantization-error E_Q and the second harmonic to the ideal 3-level output is observed in Fig.4.21(A). After mixing with carrier, the quantization-error and the second harmonic are suppressed by $H_e(f)$. The magnitude of second harmonic at frequency $f_2 = 1.01 f_{\Sigma\Delta}$ is calculated from (4.25) as $H_{2C} = 0.0024$ $(-52.4\,dB)$ and it shows good fidelity with the simulation presented in Fig.4.21(B). It can be also observed that the modified 2-level and ideal 3-level modulators exhibit similar noise performance when a first order $LP\Sigma\Delta$ modulator is used.

Let the same, single-tone input signal be supplied to the modified modulator with a

[1] In fact a small dependence exists and it is explained later in Section 4.3.7 and Section 4.4. It however does not have any significant effect on the results presented here.

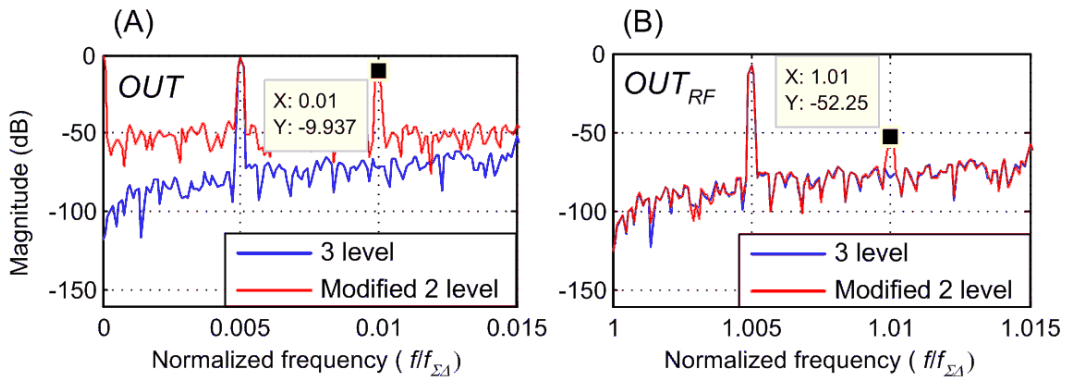

Figure 4.21: Harmonic distortion - first order ΣΔ modulator, $f_0 = 0.005 f_{\Sigma\Delta}$, $Amp = 0.8$, $M = 1$. (A) OUT. (B) OUT_{RF}.

third order $LP\Sigma\Delta$. The magnitude of quantization-error E_Q and the second harmonic are expected to be the same as in the output from the modulator employing a first order $LP\Sigma\Delta$, as shown in the simulated output spectrum in Fig.4.22(A). In contrast with the first order $LP\Sigma\Delta$ modulator however, the modified modulator employing third order $LP\Sigma\Delta$ modulator performs visibly worse than an ideal, 3-level modulator of third order. This is because the error signals E_{IN} and E_Q cannot be suppressed by the function $H_e(f)$ below the magnitude of the quantization-noise of the third-order $LP\Sigma\Delta$ modulator. Consequently, the 2-level output shows a higher magnitude of error signal in the proximity of the carrier frequency than the equivalent, 3-level modulator as observed in Fig.4.22(B). In general, due to the fixed magnitude response $|H_e(f)|$, the SNR degradation of the modified 2-level modulator to the 3-level modulator will become larger as higher order NTF are used.

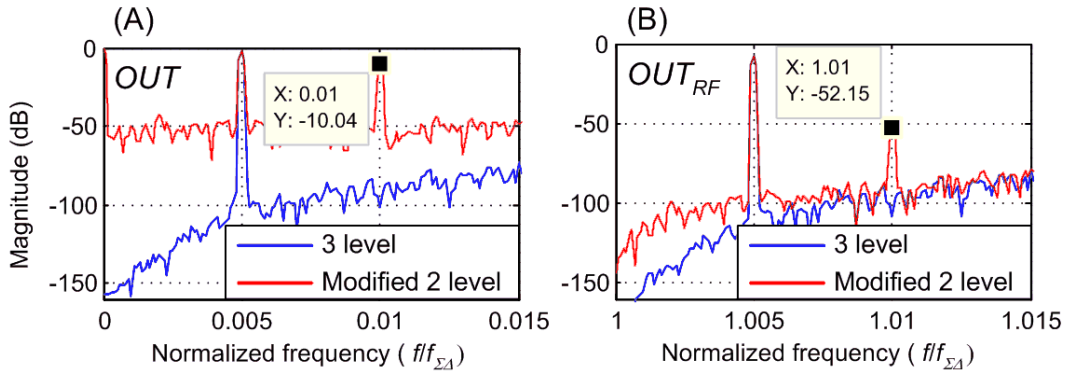

Figure 4.22: Harmonic distortion - third order ΣΔ modulator, $f_0 = 0.005 f_{\Sigma\Delta}$, $Amp = 0.8$, $M = 1$. (A) OUT. (B) OUT_{RF}.

4.3.4.2 E_{IN} and E_Q suppression vs. M parameter

The modified modulator has been analyzed and modeled in previous sections, and supporting simulations have been provided for carrier frequency $f_C = f_{\Sigma\Delta}$ and $M = 1$. The next to explain is the influence of the parameter M on the noise-shaping function $H_e(f)$. The parameter M must take a positive integer value, as it is needed for maximum suppression of the error induced in the quantizer which was explained in Section 4.1.3. The increase of M has two effects: it causes a proportional increase of the carrier frequency by equation (4.4) and, it changes the magnitude response of the function $H_e(f)$, improving the capability for error suppression in the output of the modified 2-level modulator. The magnitude responses $|H_e(f)|$ are depicted in Fig.4.23 for $M = 1$, 2 and 4.

As explained earlier, the magnitude responses $|H_e(f)|$ have maxima at frequency $f = 0$ and in the proximity of $f = 2f_C$, and one zero at carrier frequency f_C. Also, every doubling of M reduces $|H_e(f)|$ in proximity of the frequency f_C by half when the band of interest is much lower than the sampling frequency $f_{\Sigma\Delta}$. Consequently, the suppression of the error induced by the quantizer increases by $6\,dB$ for every doubling of M, which

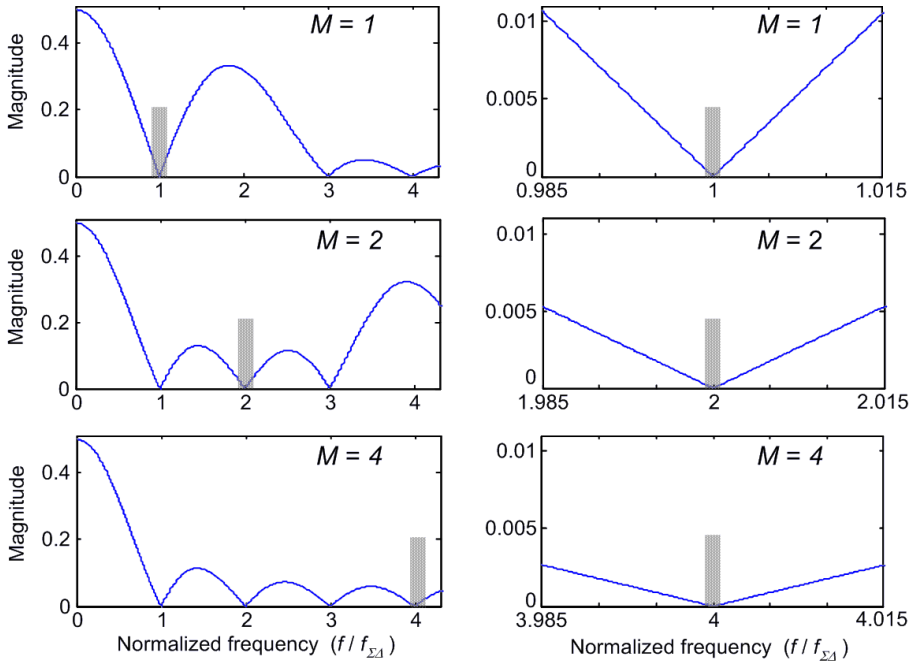

Figure 4.23: $H_e(f)$ for $M = 1$, $M = 2$, $M = 4$.

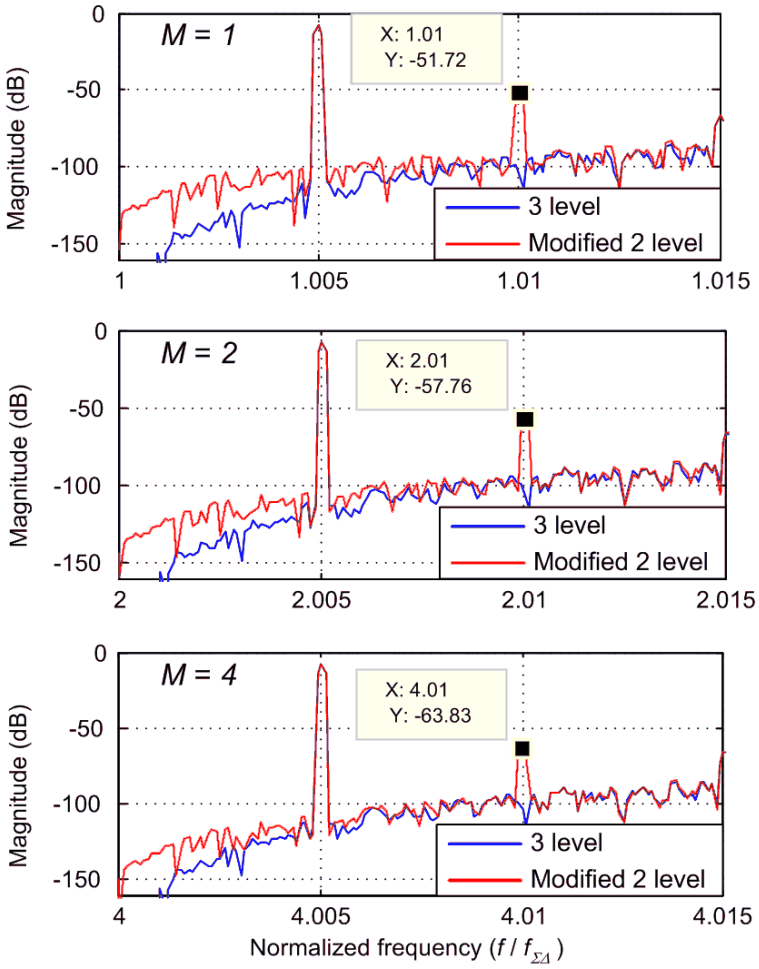

Figure 4.24: Simulated output spectrum OUT_{RF} for third order $LP\Sigma\Delta$ modulator and the single tone input with $f_0 = 0.005 f_{\Sigma\Delta}$ and $Amp = 0.8$.

improves the noise performance of the modified 2-level modulator. The effects of a change of M on the magnitude of distortion induced by the quantizer are verified in the simulation of the modified 2-level modulator employing third order $LP\Sigma\Delta$, and are observed in Fig.4.24.

4.3.5 SNR in the modified 2-level modulator's output

The signals used in wireless communication are different from a single tone test used in simulations described in the previous sections. They differ in $PAPR$ and in distribution functions which in turn has the effect on the error induced in the modified 2-level modulator. In order to observe the effects of the quantization with the zero-level offset on the quality of a bandlimited signal, a $4QAM$ stimulation was generated in Matlab. The 4QAM

input signal used was characterized by $PAPR = 5.77dB$ and a bandwidth $BW = 0.0125 f_{\Sigma\Delta}$ $\left(OSR = \frac{2f_{\Sigma\Delta}}{2BW} = 80\right)$. The $LP\Sigma\Delta$ modulators used were of first order. The *SNR* was calculated as a difference to the *SNR* of a 3-level $\Sigma\Delta$ modulator, i.e. $0dB$ indicates that a 2-level modulator provided the same *SNR* as the 3-level modulator, while $-1dB$ means $1dB$ of *SNR* degradation compared with the 3-level modulator. The calculated *SNRs* are shown in Fig.4.25. The $OSR = 80$ in the figure indicates that the *SNR* calculation was carried out only inside the signal band, while lower values of *OSR* also included the out of band noise power. It is observed that when $M = 1$, the modified 2-level modulator exhibits *SNR* that is nearly as good as the *SNR* of the 3-level modulator at low *OSR* values. The *SNR* degrades with an increase of *OSR*. The modified 2-level modulator no longer exhibits better noise performance than the conventional 2-level modulator when *OSR* increases above 35. Indeed, the modified 2-level modulator generally shows better noise performance than the conventional 2-level modulator over a wide frequency-band centered at a carrier frequency, but it exhibits more in-band error.

The *SNR* improvement in the output of the modified modulator is observed when increasing the up-converting parameter to $M = 2$ and $M = 4$. The $6dB$ reduction of the errors E_{IN} and E_Q is obtained per every doubling of M which was explained in Section 4.3.4.2. Consequently, the *SNR* performance for $M = 4$ is better than the *SNR* of the conventional 2-level modulator over the entire displayed range of *OSR*.

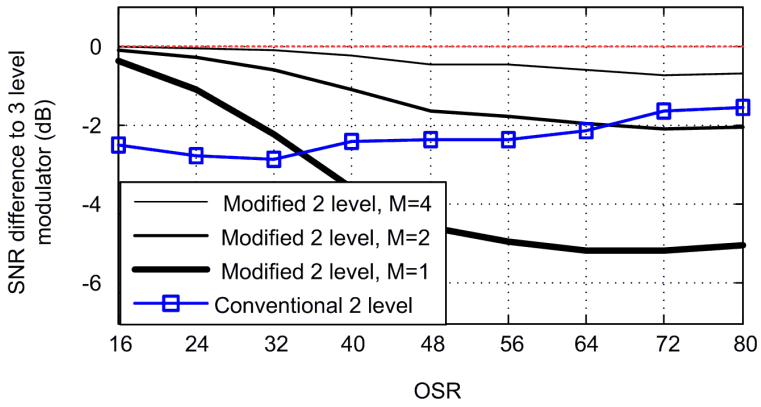

Figure 4.25: Simulated *SNR*.

4.3.6 Spectrum utilization vs. M parameter

The positive outcome from increasing M is better suppression of the error induced by the quantizer with zero-level offset as it has been observed in Section 4.3.4.2 and Section 4.3.5. The increase of M however causes a proportional increase of the carrier frequency according to equation (4.4). If, on the other hand the carrier frequency should remain unchanged while increasing M, then the sampling frequency $f_{\Sigma\Delta}$ must be decreased,

$$f_{\Sigma\Delta} = \frac{f_C}{M} \tag{4.26}$$

Although the suppression of the error induced by the quantizer with the zero-level offset improves as M increases, the overall SNR in the output of the modified 2-level modulator worsens as a consequence of the decreased frequency $f_{\Sigma\Delta}$. This SNR degradation can

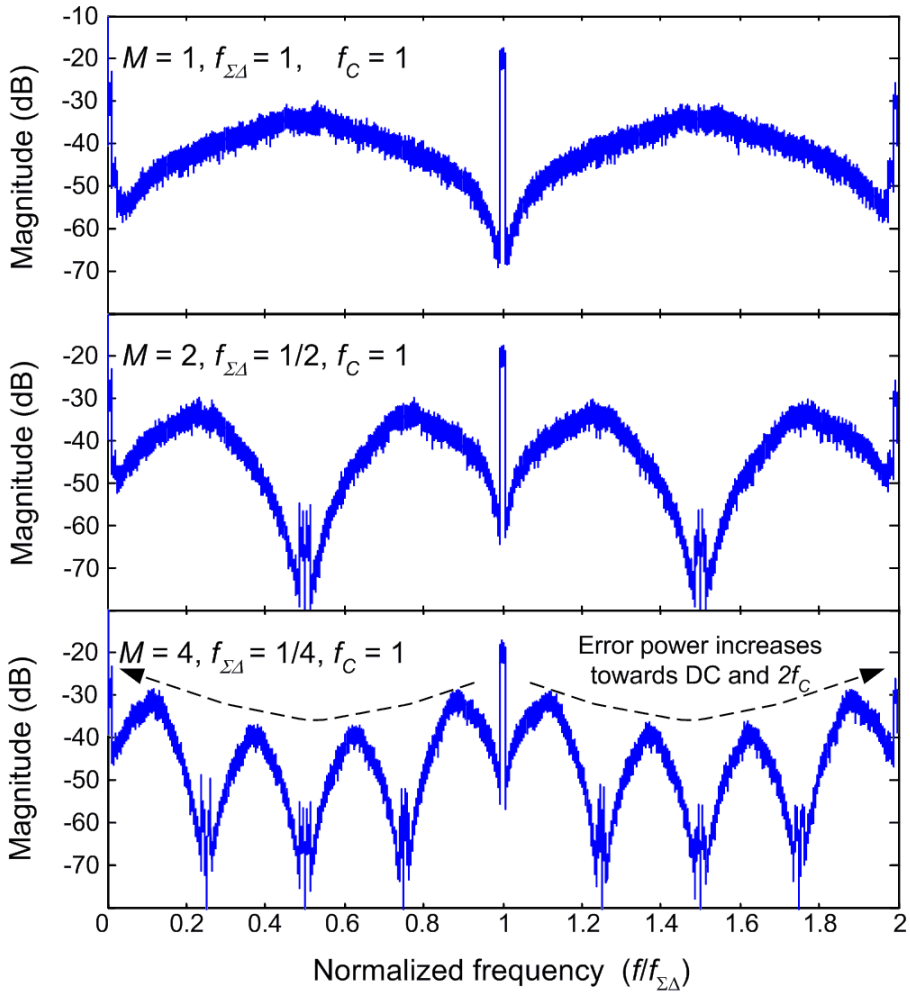

Figure 4.26: Output spectra from the modified 2-level modulator.

be demonstrated in the example of first order $LP\Sigma\Delta$: the increase of M by factor of two improves suppression of the error added in the quantizer with zero-level offset by $6\,dB$, but the reduction of sampling frequency from $f_{\Sigma\Delta}$ to $\frac{f_{\Sigma\Delta}}{2}$ results in simultaneous increase in the quantization-noise by $9\,dB$. Consequently the overall effect is worse *SNR*. Simulated output spectra for different values of M, constant f_C and a 4QAM input signal are shown in Fig.4.26, and the calculated values of *SNR* are listed in Tab.4.1. While having fixed carrier frequency f_C, the proposed modulator yields the highest *SNR* when $M = 1$ as expected.

Table 4.1: Simulated SNR for different values of M and constant carrier frequency.

f_C	M	$f_{\Sigma\Delta}$	**OSR**	**SNR**
1	1	1	80	55.3
1	2	1/2	40	50.5
1	4	1/4	20	42.5

4.3.7 The use of higher order $\Sigma\Delta$ modulator

The relationships derived in the previous sections describe accurately the modified 2-level modulator when the $LP\Sigma\Delta$ employed are of first order. This section discusses the effect of increasing the order of the $LP\Sigma\Delta$ modulator on the coding efficiency, input-output characteristic and noise performance of the proposed 2-level modulator.

4.3.7.1 Input-output transfer characteristic

When a first order, 3-level $LP\Sigma\Delta$ modulator is excited with a DC input signal, the probability of zero-output follows closely equation (4.15). However, as the order of 3-level $LP\Sigma\Delta$ modulator is increased, the modulator is more likely to produce a 3-level, instead of a 2-level output in response to a positive or negative input.

As the probability of zero-output decreases, the piecewise input-output transfer characteristic described by equation (4.14) rounds at low amplitudes of an input. This effect

is seen in the simulated input-output characteristic with a fourth order $LP\Sigma\Delta$ used in the modified 2-level modulator shown in Fig.4.27.

The lower probability p_0 changes the error signal induced in the quantizer, split into E_{IN} and E_Q, and should be taken into account in the modulator model of Fig.4.18. The changed characteristic will limit the effectiveness of a predistortion function derived for the modulator, which will be discussed in Section 4.4. The effect on coding efficiency of the modulator is discussed in the next section.

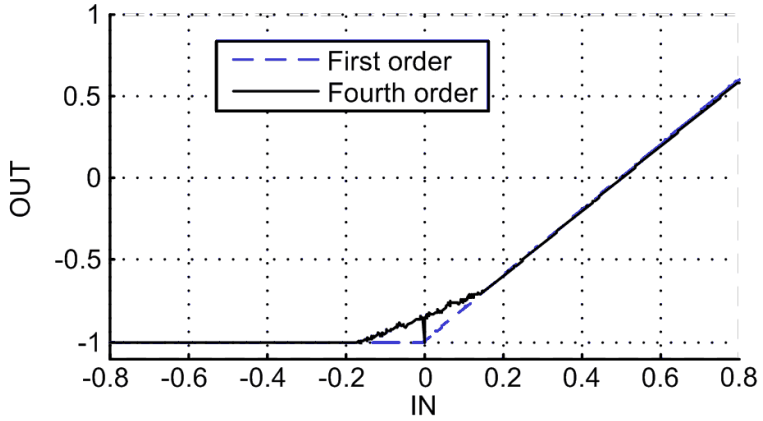

Figure 4.27: Simulated input-output characteristic of first and fourth order $\Sigma\Delta$ modulators in the modified modulator.

4.3.7.2 Coding efficiency

The lower probability of zero-output has an effect on the coding efficiency of the modified 2-level modulator. When p_0 decreases, the coding efficiency also decreases according to equation (4.27),

$$\eta_{MOD} \approx \frac{x_{rms}^2}{p_A\,(2A)^2} = \frac{x_{rms}^2}{(1-p_0)\,(2A)^2} \tag{4.27}$$

The coding efficiency of the modified 2-level modulator was calculated with $LP\Sigma\Delta$ modulators of order first and fourth. The modulator employing fourth order $LP\Sigma\Delta$ had an average of 1.4 % lower coding efficiency for a 4QAM input signal than the same modulator employing first order $LP\Sigma\Delta$. The experiments were carried out for the maximum input signal's amplitude changed from 0.1 to 0.9 of a full scale of the $LP\Sigma\Delta$ quantizer.

4.3.7.3 Signal to noise ratio and adjacent channel power ratio

An improvement of SNR in the output of a ΣΔ modulator is expected when the modulator's order increases. However, due to the E_{IN} and E_Q errors addition in the quantizer, this rule does not apply in the modified 2-level modulator's output. The error induced by the quantizer remains at the same level nearly regardless of the order of ΣΔ modulators, i.e. the functions G_e and H_e do not depend on a NTF. The impact of E_{IN} and E_Q is observed in Fig.4.28 for third order $LP\Sigma\Delta$ modulator whose NTF zeros and poles are listed in Tab.2.3.

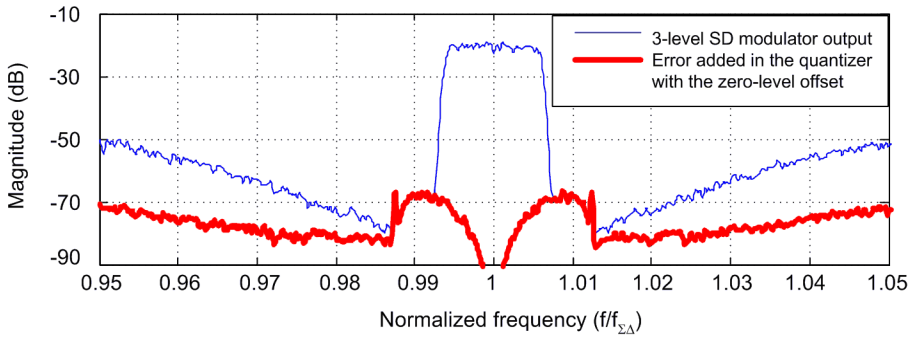

Figure 4.28: Error power increase in the output of the modified modulator with 3rd order $LP\Sigma\Delta$ modulator.

The thin line represents output of the modified modulator and the thick line represents the error induced by the quantizer. Clearly, the error induced by the quantizer becomes dominant in proximity of carrier frequency when a high order $LP\Sigma\Delta$ is employed. The distortion becomes the more apparent the higher order ΣΔ modulators are used.

4.3.8 Conclusion

This section analyzed the effects of quantization with zero-level offset on the 2-level output of the modified modulator. The error added in the quantizer depends on the input signal supplied to a $LP\Sigma\Delta$ modulator, and there is only a small correlation between the errors E_{IN}, E_Q and the order of the $LP\Sigma\Delta$ modulator. The quantization with zero-level offset can be modeled as an addition of two independent error sources suppressed at a

carrier frequency by function $H_e(f)$. It follows the analysis that part of the error added in the quantizer, i.e. E_{IN}, can be described by a function of an input-signal supplied to a $LP\Sigma\Delta$ modulator, which allows for the use of a predistortion.

4.4 Linearization of modulator's output

This section describes a predistortion function derived for the modified 2-level modulator. The predistortion bases on the linear model of the modulator described in previous section. The error cancellation described in this section applies only to the E_{IN} error, and it cannot reduce the quantization error E_Q in the modulator model of Fig.4.18.

4.4.1 Input conditions

The use of a quantizer with the zero-level offset in the modified modulator scheme of Fig.4.11 introduces an error signal in the modulator's output as described in Section 4.3.2. This error is described by equation (4.17) for large OSR, and is rewritten here for $A = 1$,

$$E_{IN} = (1 - |IN|)A_1 \tag{4.28}$$

This error is next attenuated in the output of the modified 2-level modulator by function $H_e(f)$. A fraction of this error signal however falls into the signal band, increasing in-band noise power. Since the magnitude of the in-band error signal induced by the quantizer is negligible next to the magnitude of the input signal, its cancellation is possible through subtraction applied to the inputs of both $LP\Sigma\Delta$ modulators without causing their instability.

In contrast with the analysis done in previous sections of this chapter, the modulator will be considered as a discrete-time domain system, which also includes the quadrature-mixer. The following derivation is done for $M = 1$ only, but it also applies to higher

values of the carrier up-conversion factor. Both 3-level $LP\Sigma\Delta$ in the modified modulator are assumed to have the same NTF and unity STF. The predistortion function is derived for only one of the two inputs, while the other is assumed zero, but it is valid for both modulator inputs.

4.4.2 The predistortion function

Let us assume that the error cancellation signal denoted by E_P is added directly to the modulator's input I as it is shown in Fig.4.29(A). Consequently, the input to the upper $LP\Sigma\Delta$ modulator becomes $I + E_P$. This input signal is next transferred to the carrier frequency as a result of mixing with the carrier pulse $c[nT]$. The impulse response $c[nT]$ of quadrature mixer is shown in Fig.4.29(B) for $M = 1$. The pulse $h_1[nT]$ is created by offsetting $c[nT]$ by -1 at the 0th, and 1st time indexes when $I_{\Sigma\Delta} = 0$ as it was described for continuous time pulses in Sections 4.1.2, 4.1.3. Subsequently the error E_{IN} appears in the output of the modulator suppressed by $H_1\left(e^{j\omega}\right)$, being discrete-time-Fourier-transform $(DTFT)$ of $h_1[nT]$. Using the linear model of the modulator of Fig.4.18, modulator output becomes,

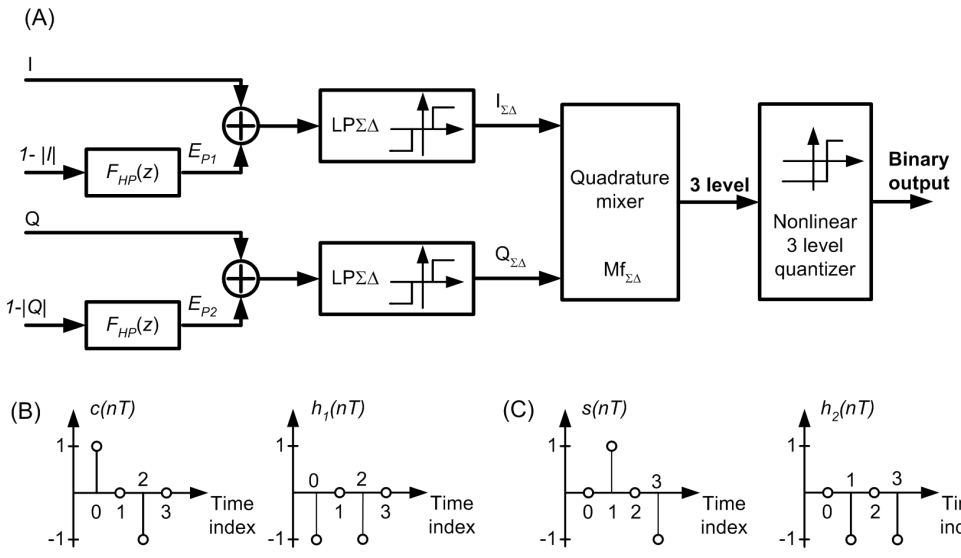

Figure 4.29: (A) Modified 2-level modulator with predistortion added. (B) Discrete time impulse responses $c[nT]$, $h_1[nT]$ for $M = 1$. (C) Discrete time impulse responses $s[nT]$, $h_2[nT]$.

$$X''_{RF}\left(e^{j\omega}\right) = \left[I\left(e^{j\omega}\right) + E_{P1}\left(e^{j\omega}\right)\right] C\left(e^{j\omega}\right) + \left[E_{IN}\left(e^{j\omega}\right) + E_Q\left(e^{j\omega}\right)\right] H_1\left(e^{j\omega}\right) \quad (4.29)$$

In order to cancel the error signal $E_{IN}\left(e^{j\omega}\right)$ in modulator's output, the following condition must be met,

$$E_{P1}\left(e^{j\omega}\right) = -\frac{E_{IN}\left(e^{j\omega}\right) H_1\left(e^{j\omega}\right)}{C\left(e^{j\omega}\right)} \quad (4.30)$$

As the error $E_{IN}\left(e^{j\omega}\right)$ induced by the quantizer is shaped in a frequency domain by function $H_1\left(e^{j\omega}\right)/C\left(e^{j\omega}\right)$, the predistorting error signal $E_P\left(e^{j\omega}\right)$ should be synthesized similarly, by pre-filtering the error signal E_{IN}. It follows that an additional transfer function $F\left(e^{j\omega}\right)$ should be used to obtain the predistorting signal E_P,

$$E_{P1}\left(e^{j\omega}\right) = E_{IN}\left(e^{j\omega}\right) F\left(e^{j\omega}\right) \quad (4.31)$$

The transfer function $F\left(e^{j\omega}\right)$ is found by substituting (4.31) in (4.30) ,

$$F\left(e^{j\omega}\right) = -\frac{H_1\left(e^{j\omega}\right)}{C\left(e^{j\omega}\right)} \quad (4.32)$$

where functions $H_1\left(e^{j\omega}\right)$ and $C\left(e^{j\omega}\right)$ can be expressed by (4.33) and (4.34) for $M = 1$.

$$H_1\left(e^{j\omega}\right) = -1 - e^{-j2\omega} \quad (4.33)$$

$$C\left(e^{j\omega}\right) = 1 - e^{-j2\omega} \quad (4.34)$$

Substituting (4.33) and (4.34) in (4.32) and transforming the result to z-domain yields the function $F(z)$,

$$F(z) = \frac{1 + z^{-2}}{1 - z^{-2}} \quad (4.35)$$

The transfer function $F(z)$ has its zeros lying at $z = \pm j$, and poles on a unit circle at $z = \pm 1$ as deduced from (4.35). Due to the occurrence of poles at $z = \pm 1$, magnitude of $F(z)$ tends to infinity when frequency approaches $f = 0$ and $f = 2f_{\Sigma\Delta}$ as shown in

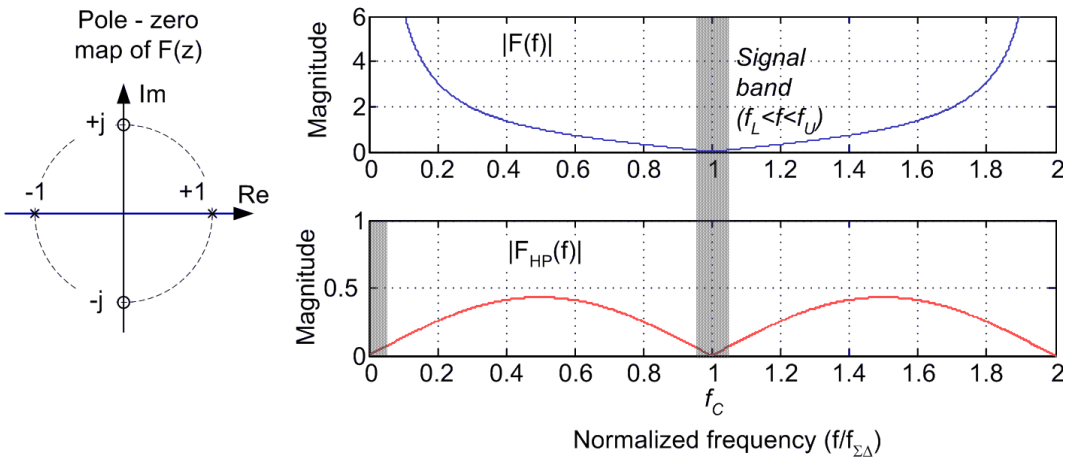

Figure 4.30: Magnitude responses of the transfer function $F(f)$ and the approximating function $F_{HP}(f)$.

Fig.4.30. In order to avoid unstable operation caused by the poles at $z = \pm 1$, the transfer function $F(z)$ should be approximated only within the narrow band of interest centered at the carrier frequency $f_C = 1$ by an other, stable transfer function. Let us denote the approximating transfer function by $F_{HP}\left(e^{j\omega}\right)$,

$$F_{HP}\left(e^{j\omega}\right) = F\left(e^{j\omega}\right) = -\frac{H\left(e^{j\omega}\right)}{C\left(e^{j\omega}\right)} \quad \text{when} \quad \omega_L < \omega < \omega_U$$

where ω_L and ω_U define frequency band over which the error E_{IN} should be canceled. The filter block $F_{HP}(z)$, must be placed before the $LP\Sigma\Delta$ modulators in the modified modulator's scheme as it is shown in Fig.4.29(A). This filter is therefore sampled at the same rate as the $LP\Sigma\Delta$ modulator and its frequency response is periodic over a frequency interval of $f_{\Sigma\Delta}$. It follows that the magnitude response of $F_{HP}(z)$ is the same in proximity of the carrier frequency $f_C = f_{\Sigma\Delta}$ and zero frequency. In order to obtain a single zero at frequency $f = f_{\Sigma\Delta}$, the transfer function $F_{HP}(z)$ must have a zero at $z = 1$. The simplest approximation is the first order high-pass transfer function written below,

$$F_{HP}(z) = g\left(1 - z^{-1}\right) \tag{4.36}$$

where g scales the magnitude response of the filter. $|F_{HP}(f)|$ is shown in the Fig.4.30(B) for $g = 0.2155$.

Separate from magnitude response, the group delay of the high-pass filter $F_{HP}(z)$ should be the same as the group delay of $F(z)$. The group delay of $F(z)$ is $\tau_F = 0.25T_{\Sigma\Delta}$, which differs from the group delay calculated for the high-pass filter $F_{HP}(z)$, $\tau_{HP} = 0.5T_{\Sigma\Delta}$. If, however, a large oversampling ratio is applied in the modulator, then the difference between τ_F and τ_{HP}, being a fraction of sampling period $T_{\Sigma\Delta}$ becomes negligible. Although a second or higher order high pass filter could be used for approximating the transfer function $F(z)$, their use is impractical as it requires more hardware and induces higher group delay, contributing to less effective cancellation of the error E_{IN}. As stated earlier in this section, the same predistortion function is applicable in both I and Q branches of the modified modulator.

4.4.3 Harmonic distortion, $M = 1$

The simulation of the modified 2-level modulator is performed under the same conditions as in Section 4.3.4, i.e one modulator is supplied with a single tone input of amplitude $Amp = 0.8$ and frequency $f_0 = 0.005 f_{\Sigma\Delta}$, and both $LP\Sigma\Delta$ modulators are of third order. The gain used in the high pass filter $F_{HP}(z)$ is $g = 0.2155$. The output spectra are simulated without and with predistortion and are shown in Fig.4.31(A, B). As observed, the second harmonic is reduced by $19.5\,dB$ after applying the predistortion function.

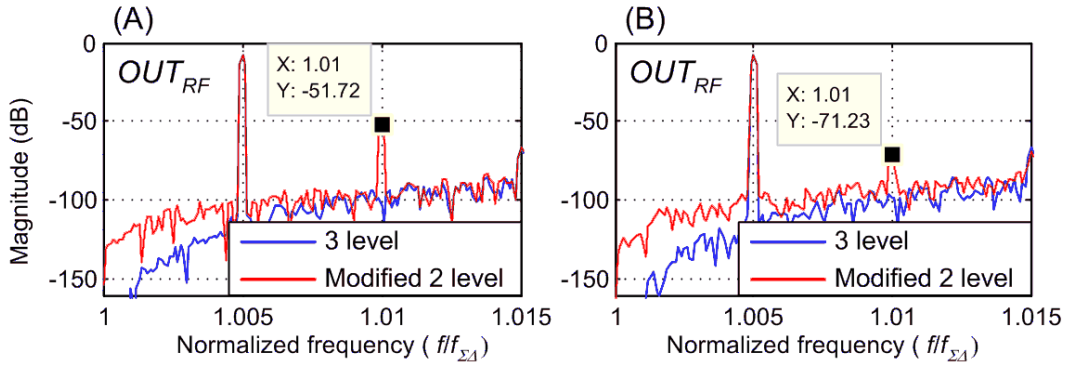

Figure 4.31: Output spectra for the modified 2-level modulator with third order $LP\Sigma\Delta$, $M = 1$ and a single tone input, $Amp = 0.8$, $f_0 = 0.005 f_{\Sigma\Delta}$. (A) No predistortion. (B) The modulator uses predistortion.

It is also observed, that the predistortion function does not affect the quantization error E_Q added by the quantizer. The quantization error maintains nearly the same magnitude in both outputs, which is an expected result.

To our knowledge the presented predistortion technique is new and its use was not reported before. This technique can find broader use in ΣΔ modulators with nonlinear effects for cancellation of harmonic distortion products.

4.4.4 Signal to noise ratio in the linearized modulator's output

This section investigates the modified 2-level modulator with the predistortion function derived earlier in this chapter. The *SNR* is calculated in the course of simulations as a function of modulator's order and input signal's amplitude, providing comparison between 3-level, conventional and modified 2-level modulators.

The $4QAM$ signal used in the simulations is characterized by $PAPR = 5.77dB$ and has a normalized bandwidth of $BW = \frac{f_{\Sigma\Delta}}{80}$, which yields the oversampling ratio of $LP\Sigma\Delta$ modulators $OSR = 80$. Coefficients and noise transfer functions for $LP\Sigma\Delta$ modulators used in the simulations are given in Tab.2.3.

4.4.4.1 First order ΣΔ modulator

The improvement gained by adding the predistortion in the modified 2-level modulator is observed as the reduction of the error in adjacent channels in the simulated output spectrum shown in Fig.4.32(A). The cancellation of error E_{IN} brings the *SNR* of the modified 2-level modulator to nearly the same level as *SNR* of the 3-level modulator which is seen in Fig.4.32(B). The predistorted modulator shows over $4dB$ of *SNR* improvement when compared with the modified 2-level modulator without predistortion. The *SNR* calculation including power in adjacent channels ($BW_{SNR} = 3BW$) versus input signal power for the $4QAM$ input has been performed for testing stable range of operation of the

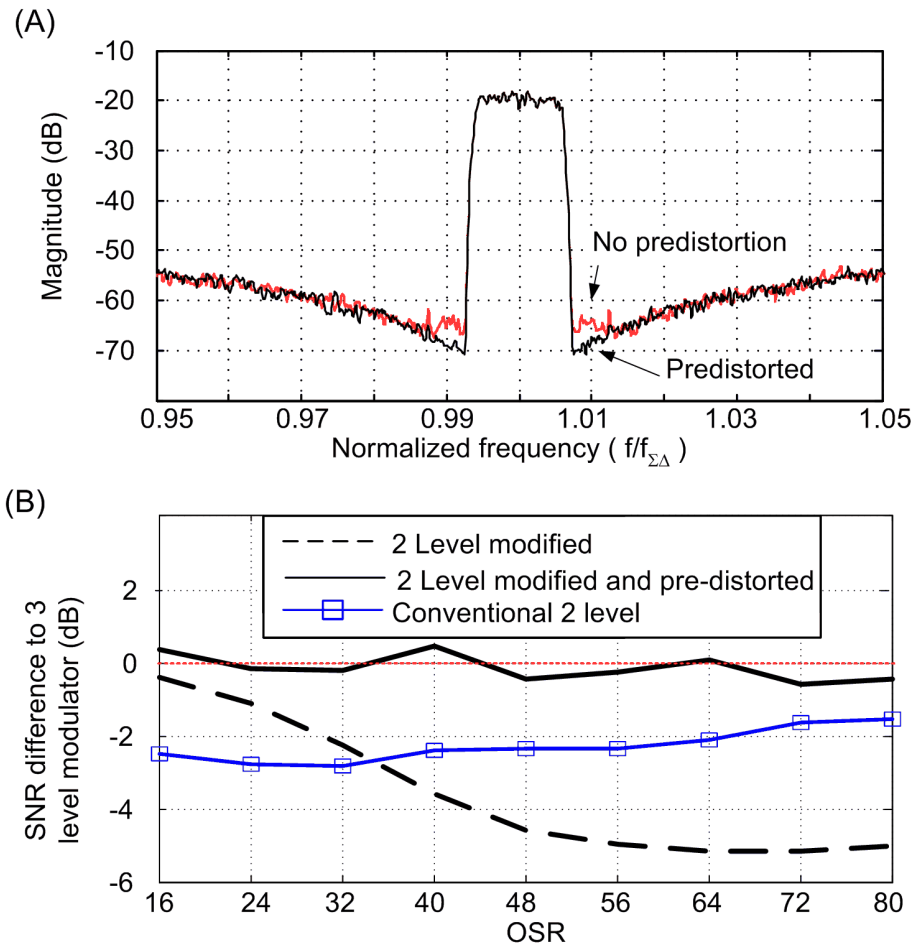

Figure 4.32: Simulated first order modulators for $M = 1$. (A) Output spectra of modified 2-level modulator before and after applying predistortion. (B) SNR in the output of 3-level and 2-level modulators.

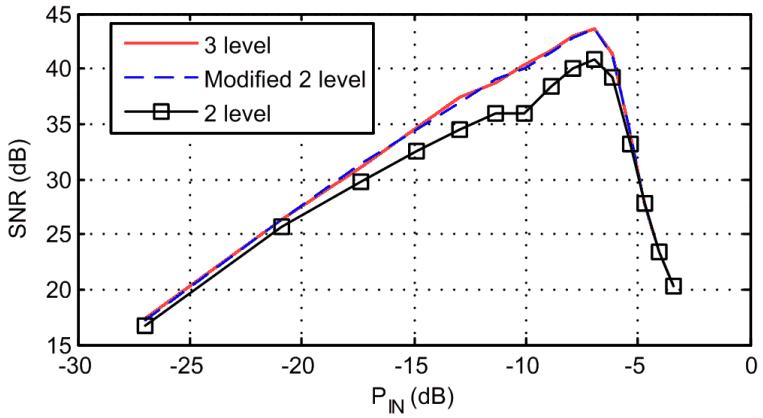

Figure 4.33: *SNR* versus input signal's power for 3-level modulator and 2-level modified and conventional modulators, $NTF = 1 - z^{-1}$, $M = 1$, $BW_{SNR} = 3BW$.

modulators, the results are shown in Fig.4.33. It is read from the figure that the modified 2-level modulator performs very closely with the 3-level one over the entire input power range and offers approximately $3\,dB$ of the *SNR* improvement over the *SNR* of the con-

ventional 2-level modulator when $P_{IN} = -6.9\,dB$. The peak SNR is achieved when the input signal reaches a power of $P_{IN} = -6.9dB$. All three modulators become unstable at the same input power level.

4.4.4.2 Second order ΣΔ modulator

The simulated output spectra for the modified modulator employing second order $LP\Sigma\Delta$ before and after applying predistortion are shown in Fig.4.34(A). A $10\,dB$ of a noise level reduction in the adjacent channels is achieved when the predistorting signal is added. As read from Fig.4.34(B), the error cancellation increases the modulator's SNR to the level of 3dB below the SNR of the 3-level modulator when $OSR = 80$, yielding a $10\,dB$ of SNR improvement in comparison with the same modulator without predistortion. It is observed in Fig.4.35 that the modified 2-level modulator performs slightly worse than a 3-level

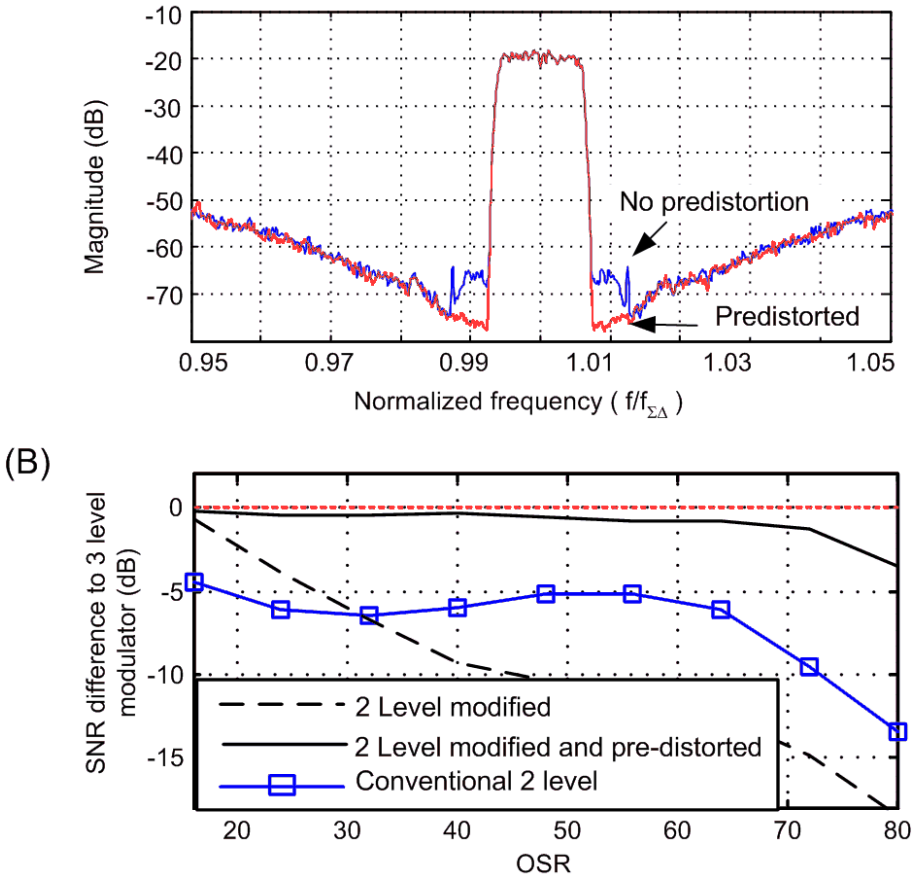

Figure 4.34: Simulated second order modulators for $M = 1$ (A) Output spectra of modified 2-level modulator before and after applying predistortion. (B) SNR in the output of 3-level and 2-level modulators.

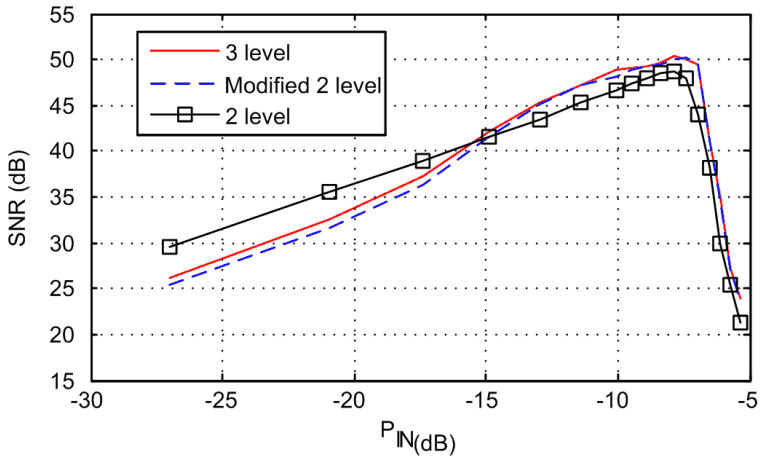

Figure 4.35: SNR versus input signal's power for 3-level modulator and 2-level modified and conventional modulators, $BW_{SNR} = 3BW$. The quadrature mixer uses $M = 1$.

modulator when input signal's power is low, and the *SNR* improves when P_{IN} increases. This effect has two causes. When modulator's order increases, the input-output characteristic begins to differ from the relation described by equation (4.16). Subsequently, the efficiency of E_{IN} error cancellation decreases at low amplitudes of the input signal. This effect was described in Section 4.3.7.1. Secondly, when the input amplitude is small, the overall error addition in the quantizer with the zero-level offset is large which is seen in Fig.4.17(C). This causes the increase of an in-band noise in the output of the modulator. It is also observed in Fig.4.35 that the modified 2-level modulator maintains good *SNR* in the presence of slightly higher input signal amplitudes than the equivalent, conventional 2-level modulator, which stems from the use of the 3-level quantizers in the *LP*ΣΔ modulators. The capability for encoding more of a signal power is important from the point of view of coding efficiency and power efficiency of a *SMPA* in class-S power amplifier.

4.4.4.3 Third order ΣΔ modulator

When a third order ΣΔ modulators are employed, the quantization noise shaping in 3-level modulators improve further, but the effectiveness of the E_{IN} error cancellation worsens. The increase of the noise power in adjacent channels of the modified 2-level modulator in comparison with the output of ideal, 3-level modulator is observed in Fig.4.36. The

SNR calculated for $OSR = 80$ is $16dB$ worse in the output of the modified 2-level modulator with the predistortion than in the output of the 3-level modulator. Also, the modified 2-level modulator's *SNR* is $10dB$ worse than the *SNR* of the conventional 2-level modulator. This shows the increasing difference in higher order ΣΔ modulators between the quantization noise power inside the signal band, where its suppression by the NTF is strongest, and the power of the error induced by the quantizer with the zero-level offset. This *SNR* degradation is caused by the presence of quantization error E_Q and by imperfect cancellation of error E_{IN}.

An *SNR* for the 3-level and 2-level modulators including noise power in adjacent channels ($BW_{SNR} = 3BW$) is shown in Fig.4.37. The proposed modulator with the predistortion performs better than the conventional 2-level modulator when the normalized input signal's power is higher than $-15dB$. It is observed that the proposed modulator has higher stable input range than the conventional 2-level modulator, which is an expected result. To achieve higher *SNR* when employing high order ΣΔ, the proposed modulator

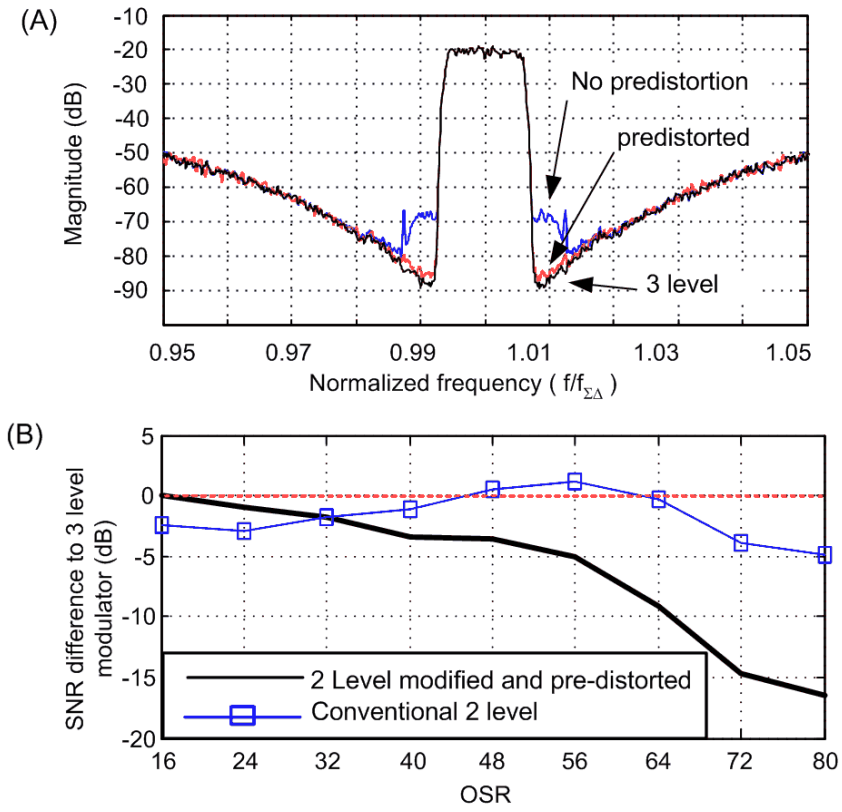

Figure 4.36: Simulated third order modulators for $M = 1$. (A) Output spectra of modified 2-level modulator before and after applying predistortion. (B) *SNR* in the output of 3-level and 2-level modulators.

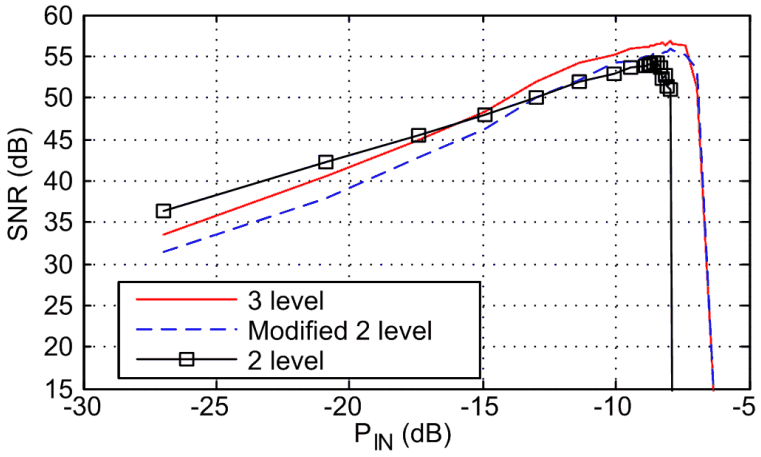

Figure 4.37: SNR versus input signal's power for 3-level modulator and 2-level modified and conventional modulators, $BW_{SNR} = 3BW$. The quadrature mixer uses $M = 1$.

needs however a more advanced predistortion function than that described in Section 4.4. This predistortion should also include some compensation for the quantization error E_Q.

4.5 Experimental results

The conventional 2-level system of Fig.4.10, and the modified 2-level modulator of Fig.4.11 have been implemented using a Virtex II Pro FPGA board.

The implementation of the modified 2-level modulator requires minor additional overhead for hardware in comparison with the conventional 2-level modulator. When implemented, the use of a 3-level instead of a 2-level quantizer increased the hardware count by an addition of four logic gates. Also, several AND gates - depending on the M parameter - were sufficient to convert 3-level output to a 2-level waveform. No significant power consumption difference between the conventional and the modified modulators should therefore be observed.

Each ΣΔ modulator was provided with a $0.625MHz$ wide baseband I, Q input, creating 4QAM signal with $PAPR$ of $5.77dB$. The same input was used for measuring output spectra of the conventional 2-level and the modified modulators. Both ΣΔ modulators were first orders with the same noise transfer function $NTF = 1 - z^{-1}$ and sampled at

the rate of $f_{\Sigma\Delta} = 100MHz$. The modified 2-level modulator was implemented without the predistortion described in Section 4.4. For $M = 1$ the corresponding carrier frequency was $f_C = 100MHz$, resulting in the output pulse stream bit rate of $400MHz$. A $20\,GSa/s$ Agilent Infiniium 54853*A* digital oscilloscope was used for measuring the output from the FPGA board.

It is observed from the measured time domain waveforms shown in Fig.4.38(A), that the total duration of high state output is shorter in the modified modulator's case, which indicates that the pulse train produced by the modified modulator has lower power than the output of the conventional modulator $\Delta^2_{MOD} < \Delta^2_{2L}$. The output spectra of both systems are shown in Fig.4.38(B, C). The noise power increase at frequencies $f = 0$ and $f = 2f_C$ caused by the functions $G_e(f)$ and $H_e(f)$ are observed in comparison with the conventional modulator. Also, matching with the expectation, the modified system generates less quantization noise than the conventional 2-level modulator in the proximity of the carrier frequency, however a slight noise level increase near the carrier frequency in the output spectrum of modified system is seen in Fig.4.38(B). This performance degradation is expected in the modified modulator without predistortion. Additionally, some of the performance degradation was caused by the error pulse shaping being different from the ideal described by $g_e(t), h_e(t)$. The difference resulted from the use of a non ideal *DAC* in the FPGA. Due to the use of non ideal *DAC* and a the presence of clock jitter, the dynamic range of the modulator implemented could not be achieved higher than approximately $40dB$ with a carrier frequency at $100MHz$. On the other hand, a $40dB$ of an *SNR* corresponds to 1% of an *EVM*, which is acceptable in $64QAM$ signals. Measured output samples were used for determining coding efficiency. In both scenarios, conventional and modified modulator, the input was characterized by $\overline{|I|} = \overline{|Q|} = 0.091V$, with an average power of $q^2_{IN} = 0.011V^2$ and an amplitude peaking between $\pm 0.25V$. Equations (4.12), (4.9) can be used to calculate the expected power in the output pulse trains,

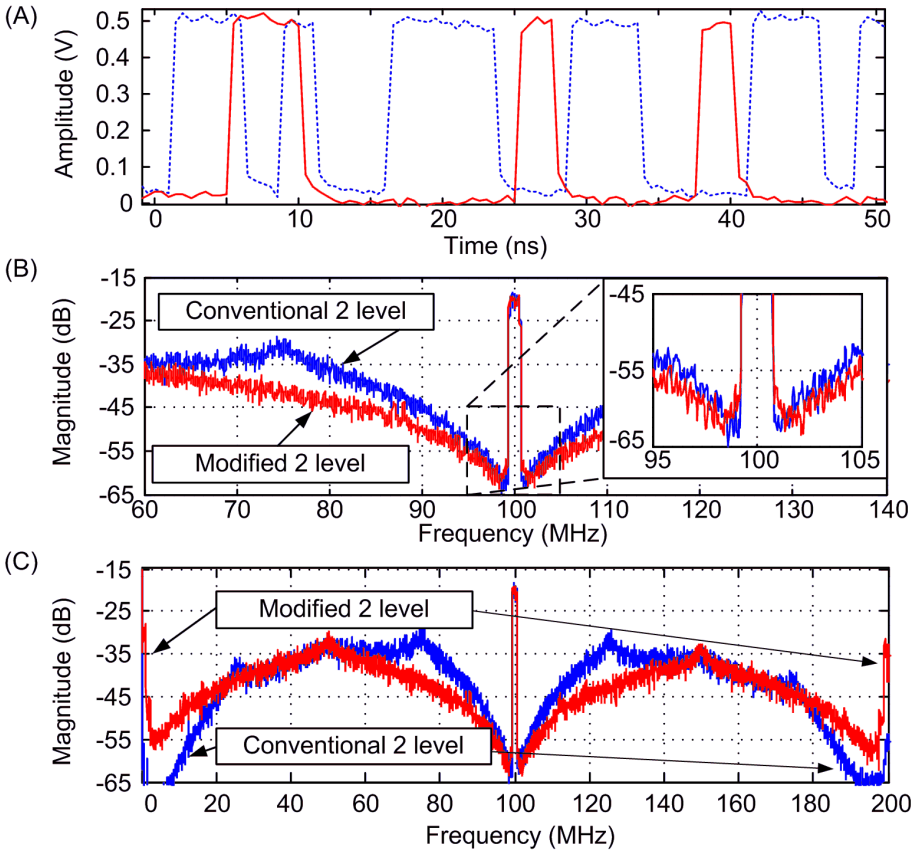

Figure 4.38: (A) Measured time domain waveforms, dashed line - conventional 2-level, continuous line - modified. (B, C) Output spectra.

$\Delta^2_{MOD-CALC} \approx 0.0455V^2$, $q^2_{2L-CALC} = 0.125V^2$. This is close to the measured values of $q^2_{MOD} = 0.053V^2$, $\Delta^2_{2L} = 0.124V^2$. Coding efficiencies for the measured signals computed with (4.13) are $\eta_{2L} = 8.9\,\%$ and $\eta_{MOD} = 21\,\%$. Tab.4.2 gives the comparison of simulated and measured outputs of conventional and modified 2-level modulators. The coding efficiencies of both simulated modulators are close to the measured results. The slightly higher coding efficiency figures in the measured outputs indicate the effect of a finite bandwidth of the digital oscilloscope and subsequent lowpass filtering of the 2-level waveform, reducing q^2_{MOD} and q^2_{2L} in equation (2.27). The *SNR* for both modulators matches the simulated results for low oversampling ratio of $OSR = 8$. As expected, the modified 2-level modulator offers better *SNR* over wide bandwidth. As the *OSR* increases to $OSR = 16$ and $OSR = 24$, the measured *SNR* visibly worsens, which is caused by the effects explained earlier, i.e. non ideal error pulses shaping and clock jitter.

Table 4.2: Coding efficiency and *SNR* comparison for conventional and modified 2-level modulators

***SNR*/coding efficiency**	**Simulation**	**Measured**
η_{2L}	8.4 %	8.9 %
η_{MOD}	20 %	21 %
$SNR_{2L}\ (OSR = 8)$	$24.5\,dB$	$24.5\,dB$
$SNR_{MOD}\ (OSR = 8)$	$27.3\,dB$	$27\,dB$
$SNR_{2L}\ (OSR = 16)$	$33.9\,dB$	$32.7\,dB$
$SNR_{MOD}\ (OSR = 16)$	$36.1\,dB$	$32.7\,dB$
$SNR_{2L}\ (OSR = 24)$	$39.5\,dB$	$36.5\,dB$
$SNR_{MOD}\ (OSR = 24)$	$40.8\,dB$	$35.1\,dB$

4.6 Conclusion

This chapter described a new approach to band pass signal modulation. It was demonstrated, that in certain cases the error introduced by 3-level quantizer with zero-level offset can be suppressed within the signal band by appropriately shaping the error pulses. The mechanism of error pulses shaping was then used to derive a modified, 2-level modulator.

As it is based on 3-level ΣΔ modulation, the modified modulator exhibits improved coding efficiency in comparison with conventional 2-level modulator, and can provide better *SNR* for a bandlimited signal than the equivalent 2-level modulator of order one or two. The modified 2-level modulator has been implemented and demonstrated for a complex-envelope signal at $100\,MHz$ carrier frequency. The measured results showed coding efficiency increase from 8.9 % in a conventional 2-level modulator to 21 % for the modified 2-level modulator. Due to the use of 3-level quantizers in *LP*ΣΔ, the modulator is also characterized by the same stable operation range as 3-level *LP*ΣΔ, which can improve power efficiency of a digital transmitter, if the modulator is used as a source encoder.

Chapter 5

Polar modulator

This chapter focuses on the signal processing in a polar transmitter with a ΣΔ-digitized envelope signal, being a sub-class of *EER* transmitters [73]. The digitized polar transmitter (DPT) splits an input RF signal into phase and envelope signals. After 2-level ΣΔ modulation of the envelope signal, the phase and pulsed envelope signals are mixed, yielding a drive signal for a nonlinear power amplifier. The digitized polar transmitter is a promising alternative to the Class-S amplifier, and it can also be classified as a digital amplifier. Both, Class-S and *DPT*, use ΣΔ modulation to shape a quantization error which offers some degree of reconfigurability of the transmitters. An important advantage of the *DPT* over the Class-S amplifier is higher coding efficiency. The drawback of the *DPT* is higher complexity of the signal conversion.

The principle of operation of the polar transmitter and conversion from Cartesian to polar coordinates of the input signal are described in Section 5.1. The spectral regrowth of phase and envelope signals and the effect of phase-envelope delay are analyzed in Section 5.2. Section 5.3 focuses on ΣΔ modulation of envelope signal and on an aliasing effect present in the *DPT*. A brief comparison of the Class-S and *DPT* is presented in Section 5.4. Section 5.5 describes the new signal modulator for the *DPT*.

5.1 Digitized polar transmitter

In the *EER* transmitter, the amplified signal X_{RF} is decomposed into envelope and phase signals. The envelope component $ENV(t)$ is amplified by an *SMPS* or Class-D amplifier driven by a pulse width modulated waveform. After eliminating the difference of the time delay occurring between envelope and phase signals, the RF signal is reconstructed in the output of a nonlinear RF amplifier with supply voltage from the *SMPS* as it is shown in Fig.5.1. Since the two amplifiers in the transmitter scheme can operate in switchmode, the resulting system is in theory power efficient and linear. In practice both, the *SMPS* and the nonlinear *RF* amplifier in the *EER* transmitter dissipate power, and the efficiency of the transmitter becomes a product of the two efficiency figures. Also, the amplitude modulation performed in the RF amplifier causes nonlinear distortion in the RF output.

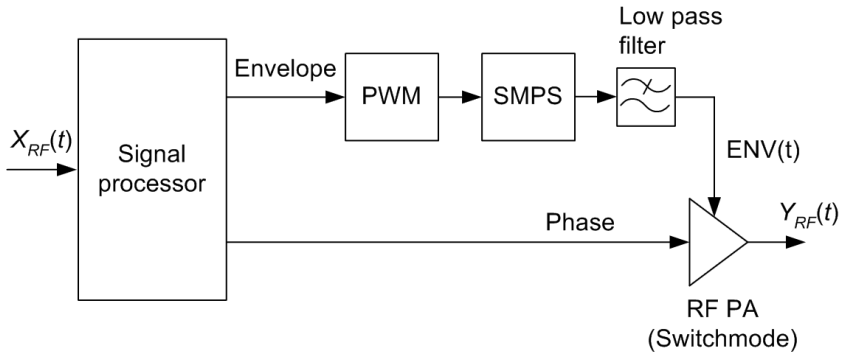

Figure 5.1: Envelope elimination and restoration transmitter.

The *EER* transmitter was next modified by Wang. Wang proposed to use a 2-level $LP\Sigma\Delta$ modulator in the envelope branch, which changes the analog envelope signal to a digital pulse train of 1 and 0 levels [73]. The modification allows for mixing the phase and digitized envelope before the amplifier, and the use of a single, switchmode PA. Subsequently the *RF* output signal is restored after a band pass filtering as it is depicted in Fig.5.2. Since the envelope signal has only two levels, the nonlinear distortion of the *RF* amplitude signal characteristic for the conventional *EER* transmitter is avoided in the digitized polar transmitter.

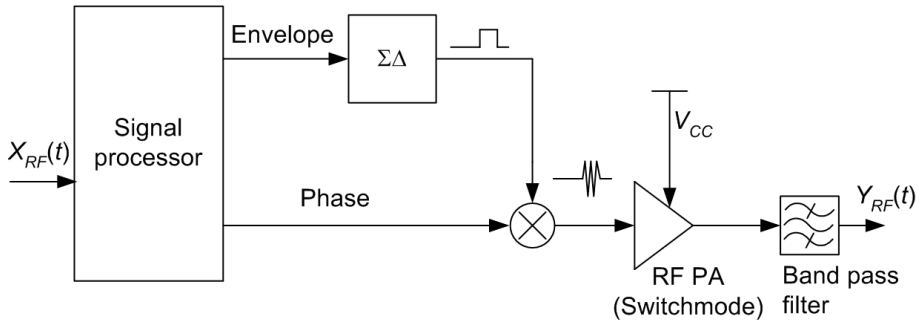

Figure 5.2: Digitized polar transmitter.

5.1.1 Conversion to polar form

In a modern digital communication systems, the transmitted signal is created by mixing the in-phase and quadrature signals with 90^0 shifted carrier signals.

$$X_{RF}(t) = I(t)\cos(\omega_C t) + Q(t)\sin(\omega_C t) \tag{5.1}$$

The in-phase and quadrature signals have their spectrum limited by pulse shaping, performed in a baseband processor, which usually adds an amplitude modulation to the RF signal. When the bandwidths of the I and Q are many times lower than the carrier frequency f_C, a linear combination of sine and cosine functions can be used to calculate the envelope of the RF signal,

$$ENV(t) = \sqrt{I^2(t) + Q^2(t)} \tag{5.2}$$

The subsequent division of the RF signal by the envelope leads to the expression for the phase signal,

$$PHA(t) = I'(t)\cos(\omega_C t) + Q'(t)\sin(\omega_C t) \tag{5.3}$$

where phase components I' and Q' are described by,

$$\begin{aligned} I'(t) &= \frac{I(t)}{\sqrt{I^2(t)+Q^2(t)}} \quad (A) \\ Q'(t) &= \frac{Q(t)}{\sqrt{I^2(t)+Q^2(t)}} \quad (B) \end{aligned} \tag{5.4}$$

and the RF signal is now expressed by,

$$X_{RF}(t) = ENV(t)\,PHA(t) \tag{5.5}$$

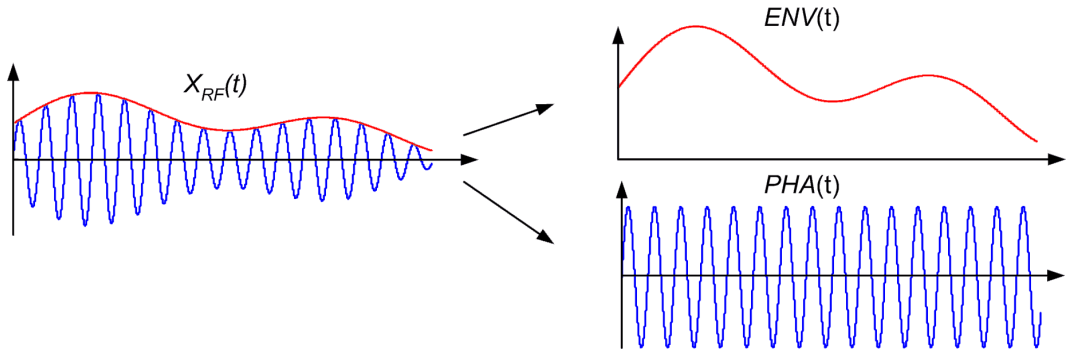

Figure 5.3: Decomposition of the transmitted input signal into phase and envelope components.

A common scheme of a modern polar modulator employs a digital signal processor for computing the envelope and the phase components, while an analog mixer is used to process equation (5.3) as it is shown in Fig.5.4 [75, 83, 86]. Until the conversion to the polar form, the baseband signals in the modulator are band limited. The computation of the square root of equation (5.2) and divisions of equation (5.4) lead to a spectral regrowth of the resulting phase and envelope signals [74,81,82], which is discussed in the next section.

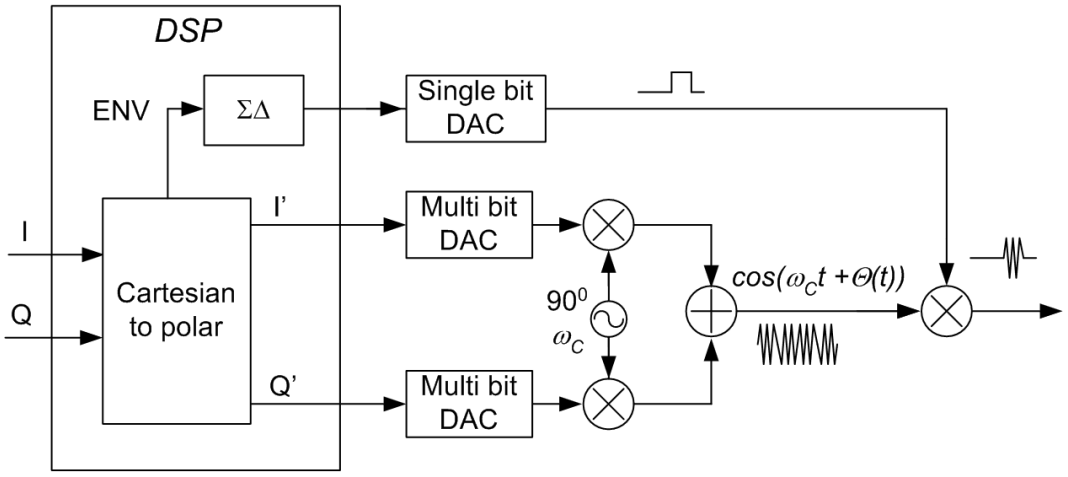

Figure 5.4: Modulator for *DPT*.

5.2 Non-ideal operation of polar transmitter

The digitized polar transmitter decomposes an input RF signal into phase and envelope signals and processes them in two separate branches. In order to avoid the *AM* distortion, the two signals must be provided with sufficient bandwidth. Equally important is that the time delay difference between these two signals is minimized before the RF signal is reconstructed. This section proposes to use an additive error to analyze the above effects on the reconstructed, RF signal. Such an approach allows for predicting the noise power in adjacent channels, but also gives an insight into *SNR* calculated inside the RF band.

5.2.1 Spectral regrowth - two tone signal

Let us consider a two tone RF signal, being a simple example of an amplitude and phase modulated signal,

$$\begin{gathered} X_{RF}(t) = Amp \cdot sin(\omega_1 t) \cdot sin(\omega_C t) = \\ = \frac{Amp}{2}\left[cos((\omega_C - \omega_1)t) - cos((\omega_C + \omega_1)t)\right] \end{gathered} \tag{5.6}$$

The RF bandwidth can be defined for the above signal as $BW=\frac{\omega_1}{\pi}$, and its center frequency is $f_C = \frac{\omega_C}{2\pi}$ with $\omega_1 \ll \omega_C$. Although the bandwidth of the X_{RF} signal is limited, the bandwidth of its envelope and phase signals are not. The RF envelope can be expressed using a Fourier series,

$$\begin{gathered} ENV(t) = Amp \cdot |sin(\omega_1 t)| = \\ \frac{2 \cdot Amp}{\pi} - \frac{4 \cdot Amp}{\pi} \sum_{n=1}^{\infty} \frac{cos(2n\omega_1 t)}{4n^2 - 1} \end{gathered} \tag{5.7}$$

and it has an infinite number of harmonics. When the number of harmonics is restricted to some finite number, e.g. due to a low sampling rate of a *DSP*, then the amplitude distortion occurs in the reconstructed *RF* signal. The RF amplitude distortion worsens as

less harmonics are allowed [80,116]. Fig.5.5 shows waveforms for the two tone signal decomposed into phase and envelope components. The effect of removing harmonics higher than 2 is observed as the difference between the continuous-line waveform representing the ideal envelope signal and the dashed-line waveform, representing envelope with the finite number of harmonics.

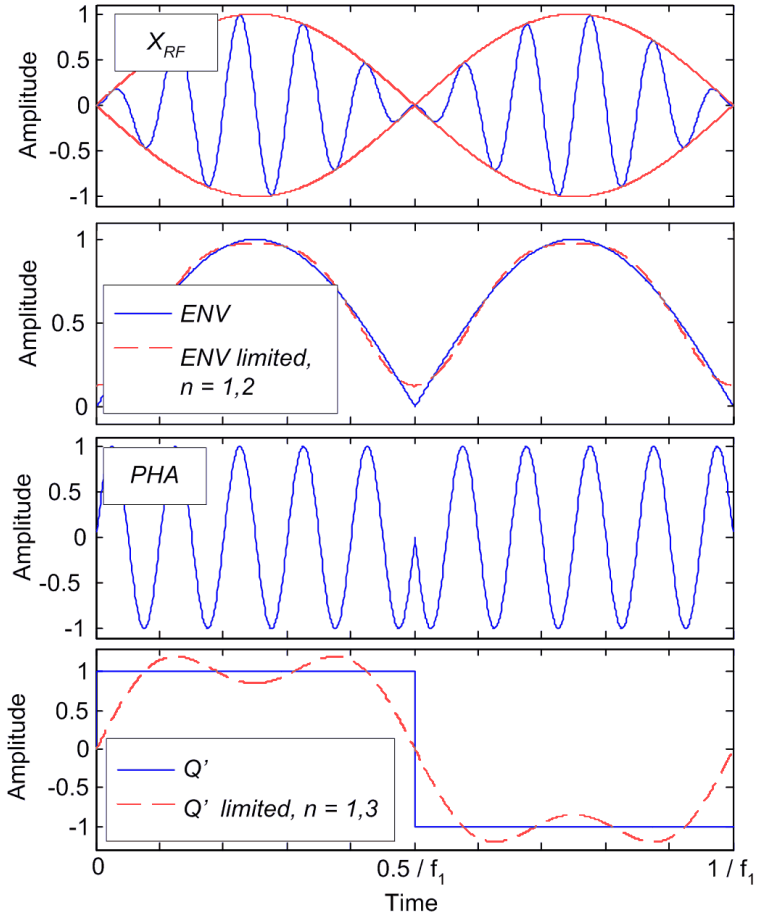

Figure 5.5: Decomposition of two tone signal into phase and envelope components.

The phase signal is calculated using equations (5.3) and (5.4),

$$PHA(t) = \frac{X_{RF}(t)}{ENV(t)} = \frac{sin(\omega_1 t)}{|sin(\omega_1 t)|} sin(\omega_C t) = Q'(t) \cdot sin(\omega_C t) \tag{5.8}$$

with the baseband phase component I' being zero, and Q' expressed by,

$$Q'(t) = \frac{sin(\omega_1 t)}{|sin(\omega_1 t)|} = \frac{4}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} sin(n\omega_1 t) \tag{5.9}$$

The baseband portion of the phase signal is a 50 % duty cycle square wave $Q'(t)$ shown in Fig.5.5. When a finite number of harmonics are allowed in the $Q'(t)$, then similarly to the $ENV(t)$ signal, distortion of the RF amplitude occurs. It should be noted that the bandlimiting of the phase signal does not cause PM distortion. This becomes evident after substituting (5.8) in (5.5),

$$X_{RF}(t) = ENV(t) \cdot PHA(t) = \left[ENV(t) \cdot Q'(t)\right] sin(\omega_C t) \tag{5.10}$$

Any variation of the ideally square waveform $Q'(t)$ caused by the bandlimiting results in a change in the RF amplitude, but it does not affect the phase of the signal. As the harmonics in $Q'(t)$ or $ENV(t)$ are limited to finite numbers, the RF signal preserves its phase information, but the change in the RF amplitude is observed. In theory the variation of the amplitude caused by bandlimiting the phase signal can be removed by a limiter, as it was done originally in the EER transmitter [80]. A large variation of the phase's amplitude may however cause an AM distortion in the output of the $SMPA$, which should be avoided.

5.2.2 Bandlimited input signal

Spectral regrowth of an envelope and phase signals similar to those described for the two-tone signal can also occur in other signals used in digital communication. These effects depend on the type of RF signal. It was shown that signals whose vector diagrams do not have zero crossings, such as $OQPSK$ or $\pi/4DQPSK$ are characterized by lower spectral regrowth of the envelope and phase signals than those, whose trajectories have crossings through the origin of a complex plane, such as the $OFDM$ signal [90, 91]. Consequently, in the case of the latter, a modulator and power amplifier in a polar transmitter are required to provide higher bandwidths than if the RF signal did not have the zero crossings. Such a signal, being the worst case scenario for a polar transmitter's bandwidth was gen-

erated in Matlab, and used to investigate the effects of bandlimiting the signals on a polar transmitter's noise performance. The bandlimited test signal has a Gaussian distribution, and its envelope is Rayleigh-distributed. While no clipping of the peak amplitudes was applied, this signal has a relatively large *PAPR* of 12 *dB* and its vector trajectory has zero crossings similar to an *OFDM* signal. The trajectory and spectra for the RF signal, phase and envelope signals are shown in Fig.5.6.

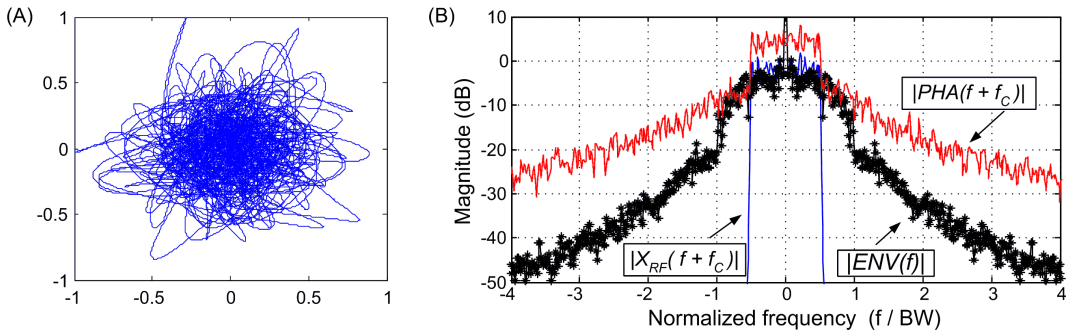

Figure 5.6: Bandlimited test signal. (A) Vector diagram. (B) Spectral regrowth of phase and envelope components.

5.2.3 Envelope band limitation

The band limiting of a phase or envelope signal can be modeled as a subtraction of the suppressed spectral components from the original signal. If we apply a lowpass filter to the envelope signal, then, assuming linear phase response of the filter, the attenuation in the filter's stopband can be expressed as a difference between magnitude in the input to the filter, and the magnitude in the output of the filter. In order to simplify the analysis, let the lowpass filter have a brick wall magnitude response depicted in Fig.5.7.

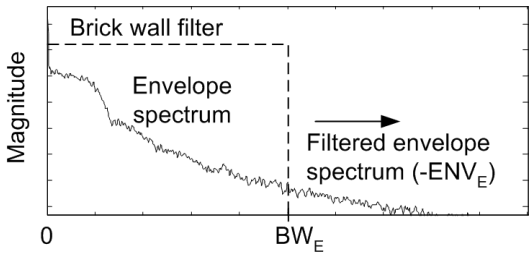

Figure 5.7: Spectral limiting of an envelope signal.

Consequently, the output and input signals are the same within the filter's passband, while the spectral components that fall into the stopband of the filter are subtracted from the original signal. Such a bandlimited envelope signal becomes a sum of the original envelope signal, ENV, and the error ENV_E which represents the removed part of the spectrum,

$$ENV_{BW-L} = ENV + ENV_E \tag{5.11}$$

Provided that the time delay between phase and the bandlimited envelope is corrected, the reconstructed RF signal can be described by,

$$X_{RF}(t) = [ENV(t) + ENV_E(t)]\,PHA(t) \tag{5.12}$$

The resulting output consists of the original signal i.e. $ENV(t)\,PHA(t)$ and the error component $ENV_E(t)\,PHA(t)$. When the magnitude spectrum of the envelope is monotonically decreasing, then the maxima of error's magnitude occur at the edges of filter's passband at $f = \pm BW_E$. After multiplying the phase and the bandlimited envelope signals, the maxima of the error appear at frequencies $f = f_C \pm BW_E$, where f_C is the carrier frequency of the transmitted signal.

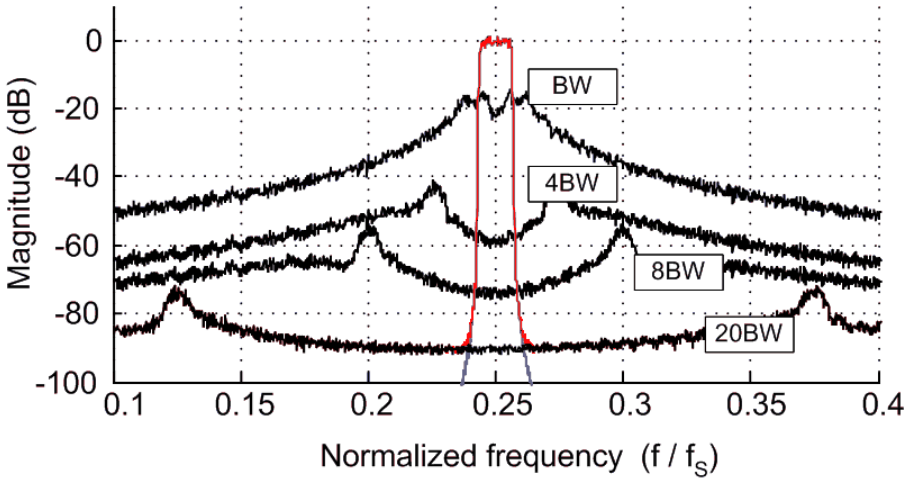

Figure 5.8: Output spectra for different envelope bandwidths, $f_C = 0.25 f_S$.

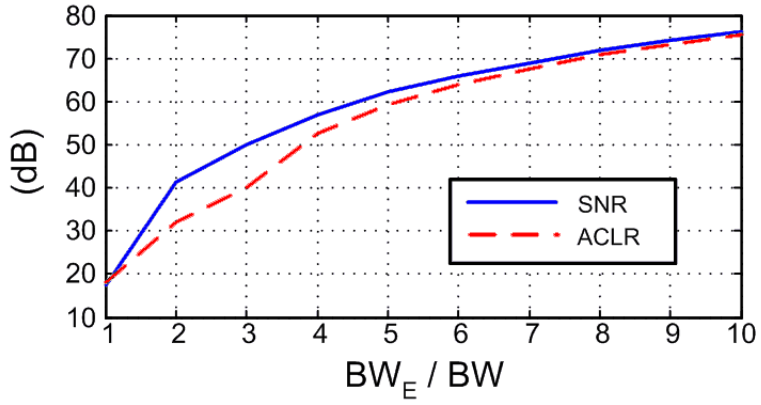

Figure 5.9: *SNR* and *ACLR* as a functions of envelope bandwidth.

As the brick-wall filter's cut-off frequency increases, the error power decreases, and the error's magnitude peaks become more distant from a carrier frequency. Simulated spectra of the transmitted signal with different envelope passbands are shown in Fig.5.8. The result of the *SNR* and *ACLR* simulation for an *RF* signal with a band-limited envelope are shown in Fig.5.9. It is observed that due to the error peaks, the polar transmitter with the bandlimited envelope signal exhibits less noise inside the RF band than in the adjacent channels. Unless the envelope bandwidth is many times wider than the RF bandwidth, the noise peaks occur close to the carrier frequency, and their suppression with a high Q output filter can be troublesome. Consequently, the passband of the envelope signal should be sufficient for maintaining power of these peaks $43dB$ below the signal power level to meet *ACLR* requirements in $UMTS$ [1]. It is read from Fig.5.8 that an envelope bandwidth at least four times wider than the RF bandwidth should be provided. On the other hand, $50\,dB$ of *ACLR* makes the envelope error signal negligible in terms of the EVM increase for $QPSK$ or $16-QAM$ signals, i.e. for $50dB$ of *SNR* the root mean square value of EVM is approximately 0.0032. Although the calculated *SNR* and *ACLR* are valid for the bandlimited test signal used in this simulation, they can be also of use as an initial estimation of *SNR* and *ALCR* for other signals used in digital communications. It should be noted that the envelope signal in a digitized polar transmitter is encoded

by a 2-level $LP\Sigma\Delta$ modulator, whose sampling rate is usually many times higher than the RF bandwidth. This is needed for suppression of a quantization noise induced by the modulator. Due to the high oversampling ratio in the envelope path, the spectral limitation of the envelope signal has a negligible impact on the SNR in the RF output of the transmitter. This advantage comes at the cost of increased quantization noise power. The effects of the use of a $LP\Sigma\Delta$ modulator in the DPT are discussed in Section 5.3.

5.2.4 Phase passband limitation

The limitation of the phase bandwidth has a similar effect on the reconstructed RF signal in the polar modulator as band limiting of the envelope signal described in the previous section. The suppression of the phase signal below frequency $f_1 = f_C - BW_P/2$ and above frequency $f_2 = f_C + BW_P/2$, where BW_P denotes the allowed phase bandwidth, has the consequence of the error power peaks which occur in the output spectrum. Let us express the effect of the phase band-limiting as an addition of the error PHA_E. Subsequently, the reconstructed output becomes,

$$X_P(t) = ENV(t) \cdot [PHA(t) + PHA_E(t)] \tag{5.13}$$

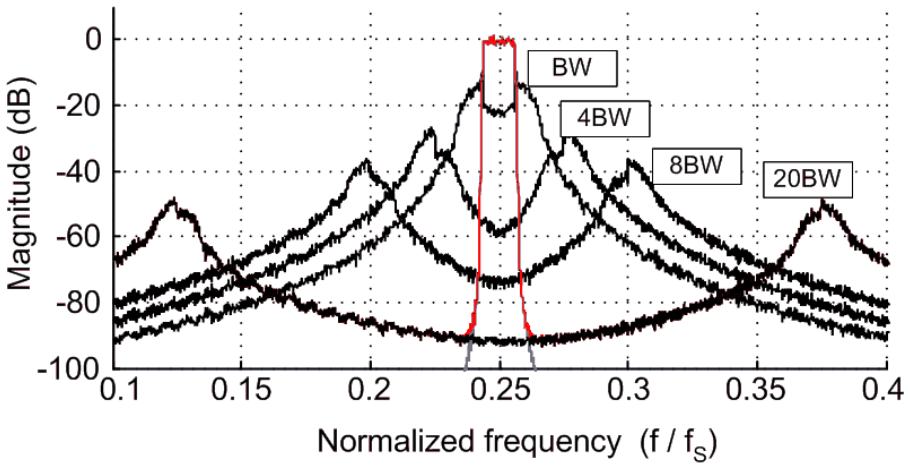

Figure 5.10: Output spectra of polar modulator with different phase bandwidths, $f_C = 0.25 f_S$.

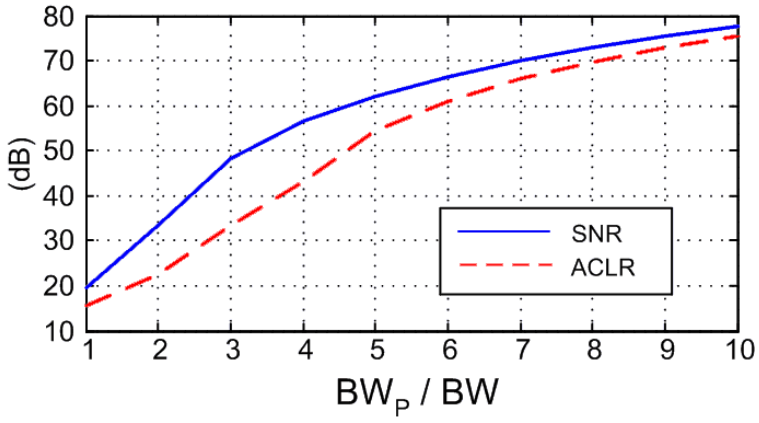

Figure 5.11: *SNR* and *ACLR* as a functions of a phase bandwidth.

Fig.5.10 shows simulated spectra for the bandlimited input signal with different bandwidths BW_P. The bandpass filter used in the simulation has the unity magnitude response within the passband, and zero magnitude otherwise. As expected, the error peaks are observed at the cut-off frequencies of the bandpass filter. Fig.5.11 shows the *SNR* and the *ACLR* calculated for the input bandlimited signal. It is read that a phase bandwidth approximately four times wider than the RF bandwidth can be sufficient for achieving the $43dB$ of the *ACLR*. On the other hand, the error peaks in the output spectrum of Fig.5.10 are well above the $-43\,dB$ when $BW_P = 4BW$. To meet the requirement of $-43\,dB$ for the out of band emission, the phase bandwidth should approximately be ten times wider than the RF bandwidth, as extrapolated from Fig.5.10.

$$BW_{P-MIN} = 10 \cdot BW \tag{5.14}$$

5.2.5 Phase-envelope Delay

Phase and envelope components of the transmitted signal undergo different signal processing operations in a polar transmitter, which causes different time delays induced in these branches. The time misalignment between phase and envelope signals becomes the third important contributor to *SNR* degradation in a polar transmitter.

Let us express the retarding $ENV\,(t-\tau)$ or advancing envelope signal $ENV\,(t+\tau)$ as

a sum of the ideally aligned envelope $ENV(t)$, and the delay error; $ENV_{\tau D}$ for delaying and $ENV_{\tau A}$ for advancing envelope signals. Because the *SNR* degradation depends on the absolute time difference between the phase and envelope signals, the following analysis can be reduced to one case. Consequently the delaying-envelope scenario is considered next.

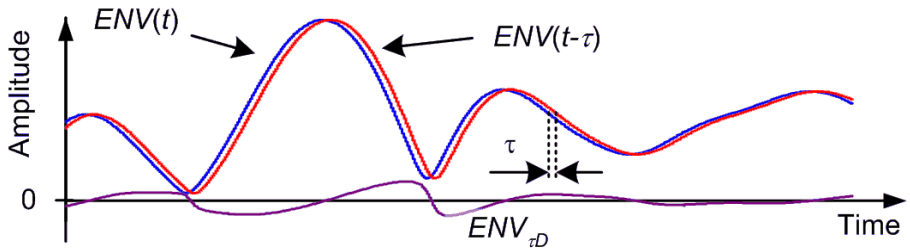

Figure 5.12: Retarding envelope signal.

The delaying envelope shown in Fig.5.12 is expressed by,

$$ENV(t-\tau) = ENV(t) + ENV_{\tau D}(t) \tag{5.15}$$

Subsequently, the delay error becomes,

$$ENV_{\tau D}(t) = ENV(t-\tau) - ENV(t) \tag{5.16}$$

Using the Fourier transform to write equation (5.16) in the frequency domain yields,

$$ENV_{\tau D}(f) = ENV(f)e^{-j\omega\tau} - ENV(f) = ENV(f)\left(e^{-j\omega\tau} - 1\right) \tag{5.17}$$

and using the above equation in the expression for modulator's output X_{RF} yields,

$$X_{RF}(f) = \left[ENV(f) + ENV(f)\left(e^{-j\omega\tau} - 1\right)\right] \star PHA(f) \tag{5.18}$$

It is observed from equations (5.17), (5.18) that the error resulting from delay time τ is the same as the high pass filtered envelope $ENV(f)$. The high pass function has a zero at DC, and its magnitude increases as the the delay time τ increases, indicating the growth of the error power. Despite the first order highpass filtering, the delay error maintains the

largest magnitude at low frequency, subsequently shaping the error power inside the RF band in the output of a polar transmitter.

The simulated output spectra for different products of the time delay-bandwidth are shown in Fig.5.13. It is observed that the maximum of the error power falls inside the RF band as expected. Also, the effect of high pass filtering by the function $\left(e^{-j\omega\tau}-1\right)$ is seen as the noise-notch at frequency f_C.

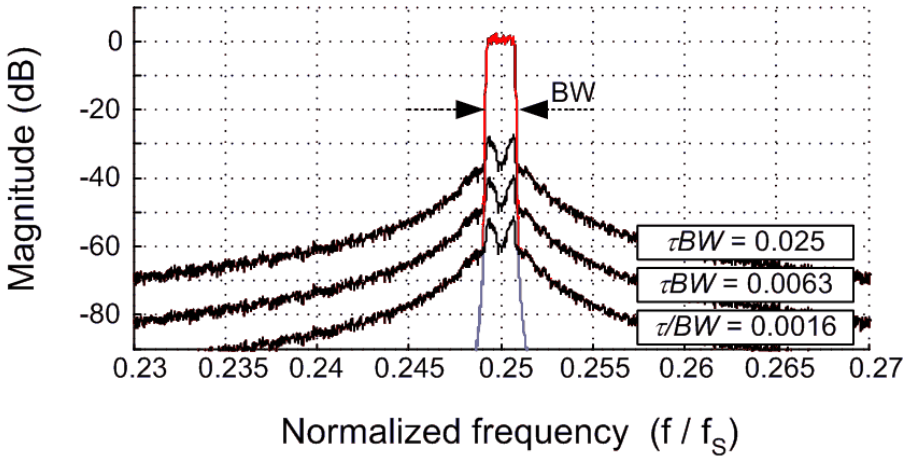

Figure 5.13: Output spectrum of polar modulator with different envelope-phase delay, $f_C = 0.25 f_S$.

Since the largest concentration of the error power occurs inside the RF band, this property can be used to estimate an *SNR* degradation caused by the delay time.

Let us assume the worst case scenario when 100% of the delay-error power falls into the RF band of the polar transmitter. Based on the above assumption, the minimum *SNR* can be calculated for the polar transmitter as the ratio of the envelope, and the high pass filtered envelope power,

$$SNR_{\tau_{MIN}} = \frac{\int_0^{\frac{BW}{2}\pi\tau} 1^2 d\left(\frac{\omega\tau}{2}\right)}{\int_0^{\frac{BW}{2}\pi\tau} \left|(e^{-j\omega\tau}-1)\right|^2 d\left(\frac{\omega\tau}{2}\right)} \tag{5.19}$$

which yields the minimum *SNR*,

$$SNR_{\tau_{MIN}} = 1/\left\{2\left[1-sinc\left(\frac{1}{2}\pi BW\tau\right)cos\left(\frac{1}{2}\pi BW\tau\right)\right]\right\} \tag{5.20}$$

Concluding from (5.20), the *SNR* is a function of the RF bandwidth *BW* and delay time τ product, being in agreement with the observation made by Raab [74]. As the largest portion of error's power falls inside the RF signal band, more of a degradation of *SNR* than *ACLR* is observed in Fig.5.14. The *SNR* calculated using (5.20) approximates the delay error with $5dB$ of accuracy when compared with the simulated results for the bandlimited input signal.

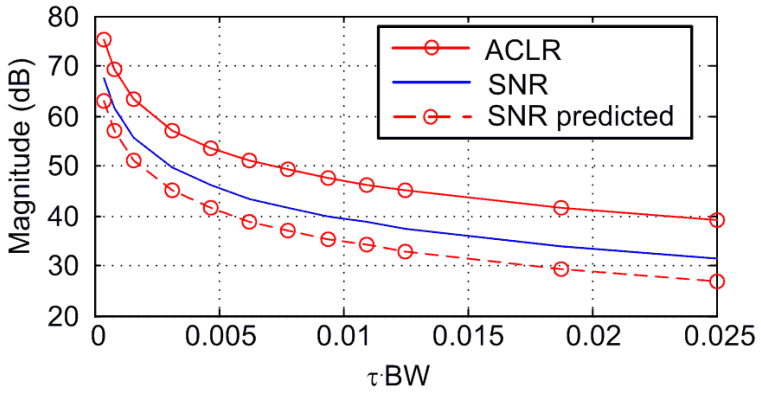

Figure 5.14: *SNR* and *ACLR* as a function of different delay times.

Table 5.1: Minimum *SNR* for time delay τ.

$SNR\ (dB)$	$BW\ (MHz)$	$\lvert\tau\rvert_{max}\ (ns)$	τBW
30	1.25	14	0.0175
30	5	3.5	0.0175
30	20	0.875	0.0175
40	1.25	4.4	0.0055
40	5	1.1	0.0055
40	20	0.275	0.0055
50	1.25	1.4	0.00175
50	5	0.35	0.00175
50	20	0.0875	0.00175
60	1.25	0.4	0.0005
60	5	0.1	0.0005
60	20	0.025	0.0005

Tab.5.1 lists conservative delay margins $\lvert\tau\rvert_{max}$ calculated with equation (5.20) required for achieving desired values of *SNR*. It is observed that for *SNR* of $50-60\,dB$, the corresponding maximum time delay error becomes a fraction of a nano second. Precise

adjustment of delay between phase and envelope signals becomes critical to the *SNR* performance of a polar transmitter, especially for a wideband signals. Due to the maximum error power occurring inside the RF band, the delay error may not be easily detected by inspecting the noise in adjacent channels of a polar transmitter, it can however cause an increase of the EVM.

5.2.6 Conclusion

This section analyzed the effects of bandwidth limitations in phase and envelope signals on the modulator's performance as well as the effect of time misalignment between these two signals. A new approach to analysis, using additive errors was employed, which gives insight into noise performance in adjacent channels, but also inside the RF band. The additive-error technique showed the large increase of error power inside the RF band, which was not clearly explained before [74, 90, 116].

5.3 ΣΔ modulation of envelope signal

The *LP*ΣΔ modulation of an envelope signal in the digitized polar transmitter offers some improvements to the conventional polar transmitter. The 2-level envelope signal does not require the *RF* power amplifier output to be a linear function of a supply voltage, and therefore avoids distortion in the process of envelope restoration [73, 87, 88]. Moreover, the 2-level pulse modulation can be done on a low-power drive signal instead of on a PA's supply voltage as it is done in the EER technique [73]. The drawback of the digitized polar transmitter is the large quantization noise power in the output spectrum. Also, which was not clear before [73], the digitization of the envelope signal causes aliasing in the RF band and subsequent *SNR* degradation, regardless of the *LP*ΣΔ modulator's sampling rate. The above problems are analyzed and quantified in this section.

5.3.1 Sampled envelope's spectrum

The digitized envelope signal in the polar transmitter of Fig.5.4 can be expressed as a sum of the envelope signal, ENV and the quantization noise ENV_Q induced by the $LP\Sigma\Delta$ modulator. Since the digitized envelope is a sampled signal, its spectrum replicates in frequency domain with the interval equal to the sampling rate of the $LP\Sigma\Delta$ modulator, f_E as it is depicted in Fig.5.15.

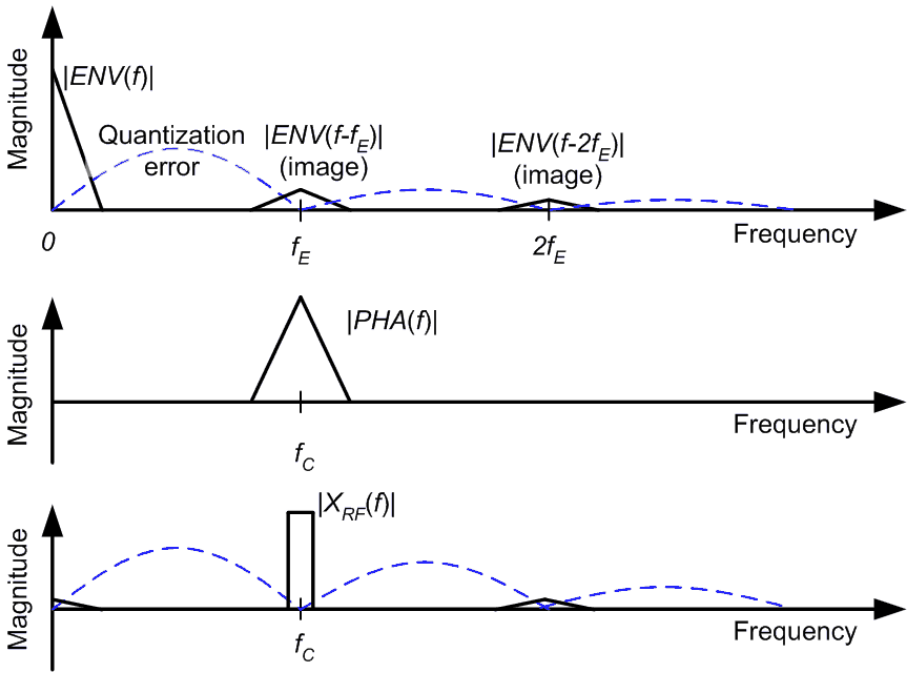

Figure 5.15: Mixing of a digitized envelope and phase signals.

When any of the two components, quantization noise or the spectral copy of the sampled envelope signal falls at a frequency $\omega = 2\omega_C$, and $f_C = \frac{\omega_C}{2\pi}$, then the output of the mixer yields spectral components at frequencies ω_C and $3\omega_C$, being the result of mixing with the phase signal having fundamental frequency ω_C. This is illustrated by the example of two sinewaves having amplitudes E_1 and E_2 and frequencies ω_C and $2\omega_C$,

$$E_1 sin(\omega_C t)\, E_2 sin(2\omega_C t) = \frac{1}{2} E_1 E_2 \left[\underline{cos(\omega_C t)} - cos(3\omega_C t)\right] \tag{5.21}$$

Although the component at the frequency $3\omega_C$ can be easily removed from the output of the transmitter by a lowpass filter, the component at frequency ω_C causes distortion in the transmitter's output. In order to minimize this distortion, the sampling rate of the

envelope *LP*ΣΔ modulator must be chosen such that its output spectrum exhibits minimal quantization noise at the frequencies 0 and $2\omega_C$. A separate problem in a digitized polar transmitter is caused by a spectral copy of the sampled envelope signal, which usually occurs at the frequency $2\omega_C$. These two problems are discussed in the following sections.

5.3.2 Maximum sampling rate of the envelope *LP*ΣΔ modulator

In order to ensure that no quantization noise falls into the RF band at the frequency f_C, the NTF of the *LP*ΣΔ modulator must have zeros at both frequencies, $f = 0$ and $f = 2f_C$. The quantization error suppression at frequency $f = 0$ is usually ensured by placing a zero in the noise transfer function at $z = 1$. A practical way of achieving the suppression of the quantization error at frequency $2f_C$ is by ensuring that the sampling rate f_E of the *LP*ΣΔ modulator is related to the frequency $2f_C$ by a positive integer number M,

$$f_E = \frac{2f_C}{M},\ M = 1, 2, 3, 4, \ldots \tag{5.22}$$

When this condition is met, then the quantization noise is always suppressed at the frequency $2f_C$ due to replication of the NTF zero every frequency f_E. Examples of low pass noise transfer functions for $M = 1, 2,$ and 4 are drawn in Fig.5.16. Note that while all displayed noise transfer functions have at least one zero at frequencies $f = 0$ and $f = 2f_C$, the quantization noise suppression at the carrier $f = f_C$ frequency is not necessary. Example of a waveforms for a pulsed phase signal for different M values are shown in Fig.5.17.

It is observed that for the maximum sampling rate $f_E = 2f_C$, the output pulses are of duration equal to half of the period of carrier frequency. The number of periods during the single pulse increases as the sampling rate f_E decreases. In practice, any real mixer and *SMPA* is characterized by a finite bandwidth, and subsequently nonzero rise and fall times occur, as it is depicted in Fig.5.18. Due to these transients it is often practical to use a sampling rate for the envelope *LP*ΣΔ modulator several times lower than the carrier

frequency f_C, [23, 75] which compromises the in-band and adjacent channel quantization error power with power efficiency of the polar transmitter. The minimum value of M depends on the technology of a transmitter's implementation, and it is beyond the scope of this chapter.

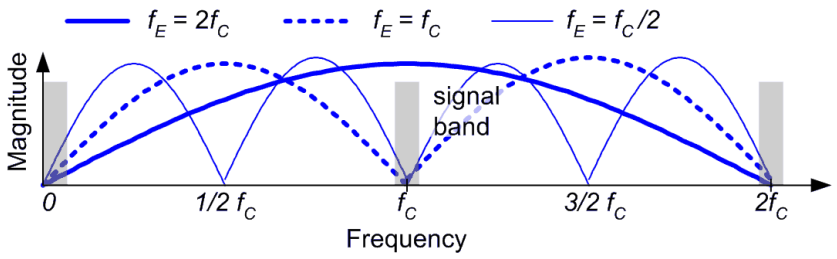

Figure 5.16: Low pass noise transfer functions with sampling rates described by (5.22).

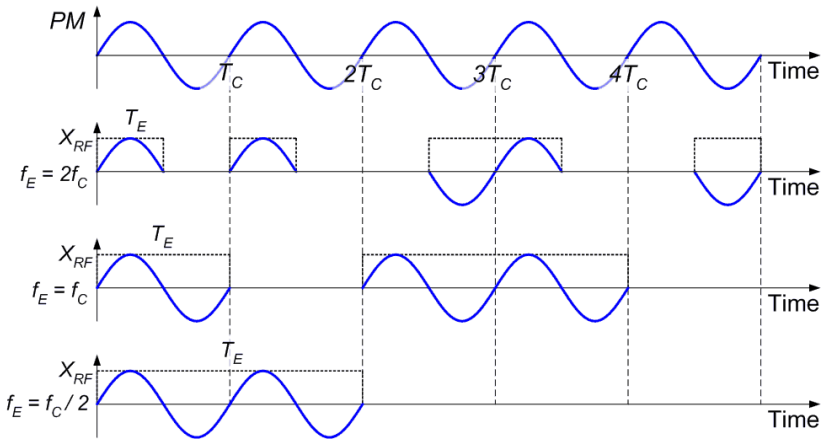

Figure 5.17: Mixer output waveforms for different envelope *LP*ΣΔ sampling rates.

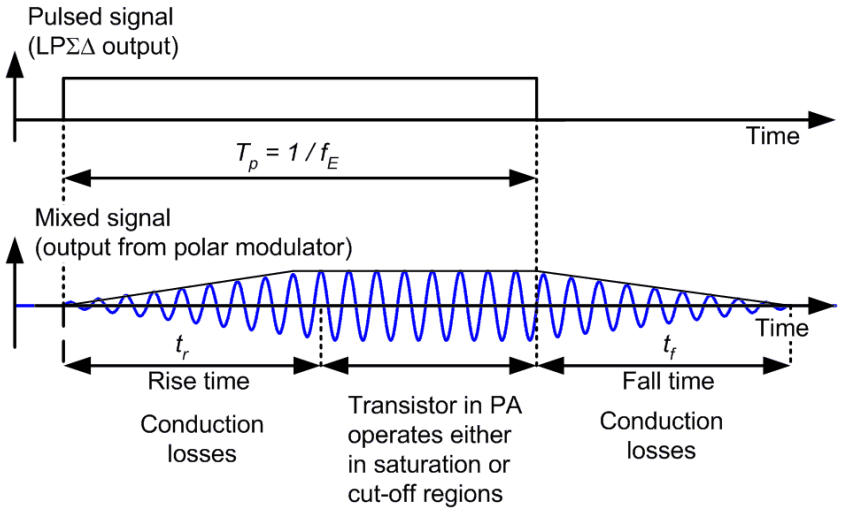

Figure 5.18: Pulse modulated phase with a finite rise and fall times.

5.3.3 Envelope aliasing

This section analyzes the aliasing effect in the *DPT*, assuming that sampling frequency f_E and carrier frequency f_C are related by equation (5.22). The analysis is based on an assumption of ideal, no return to zero $(NRZ)DAC$ in the envelope path, and zero rise and fall times in the output of the mixer. The aliasing effect is demonstrated for a three tone stimulation without a $LP\Sigma\Delta$ in the envelope path first, and it is followed by simulated results for a *DPT* employing 2-level, 3-level, 4-level and 6-level $LP\Sigma\Delta$ modulators and the bandlimited signal described in Section 5.2.2.

For power efficient operation of a switchmode power amplifier, the pulsed phase signal of Fig.5.18 should be characterized by very short rise and fall times in comparison with the pulse period T_E. When the *DAC* pulse has duration of $T_E = \frac{1}{f_E}$, and zero rise/fall times, then the pulse's Fourier transform is a *sinc* function,

$$G(f) = \frac{1}{T_E} sinc\left(\pi f / f_E\right) \tag{5.23}$$

Two observations are made at this stage; the Fourier transform $G(f)$ has a zero at frequency $2f_C$, which suppresses the envelope's alias $ENV(f-2f_C)$. Also, the suppressed alias magnitude is proportional to the RF bandwidth due to the shape of $|G(f)|$ in the proximity of the frequency $2f_C$ as seen in Fig.5.19. Let us relate the argument of the *sinc* function to the carrier frequency by substituting (5.22) in (5.23),

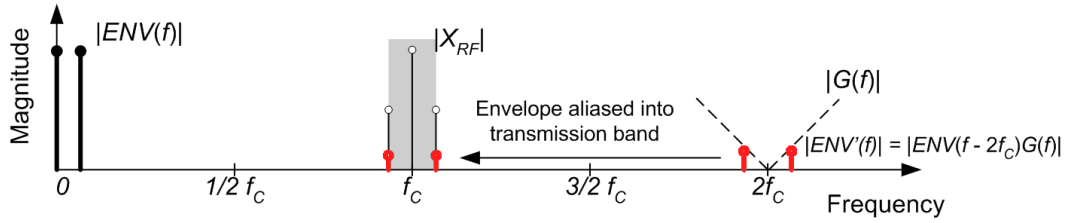

Figure 5.19: Spectral copy of an envelope signal falling at frequency $2f_C$.

$$G(f) = sinc\left(\frac{M\pi f}{2f_C}\right) \tag{5.24}$$

For an RF bandwidth denoted by BW the largest power aliased into the transmission band occurs at the edges of the RF band, i.e. at frequencies $f_C \pm BW/2$. Since $|G(2f_C + BW/2)| \approx |G(2f_C - BW/2)|$ when $BW \ll 2f_C$, we can limit the analysis to the single frequency, e.g. $2f_C + BW/2$. Now the minimum suppression of the alias $ENV(f - 2f_C)$ becomes,

$$|G(2f_C + BW/2)| = \left| sinc\left(M\pi\left(1 + \frac{BW}{4f_C}\right)\right)\right| \tag{5.25}$$

It is observed that the magnitude of $G(f)$ shows negligible dependence of M for $f_C - BW/2 \leqslant f \leqslant f_C + BW/2$ when $BW \ll 2f_C$. It follows that the distortion caused by the aliasing depends of the RF bandwidth BW and carrier frequency f_C when the sampling rate is defined by (5.22), but it does not depend on ΣΔ sampling frequency f_E. Since $\frac{dG(f)}{df} \approx const$ in the proximity of frequency $2f_C$, i.e. the $|G(f)|$ decrement towards $2f_C$ is nearly constant as seen in Fig.5.19. Basing on the above it is concluded, that for a bandlimited signal having an uniform distribution of power across its bandwidth, a $6dB$ of the aliased signal power increase per every doubling of the BW is expected.

5.3.3.1 Three tone input signal

This section uses a three tone, double sideband amplitude modulated signal (DSB-AM) to demonstrate the effect of aliasing on the output of the DPT. The $DSB - AM$ signal is described by equation (5.26). Subsequently, this signal is decomposed into envelope and phase components given by (5.27). The $DSB - AM$ signal described below has phase and envelope components characterized by finite bandwidths which simplifies the following analysis, while still providing an insight into the aliasing mechanism in the DPT. Fig.5.20 shows the time domain waveform of the three tone $DSB - AM$ signal.

$$X_{RF}(t) = [sin(\omega_1 t) + 1]\, sin(\omega_C t) \tag{5.26}$$

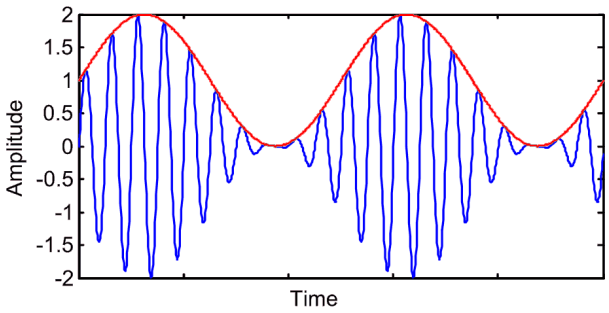

Figure 5.20: Three tone DSB-AM signal.

$$\begin{aligned} ENV(t) &= [sin(\omega_1 t) + 1] \\ PHA(t) &= sin(\omega_C t) \end{aligned} \tag{5.27}$$

Let us assume that the envelope signal is sampled at a rate $f_E = 2f_C$ (or lower defined by (5.22)), and the quantizer is multibit such that the quantization noise power is negligible. The signal is next passed through a digital to analog converter responding to input samples with a square pulse characterized by zero rise and fall times. All envelope's spectral replicas apart from the image at frequency $2f_C$ are neglected as having no impact on the RF band. In consequence the sampled envelope signal simplifies to the baseband portion and the replica at frequency $2f_C$,

$$ENV_D(t) = ENV(t) + h_1 sin(2\omega_C t - \omega_1 t) + h_2 sin(2\omega_C t + \omega_1 t) \tag{5.28}$$

where h_1, h_2 denote magnitude of the $G(f)$ function at frequencies $2f_C \pm f_1$. The RF bandwidth can be defined as $BW = 2f_1 = \frac{\omega_1}{\pi}$,

$$|h_1| \approx \left| sinc\left(\pi\left(1 - \frac{f_1}{2f_C}\right)\right)\right| = \left| sinc\left(\pi\left(1 - \frac{BW}{4f_C}\right)\right)\right| \tag{5.29}$$

$$|h_2| \approx \left| sinc\left(\pi\left(1 + \frac{f_1}{2f_C}\right)\right)\right| = \left| sinc\left(\pi\left(1 + \frac{BW}{4f_C}\right)\right)\right| \tag{5.30}$$

After mixing the sampled envelope (5.28) with the phase signal (5.27) the output becomes,

$$\begin{aligned} X_{RF-DT}(t) = &\left\{\tfrac{1}{2}[cos(\omega_C t - \omega_1 t) - cos(\omega_C t + \omega_1 t)] + sin(\omega_C t)\right\}_{X_{RF}} + \\ &+\tfrac{1}{2}\left\{-h_1 cos(\omega_C t - \omega_1 t) + h_2 cos(\omega_C t + \omega_1 t)\right\}_{DIST} \end{aligned} \tag{5.31}$$

Note that the modulation products at frequency $3f_C$ are neglected in (5.31). The first term in the curly brackets denotes the transmitted signal, while the second pair of curly brackets encloses the distortion. The magnitude of distortion products at frequencies $f_C - f_1$ and $f_C + f_1$ are calculated below the magnitude of transmitted tones at the same frequencies from (5.29) and (5.30). The results are listed in Tab.5.2 as a function of signal bandwidth $BW = 2f_1$ and carrier frequency f_C. The values of $h_{1/2}$ in Tab.5.2 indicate a power ratio of signal tones to the aliased tones. Also, h_1, h_2 are calculated at the edges of transmission band, where the aliased elements have largest magnitudes. The values in Tab.5.2 could be thus used for predicting distortion in a *DPT*, giving some initial estimation of the distortion range caused by the sampling of the envelope signal. Clearly, this distortion does not depend on the quantization noise induced by a ΣΔ modulator only, which is the case of a Class-S amplifier.

Table 5.2: Distortion in digitized polar modulator's output spectrum.

BW/f_C	$\lvert h_{1/2} \rvert$ (dB)
$1/1000$	-72
$2.5/1000$	-64.1
$5/1000$	-58.1
$10/1000$	-52.1
$20/1000$	-46
$40/1000$	-40
$60/1000$	-36

5.3.3.2 Aliasing in the ΣΔ digitized polar modulator

The aliasing effect can be observed when comparing performance of *DPT* with and without envelope images cancellation.

Given a sampled, but not quantized envelope signal ENV_S, and a continuous time envelope signal ENV, the spectral copies of the sampled envelope signal can be computed by subtracting the two signals,

$$ENV''(t) = ENV_S(t) - ENV(t) \tag{5.32}$$

Subsequently the images cancellation in the digitized envelope signal E_D is obtained by subtracting the ENV'' signal,

$$ENV_C(t) = ENV_D(t) - ENV''(t) \tag{5.33}$$

Note that while equation (5.32) yields image-canceled digitized envelope signal ENV_C, it does not affect the quantization error induced by a $LP\Sigma\Delta$ modulator. The use of (5.33) allows for calculation of SNR as a function of a $LP\Sigma\Delta$ sampling rate only in a DPT.

Fig.5.21 shows a simulated SNR in the output from digitized polar transmitter with and without the image cancellation. The increase of the sampling rate improves SNR when image-canceled envelope signal is used in the polar transmitter. In contrast, the SNR deterioration is observed in the output of the DPT without image cancellation.

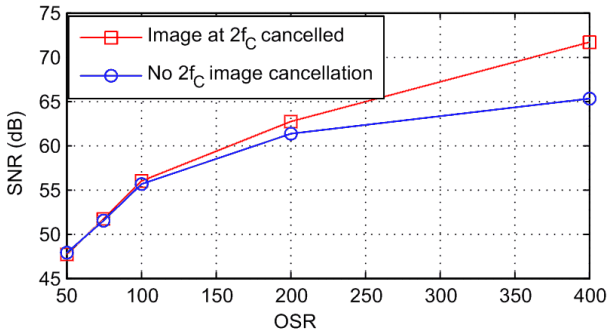

Figure 5.21: The aliasing effect on SNR in digitized polar transmitter, $BW/f_C = 2.5/1000$.

Although the described cancellation technique can be easily applied in the course of simulation, it would be impractical to use it in a real circuit of DPT. The described above subtraction would lead to the operation on a signal whose frequency was two times higher that the carrier frequency f_C. If the image cancellation is needed for improving SNR of DPT, a predistorting signals should be added to baseband I and Q signals instead.

5.3.4 Envelope ΣΔ modulation

While input signals to ΣΔ modulators have typically probability density functions (*PDF*) being even functions, example of which can be multicarrier signals, this property does not always apply to *PDF* of envelope signals.

A 2-level ΣΔ modulator whose input signal's amplitude approaches or exceeds quantizer's full scale range is at a risk becoming unstable. The stable operation is maintained by scaling an input signal such as depicted in the example a baseband signal's *PDF* in Fig.5.22. As a result of the scaling, the input signal's amplitude remains in a stable operation range of the ΣΔ modulator. The situation is different in the case of an envelope signal having Rayleigh-distribution. Such signal is supplied to the input of a 2-level, *LP*ΣΔ modulator in the *DPT*. The lower quantizer level in the 2-level *LP*ΣΔ modulator is zero, which is also the minimum value of the envelope signal. Scaling of such an input prevents from overloading the *LP*ΣΔ modulator by large input values, but on the other hand it also increases the probability of zero input amplitude which is depicted in Fig.5.22. The scaling of the envelope signal therefore does not entirely solve the stability problem of the *LP*ΣΔ modulator in the *DPT*.

A simple remedy to the low input amplitude in the input to *LP*ΣΔ modulator would be to offset the envelope signal by some constant value. An addition of a constant a in (5.34) to the *LP*ΣΔ modulator input signal will shift the minimum envelope amplitude away from zero improving modulator's stability. Unfortunately, such operation will also result in the addition of a phase signal and in a subsequent increase of noise power in adjacent channels of the transmitted signal.

$$X_{RF-offset}(t) = (ENV(t) + a)\,PHA(t) = X_{RF}(t) + aPHA(t) \tag{5.34}$$

A Matlab experiment with the envelope of the input signal X_{IN} showed that among simulated, modulators of first and second order only maintained stable operation. Conse-

quently, the *SNR* in *DPT* with first and second order ΣΔ modulators only is investigated in the following section.

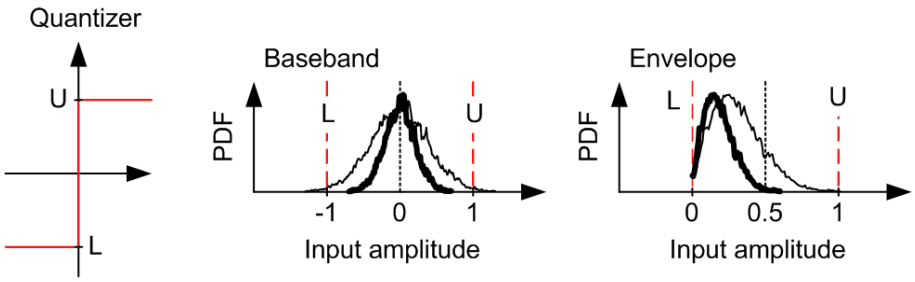

Figure 5.22: PDF of a baseband signal *I* and the envelope signal with two different scaling factors.

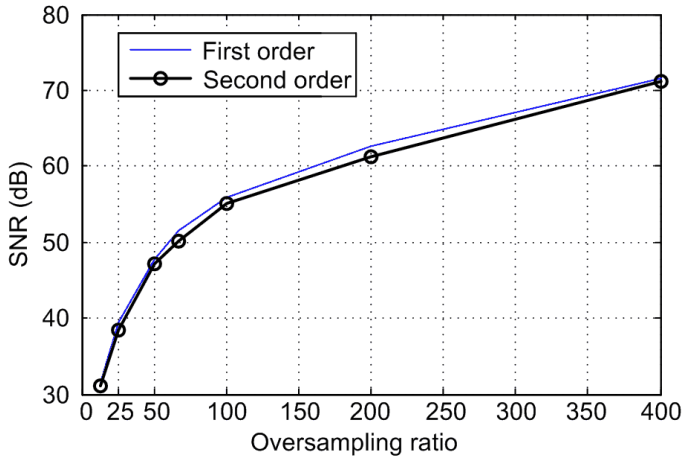

Figure 5.23: Signal to noise ratio comparison for digitized polar modulator employing first and second order *LP*ΣΔ modulators.

5.3.4.1 First and second order ΣΔ

The polar transmitter has been simulated with 2-level *LP*ΣΔ modulator of first and second order. The *LP*ΣΔ modulator was supplied with envelope of the $12dB$ *PAPR* signal X_{IN}. In the course of simulation, *LP*ΣΔ modulator's sampling rate was varied by changing value of $'m'$ in (5.22). The calculated *SNR* is expressed as a function of an oversampling ratio related to the bandwidth of the input signal X_{IN}, $OSR = \frac{f_E}{2BW}$. Both, first and second order *LP*ΣΔ modulators were characterized by unity signal transfer function. The noise transfer function of first order modulator was $NTF_{1st} = 1 - z^{-1}$. The numerator of second order noise transfer function was $NTF_{N-2nd}\left(1 - z^{-1}\right)^2$ with a maximum gain

of $|NTF(z=1)=1.5|$. The 2nd order modulator's structure used was *CIFB* shown in Fig.3.3(B), with coefficients listed in Tab.2.3. Both *LP*ΣΔ modulators yielded similar signal to noise ratios with little advantage of first order modulator as seen in Fig.5.23, which proved better stability in a presence of input signal reaching low valued amplitudes. Since there was no significant difference between signal to noise ratios, the first order *LP*ΣΔ modulator is chosen for the digitized polar modulator studied in this chapter.

5.3.4.2 Two level and multilevel *LP*ΣΔ modulator

Although the use of a multilevel quantizer in the *LP*ΣΔ modulator of *DTP* increases design challenges, the reduction of quantization error power in the output spectrum and subsequent *SNR* improvement is worth consideration.

In contrast with a two level, a digitized multilevel envelope signal cannot be encoded into the drive signal of switchmode power amplifier, and the envelope amplifier is needed in the polar transmitter which is depicted in Fig.5.24(B).

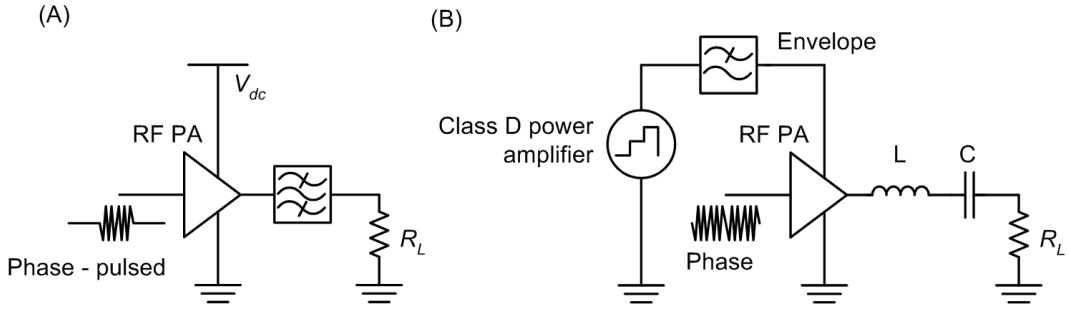

Figure 5.24: (A) DPT employing 2-level ΣΔ modulator. (B) DPT employing multilevel ΣΔ modulator.

The multilevel operation increases complexity and brings the linearity problem of output amplitude versus supply voltage. Apart from the quoted drawbacks, the multilevel *LP*ΣΔ modulation offers also some advantages. The digitized two level or multilevel envelope signal is low pass filtered prior to supplying it to the *RF* power amplifier, as it is depicted in Fig.5.24(B), which eliminates the need for a narrowband, low-insertion loss band pass filter of the scheme in Fig.5.24(A). Also, the low pass filtering eliminates the

envelope aliases described in Section 5.3.3.

In order to compare the *SNR* performance of a polar modulator, simulations with 2-level and multilevel quantizers were performed, and their results are shown in Fig.5.25. The simulations assumed a linearity of the RF SMPA's output amplitude as a function of supply voltage. The improvement of signal to noise ratio is observed as the number of levels increases. The increase from a 2 level to 3, 4 and 6 level quantization resulted in an average $7dB$, $10.8dB$ and $16.3dB$ of *SNR* improvement. The calculations of *SNR* were done for transmitter with and without the envelope's image cancellation. The dashed lines indicate the *SNR* calculated without the envelope's image cancellation.

As predicted in the previous sections, apart from a sampling rate and a number of quantizer levels, the maximum *SNR* in the output of a modulator also depends on the ratio of a signal bandwidth to carrier frequency. It is observed that the digitized polar transmitter without the envelope's image cancellation can deliver maximum of *SNR* of $67dB$ at the bandwidth-to-carrier ratio $BW/f_C = 2.5/1000$. The maximum value of the

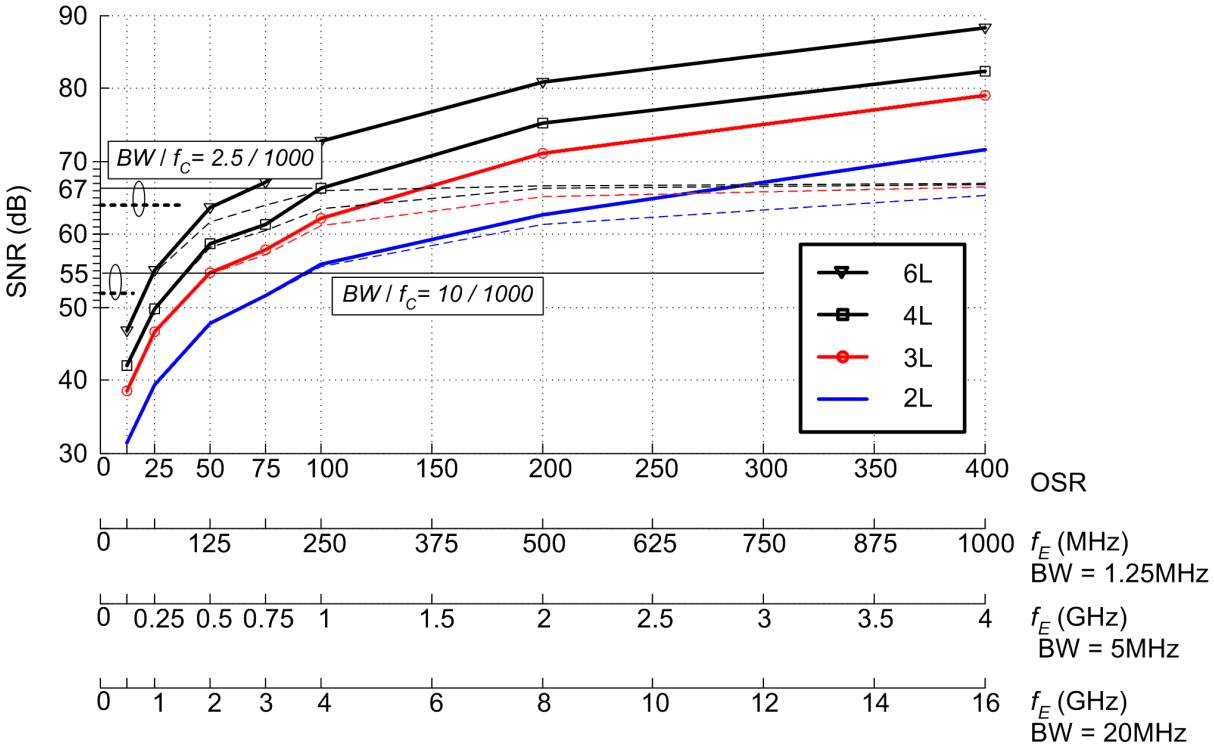

Figure 5.25: *SNR* comparison for 2, 3, 4 and 6 level *LP*ΣΔ modulators.

signal to noise ratio is regardless of oversampling ratio or number of quantizer levels, which clearly shows the influence of the aliasing. The simulated *SNR* at bandwidth-to-carrier ratio of $BW/f_C = 2.5/1000$ can be used to predict maximum achievable *SNR* in digitized polar transmitter. The maximum *SNR* becomes worse as the ratio of BW/f_C increases. The simulation for $BW/f_C = 10/1000$ resulted in the maximum achieved signal to noise ratio of $SNR = 53dB$. The two simulated limits of maximum *SNR* in a *DPT* are in close agreement with the predicted values listed in Tab.5.2. The simulated *SNR* are approximately $3dB$ higher than the predicted values. The calculated values can be used for an initial estimation of a maximum achievable signal to noise ratio in a *DPT*.

5.3.5 Conclusion

This section analyzed the effect of digitization of the envelope signal by the *LP*ΣΔ modulator in a polar transmitter. The use of a 2-level *LP*ΣΔ modulator in a polar transmitter allows for the use of a single, nonlinear RF PA, which simplifies the *EER* transmitter, but it also generates problems. The quantization of the envelope signal affects *SNR* and requires wideband operation of the *RF PA*. As demonstrated, the improvement of *SNR* in the *DPT* output is not only a function of *LP*ΣΔ modulator sampling rate, but it also depends on the bandwidth to carrier ratio due to the aliasing effect.

5.4 Comparison of Class-S amplifier and *DPT*

Class-S amplifier and the *DPT* have been introduced and discussed. The two amplifier systems use ΣΔ modulators for encoding the RF signal, which creates similarities in terms of the quantization noise shaping in their outputs and broadband operation of the amplifiers. Because the RF signals are created differently, there is a difference between the maximum output power delivered by these two systems, which is discussed in this

section.

The coding efficiency of a *BP*ΣΔ modulator in Class-S amplifier depends on the input signal, the ratio of carrier frequency to the sampling frequency of the modulator and on the stable input range of the *BP*ΣΔ. Despite the large variety of possible configurations in both, *DPT* and Class-S amplifier, the following comparison is narrowed to a single case, in which both amplifiers can drive the same switchmode power amplifier operating in Class-D. The purpose of this comparison is therefore to show the difference between how the RF signals are created in both systems, rather than carry out an extensive analysis.

Let us chose a first order *LP*ΣΔ modulator characterized by $NTF = 1 - z^{-1}$ for the *DPT*, and its $z \rightarrow -z^{-2}$ transformation for Class-S amplifier. Few observations can be made at this point. A *BP*ΣΔ modulator having center frequency $f_C = \frac{f_{\Sigma\Delta}}{4}$, and zero/pole locus symmetric across imaginary axis in the complex plane, can be considered as a transformation $z \rightarrow -z^{-2}$ of a *LP*ΣΔ modulator. Consequently, the *LP*ΣΔ or its bandpass transformation will exhibit the same discrete coding efficiency, when the input to the *BP*ΣΔ modulator is the same as the input to the *LP*ΣΔ shifted in the frequency domain by $\frac{1}{4}f_{\Sigma\Delta}$. Secondly both, *LP*ΣΔ and *BP*ΣΔ modulator with $f_0 = \frac{1}{4}f_{\Sigma\Delta}$ may exhibit lower discrete time coding efficiency than *BP*ΣΔ modulators with $0 < f_0 < \frac{1}{4}f_{\Sigma\Delta}$. The reduced stable input range of a fifth order *LP*ΣΔ modulator was observed by Schreier [97], while Johnson observed a dip in a coding efficiency of a fourth order *BP*ΣΔ modulator at $f_0 = \frac{1}{4}f_{\Sigma\Delta}$ [28]. This reduction of coding efficiency in a higher order *LP*ΣΔ modulator arises from a slowly changing input, whose amplitude approaches and remains at the boundary of the modulator's stable range operation. The above aspect of coding efficiency however concerns higher order modulators, and it is beyond the discussion carried out it this section, whose main focus is on differences in signal processing in the two types of transmitters using first order ΣΔ modulators.

Let us consider a *BP*ΣΔ modulator in Class-S amplifier, being stable over a full scale

range of a quantizer and having a carrier frequency $f_C = f_{\Sigma\Delta}/4$. Consequently the peak output power becomes $P_{P-S} = 0.81 \cdot A^2$, where A denotes quantizer upper or lower level as was explained Section 2.3.7.2. Also, let us assume that the phase signal in a *DPT* is a square-waveform, which is needed for switchmode operation. The first harmonic for a 50 % duty ratio waveform has the amplitude of $Amp_1 = \frac{4}{\pi}$. When the $1\,bit$ *DAC* in the output of the envelope *LP*ΣΔ modulator has the ideal square pulse response of amplitude A and zero rise/fall times, then the magnitude response of the *DAC* is unity at a zero frequency. Provided that $A = 1$ and the ΣΔ maintains stable operation for full scale range input, i.e. $0 \leqslant ENV \leqslant A$, then the peak power in the output of the modulator for the *DPT* becomes $P_{P-DPT} = 1.62 \cdot A^2$, which is two times higher than the output power from a Class-S power amplifier. Moreover, when the carrier frequency is related to sampling frequency of the *LP*ΣΔ modulator in the *DPT* by the integer number M, i.e.,

$$f_C = \frac{M f_E}{2}$$

then the 3-level waveform can be converted to a 2-level waveform and used to drive Class-D power amplifier. Fig.5.26 shows the *DPT* and Class-S driving the same Class-D PA. The Class-S amplifier uses carrier frequency $f_C = f_{\Sigma\Delta}/4$, and the input gain block for compensating for the $3\,dB$ of the output power difference to the digitized polar transmitter's output. In order to compare these two systems, a simulation is performed using first order ΣΔ modulators.

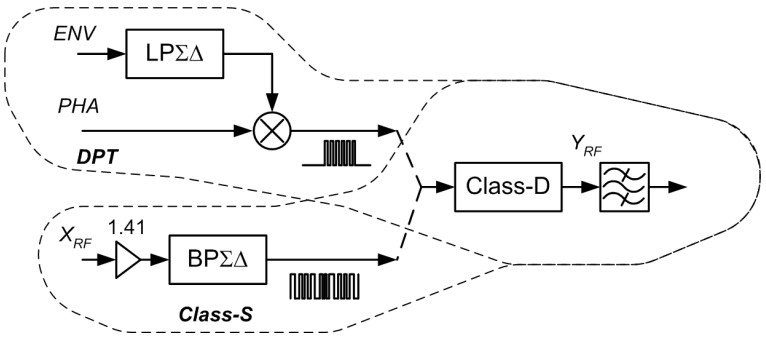

Figure 5.26: Class-S and polar transmitter with digitized envelope signal.

The *LP*ΣΔ modulator in the *DPT* had a sampling rate $f_E = f_C$ and the *BP*ΣΔ modulator used two times higher frequency $f_{\Sigma\Delta} = 2f_C$. The lower frequency for the *LP*ΣΔ modulator was chosen since its input signal bandwidth was equivalent to half of the RF band. Consequently both systems used the same oversampling ratio, $OSR = 50$. The input RF signal was an $8-tone$ signal, and both discrete time outputs were up-sampled to simulate continuous time waveforms. The resulting *SNR* in the output of both systems are displayed in Fig.5.27.

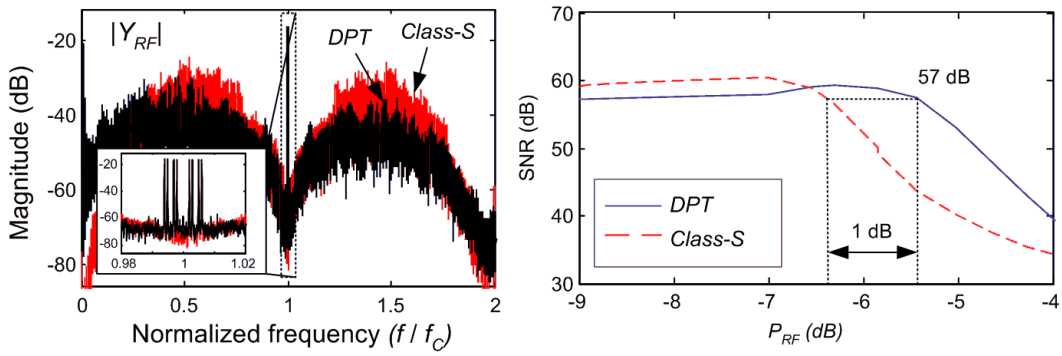

Figure 5.27: SNR comparison for Class-S and polar transmitter with digitized envelope signal.

It is observed that the *DPT* exhibits approximately $1\,dB$ lower *SNR* at low input signal amplitudes. This can be explained by the different PDF functions of the input signals to the *BP*ΣΔ and *LP*ΣΔ modulators discussed in Section 5.3.4. The *SNR* degradation in the *DPT* is caused by input amplitudes approaching lower quantizer level, which is regardless of the RF amplitude. On the other hand, the *DPT* was capable of delivering a $1\,dB$ more of the output power than equivalent Class-S amplifier while maintaining $57\,dB$ of the *SNR*. The $3\,dB$ of the output power advantage estimated earlier was reduced to approximately $1\,dB$ due to a lower stable range of a *LP*ΣΔ modulator supplied with the input envelope signal. The $1\,dB$ in the output power difference however indicates higher power efficiency of a *DPT* than a Class-S amplifier, provided that both systems dissipate the same power due to driving the *SMPA*, switching and conduction losses.

5.5 Proposed polar modulator

This section describes the concept of a signal modulator for *DPT* with reduced analog signal processing in comparison to conventional modulator schemes. The hardware reduction on the analog side is achieved at the cost of moving some of the operations in the phase path from analog to digital domain. The advantage of this modification is increased reconfigurability of the modified polar transmitter.

5.5.1 Phase signal

A scheme of conventional modulator for *DPT* was presented in Section 5.1 in Fig.5.4. The proposed modulator performs the same signal processing steps as the conventional modulator, except of synthesizing the phase signal. The major difference between the conventional, and the proposed modulator is that the quadrature mixing section responsible for synthesizing phase signal is implemented in a DSP (*FPGA*), instead of using analog quadrature mixer. The use of *FPGA* for synthesizing phase signal increases reconfigurability of the proposed modulator and reduces signal processing in analog part of the modulator.

In theory, a signal processing needed for generating the phase signal could be implemented directly in an *FPGA* and provided to an output through a fast, 1-bit serial register. To achieve this however, the sampling rate of the register must be many times higher than a carrier frequency of the transmitted signal, which is often beyond a reach in the available hardware. Due to the discretization of the time step, the direct approach is similar to a 2-level quantization described in Section 2.3, and it results in an addition of an error signal. To visualize this, let the phase signal be represented by a 2-level waveform of amplitude A, a period $T_C = 1/f_C$, and the sampling step of the 1-bit register be $T_S = 1/f_S$. The subsequent addition of a phase error occurs in a result of applying a finite time step

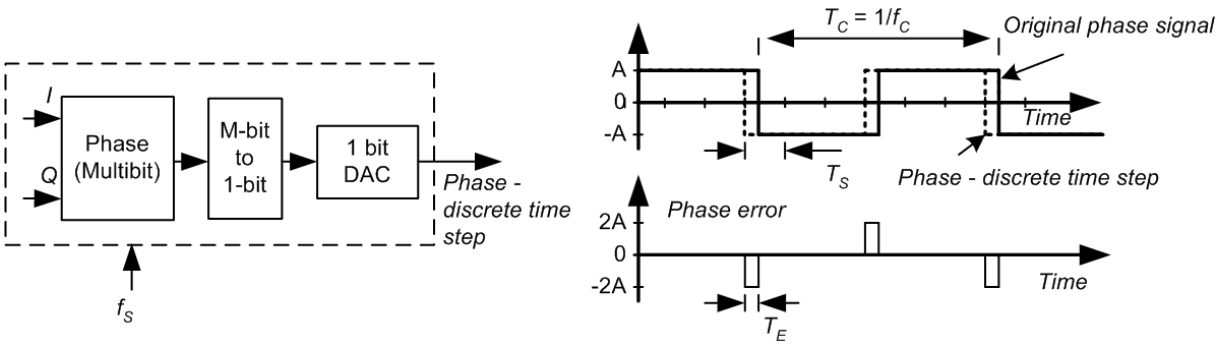

Figure 5.28: Phase error.

as depicted in Fig.5.28. The error pulse of amplitude $2A$ and a maximum duration of $T_S/2$ occurs every time the phase changes its sign, i.e. two times per every period T_C. By making similar assumptions as in Section 2.3 for a linear quantizer model, i.e. the time offset T_E has properties of white noise and its distribution between $\langle -T_S/2; T_S/2 \rangle$ is uniform, we find that the absolute deviation of the time from the zero crossing of the original phase signal is $\overline{T_E} = \frac{1}{4}T_S$, which is the same as duration of the corresponding error pulse. Consequently, the average power of the phase error can be calculated as

$$e^2_{PHA} = (2A)^2 \frac{2\overline{T_E}}{T_C} = 2A^2 \frac{T_S}{T_C} \tag{5.35}$$

Because the phase error is not distributed uniformly between frequencies $-f_S/2; f_S/2$, but its power concentrates at the carrier frequency f_C, the inband error power is higher than for the uniform distribution described by (2.15). Consequently, the maximum SNR of the quantized phase signal can be estimated as the ratio of the phase to the inband error power calculated for the uniform distribution,

$$SNR < \frac{A^2}{e^2_{PHA-INB}} = \frac{OSR}{2} \frac{T_C}{T_S} \tag{5.36}$$

Using the above expression for calculating the SNR, we find that the direct technique requires very high oversampling ratio to achieve satisfying results. For instance, when generating a phase signal at a carrier frequency in Band 1, $f_C = 2140\,MHz$ and,

$BW = 5\,MHz$ ($BW_{PHA} = 50\,MHz$ according to (5.14)), with the minimum sampling step of $T_S = 1/6.6\,GHz$ (the same as in GTX transceiver of Virtex 6 $FPGA$ [4]), we obtain poor signal to noise ratio, $SNR < 21\,dB$.

An alternative, and promising technique for a DPT is when the ΣΔ-digitized envelope signal is aligned with a phase signal, as described in [76]. The use of a phase signal as a clock for the modulator ensures that transitions in an RF $SMPA$ occur at the same time instants as the transitions of the digitized envelope signal. Such approach allows for avoiding amplification of very short phase pulses which may occur otherwise as shown in Fig.5.29(A, B), and which may lead to less efficient PA operation. This technique may also enable minimizing the demonstrated in Fig.5.28 phase error pulses, if an external phase source connects to a delay-locked loop (DLL) in a digital hardware. Although such approach is impractical for RF signals due to their clock frequency limitation, it may yield a valid solution in future.

An approach where advantage of digitally implemented ΣΔ modulators for generating phase signal, enabling an analog hardware reduction is presented in the next section.

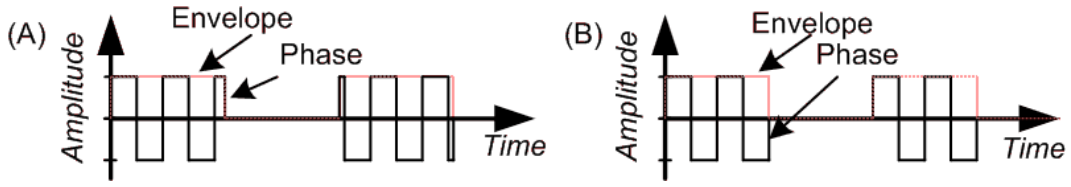

Figure 5.29: Polar modulator outputs. (A) Fixed sampling rate of the envelope ΣΔ modulator. (B) Phase signal used as a clock for the ΣΔ modulator.

5.5.2 Modulator with ΣΔ-digitized phase signal

The proposed modulator's scheme is shown in Fig.5.30. A digital signal processor in the proposed modulator calculates envelope (5.2), and phase signals (5.4) in a similar fashion as it is done by the conventional modulator. The process of synthesizing of the phase signal is however different.

The phase signal components in the modified modulator, I' and Q' undergo binary $LP\Sigma\Delta$ modulation. Once the two signals are encoded into binary signals, a quadrature mixing simplifies to inversion and time interleaving operation on binary sequences I'_d and Q'_d, and is implemented as a digital quadrature mixer (DQM) in a DSP. The DQM is followed by an additional mixer for shifting the phase spectrum at a desired carrier frequency. Subsequently, the binary, phase signal is digital-to analog converted. In the last step of phase synthesis, quantization noise induced by $LP\Sigma\Delta$ modulators is attenuated by an analog band pass filter. The envelope and the phase signal are mixed in the same way as is done in the conventional polar modulator. At the cost of moving some of the signal processing into $FPGA$, the analog operations in the phase path reduce to a filtering of a quantization error induced by $LP\Sigma\Delta$ modulators, avoiding the need for multibit digital-to-analog converters and a quadrature mixer in the conventional modulator scheme. The detailed description of the modulator, including required sampling rates of $LP\Sigma\Delta$ modulators, maximum bandwidth of an input signal and a performance trade-offs are provided in following sections.

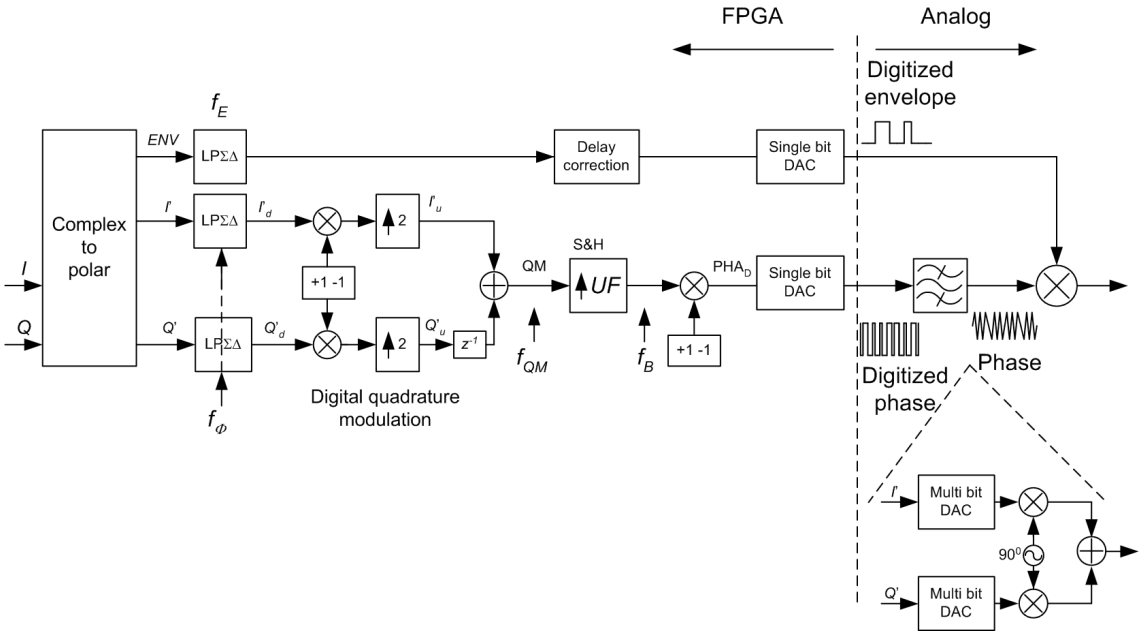

Figure 5.30: Proposed polar modulator.

5.5.3 Sampling rate of phase $LP\Sigma\Delta$ modulators

A phase passband and a phase noise are factors that affect the quality of the output signal of a polar transmitter. Since in the proposed scheme the digital to analog conversion of a phase signal is executed with the use of $LP\Sigma\Delta$ modulators, large sampling rate should be provided in order to minimize quantization noise falling into the signal band of a transmitted signal. The effect of quantization noise addition is observed in Fig.5.31, showing results of simulation of digitized phase component I' ($BW_I = 2.5MHz$) at different sampling rates of the $\Sigma\Delta$ modulator. In order to maximize OSR of the $LP\Sigma\Delta$ modulators in the phase path, the concept of parallel $\Sigma\Delta$ modulator described in Chapter 3 of this work is employed. A Virtex 6 $FPGA$ of Xilinx is used to implement digital part of the DPT. The upper limit of achieved sampling rate of the first order $LP\Sigma\Delta$ modulator was in a range of $f_S = 856MHz$. Consequently, the maximum sampling rate of the phase $LP\Sigma\Delta$ pair is,

$$f_{\phi_{MAX}} = 856MHz \tag{5.37}$$

A first order, 2-level $\Sigma\Delta$ modulator achieves a maximum SNR of approximately $38dB$ when an oversampling ratio of 16 is provided according to empirical results in [69]. The EVM for such SNR is in a range of 1.3%. Choosing this oversampling ratio value as a minimum for phase $LP\Sigma\Delta$ modulators, a maximum allowed signal's bandwidth is calculated as a function of a phase passband defined in Section 5.2.4 by (5.14), yielding

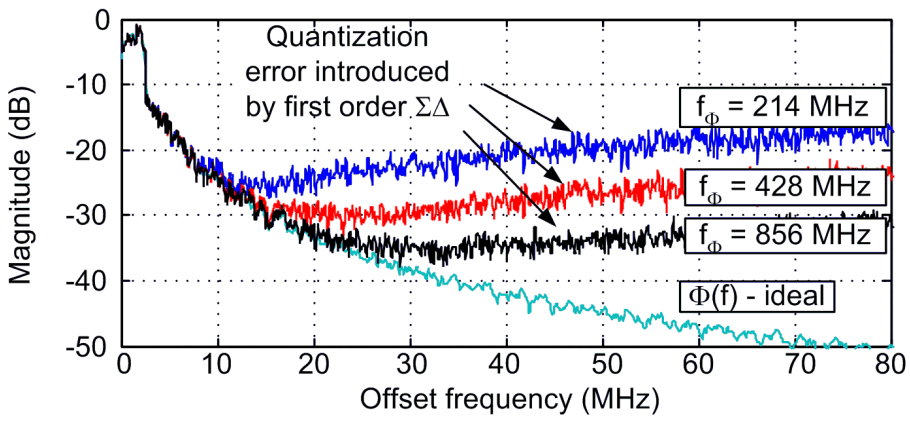

Figure 5.31: The effect of quantization on phase spectrum.

$BW_{MAX} \leqslant \frac{f_{\phi_{MAX}}}{10 \cdot OSR} = 5.35MHz$. Although the bandwidths of telecommunication signals already reach up to $20MHz$ in LTE and up to $100MHz$ in LTE Advanced, new generations of $FPGA$ are emerging every year allowing for higher sampling rates. The quoted bandwidth limitation of $5.35MHz$ should therefore be associated with this particular modulator's implementation only.

5.5.4 Bit rate of digitized phase signal

The concept of digital quadrature mixing for the phase path is based upon the assumption that the $DQM's$ sampling rate is four times higher than its output carrier frequency. Denoting the carrier frequency of DQM as f_C, the output is described by,

$$QM = I_d^{'} cos(2\pi f_C t) + Q_d^{'} sin(2\pi f_C t) \mid_{f_B = 4f_C} \tag{5.38}$$

While the values of transmitting frequency in $UMTS$ range from several hundred megahertz to over three gigahertz, the direct use of equation (5.38) requires serial buffer in the $FPGA$ operating at a bit rate four times higher than the carrier frequency. The maximum sampling rate of the serial buffer in Virtex 6 $FPGA$ boards is $f_{B_{MAX}} = 6.6Gb/s$ [4] which limits the carrier frequency from DQM to $f_C = \frac{f_{B_{MAX}}}{4} = 1.65GHz$. In order to utilize higher carrier frequency, the up converting and mixing block is added in the digitized phase path of Fig.5.30. Such an approach facilitates increasing the maximum achievable carrier frequency by placing it near to half, instead of one fourth of the output buffer's sampling frequency f_B. Implications from the use of a second mixing block are discussed in next two sections.

5.5.4.1 Carrier frequency

The digital quadrature mixing of the $LP\Sigma\Delta$ modulated phase components in the proposed polar modulator is similar to the parallel $BP\Sigma\Delta$ modulation scheme described in Chapter

3 of this work. The $LP\Sigma\Delta$ modulators followed by pair of mixers have the baseband components of a phase transferred to half of the $LP\Sigma\Delta$ modulators sampling frequency $f_\phi/2$. The two mixed signals are next up-sampled by a factor of two and added. The 90° phase shift between $I_d^{'}$ and $Q_d^{'}$ of the quadrature mixer is realized by inserting a delay in a $Q_d^{'}$ path as depicted in Fig.5.30. The addition of the two signals creates digitized phase signal described by (5.38) at intermediate carrier frequency denoted by f_{IM},

$$QM = I_d^{'} cos\left(2\pi f_{IM} t\right) + Q_d^{'} sin\left(2\pi f_{IM} t\right) \tag{5.39}$$

The intermediate carrier frequency f_{IM} is related to sampling rates of $LP\Sigma\Delta$ modulator and DQM by,

$$f_{IM} = \frac{f_\phi}{2} = \frac{f_{QM}}{4} \tag{5.40}$$

The second up-conversion repeats the input sample increasing the sampling rate to f_B,

$$f_B = UF \cdot f_{QM} = UF \cdot 2 \cdot f_\phi \tag{5.41}$$

The subsequent mixing allows to utilize one of the two phase images at frequency either above or below half of the output sampling rate f_B.

$$f_L = \frac{f_B}{2} - f_{IM} \tag{5.42}$$

$$f_U = \frac{f_B}{2} + f_{IM} \tag{5.43}$$

When the DQM is followed by the second mixing block, the carrier frequency can be either f_L or f_U. Additionally, the carrier frequency is a function of f_ϕ, and UF factor. While several configurations for providing a desired carrier frequency is possible, three most practical ones for $f_C = 2.14GHz$ are discussed in the Section 5.5.4.2.

5.5.4.2 Amplitude of the phase signal

The pulsed phase signal from the polar modulator, after an initial amplification, drives a transistor in a SMPA. Consequently, the output signal from the polar modulator must be amplified by a broadband driver in order to deliver sufficient power level to the transistor gate. Since the phase signal from the proposed polar modulator is extracted from a high-speed FPGA buffer, the power level of the phase signal is expected to be low. Approximately $-20dBm$ of output signal power was measured in the output from $FPGA$ board after band pass filtering. In order to deliver drive signal power of e.g.$10dBm$ needed for NPTB00004 GaN device, at least $30dB$ of gain is necessary. It becomes important that power of the phase signal from the polar modulator is possibly large. The power level extracted from an output of a $BP\Sigma\Delta$ modulator depends on the sampling frequency and on the carrier frequency [26, 28]. The output sampling frequency in the implemented modulator must be less than $6.6GHz$, as limited by the Virtex 6 FPGA platform used.

In the direct approach, the up-conversion block is bypassed in the scheme of Fig.5.30, and the digitized phase signal is supplied from the DQM directly. For simplicity when calculating phase's amplitude, it is assumed that digitized phase signal has amplitude $A_{DT} = 1$. The Fourier transform of DAC pulse $g_1(t)$ shown in Fig.5.32(A, C) causes attenuation of the phase signal by $-0.82dB$ at the carrier frequency, i.e. the normalized phase's amplitude becomes $A_{CT} = 0.91$. The required frequency f_B for the direct DQM is the highest among considered configurations, $f_B = 4f_C = 8560MHz$. When the up-conversion block is added in the modulator's scheme, the equivalent DAC pulse becomes $g_2(t)$ shown in Fig.5.32(B). The change of the pulse's shape affects magnitudes of upper and lower images at frequencies f_L and f_U (5.42), (5.43). Example of the utilization of lower phase's image is shown in Fig.5.32(D). In the presented case the sampling rate of phase $LP\Sigma\Delta$ modulators is $f_\Phi = 1426MHz$. While the desired carrier frequency of

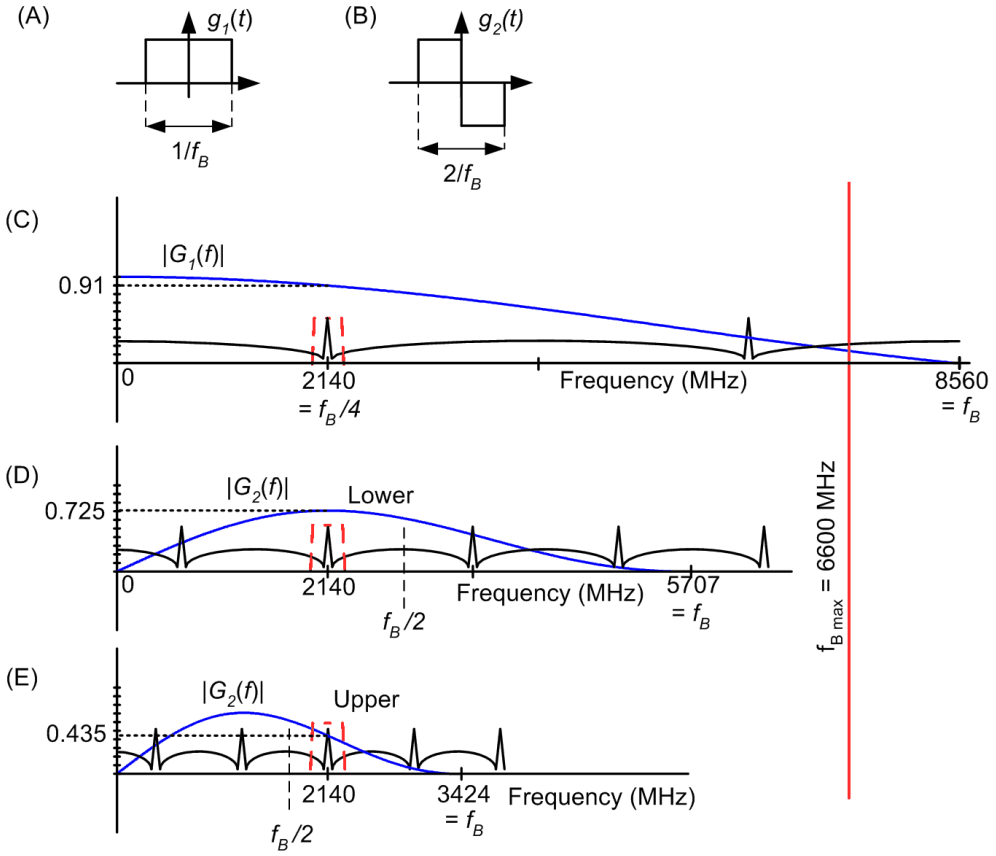

Figure 5.32: Phase magnitude versus sampling rate. (A) Pulse shape without the second up-conversion. (B) Pulse shape with the second up-conversion. (C) Utilization of the image at $f_B/4$. (D) Utilization of the lower image. (E) Utilization of the upper image.

$f_C = 2140MHz$ is obtained, $G_2(f)$ attenuates the phase's power at the carrier frequency by $-2.8dB$ ($A_{CT} = 0.725$). The frequency of the output buffer however reduces to $f_B = 5.707GHz$, which already meets the required limit of $f_B \leqslant 6.6GHz$ of the used FPGA. The utilization of the upper image results in further attenuation of phase's magnitude, but it also allows further reduction of the frequency f_B. When the sampling rate of phase $LP\Sigma\Delta$ modulators pair is $f_\Phi = 856MHz$, the frequency of the output buffer reduces to $f_B = 3424MHz$. In this configuration $-7.2dB$ ($A_{CT} = 0.435$) of phase power reduction is expected. The summary for sampling rates and phase's power is given in Tab.5.3.

The reduction in phase amplitude affects power consumption of a DPT since higher gain in a broadband driver is needed between the modulator and switchmode power amplifier. Approximately $2dB$ more of the gain than for direct DQM ($f_B = 8560MHz$) is needed when lower image ($f_B = 5707MHz$) and $6.4dB$ more when upper image ($f_B = 3424MHz$)

are utilized. Despite the largest reduction in the generated signal power, the upper image with $f_\Phi = 856MHz$, $f_B = 3424MHz$ has been chosen in the experimental polar modulator implementation. It allows for the lowest sampling rate of the output buffer among the considered configurations to be used.

Table 5.3: Amplitude reduction in the digitized polar modulator's output.

f_Φ (MHz)	UF	f_B (MHz)	SC (dB)
856	2 (upper)	3424	-7.2
1426	2 (lower)	5707	-2.8
8560	1 (direct)	8560	-0.82

5.5.5 Simulated results

The bandlimited X_{IN} signal has been used in simulation of the proposed polar modulator. The sampling rates of phase $LP\Sigma\Delta$ modulators pair and envelope $LP\Sigma\Delta$ were $f_\Phi = 856MHz$ and $f_E = 214MHz$ respectively. The band pass filter was simulated as a 4th order, digital Butterworth filter with a $3dB$ passband of $BW_{BPF} = 45MHz$. The phase-envelope mixing was simulated by an ideal multiplier characterized by zero rise and fall times. Due to the largest delay induced by the band pass filter, delay correction was provided in the envelope path. The phase baseband components I' and Q' were scaled to 0.8 of a $LP\Sigma\Delta$ full scale range to avoid overloading the modulator. For unity STF of $LP\Sigma\Delta$ modulators the recovered phase's amplitude is $A_{PM} = 0.8 \cdot 0.435 = 0.345$. The simulated, pulsed waveform is shown in Fig.5.33. A maximum SNR achievable with the proposed modulator has been simulated without $LP\Sigma\Delta$ modulator in the envelope path, i.e. envelope signal was not quantized. As a result, the phase $LP\Sigma\Delta$ modulators were the only sources of distortion in the modulator. The aliasing effect can be neglected for $BW/f_C \leqslant 10/1000$, which yields $h_{1/2} \leqslant -52.1dB$ as read from Tab.5.2. The maximum SNR was calculated for three different input signal bandwidths, and the results are provided in Tab.5.4. The time domain waveform and the output spectrum for an input signal

bandwidth of $BW = 5.35MHz$ and the envelope $LP\Sigma\Delta$ sampling rate of $f_E = 214MHz$ is shown in Fig.5.33. The dynamic range of $35dB$ obtained in the output spectrum and the large amount of quantization error power in adjacent channels does not meet the spectral mask requirement of $43dB$ for $UMTS$ standard. It is however caused by insufficient sampling rate of the envelope $LP\Sigma\Delta$ modulator rather than by the proposed approach to the generation of phase signal in the proposed modulator. This however is limited by elements in the modulator, a mixer and an RF power amplifier's bandwidth. These problems will be discussed in Section 6.2.

Table 5.4: Maximum SNR and $ACLR$ in the output from the proposed modulator.

BW(MHz)	5.35	10.7	21.4
SNR(dB)	42.2	38.2	32.5
$ACLR$(dB)	45	31	22

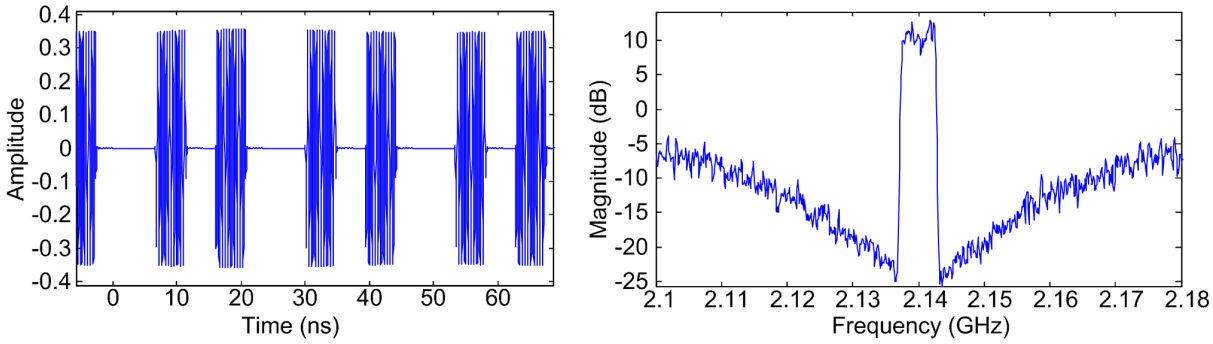

Figure 5.33: Modulator output in time and frequency domain, $BW = 5MHz$, $PAPR = 12dB$.

5.6 Conclusion

This chapter analyzed the process of signal conversion from Cartesian to polar coordinates in a DPT. In the first part, the chapter analyzed effects of a band limitation of phase and envelope signals and time misalignment between the two signals on performance of the output signal. While an envelope or phase bandwidth four times wider than transmitted signal bandwidth is sufficient for achieving SNR of $50dB$, the band limiting creates

error power peaks occurring outside the transmission band which can cause interference in adjacent channels. In order to meet the $43dB$ requirement for spurious emissions, the envelope and phase signals should be provided with bandwidths approximately four and ten times wider than the RF bandwidth. In contrast with the bandwidth limitation, the time misalignment between phase and envelope signals results in an error power concentrating inside the RF band. A precise delay correction must be provided to prevent *SNR* degradation and subsequent increase of *BER* in a receiver. Analytic prediction and simulated results have been demonstrated for inband error power increase caused by the delay between phase and envelope signals.

Although it could be expected that the increase of $LP\Sigma\Delta$ sampling rate in the envelope path should be accompanied by improvement of *SNR*, it is not always true in a *DPT*. An aliasing is caused by a spectral replica of digitized envelope at frequency $2f_C$. The sampled envelope is mixed with the phase signal, which has the effect on degradation of *SNR*. A three tone $DSB-AM$ signal has been used to estimate the magnitude of distortion in a digitized polar transmitter as a function of a carrier frequency and signal's bandwidth which provides an insight into the distortion mechanism. The aliasing in the *DPT* limits maximum achievable *SNR* regardless of the number of levels in a $LP\Sigma\Delta$ quantizer or of its sampling rate.

The second part of the chapter introduces the concept of modified modulator for a *DPT*, designated for *FPGA* implementation. The new modulator uses digital, instead of analog quadrature mixer which reduces analog hardware and increases reconfigurability of the modulator at the cost of some performance degradation. The use of $LP\Sigma\Delta$ modulators preceding the digital quadrature mixer induces quantization error in the phase signal. A high oversampling ratio needed for the phase $LP\Sigma\Delta$ modulation limits maximum bandwidth of a transmitted signal. The practical design and implementation of the modulator are presented in the next chapter.

Chapter 6

Modulator for digitized polar transmitter

This chapter focuses on the practical issues concerning generation of the RF drive signal for a DPT. The first part of the chapter describes the functional blocks in a digital signal processor and the phase-envelope mixing circuit employed in the polar modulator. The second part of this chapter provides measured results for three different sampling rates of the envelope $LP\Sigma\Delta$ modulator and focuses on the linearization of the $AM-AM$ characteristics in the implemented modulator.

6.1 Digital and analog design

The block diagram of the modulator implemented in the Virtex 6 $FPGA$ platform is shown in Fig.6.1. The major functional blocks are the baseband signal generator, CORDIC, division, GTX transmitter and $LP\Sigma\Delta$ modulators sections in the envelope and phase paths. The phase signal in the proposed modulator is reconstructed by band pass filtering the digitized signal in a microstrip filter. The obtained continuous-time phase signal is subsequently mixed with the digitized envelope in a GaAs switch, yielding the drive signal

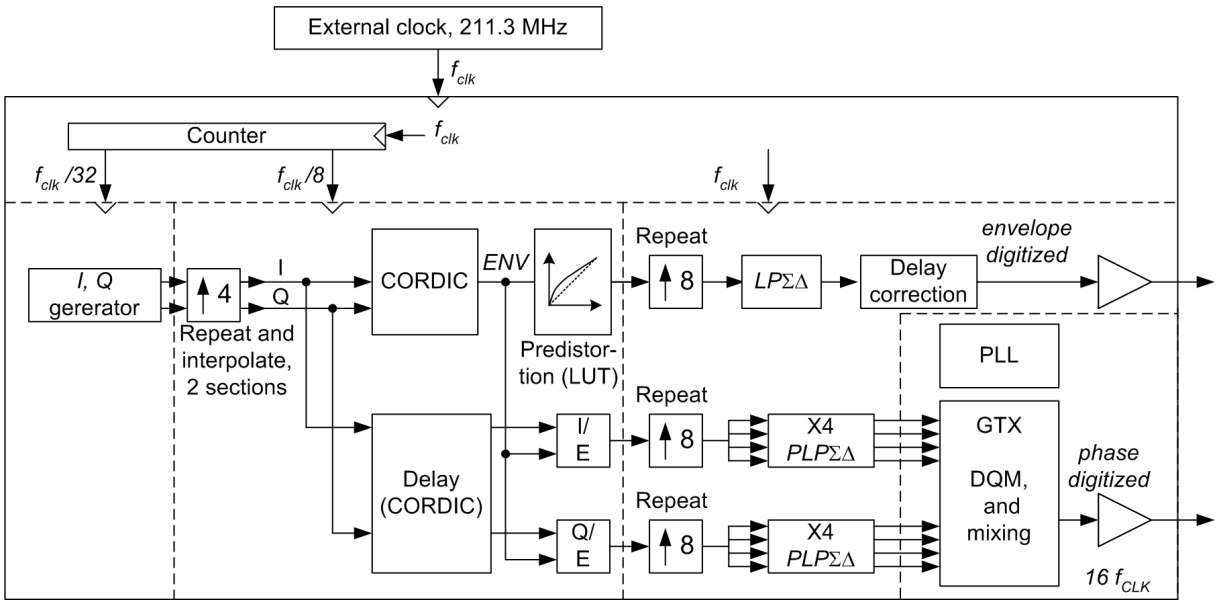

Figure 6.1: Digital signal processing in the polar modulator.

for the RF PA. A description of the modulator's blocks is provided in the following sections.

6.1.1 Input signal

The input signal for the modulator is generated by two binary, pseudo-random generators based on $16-bit$ linear feedback shift registers ($LFSR$) followed a by pair of Nyquist filters. The Nyquist filters have impulse responses restrained to finite sequences by applying a Hann window. The filters span 32 symbol durations and have a roll-off factor $\beta = 0.14$. The impulse and magnitude responses of the filters are shown in Fig.6.2. Both filters are implemented as a transposed direct form FIR filters of lengths $L = 193$. The RF

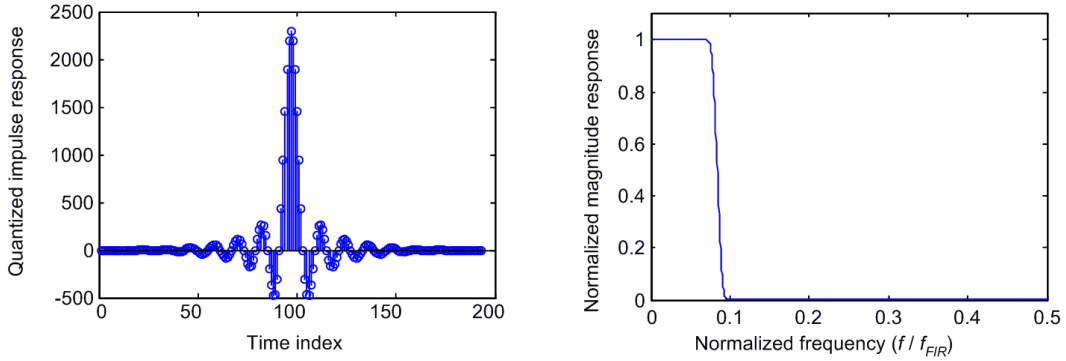

Figure 6.2: Impulse and magnitude response of the low pass filters used.

output signal has a $4QAM$ constellation and a bandwidth of $BW_{\beta=0} = 1.1MHz$ when $f_{FIR} = 211.3MHz/32$. The clock frequency for the $FPGA$ was changed in the experimental modulator from assumed earlier $f_{CLK} = 214MHz$ to $f_{CLK} = 211.3MHz$ in order to adjust the carrier frequency to the center frequency of the fabricated analog BPF, as will be explained in Section 6.1.8.

6.1.2 Sampling rates

The digital signal processing in the polar modulator is divided into four main sections: input signal generation, CORDIC and division, ΣΔ modulation and GTX transceiver section. Each of these sections operates at a different sampling rate.

The baseband signals I and Q are synthesized and band limited at a sampling rate being several times higher than their bandwidths. The spectral regrowth of the envelope and the phase components however necessitate increasing the sampling rate before the signals are supplied to CORDIC and division blocks. The sampling rate is also increased before the ΣΔ and GTX transceiver sections. The sampling rate alteration across the digital part of the modulator allows for more efficient utilization of $FPGA$ resources in terms of hardware count and power consumed than if all sections operated at the same sampling rate. The sampling rate is increased with an upsampler block. The upsampler provides an output signal sampled at N times higher ($N = 2,3,4...$) rate than the rate of an input signal.

$$f_2 = Nf_1 \tag{6.1}$$

The upsampler can either repeat the input sample N times, or pass it only one time while padding with zeros the remaining samples. The former method is often more efficient for upsampling baseband signals since it also provides zero-order interpolation. When increasing the sampling rate, an interpolating filter that suppresses spectral replicas present

in upsampled signal's spectrum is often necessary. The upsampled output spectrum consists of the input signal's spectral copies at integer multiplies of the original sampling rate f_1. The nearest to the baseband spectral copy is centered at frequency $f = f_2/N$. The low pass filter's stopband should therefore begin at frequency f_{stop} as shown in Fig.6.3.

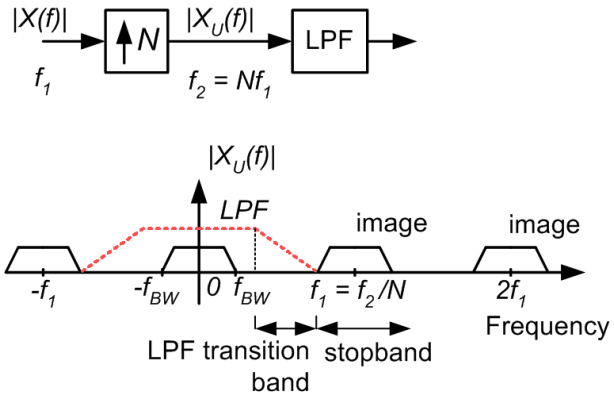

Figure 6.3: Upsampler followed by interpolating filter.

$$f_{stop} = f_2/N - f_{BW} \tag{6.2}$$

An upsampling with a large factor N usually leads to short transition band requirement in a frequency response of the interpolating filter. The requirement for a sharp characteristic of the filter can be relaxed if the interpolator is divided into sections of lower degree of upsampling [66]. The interpolator employed in this work consists of a factor of two, repeating upsampler followed by a low pass Butterworth filter of second order. The filter's transfer function is chosen such that both its conjugate zeros lie at $z = -1$. The filter stopband is therefore centered at frequency $f = f_2/2$, being the centre frequency of the signal image. The zeros at $z = -1$ yield the transfer function's numerator whose coefficients are expressible by 2^n numbers, where n is an integer,

$$H_{num} = a\left(z^2 + 2z + 1\right) \tag{6.3}$$

The coefficient a in (6.3) is a constant that scales the magnitude response of the filter. Since the multiplication by 2^n numbers simplifies to left or right shift operation, the mul-

tipliers can be replaced by much faster barrel-shifters. The coefficients in the denominator are also rounded to the nearest 2^n numbers ($a_1 = 0, a_2 = 0.1875 = 2^{-3} + 2^{-4}$) yielding,

$$H_{den} = 1 + 0.1875z^2 \tag{6.4}$$

The direct form *IIR* structure and frequency response of the filter are shown in Fig.6.4. The passband and stopband marked in the figure indicate approximated location of the baseband portion of I or Q signals upsampled by a factor of two. Approximately $20dB$ or more of suppression is provided in the stopband of the filter. A higher degree of suppression, if needed, can be achieved by cascading two *LPF* sections.

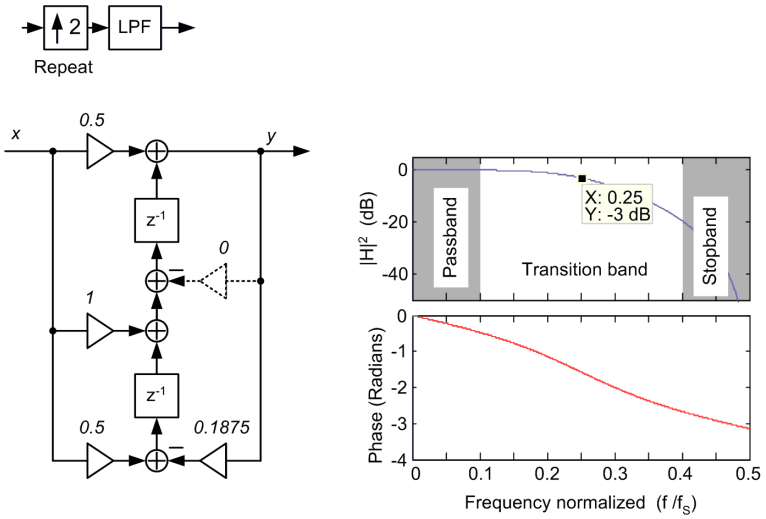

Figure 6.4: The interpolator used in this work..

6.1.3 Clock signal in the signal processor

The $211.3\,MHz$ clock signal for the Virtex 6 $FPGA$ was supplied from the signal generator $HPE4433B, ESG-D$. The change from the assumed earlier $214\,MHz$ was done to adjust the carrier frequency of the modulator to match the microstrip filter's passband, being centered at $2113\,MHz$. Low frequency clock signals, $211.3\,MHz/m$ needed across the $FPGA$ were obtained with a counter implemented in the $FPGA$ board. The high frequency clock signal, $3380.8\,MHz$, for the parallel to serial register was generated by the *PLL* present in the GTX transceiver.

6.1.4 CORDIC algorithm

The COordinate Rotation DIgital Computer [120] algorithm was employed to calculate the square root of the in-phase and quadrature signals, yielding the envelope signal. The algorithm performs rotation of vector of coordinates $x = I$ and $y = Q$ (or $x = Q$ and $y = I$) until the angle obtained is nearly zero and the x approximates the square root of equation (5.2) multiplied by a constant. The CORDIC block in the polar modulator consists of three pipelined subsections. The first subsection calculates the moduli of the input 2-complementary numbers, the second subsection arranges the I and Q such that they create a vector having an angle of $0^0 \leqslant \alpha \leqslant 45^0$. The third subsection executes seven iterations of vector rotation. The average approximation error for 5 iterations and an initial vector's angle of $0^0 \leqslant \alpha \leqslant 45^0$ was computed in Matlab as 0.034%. The delay block in the CORDIC section compensates for the delay between envelope and baseband signals, which is necessary to avoid error in subsequent division sections.

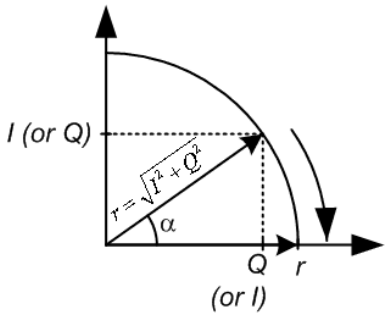

Figure 6.5: CORDIC - vector rotation.

6.1.5 Long division

The phase components in a polar modulator are calculated by performing divisions operations $\frac{I[n]}{ENV[n]}$, $\frac{Q[n]}{ENV[n]}$ in (5.4). Since the Virtex 6 FPGA does not provide dedicated dividers, the division block for the polar modulator was implemented using a long division algorithm. The implemented divider scales dividend and divisor numbers in the first step. After detection of the most significant bits (*MSB*), the divisor, being lower

than the dividend, is shifted to the left aligning MSBs of the two numbers. Subsequently, the division block executes 10 iterations providing the quotient. The division is performed on the moduli of the numbers, and the sign of the quotient is recovered after the last iteration. Due to the complexity of the division and CORDIC algorithms, these two sections were operable at a maximum clock frequency of $26.41\,MHz$. This maximum clock frequency yields a Nyquist frequency limiting the phase bandwidth to $BW_P = 26.41\,MHz$. Consequently, the maximum RF bandwidth is calculated using equation (5.14) as $BW = 0.1 \cdot BW_P = 2.6341\,MHz$. For RF signals having bandwidth wider than $2.6341\,MHz$, the sampling rate can be increased by implementing the necessary number of division and CORDIC sections in parallel or by pipelining in these two functional blocks.

6.1.6 $\Sigma\Delta$ modulators

The implemented polar modulator utilizes two pairs of time-interleaved $LP\Sigma\Delta$ $(TI - LP\Sigma\Delta)$ modulators in the phase path. The design and implementation of first order $TI - LP\Sigma\Delta$ modulators was described in Chapter 3. The digitized phase signal sampled at $3.3808\,MHz$ frequency is supplied to the output of $FPGA$ board through a CML buffer. The envelope $LP\Sigma\Delta$ modulator can operate at either full clock frequency of $211.3\,MHz$ or at its positive integer fraction. The envelope $LP\Sigma\Delta$ modulator has its binary output connected to the pair of $LVCMOS$ output buffers. The output buffers are connected with a voltage level shifter designed for driving the RF switch which will be described in Section 6.1.9.

6.1.7 Parallel to serial register

The digital quadrature modulator (DQM) and the up-converting block present in the phase path of the proposed polar modulator (see Fig.5.30) were implemented in the GTX

transceiver of the Virtex 6 $FPGA$. The GTX is synchronized with the $FPGA$'s clock signal by the internal PLL block. Every clock cycle, eight 1-bit outputs from the two $TI-LP\Sigma\Delta$ modulators are up sampled by factor of two, yielding the 16-bit signal. This 16-bit signal undergoes two mixing steps, described in Section 5.5. The resulting signal is subsequently written into the parallel register. The PLL frequency is calculated from [4],

$$Line\,rate = clock\,rate \cdot Internal\,data path\,width = 16 \cdot 211.3\,MHz = 3.3808\,MHz$$

The binary output sampled at $3.3808\,MHz$ is fed through the pair of CML buffers to the SMA connectors on the $ML605$ [6] board.

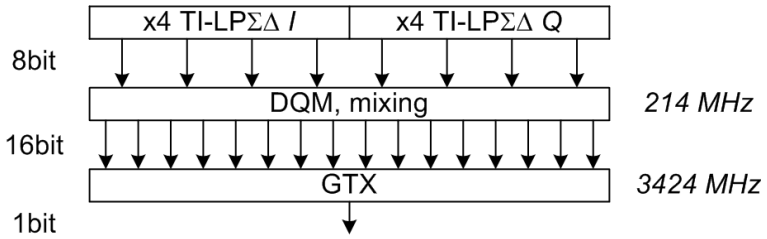

Figure 6.6: GTX as a parallel to serial register.

6.1.8 Band pass filter

The microstrip band pass filter for the phase path was designed with Agilent Genesys 2010.05 software. The design parameters of the filter were $35MHz$ of a passband and a centre frequency of $2140MHz$. Due the relatively narrow passband and a large tangent loss of the $FR4$ substrate used ($tan\delta \approx 0.02$), the fabricated filter is characterized by large insertion loss, $IL \approx 18dB$. The measured magnitude response of the filter is shown in 6.7. The obtained filter's centre frequency is $2113\,MHz$ instead of the assumed $2140\,MHz$. This frequency offset was caused by imprecise permittivity information given for the $FR4$ substrate but it was acceptable for testing the modulator.

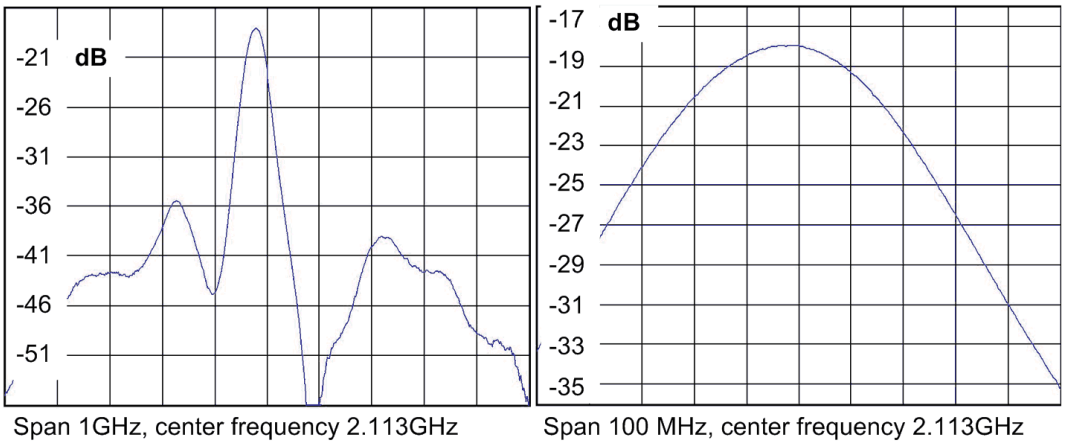

Figure 6.7: Measured magnitude response of band pass filter.

6.1.9 The mixing circuit

The $HMC231$ GaAs switch of Hittite [2] was employed as a mixing device in the polar modulator. The switch either passes the input phase signal to a $50\,\Omega$ matched output or terminates both the switch's input and the output to internal $50\,\Omega$ resistances as shown in Fig.6.8. The switch is characterized by $3\,ns$ rise and $6\,ns$ fall times, an input signal pass-band of $0-6\,GHz$ and isolation of $50\,dB$ at $3\,GHz$ frequency. The rise and fall times of the selected switch are slightly better than other, commercially available devices, e.g. Analog Devices $ADG901$ is characterized by rise and fall times of $3.1\,ns$ and $6\,ns$ respectively.

6.1.9.1 Voltage levels shifting

The $HMC231$ switch requires negative drive voltage levels which can not be supplied from the Virtex 6 $FPGA$ output. Consequently, a voltage level shifter circuit capable of achieving transient times in a range of few nanoseconds is necessary for maximizing the sampling rate of the envelope $LP\Sigma\Delta$ modulator. Such a fast voltage levels shifting can be achieved by employing a pair of common base amplifiers.

The digitized, differential envelope signal is supplied from the $FPGA$ through two $LVCMOS$ buffers having voltage levels of $V_H = +2.5V$, $V_L = 0V$. The conversion to

negative levels, $V_H = 0V$, $-5V < V_L < -2.5V$, is achieved by using a pair of common base amplifiers and the external voltage supply $V_1 = 2.5V$ as shown in Fig.6.8. The two amplifiers employ low power RF *PNP* transistors which ensure short transient times when switching between the two voltage levels. The resistances in the voltage shifter are chosen such that when the output voltage of *LVCMOS* buffer is $V_H = +2.5V$, the corresponding emitter's current becomes $I_E \approx (2.5V - 0.6V)/(15\Omega + 180\Omega) = 9.7mA$. The resulting collector current $I_C < 9.7mA$ produces a voltage across the resistance R_2 that subtracted from V_1 yields the output voltage of $V_{D1} \approx -0.2V$. The zero *LVCMOS* output voltage results in zero collector current. Consequently the output voltage becomes $V_{D1} = -V_1 = -2.5V$. In order to reduce the time of charging and discharging capacitances in the switch's drive inputs, two buffers $74HCT3244$ are added between the common

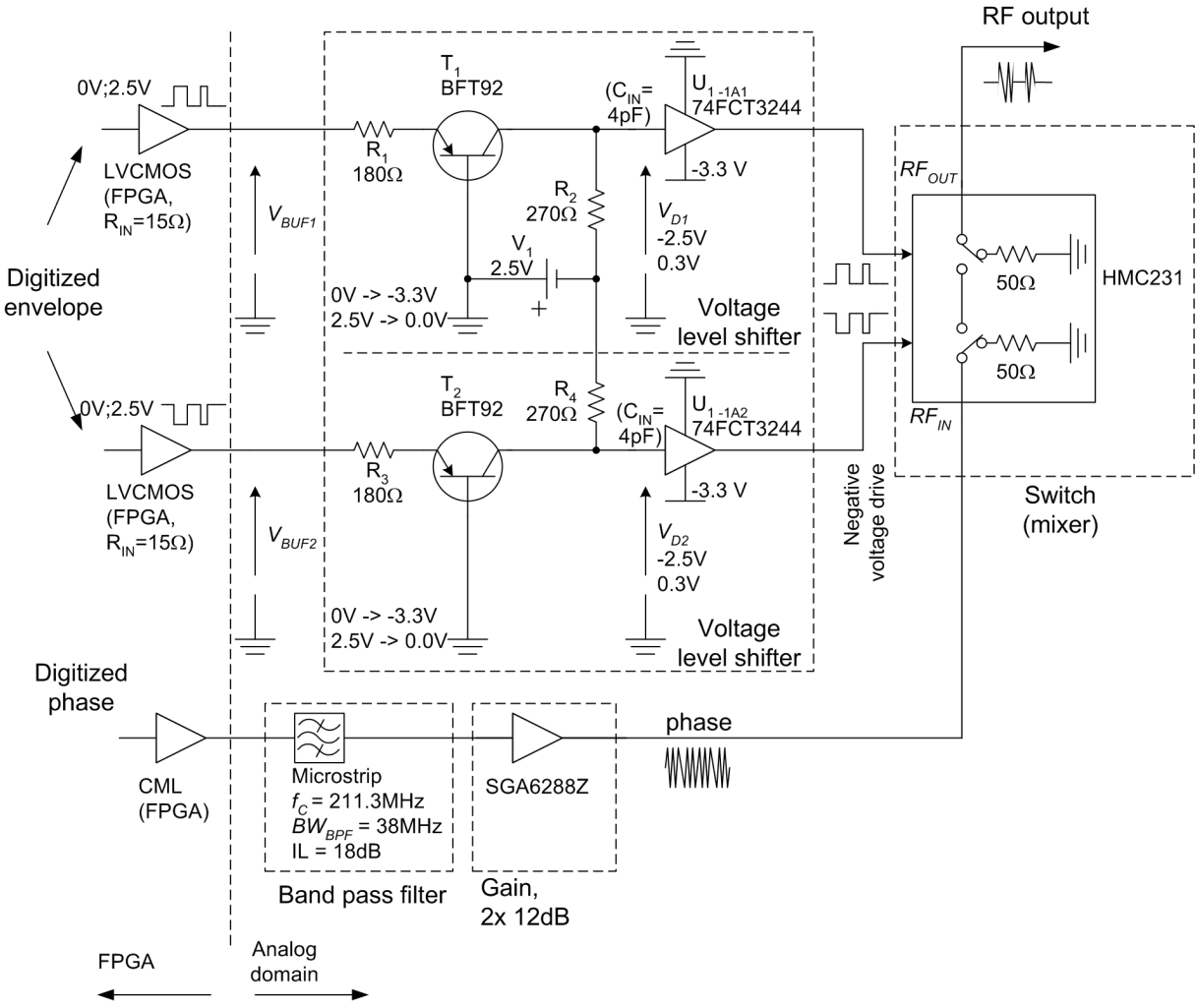

Figure 6.8: Mixer circuit.

base amplifiers and the switch. According to simulations done in Agilent ADS, the charging-discharging time of $4\,pF$ input capacitances is approximately $2\,ns$ as seen in Fig.6.9, which is less than the switch rise time of $3\,ns$. Such short rise and fall times of the voltage level shifter would be difficult to achieve with commercially available voltage level shifters.

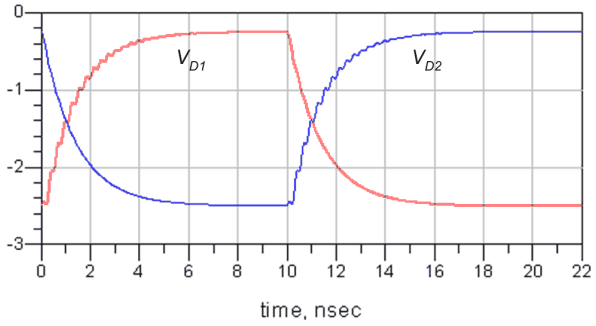

Figure 6.9: Rise-fall times of the voltage level shifter.

In order to compensate for low amplitude swing in the output from phase's *CML* output buffer and large insertion loss of the microstrip filter, a pair of $12\,dB$ amplifiers *SGA*6288*Z* have been added in the polar modulator's circuit providing a total of $24\,dB$ of gain at the carrier frequency.

6.2 Experimental results

This section presents the measured results for the implemented modulator. The experimental modulator is shown in Fig.6.10 and it consists of the digital signal processor implemented in Virtex 6 FPGA, the microstrip band pass filter and the switch *HMC*231. The clock signal for the $FPGA$ and the RF, single-tone test signal were supplied from two signal generators $HPE4433BESG-D$. The time domain measurements were taken by digital oscilloscope Agilent Infiniium 54853*A* at a sampling rate of $20GSa/s$. Frequency domain measurements were captured by digital spectrum analyzer $FSL\,9\,kHz-6\,GHz$ of *Rohde & Schwarz*.

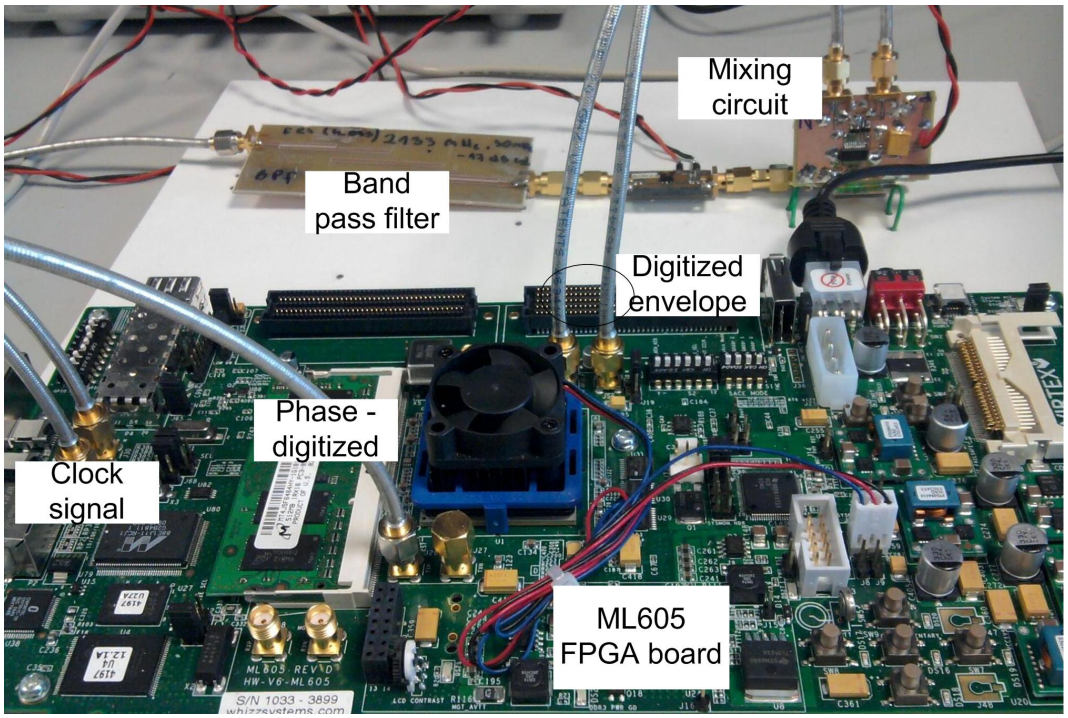

Figure 6.10: Polar modulator.

6.2.1 Switch response

The set-up for testing the switch response to the $LP\Sigma\Delta$ envelope pulses is shown in Fig.6.11. The envelope $LP\Sigma\Delta$ modulator was supplied with a DC input signal of different values, while the switch's RF input was supplied with the single-tone signal of frequency $2113 MHz$. The captured pulse-modulated waveforms are shown in Fig.6.12.

The time domain waveforms show approximately $2ns$ of a rise and fall times, being in a range of expected values provided in the switch's documentation. Apart from the rise and fall times, the pulses shapes depend on the value of the DC input. The largest deformation of the pulses occurs at low values of the DC input and at high sampling rates

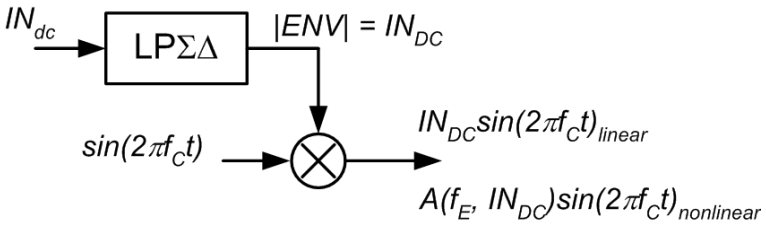

Figure 6.11: Test set-up.

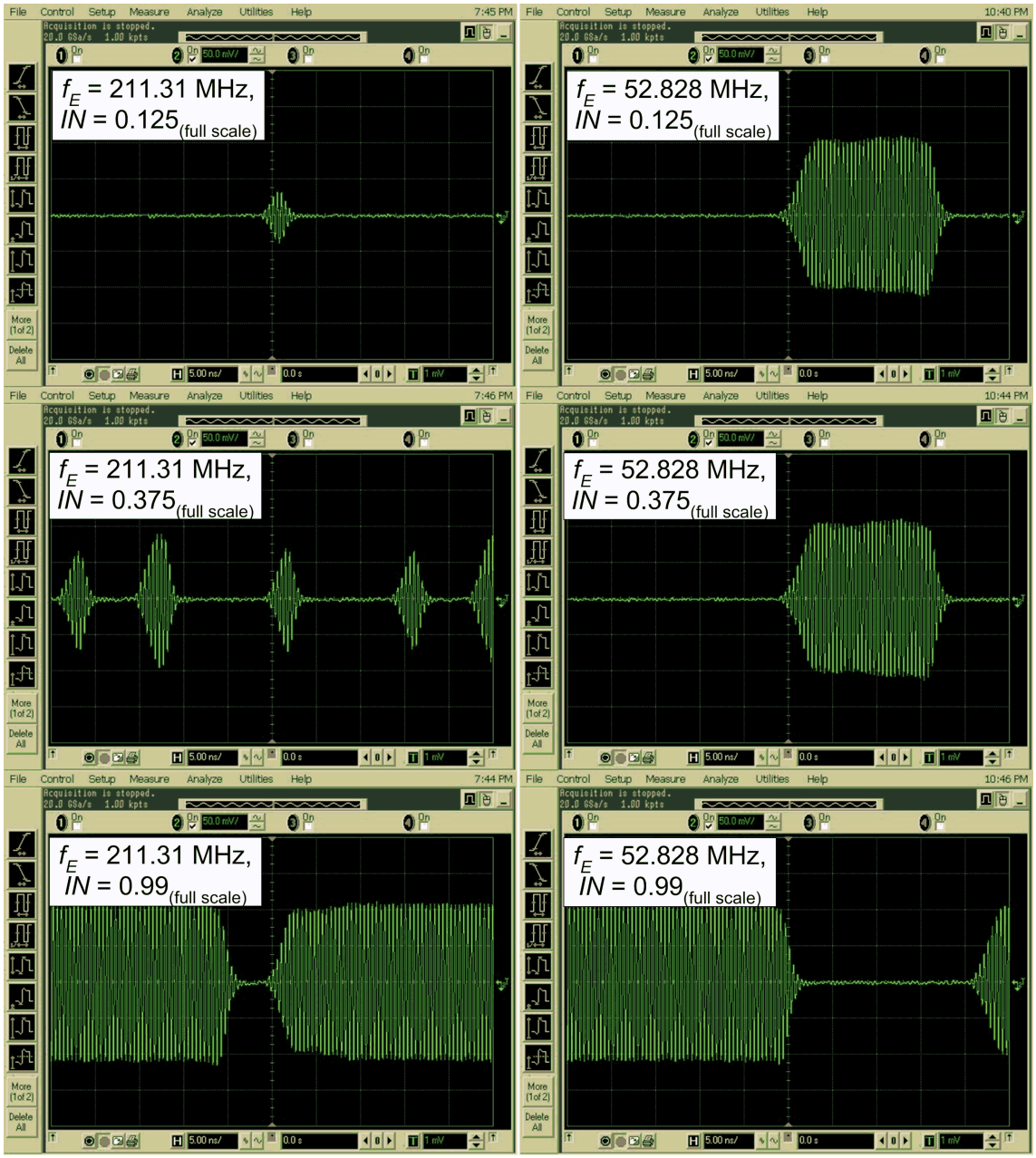

Figure 6.12: Output waveforms for $f_E = 53MHz$ and $f_E = 211MHz$.

of the $LP\Sigma\Delta$ modulator, i.e. when the pulses are short and their density is low. This effect is observed when $IN = 0.125$ and $f_E = 211.3\,MHz$. The pulse shapes improve when the DC input value increases, e.g. $IN = 0.375$ or $IN = 0.99$ or the sampling rate decreases. Clearly, the response time of the switching circuit depends on the density of envelope pulses, which implies a memory effect in the envelope-phase mixing circuit. Since the shape of the output pulses changes with envelope signal and with the sampling rate f_E, a nonlinearity of the amplitude characteristics is expected.

6.2.2 $AM-AM$ characteristics of the modulator

It was observed in the previous section that when the sampling rate f_E of the envelope $LP\Sigma\Delta$ increases, pulse shapes in the output of the polar modulator are becoming more susceptible to distortion caused by finite rise and fall times and by the memory effect. On the other hand, when the sampling rate f_E is fixed, the distortion of the pulse shapes depends on the input signal's amplitude IN as was observed in Fig.6.12.

The deterioration of the pulse shapes affects the digitized envelope signal E_D in the output from the polar modulator and causes distortion of the RF amplitude.

$$\begin{cases} X(t) = IN(t) \cdot PHA(t) \\ Y(t) = ENV_D(t) \cdot PHA(t) \end{cases} \tag{6.5}$$

We can assume that for a large oversampling ratio of the $LP\Sigma\Delta$ modulator, the envelope signal resembles a constant input over some large and finite number of pulses. Moreover, for a constant input the average error caused by the envelope pulses deformation is constant, and depends on the DC input to the $LP\Sigma\Delta$ modulator. Using this property, the

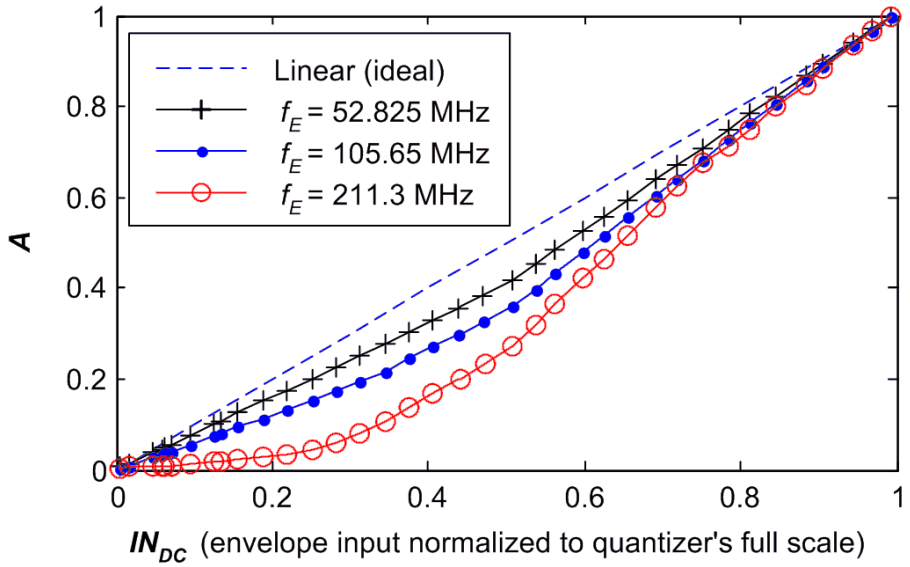

Figure 6.13: Measured of input-output characteristics of the modulator for $f_E = 52.825\,MHz$, $f_E = 105.65\,MHz$, $f_E = 211.3\,MHz$ and input signal's frequency $f_C = 2113\,MHz$.

$AM-AM$ transfer characteristics of the modulator can be measured by supplying the envelope $LP\Sigma\Delta$ modulator with a DC input IN in the $FPGA$, and by supplying the mixing circuit with a sinewave at the carrier frequency f_C as was depicted in Fig.6.11. The mixing of the $LP\Sigma\Delta$ modulator's output with the sinewave produces a tone at the carrier frequency f_C having amplitude A, being ideally a linear function of the input signal amplitude IN. The measured $AM-AM$ characteristics of the polar modulator are shown in Fig.6.13 for three different sampling rates of f_E and for the carrier frequency $f_C = 2113\,MHz$. It is evident that the memory effect delinearizes the modulator characteristics the more the higher the sampling rate f_E used.

6.2.3 Predistortion in the envelope path

A predistorting block was added in the embedded processor before the envelope $LP\Sigma\Delta$ modulator as depicted in Fig.6.1. The predistortion block was implemented as a look up-table (LUT), storing 31 offset values of the envelope signal for each sampling rate f_E. Every clock cycle the envelope signal addresses the LUT, and appropriate correction is added to the $LP\Sigma\Delta$ input. Fig.6.14 shows $AM-AM$ characteristics for $f_E = 105.65\,MHz$ and $f_E = 211.3\,MHz$ after implementing the predistortion block. The improvement in

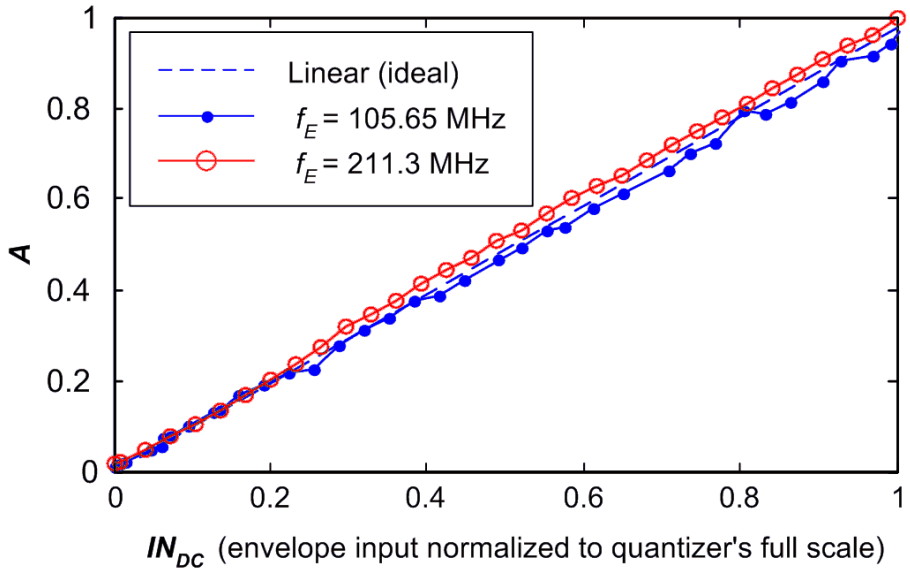

Figure 6.14: $AM-AM$ characteristics of modulator with predistorted input signal.

linearity is seen when comparing Fig.6.13 and Fig.6.14. The predistortion for the lowest sampling rate, $f_E = 52.825\,MHz$ had little impact on the measured frequency response of the polar modulator, and subsequently was not applied in the modulator processor. The RF amplitude error correction bases on the assumption of the large oversampling, which becomes less efficient when the sampling rate decreases.

6.2.4 Measured frequency responses

The output spectra for $f_E = 52.825\,MHz$ and the $4QAM$ input signal are shown in Fig.6.15. The modulator output shows large error power when the delay in the phase path is not compensated. The improvement is observed after adding delay in the envelope path. The delay correction in the $FPGA$ uses simple, programmable chain of delays blocks $\left(z^{-1}\right)$ sampled at $f_S = 211.3\,MHz$. The corresponding, maximum delay error becomes $\frac{0.5}{f_S} = 2.366\,ns$, and it is sufficient for maintaining good signal to noise ratio of $SNR \geqslant 46.5\,dB$ when $BW = 1.1\,MHz$ as calculated from (5.20) with the assumption that all other distortion effects are not present.

The predistorting of the envelope signal visibly improves the noise performance of modulators sampled at $f_E = 105.65\,MHz$ and $f_E = 211.3\,MHz$. The output spectra before

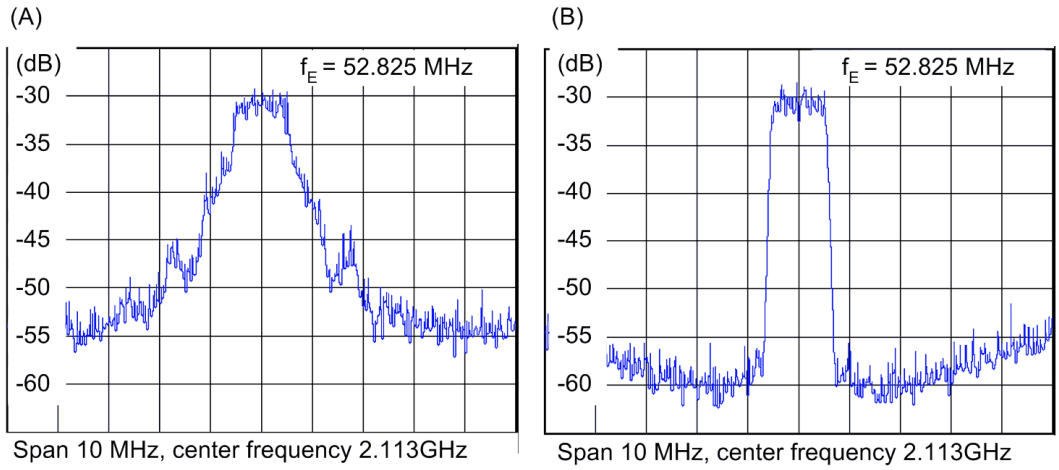

Figure 6.15: Output spectra from polar modulator. (A) Phase signal is retarding. (B) Corrected delay.

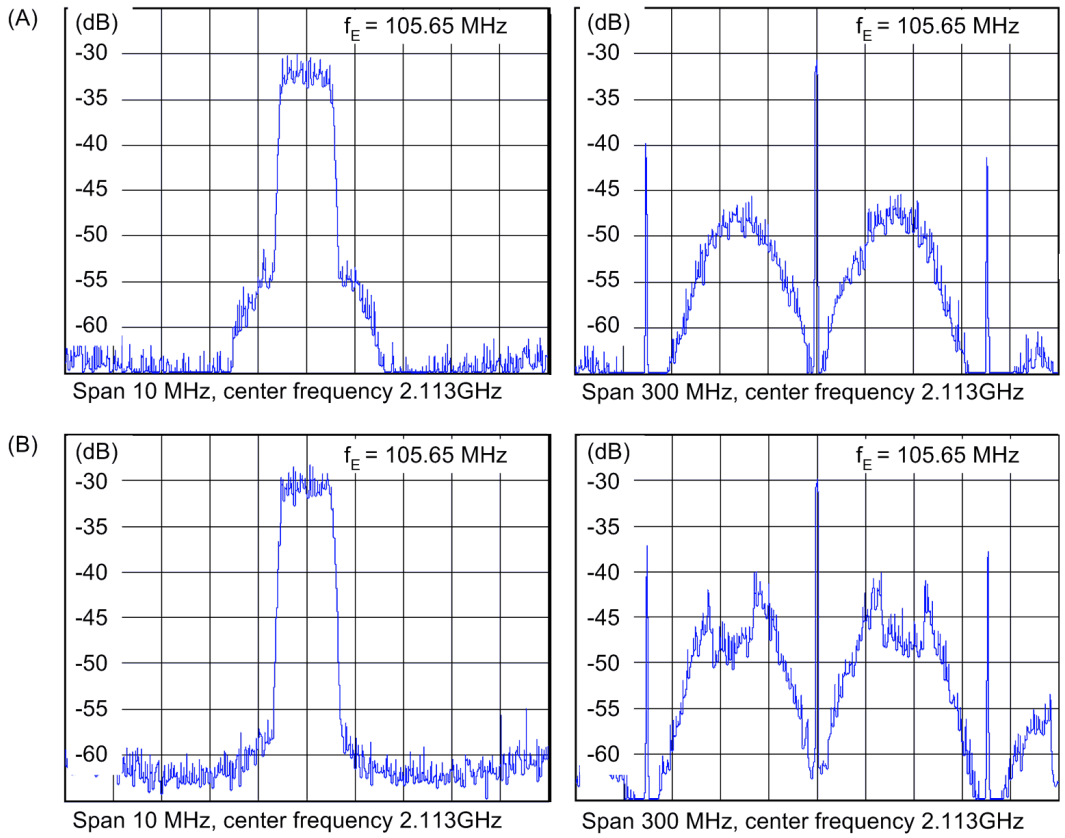

Figure 6.16: Output spectra for $f_E = 105.65\,MHz$. (A) No predistortion. (B) Predistorted.

and after predistortion are shown in Fig.6.16 for $f_E = 105.65\,MHz$ and Fig.6.17 for $f_E = 211.3\,MHz$. The large improvement in *ACLR* performance is observed especially for the highest sampling rate, $f_E = 211.3\,MHz$. The output spectrum exhibits approximately $30\,dB$ of *ACLR* despite severe distortion of the pulses in the output of the modulator. The $AM-AM$ predistortion technique described in this chapter can be also useful in the *DPT*, where similar deterioration of the pulses is expected in the output from a *SMPA*. The predistortion should be applied analogically as in the polar modulator, with the signal amplitude measured in the output of *SMPA* instead of the output of polar modulator.

Although the nonlinear $AM-AM$ characteristics of the polar modulator are correctable, the deterioration of pulse shapes affects the quantization-noise shaping of the envelope $LP\Sigma\Delta$ modulator. This effect is observed in the wide-span plots of Fig.6.16(B) and Fig.6.17(B), where additional quantization noise-power minima appear on both sides of the carrier frequency. Although not verified here, an increase of the inband noise is ex-

pected as a result of the changed pulse shapes to the ideal $LP\Sigma\Delta$ modulator.

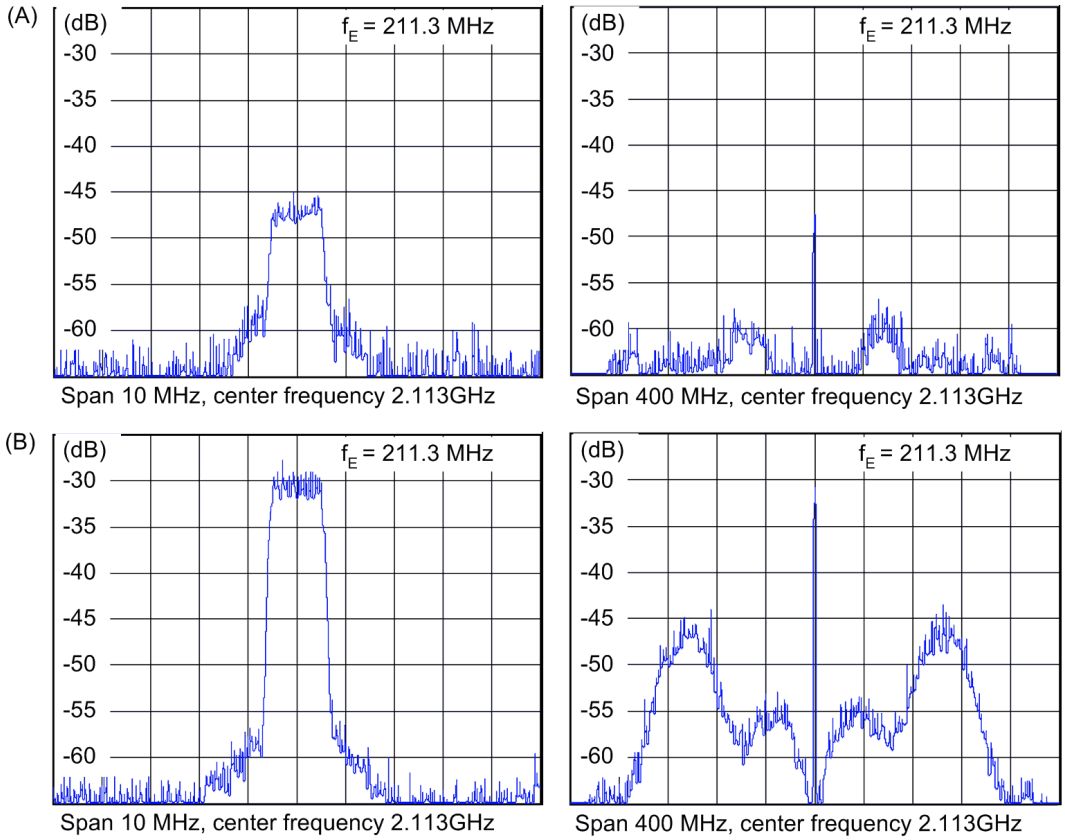

Figure 6.17: Output spectra for $f_E = 211.3\,MHz$. (A) No predistortion. (B) Predistorted.

6.2.5 Causes of distortion in the polar modulator

Despite meeting the sampling rate requirements for phase and envelope signals and the use of predistortion in the envelope path, the experimental modulator exhibits noise performance degradation when compared with simulated results. The polar modulator, simulated for $5\,MHz$ wideband input signal at sampling rate $f_E = 214\,MHz$, was shown in the previous chapter in Fig.5.33. The measured spectrum for $1.1\,MHz$ wideband input signal at nearly the same carrier frequency and sampling rate f_E is shown in Fig.6.17(B). Comparison of these two figures proves better noise performance of the simulated modulator, despite over 4.5 times wider bandwidth of the input signal used in simulation. Three factors that contribute to performance degradation in the implemented modulator are discussed in the following sections.

6.2.5.1 Quantization in the signal processor

The input signal in the polar modulator undergoes several conversion steps. Functional blocks; interpolating filters, CORDIC, division; add error caused by quantization. In order to minimize the quantization error, the baseband signals in the output of raised cosine filters, interpolation filters and CORDIC use high resolution, 16-bit wordlength. The word-length is reduced to 11-bit in the last steps of signal conversion, i.e. in divider and $TI-LP\Sigma\Delta$ modulators. The wordlength of 11-bit yields a signal-to-quantization-noise-ratio $SQNR \approx 6.02 \cdot 11 = 66.22\,dB$ in envelope and phase signals. The impact of the quantization is however negligible next to the quantization error induced by the 2-level $LP\Sigma\Delta$ modulators in envelope and phase paths, which was explained in Section 5.3 and Section 5.5.

6.2.5.2 Jitter

The phase signal in the digitized polar modulator is encoded into a binary pulse stream of a band-pass $\Sigma\Delta$ modulator's output i.e. the pair of $TI-LP\Sigma\Delta$ modulators create a bandpass modulator similar to the modulator described in Section 3.5.4. The high frequency clock generates a jitter distorting the phase signal, which influences the performance of the modulator. The maximum jitter in the output of GTX transmitter is $0.2-0.34\,UI$

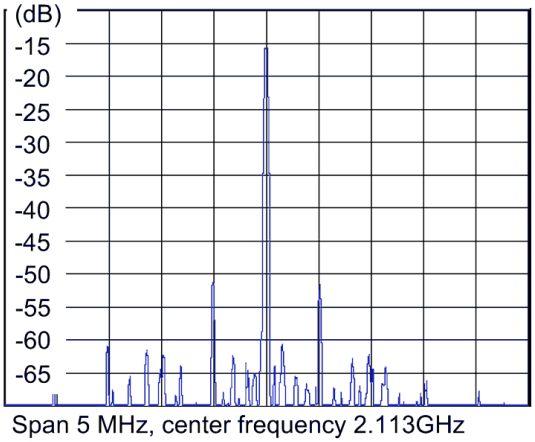

Figure 6.18: Single tone at the carrier frequency in the output of GTX transmitter.

(Unit Interval) [7] for clock frequency of 3380.8 MHz, which yields a maximum jitter of $59-100\,ps$. A tone generated in the output of GTX transmitter at the carrier frequency is shown in Fig.6.18, showing 35 dBc of a spurious-free dynamic range. The large amount of jitter in the GTX output creates phase noise and becomes the major performance-limiting factor in the implemented polar modulator.

6.2.5.3 Band pass filter

The phase signal in the proposed modulator is obtained by attenuating the quantization error induced by $\Sigma\Delta$ modulators. While the band pass filter should be characterized by a flat magnitude response and linear phase response in the passband, the measured responses prove otherwise as shown in Fig.6.7. The magnitude and nonlinear phase response should be corrected by implementing appropriate filters to I' and Q' signals to avoid PM distortion in the implemented modulator.

6.3 Conclusion

This chapter presented practical implementation of the polar modulator for a DPT, demonstrating factors limiting noise performance in the output, RF signal. The practical problems were encountered on both, digital and analog sides of the modulator.

The major factor contributing to SNR degradation in the signal processor was jitter induced by the PLL in the GTX transceiver. While phase noise in the proposed modulator's output is affected by the jitter, its reduction can be achieved through the use of an external parallel-to-serial register.

The second performance limitation was caused by the spectral regrowth of the phase and envelope signals, and subsequent requirement for a sampling rate higher than that used for sampling baseband signals as was described in Section 5.2. The experimental

modulator uses the new time-interleaving technique described in Chapter 3 to implement ΣΔ modulators, which allows the sampling rate to be increased in comparison to conventionally implemented ΣΔ modulators.

The problem encountered in the analog part of the modulator was associated with $AM-AM$ distortion caused by rise and fall times and memory effect in the phase-envelope mixing circuit. In contrast to Class-S amplifier, where both, phase and amplitude modulated RF signal is encoded by $BP\Sigma\Delta$ modulator, the DPT processes phase and envelope signals separately. This allows for separate predistorting, and consequent simplification of the linearization of the transmitted signal. It was demonstrated that a predistortion implemented in the envelope path of a modulator can significantly improve the noise performance of the modulator in the presence of deterioration of pulses shapes. The demonstrated correction of the $AM-AM$ characteristic can be also used for predistorting a complete DPT, i.e. polar modulator connected with a $SMPA$. A similar effect to the observed pulses deterioration in the polar modulator's output can be expected in the output of $SMPA$. The relatively simple to implement predistortion allows for increasing sampling rate of the envelope $LP\Sigma\Delta$ modulator and reduction of spurious emissions in the output of a transmitter.

Chapter 7

Conclusion and Future Work

7.1 Conclusions

An RF power amplifier is a necessary element in every wireless transmitter. Since the RF signals in third and fourth mobile generations have modulated amplitudes, linear operation of the power amplifier is required. Unfortunately amplifiers operating in classes A or AB, when used to transmit signals with high *PAPR* such as $W-CDMA$ or $OFDM$, are characterized by low power efficiency which contributes to short battery life in handsets and large power dissipation in mobile base stations. In contrast a $\Sigma\Delta$ modulation of the RF signal allows for the use of highly nonlinear but also power efficient, switchmode power amplifiers, while preserving linear operation of the amplifier system.

Although there has been a large research effort on the efficiency improvement and analysis of nonlinear effects in the switchmode power amplifiers, problems concerning the process of the RF signal modulation have received less attention. This thesis addresses several important problems on the modulation side of the digital power amplifiers utilizing $\Sigma\Delta$ modulators, and gives an insight into mechanisms of signal processing and distortion.

1. High sampling rate of a $\Sigma\Delta$ modulator is needed to ensure sufficient *ACLR* for wideband RF signals used in third and fourth mobile generations. The achievable sam-

pling rate depends on a computation time in a critical path, which in turn depends on modulator's structure. New structures for $BP\Sigma\Delta$ modulators with reduced critical path have been designed. The reduction of critical path has been achieved by using delaying loop filter sections in a distributed feedback topology. The obtained $BP\Sigma\Delta$ modulator can have NTF zeros at $0 \leqslant f \leqslant f_{\Sigma\Delta}/2$.

2. The shortest critical path can be obtained in a $LP\Sigma\Delta$ modulator whose NTF has all zeros placed at DC. In order to take advantage from the short critical path in a $BP\Sigma\Delta$, the lowpass to bandpass transformation $z \rightarrow -z^2$ can be used. The resulting $BP\Sigma\Delta$ has fixed NTF zeros at $f = f_{\Sigma\Delta}/4$. It has been found that the obtained $BP\Sigma\Delta$ modulator is equivalent to two, lowpass to highpass $(z \rightarrow -z)$ transformed modulators operating in parallel. Subsequently this property has been used to increase the sampling rate by a factor of two in the parallel system. A generic lowpass to time-interleaved transformation scheme is provided.

3. Outputs at consecutive time indexes can be computed for a $\Sigma\Delta$ modulator by transforming its discrete time domain state equations by means of $n \rightarrow n+1$. The repetition of arithmetic operations is used to obtain a generic transformation scheme of a time-interleaved $\Sigma\Delta$ modulator. The transformation can be applied to any of a lowpass, bandpass or highpass $\Sigma\Delta$ modulators, increasing the effective sampling rate of the $TI-\Sigma\Delta$ modulator. The two TI-expansion techniques can be used together to achieve the highest sampling rate in a $BP\Sigma\Delta$ modulator.

4. The use of lowpass STF has been proposed for suppressing input aliases in a zero-insertion $TI-LP\Sigma\Delta$ modulator. The aliases are induced by the use of an input expander in the $TI-LP\Sigma\Delta$. The lowpass STF has been demonstrated to increase the stable input range in a $TI-LP\Sigma\Delta$ modulator to the level comparable with equivalent, conventional $LP\Sigma\Delta$.

5. The $TI-LP\Sigma\Delta$ modulators of order one and two have been designed, simulated and implemented. The experimental results validate the proposed technique for expansion to a time-interleaved system.

6. The use of a 2-level $\Sigma\Delta$ guarantees linearity of a *DAC*, but also induces the largest quantization noise power. The nonlinear *DAC* effect in a $BP\Sigma\Delta$ modulator with a 3-level quantizer has been analyzed and the property of an error shaping in the imperfect 3-level *DAC* has been found. The error pulses added in the 3-level *DAC* have Fourier transforms whose zeros coincide with the carrier frequency of the $BP\Sigma\Delta$ modulator, providing suppression of the nonlinear distortion effects.

7. The error pulses shaping has been used to derive the new, 2-level $BP\Sigma\Delta$ modulator. The new modulator uses two quantization steps: first is 3-level, and the second converts the 3-level signal to a 2-level signal. The 2-level output of the modulator yields less of the quantization error than a conventional 2-level $BP\Sigma\Delta$ modulator. The new modulator has been analyzed, and a linear model has been derived.

8. Based on the linear model, a predistortion is designed for the new modulator, which cancels part of the error induced in the course of 3-level to 2-level conversion and subsequently improves *SNR* in the output of the modulator.

9. The new modulator's performance has been compared against equivalent conventional 2-level and 3-level modulators in the course of extensive simulations. Also, the experimental results have been provided.

10. Signal processing steps in a polar transmitter with a $\Sigma\Delta$-digitized envelope signal have been analyzed. The effects of spectral regrowth, time delay and aliasing in the *DPT* have been modeled providing insight into distortion mechanisms in the transmitter. New method of analysis uses the additive error to express the effects of

spectral limitation of the envelope and phase signals and the time misalignment.

11. New method of generation of a phase signal for the digitized transmitter has been presented. The modified modulator utilizes the $TI-\Sigma\Delta$ modulators for replacing multibit *DAC*s and quadrature mixer, which simplifies the analog part of the conventional signal modulator for the *DPT*.

12. The modulator has been simulated and implemented, based on sampling rates requirements derived earlier in this work. It has been demonstrated that the pulses deformation in a polar modulator have the effect on RF amplitude. This effect can be corrected by placing predistortion in the envelope path of a *DPT*.

7.2 Future work

The future improvement of the $TI-\Sigma\Delta$ modulators will require the use of a low level of abstraction design of some of the functional blocks. The use of dedicated adders available in Virtex II Pro FPGA using fast carry logic increases the computation speed in a critical path. In contrast, the in-theory simple operation of a 2-level quantization is synthesized using a generic logic, which induces more of propagation delay than if dedicated arithmetic blocks were used. A careful gate-level design oriented to minimize the propagation delay should however allow for increasing the sampling rate in the $TI-\Sigma\Delta$ modulators beyond the limits reported in Section 3.6.

The development of the polar modulator described in Chapter 5 should include the increase of a sampling rate of the $\Sigma\Delta$ in the phase path. An improvement can be attained by employing the modified bandpass modulator based on 3-level quantization described in Chapter 4. In order to transmit a wideband signals such as *LTE*, the envelope sampling rate should be increased by integrating the modulator with a *SMPA*. The integration will

reduce parasitic capacitances and reduce response time of a mixer and the *SMPA*. Also, the use of 3-level or 4-level ΣΔ modulation, as demonstrated in [23], can improve power efficiency of a transmitter in the presence of large *PAPR* of the RF signal and it should be considered. The quantification of nonlinear effects should be done for a *SMPA*, i.e. the effects of nonlinear R_{ON} resistances and nonlinear parasitic capacitances in transistors on the RF phase and amplitude. The complete model of the transmitter should allow for designing an efficient predistortion and improvement of the still, poor *SNR* reported for the digitized polar transmitters used with wideband RF signals.

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