A PIPELINE VOLTAGE-TO-TIME CONVERTER FOR HIGH RESOLUTION SIGNAL EXTRACTION OFF-CHIP

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Abstract

In this paper a pipelined voltage to time converter is presented. It is targeted at the extraction, in digital form, of sensitive analog signals from an integrated circuit. The tester is able to measure the period of this signal and derive the original voltage. The input signal is low frequency. This paper provides solutions to the main challenges in implementing this modulator and how it may be integrated with a digital tester.

1 Introduction

The development of CMOS and BiCMOS technologies has made it possible to combine digital and analog circuits on the one chip increasing system functionality and integration. While the test challenges relating to digital circuits have been addressed through the availability of CAD tools and structured test strategies, mixed signal test is still function based and therefore complex. The challenges and limitations facing mixed signal analog function based test are: increased resolution; increased bandwidth; higher direct conversion rates; and lower permitted noise floor (an extract from the ITRS road map is shown in Table 1) [11]. Current technology for automated testers (ATE) will find it increasingly challenging to measure these devices. Therefore, new increasingly expensive ATE will have to be developed, see shaded areas of Figure 1 for more information. This is increasing the cost of analog and mixed signal test.

Verifying the performance of critical analog or mixed signal components on a large, primarily digital, device is challenging. While the majority of the device can be tested on a standard digital tester, the analog or mixed signal component requires special analog input and output pins (I/O), with large dynamic range and high noise tolerance. While many testers have some analog I/O included, this is at a high cost for the overall system. From another perspective, the same problem restricts the use of built in self test (BIST) techniques. Often, the BIST technique is larger in area or more complex in design than the analog circuitry being tested. This commonly makes BIST economically non-viable.

Year of First Production Shipment Technology Generation	2006 100nm	2009 70nm	2012 50nm
Low Frequency Source & Digitizer			
BW(MHz)	4	4	4
Fs (MS/s)	10	10	10
Bits	20-23	20-23	20-23
Noise Floor (dB/RT Hz)	-160	-160	-160
High Frequency Waveform Digitizer			
Level V (pk-pk)	4	4	4
BW (MHz) (undersampled)	2000	3000	3000
Fs(MS/s)	1/40/320	1/40/640	1/40/1280
Bits(AWG/Sine)	18/14/12	18/14/12	20/16/12
Noise Floor (dB/RT Hz)	-120	-120	-120

Table 1: Future test measurement requirements

This paper proposes a modified constant current, voltage controlled relaxation oscillator structure for use as an embedded oscillator for test. Relaxation oscillators are commonly used circuits [2,4,5] but resolution has been typically restricted to 10-bits. The resolution is limited by the linearity of the current source, the capacitor and the performance of the comparator.

To achieve higher resolution, we purpose to construct a pipelined sequence of oscillators that uses switched-capacitor charge-summation as the reference for the relaxation oscillator. The remainder of this paper presents an architecture for such an oscillator with 16-bit linearity.

2 Relaxation Oscillators

Figure 1 below shows a typical constant current relaxation oscillator [4,5].

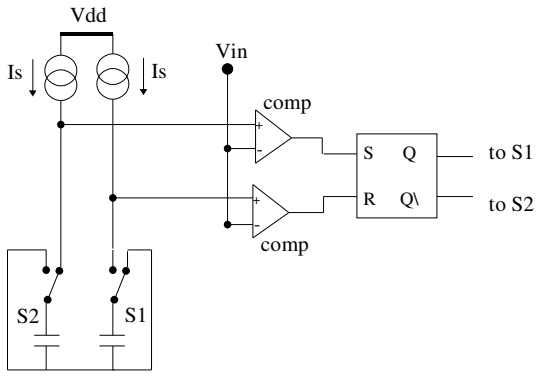

Figure 1: Voltage controlled constant current relaxation oscillator

Depending on the state of the switches, one of the capacitors is charged linearly by one of the constant current sources. The output of the capacitor is connected to a comparator where this voltage is compared with V_{in}. When the capacitor voltage exceeds V_{in}, the SR flipflop is triggered which results in the output and the switches, S1 and S2, changing state. This alternates the charging and discharging of the capacitors, Figure 2 shows some ideal waveforms.

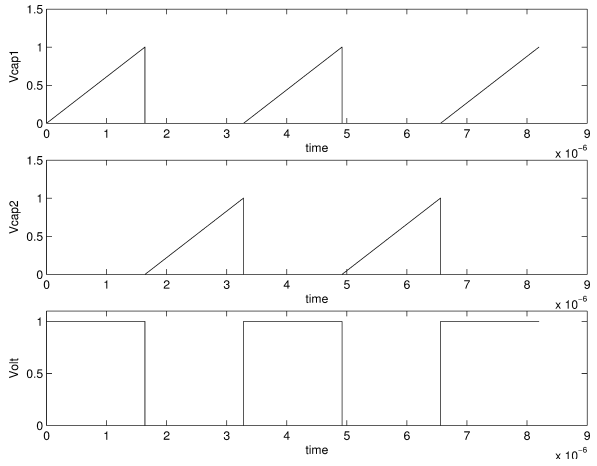

Figure 2: Capacitor voltage waveforms and flipflop output.

The voltage on a capacitor is given by,

$$v = \frac{I_s \cdot t}{C} \tag{1}$$

The output time period t is given by

$$t = \frac{2 \cdot v_{in} \cdot C}{I_s} \tag{2}$$

And the corresponding frequency as

$$f_{osc} = \frac{1}{t} = \frac{I_s}{2 \cdot v_{in} \cdot C} \tag{3}$$

One important source of deviation from this linear relationship is the effect of time delay, T_D. Time delay is the time it takes the comparator to make a decision, and the flipflop and the switches to change state. The effect of this time delay results in an offset for voltage controlled oscillators, shown in Figure 3, which can be corrected for. This is a significant advantage over the non-linear effect in current-controlled oscillators, shown in Figure 4. As can be seen the output frequency becomes nonlinear as the frequency approaches $1/T_D$.

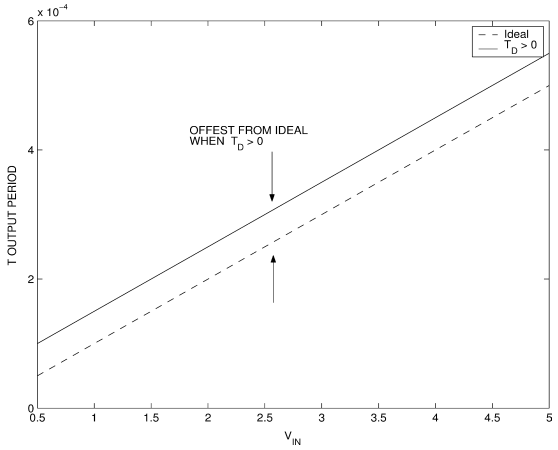

Figure 3: Voltage controlled oscillator.

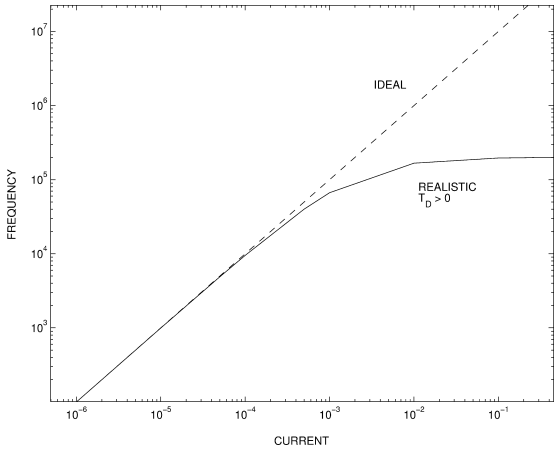

Figure 4: Current controlled oscillator.

Relaxation oscillators are normally restricted to resolutions of less than 10 bits. This is due to nonlinearities in the current source and noise in the comparator circuit, which causes jitter in the output waveform. Abidi and Meyer [1] showed that the jitter in relaxation oscillators can be approximated by the following equations:

$$\text{jitter} = \frac{\sigma_T}{\mu_T} \quad (4)$$

where σ_T and μ_T are the standard deviation and mean respectively, of the oscillation pulsewidth.

$$\sigma_t = \frac{\alpha \cdot \sqrt{6} \cdot V_n(\text{rms})}{S} \quad (5)$$

where S is the slope of the capacitor voltage waveform and α is a constant valued between 0.5 and 1, depending on the bandwidth of the noise [1]. Thus to minimize jitter we can either increase the slope of the capacitor voltage waveform, reduce the bandwidth of the noise by filtering or minimize the noise by design.

3 Modified Oscillator

For the purposes of an embedded oscillator for test, the design constraints are to minimize area while maintaining a linear relationship between output time period and input voltage. It is also important to minimize any additional noise contributions to the measured signal. As the embedded oscillator will only be used for production test, the primary constraint is the die area of the modulator. It is presumed that digital post-processing may rectify any performance issues.

Standard relaxation oscillators [2,4,5] used a linear voltage ramp as the voltage reference to the comparator. This method was prone to nonlinearity in the voltage waveform due to channel length modulation [8]. Instead of using a constant linear voltage waveform, we purpose to use a voltage staircase as the voltage reference to the comparator as shown below in Figure 5.

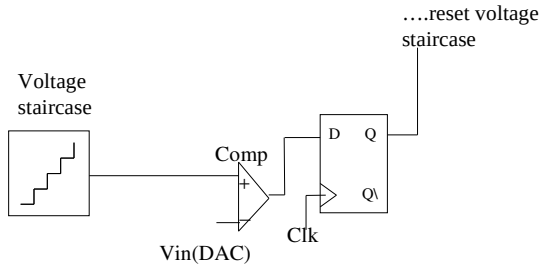

Figure 5: Modified oscillator using voltage staircase

The full circuit block diagram of this switched capacitor oscillator is shown in Figure 6.

The voltage staircase at V_o is described by the following,

$$V_o(n) = n \cdot (V_i) \cdot \left(\frac{C_R}{C}\right) \quad (6)$$

where C_R is equal to C.

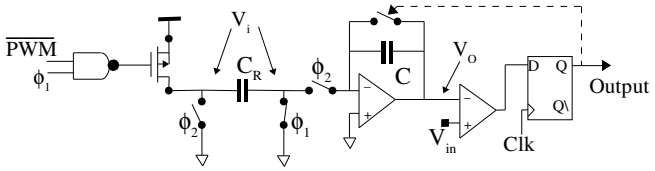

Figure 6: Switched capacitor oscillator.

The input voltage, V_i is described by,

$$V_i = \frac{I_D \cdot T_\Phi}{C_R} \quad (7)$$

3.1 Digital Current Source

In most relaxation oscillators the current source is provided through a current mirror driven from either a bandgap reference or from an input driven g_m cell. For an embedded modulator for test purposes, including a bandgap reference would increase the area overhead substantially. We propose to use a single PMOS transistor driven via a pulse-width modulated (PWM) voltage signal, as a current source.

When the gate voltage is high no current flows through the PMOS, and when it is low, the drain current can be approximated by the saturated MOSFET equation:

$$I_D = \frac{\beta'}{2} \cdot \frac{W}{L} (V_{GS} - V_T)^2 \quad (8)$$

No channel length modulation is included as the voltage across C_R reaches only V_{1LSB}, therefore the voltage across the PMOS is almost constant.

If the PWM switching frequency is high, and the drain current is appropriately low pass filtered, via CR, then the output drain current may be considered constant. The step size of the voltage staircase depends on the switches switching frequency($1/T_\varphi$). The longer T_φ is, the longer C_R charge time, thus the bigger the step size.

The system requires two non-overlapping clocks, ϕ_1 and ϕ_2, and a clock twice the frequency of ϕ_1 and ϕ_2 for the flipflop. These could be generated from a clock already on chip or externally from the tester.

3.2 Finite Op-amp Gain Error

The problem of a nonlinear voltage ramp remains due to finite amplifier gain. Finite gain influences not only the value of the input, on C_R, but also the value stored on the integrating capacitor C. V_{out} of the integrator is described as:

$$V_o = \left(\left(\frac{C_R}{C}\right) \cdot V_i + V_{stored}\right) \cdot \frac{A}{(A+1)} \quad (9)$$

where A is the open loop gain of the amplifier and V_{stored} is V_o of the previous step in the voltage staircase.

The effect of the finite gain is to continually reduce the contribution from the previous steps(N) as follows,

$$V_o(N)=\sum_{i=1}^{N} i\cdot V_i\cdot[\frac{A}{(1+A)}]^{N-i} \qquad (10)$$

This causes a nonlinear voltage ramp as shown in Figure 7.

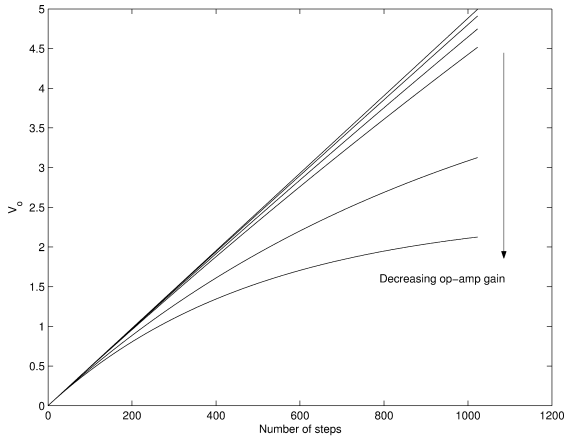

Figure 7: Nonlinearity due to finite op-amp gain.

The problem is related to the number of steps in the staircase not the size of the step itself. To keep the INL error to be less than a quarter of an LSB, requires the following minimum gain for the integrator amplifier,

Resolution(bits)	Min Gain(dB)
8	102
12	150
16	198

Table 2: Simulated minimum op-amp gain for 1/4LSB INL.

Despite the low frequency of operation, for high performance exceptionally high gain values are needed, which are typically unobtainable. This problem can be partially solved through the use of finite-gain insensitive integrators [7,9,10].

4 Pipeline Architecture

It is clear that the nonlinearity in the voltage waveform used as the voltage reference for the comparator is the limiting factor on the achievable resolution for a single stage oscillator. Finite gain is the cause of this nonlinearity in the switched capacitor case, whilst current source nonlinearity through channel modulation is responsible for a nonlinear capacitor voltage ramp in the constant voltage case.

Therefore we propose to pipeline two lower resolution oscillators to achieve the higher resolution required, at the expense of a slower sampling speed. The architecture is shown in Figure 8. Both stages contain the switched capacitor (SC) oscillator shown in Figure 6.

The normal requirement for a DAC in pipeline converters is avoided [6] in this architecture, as the analog voltage level at which the comparator triggered is available, shown in Figure 8 as $S/H_{clk(n-1)}$. This is advantageous as it keeps the die area of our architecture low. It does mean that the linearity error in the first stage voltage staircase must be kept low, so as not to cause errors in the second stage conversion.

The system operates as follows; the first stage calculates the most significant bits(MSB). The sample and hold circuit, in the first stage, holds the analog voltage value of the voltage step prior to the comparator triggering. This value is used to calculate the residue voltage. The residue voltage is sampled and amplified before being applied to the second stage. The gain(G) is equal to 2^N, the number of codes in the first stage. The second stage calculates the least significant bits(LSB). The final result is calculated as follows:

$$D_{out}=N_2\cdot D_{out(1^{st})}+D_{out(2^{nd})} \qquad (11)$$

where N_2 is the number of codes in the second stage, and D_{out} is the digital output from each stage. This is illustrated in Figure 9.

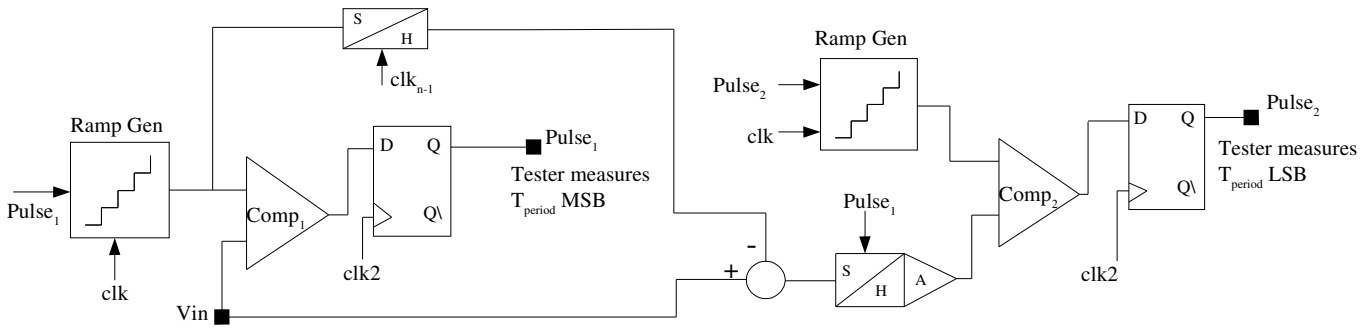

Figure 8: Pipeline oscillator architecture.

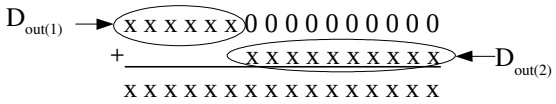

Figure 9: Calculation of output code.

4.1 Measurement and Calibration

Measurement of the period of the output waveform can be performed by two external edge counters driven by an external reference clock. This will enable accurate measurements of signals if taken over a long period of time.

$$\frac{T_{period}(\text{ref clock})}{T_{period}(\text{signal})} = \frac{N_{edges}(\text{signal})}{N_{edges}(\text{ref clock})} \qquad (12)$$

Since this process is an integration operation, increased measurement time will also reduce the effect of cycle to cycle jitter on the final accuracy. It is important to calibrate the linear relationship of input voltage to oscillation period, through measurement of some known points. If a reference voltage can be applied that is available elsewhere on the chip or externally, it and fractions of it could be used. Also if a zero input is used, the system can be designed so that it will oscillate at the minimum period of the system, defined by T_D. Where the modulator is interfaced with a tester, a preliminary set of measurements would identify the scaling factors, which than can be used in later measurements.

4.2 Example Pipeline Oscillator

To explore the performance of the system, a MATLAB(R) simulation was created for a 16 bit modulator. That assumed transistor level performance as described by equation (8). An ideal saturation current of 1.6µA was used with a capacitor value of 80pF. A switching time delay of 3ns was assumed, which is conservative given modern logic. Simulations have shown that large switching time delays(T_D) have little effect on performance, Figure 5.

The voltage staircase in the first stage must be as least as accurate as the resolution of the entire system, in order to prevent errors in the second stage conversion. For this reason a first stage resolution of 6 bits and a second stage resolution of 10 bits were chosen. To achieve this the op-amp gain for the first stage will have to be 127dB as shown in Figure 10. As mentioned previously in section 3.2, through the use of finite-gain insensitive integrators [7,9,10] this minimum gain can be reduced.

The tester will sample the output waveforms at a speed of 1000 samples per second. This requires a clock frequency for φ_1 and φ_2 of 64KHz for the first stage, and 1.024MHz for φ_1 and φ_2 of the second stage. And clock frequencies of 128KHz and 2.048MHZ for the D-type flip-flops for the first stage and second stage SC oscillators (Figure 6). Previous simulations [3] have shown that the added noise due to a PWM switching frequency of 10Mhz and a 50/50 duty cycle, is low, below -100dB.

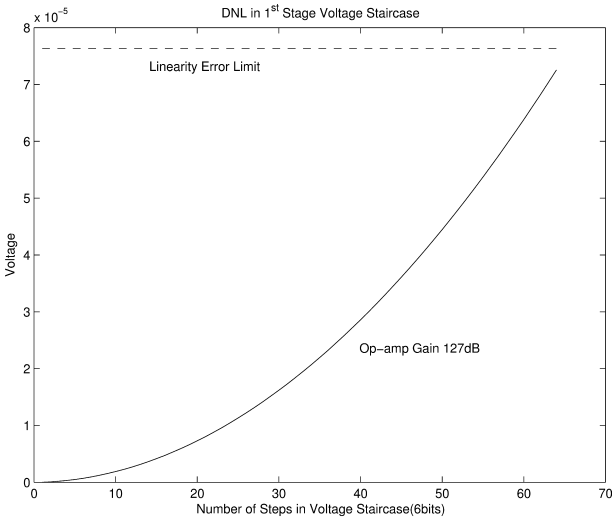

Figure 10: DNL in 1st stage voltage staircase

Figure 11 shows the INL and DNL for the simulated oscillator, its output time period is ideally linear with the input voltage.

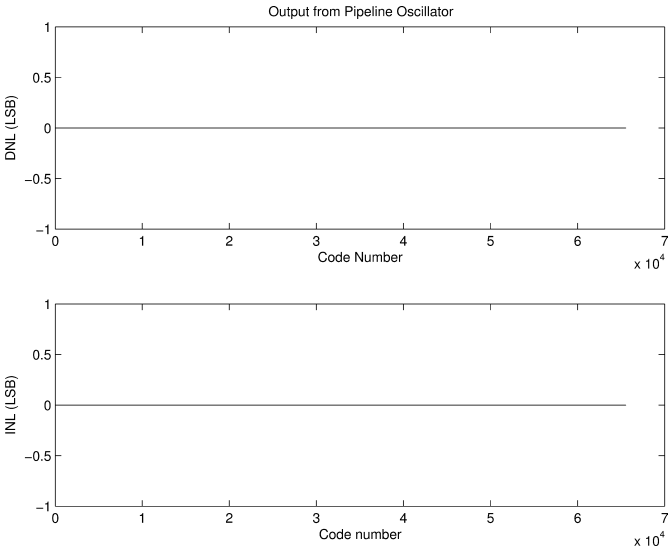

Figure 11: Output from pipelined oscillator.

5 Conclusion

The purposed architecture meets the requirement of high sensitivity and performance with low die area. The architecture trades sampling speed for performance in a linear manner. Current trends in process technologies and device speeds will enhance its performance, allowing for either faster sampling or increased resolution. It is robust to process variations and has an inherent method for calibration and self test. Work is ongoing to develop a prototype of the modulator in Figure 8, the purposed architecture has the potential for achieving high resolution with a very small die footprint.

Acknowledgments

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