Embedded Built-In-Test Detection Circuit for Radio Frequency Systems and Circuits

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Abstract: An embedded rectifier-based Built-In-Test (BIT) detection circuit for the RF integrated circuits is proposed in this work, and charge pump rectifier is adopted to transform the RF output signal into DC signal. In this BIT circuit, low threshold voltage MOS transistor with positive substrate bias is used to act as diode to further improve the conversion efficiency and the detecting sensitivity. With this BIT circuit, the minimum input testing sensitivity can be improved to -50dBm. Also, this circuit doesn't consume current and has very high operating frequency scalability. As an example 2.4GHz low noise amplifier by using this BIT detecting circuit has been verified, and gain and linearity information can be obtained without influencing the performance of the attached RF circuits.

Keywords: BIT, Rectifier-based, RF

Introduction

The continual scaling down of integrated circuit technology has made the manufacturing cost fall or nearly the same. However, with the increase in the operating frequency and the level of integration of wireless communication systems the testing becomes more expensive and complicated. For RF and multi-GHz circuits, the cost of the testing instruments is becoming prohibitive. So, reliable high frequency testing has become a significant restrictive and influencing factor for the time-to-market of novel wireless products [1-3]. At present, researchers have done some advanced works to develop efficient testing techniques for the RF systems and individually building blocks in order to reduce the high frequency testing cost [4-7], in which embedded Built-In-Test (BIT) has been considered as a feasible way for functionality verification and production real-time monitoring. In general, precise RF measurements using mature technologies and methods are relatively expensive, forcing the BIT designer towards simplicity and an integrated built-in-test approach. As MMIC and RF-SOC become more complicated, embedded BIT becomes a necessity. Shown in Fig.1, embedded BIT reduces the tester complexity by using low-cost DC or low frequency test instruments, eliminates the need for off-chip interfacing by integrating with the tested circuit on-chip, and allows the circuit-under-test (CUT) to be tested many times during the production evaluation. Because the BIT circuit is customized and optimized to the CUT and that set-up and performance requirements for the external tester are drastically reduced, the testing time can be reduced.

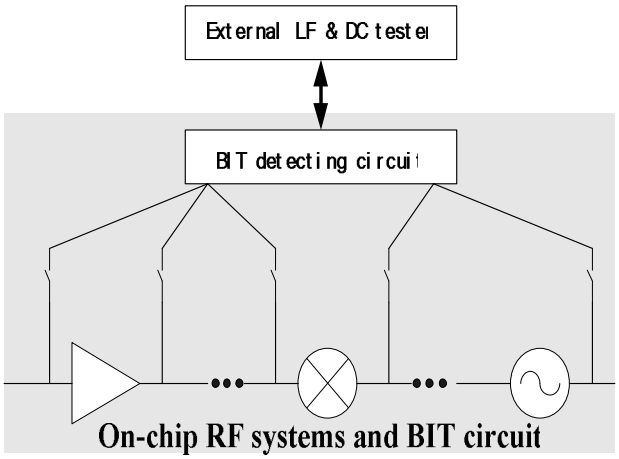

Fig.1 the schematic of using embedded BIT for RF systems and circuits

Although many BIT schemes have been proposed [8-13], recent efforts in RF integrated circuit testing

have focused on the design of on-chip embedded detectors or sensors where the output signals can be tested easily [8,11,12], and on the methodologies and algorithms for automated test design [10,11,14]. In [10], a BIT method for RF testing by using mapped feature extraction sensors was proposed, in which specialized functions of the output response from an alternate test were computed using built-in feature extraction sensors, and a complex function of the response waveform was measured and a DC signal was gotten. Reference [8] presented a CMOS RMS detector for the testing of a wireless transceiver. By using a three-stage rectifier the output of the high frequency circuit can be converted into a DC signal. Soumendu Bhattacharya, etc. [11] set up a RMS detector whose output was correlated with the target test specification values of the CUT. Instead of testing the devices specifically for performance metrics, the outputs of the sensors were used to estimate the target test specs when the CUT was stimulated with sinusoidal stimulus.

However, it is not an easy task to design a BIT detecting circuit as there are several issues that need to be considered. The ideal BIT circuit should:

- not influence the high frequency RF circuit performance
- not consume much chip area or power
- have high sensitivity and can detect the weak RF signal
- have wide operating frequency range
- reflect necessary information, such as gain and linearity of the tested RF circuit

This work presents an embedded on-chip CMOS BIT detecting circuit for the testing of RF integrated circuits and systems. By using a charge pump rectifier with positively biased low-threshold-voltage MOS transistors acting as rectifying diodes, this detecting circuit has higher sensitivity and has no influence on the performance of the attached RF circuit. Meanwhile, this detecting circuit has high scalability and can be used in even higher operating frequency. By utilizing this circuit, the high frequency output signal of RF circuits can be transformed into DC signal and can be tested easily by using low frequency or DC testing instruments, which can improve the efficiency to a large extent. This circuit can give the information such as gain and linearity and can be used to characterize the performance of many RF systems and circuits.

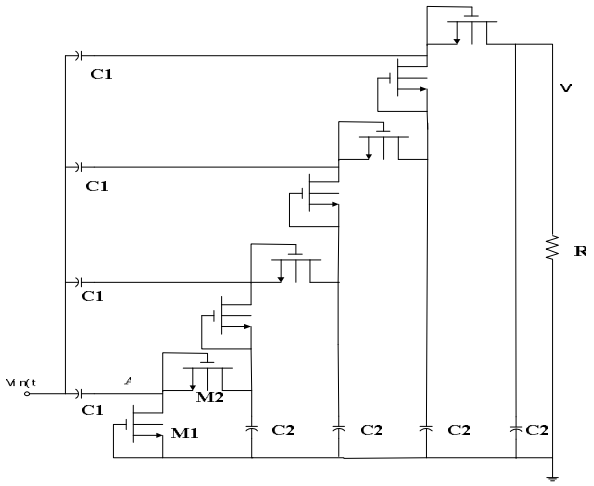

Fig.2 four-stage charge pump rectifier with low threshold voltage substrate-positively-biased MOS devices

BIT Detection Circuit

The BIT detecting circuit, which is illustrated in Fig.2, is a charge pump rectifier configuration like the one in [15], and four stages are adopted. This circuit can transform the input high frequency signal to DC signal by using the diode-connected MOS transistors and capacitors. In order to detect the low input signal amplitude, a lower turn-on voltage for the diode is required. Capacitor C_1 and diode-connected MOS transistor M_1 shift the voltage $\upsilon_{in}(t)$ up at A and C_2. Diode-connected MOS transistor M_2 rectifies the voltage at A (AC and DC components). After a short transient, equilibrium is reached and the circuit enters its steady state mode. In this mode, the rectifier delivers a constant output current and a constant output voltage. Fig.3 shows the transient dependence of output voltage on the input signal amplitude. The voltage amplitude of input signal, a_1, sweeps from 0.1V to 1V in 0.2V steps, and the operating frequency is 2.4GHz. It can be seen that this circuit can transform the input high frequency signal into DC value and the output voltage changes with the variation of input signal amplitude. Because there is no biasing voltage needed, this detection circuit is effectively a passive circuit, and a separate supply pad for the separate control of this circuit is omitted. The parameters of the components in the circuits in this design are C_1 is 100fF, C_2 700fF, and the channel length and width of MOS transistors are 0.3μm and 0.35μm respectively. Although capacitance of C_2 is a little larger, it can be used as on-chip decoupling capacitor to filter the noise coming from the supply.

The circuit parameters can be optimized to give the most optimal performance according to the requirement of the circuit specifications when the performance metrics such as the sensitivity and operating frequency, etc. are considered.

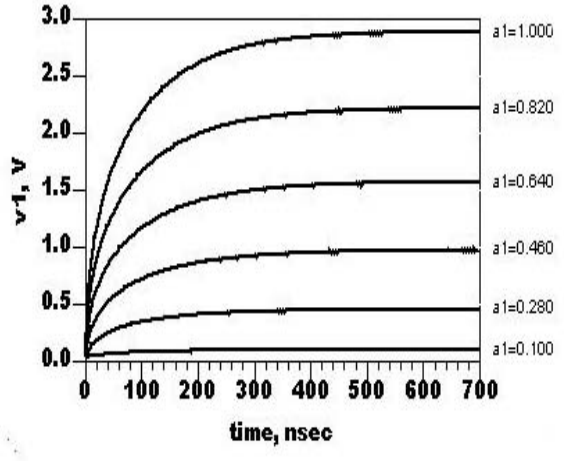

Fig.3 the transient dependence of DC output of BIT detecting circuit on different input amplitude

To improve the conversion efficiency, the threshold voltage of diode-connected MOS transistor should be low in order to detect weak RF signals. In this design, UMC 0.18um low threshold voltage MOS transistor is selected for use in the rectifier. Using this low threshold voltage MOS transistor can improve the ability of this circuit to detect weak input amplitude. At the same time, positive substrate bias scheme with 0.6V were also adopted to further reduce the threshold voltage of MOS transistor and to improve the input sensitivity of the detecting circuit, which can be seen in Fig.8.

Fig.4 investigates the frequency scalability of this BIT detection circuit and illustrates the dependence of the output voltage on the input signal frequency. The input frequency changes from 1GHz to 50GHz. The results illustrate that there is no significant change of the output DC voltage under this frequency range. This figure illustrates the high scalability of this circuit when using it to test the even higher frequency RF circuits.

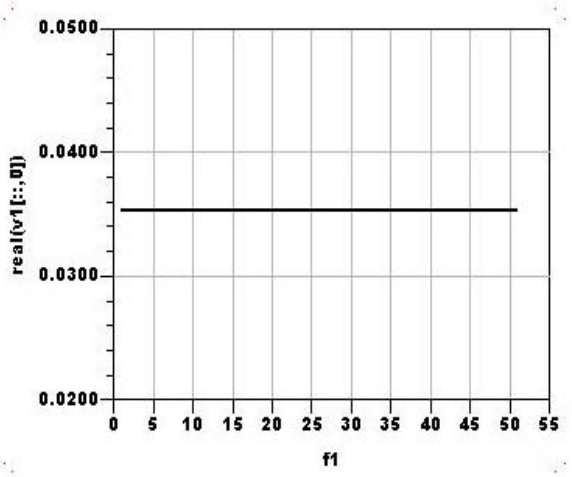

Fig.4 the dependence of DC output voltage V1 (unit: V) of the BIT detecting circuit on input signal frequency (unit: GHz)

LNA Test Example

In order to test the validity of this BIT detecting circuit for the RF systems and circuits testing, a two-stage 2.4GHz low noise amplifier with full on-chip input matching network was designed, using the UMC 0.18um mixed signal design kits. The schematic is shown in Fig 5. The small signal high frequency performance of the LNA is summarized in table I.

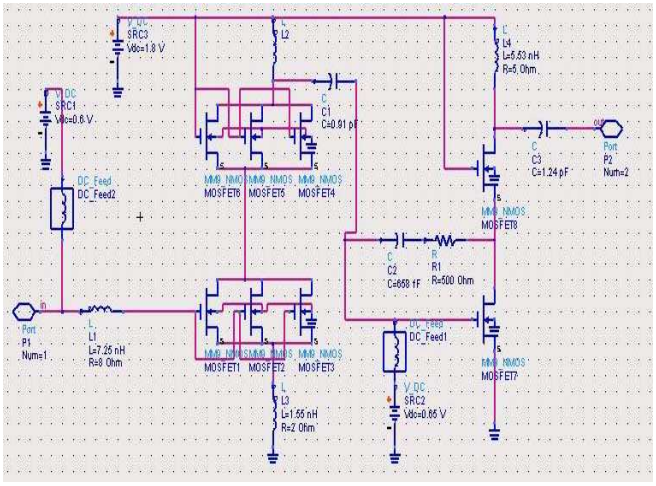

Fig.5 the schematic of 2.4GHz LNA circuit

Table I the performance of 2.4GHz stand-alone low noise amplifier

Frequency	Gain (dB)	NF (dB)	S11 (dB)	IP1dB (dBm)
2.4GHz	17.38	2.05	-7	-10

Results

Fig.6 shows the final circuit schematic, including the 2.4GHz LNA from Fig.5, the BIT detection circuit from Fig.2 and input testbench. The input signal amplitude sweeps from -40dBm to 0dBm in steps of 5dB. Fig.7 shows the output time domain signal of the detecting circuit in Fig.6. From Fig.6 it can be seen that this circuit can realize the transformation from RF output signal to DC signal with the change of input RF signal amplitude of low noise amplifier. At the same time, it has been testified that this detection circuit can operate over a wide frequency range. It is also suitable for other higher frequency RF circuits, such as power amplifier, mixer, and VGA.

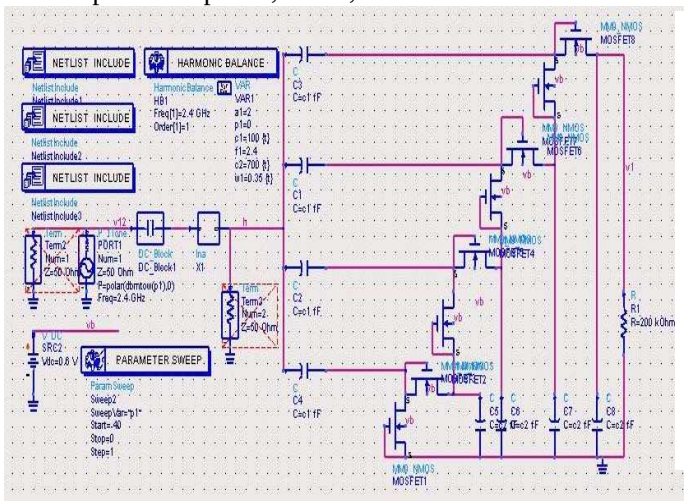

Fig.6 combined circuit schematic with 2.4GHz LNA, BIT detecting circuit and testbench

Fig.8 evaluates the effectiveness of the positive substrate bias during the transformation of RF signal into DC signal. With substrate-positively-biased diode-connected MOS transistors in the detecting circuit, for -40dBm input power, the output voltage is 42mV (marker m1 in figure 8), and for -30dBm input power, the output voltage is 99mV. While for -40dBm input power, the output voltage is 6mV (marker m2), and for -30dBm input power, the output voltage is 66mV when without using substrate-positively-biased scheme, and it can be seen that the sensitivity has been improved a lot by utilizing this scheme. So, without substrate positively biased, it can be seen that the transforming efficiency of the detecting circuit gets lower, and it is a little difficult to identify weaker input RF signal.

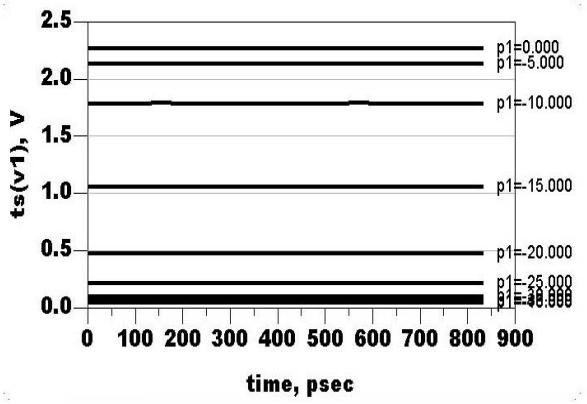

Fig.7 the output transient signal of the combined circuit in Fig.6

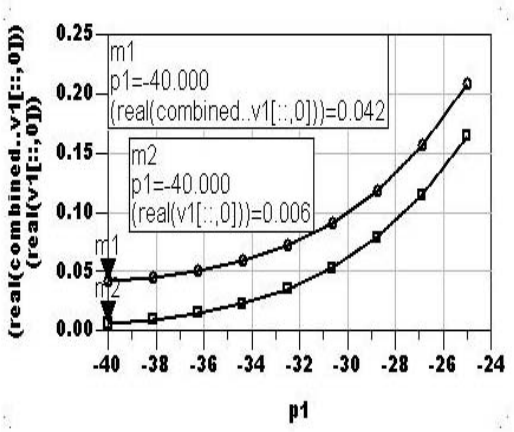

Fig.8 the comparison of output signal of the combined circuit with and without positively biased substrate of MOS transistors

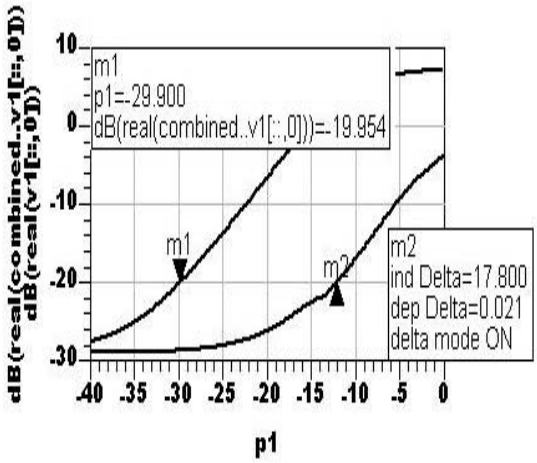

Fig.9 the gain information got from the output of BIT detecting circuit both at the input and output of LNA

Fig.9 gives the information of small signal high frequency gain of LNA which is measured by using the BIT detection circuit attached to the input of the LNA and output of LNA respectively with the control of digital switch. The curve with marker m2 is the output of detection circuit when attached to the input of the LNA and the curve with marker m1 is the output of the detection circuit when attached to the output of the LNA. The input amplitude p1 is swept from -40dBm to 0dBm in steps of 0.1dBm. The gain of the LNA can be measured as the distance in dB between marker m1 and m2 when two curves enter into linear region. It can be found that the gain is 17.8dB and has little difference with the result of stand-alone LNA performance listed in Table I.

Figure 10 is the comparison of the output of the LNA with BIT detection circuit attached and the output of combined circuit in Fig.6. It can be observed that the linearity performance from the output of combined circuit and the input 1dB compression point can be obtained from the curve of the output decibel voltage characteristics of the circuits, which is, in this example, -12.5dBm.

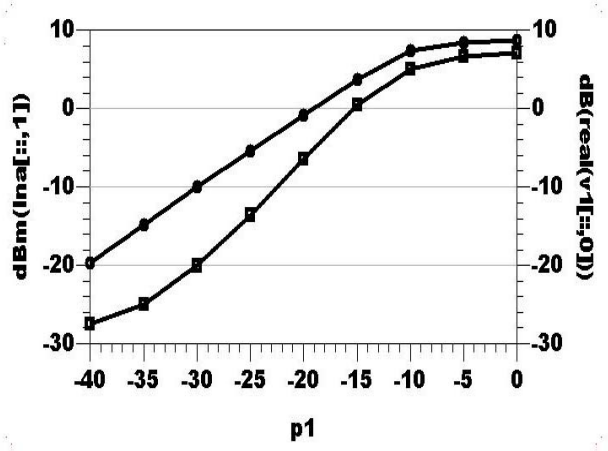

Fig.10 the linearity information of LNA output and BIT detecting circuit

Table II summarizes this 2.4GHz LNA performance with BIT detecting circuit attached in order to verify the influence of the detecting circuit on the attached RF systems and circuits.

Table II the performance of 2.4GHz low noise amplifier with BIT detecting circuit attached

Frequency	Gain (dB)	NF (dB)	S11 (dB)	IP1dB (dBm)
2.4GHz	17.35	2.05	-7	-10

From the data shown in table I and II, it can be found there is only little influence for the gain performance of the LNA circuit due to the attached BIT detection circuit.

Fig.11 shows the sensitivity of the BIT detection circuit for the weaker input signal amplitude when attached to this LNA circuit. For -50dBm input signal power, the output DC voltage is 36mV and can be measured accurately by using high resolution DC voltmeter. The maximum input signal power should not be limited by the circuit and should be related to the linearity performance of the RF circuit under test.

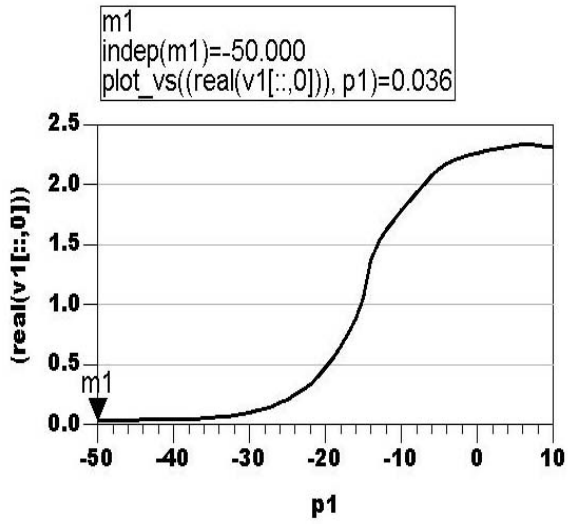

Fig.11 the investigation of the input sensitivity of the combined circuit in Fig.6

Conclusions

In this work, a fully embedded CMOS Built-In-Test (BIT) detecting circuit for RF systems and circuits is proposed. The performance metrics evaluation of the RF circuits by using this BIT detecting circuit has been described and the validity and the influence of the BIT detecting circuit on the RF circuit has been verified. In this on-chip charge pump rectifier-based BIT circuit, a low threshold voltage MOS transistor with a positively-biased substrate is used to act as diode to further improve the conversion efficiency from RF signal to DC signal. By using this circuit, the minimum input testing sensitivity can be greatly improved. In addition, this BIT circuit has a very low power consumption and remains accurate at very high frequencies. By using this method the circuit can give gain and linearity information without influencing the performance of the attached RF circuits. The achieved results show that this BIT detecting circuit can be attached to RF systems and circuits by using switch control and used to monitor the performance of the circuit without affecting the

measured RF systems and circuits.

5 Acknowledgements

This work is supported by Enterprise Ireland under the Commercialization Fund.

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