Design of Fourth Order Digital PLLs Using Filter Prototypes

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Abstract – **In this paper an investigation of different filter prototypes and their applicability to digital phase locked loop design is carried out. A novel design technique using the superior filter prototype for the 4th order Digital PLL is also introduced. The optimum choice of each design parameter is considered, while maintaining realisable component values as a priority. Finally the proposed design technique is used to design a 4th order Digital PLL with optimum filter cut-off, stability and lock time. This 4th order design method is an improvement on existing methods that exist in the literature to date, this is verified using simulation of a Digital PLL designed using the proposed technique.**

I. INTRODUCTION

The Digital PLL (DPLL) is a versatile component block widely used in electronics for operations such as frequency synthesis, clock data recovery, and demodulation. The DPLL system consists of a phase frequency detector (PFD), a charge pump (CP), and a voltage controlled oscillator (VCO), all of which are vital to the operation of the DPLL. The DPLL may also include a low pass loop filter (LF) or a frequency divider. A typical DPLL is shown in Fig. 1. The first order DPLL, with no loop filter is globally stable but produces large frequency jitter (phase noise) on the output signal that is intolerable for most applications. The solution is to include a simple RC low pass filter at the output of the CP to reduce this jitter. However discrete V_C voltage jumps still exist due to voltage jumps across the filter resistor, these are commonly attenuated by including an additional ripple capacitor (C_2 in Fig. 2) in parallel with the loop filter, increasing the PLL order to three, Fig. 2.

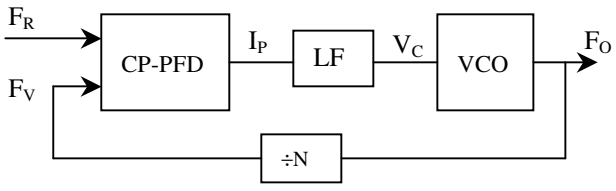

Fig. 1. DPLL Loop Block Diagram

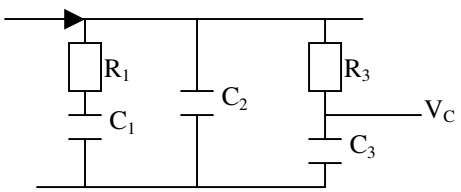

Fig. 2. 4th order DPLL loop filter structure

The loop filter performs two operations on the CP output; first it converts the discrete like current output of the CP to a continuous DC like voltage for operation by the VCO; and second it attenuates high-frequency noise on the control voltage signal. It is necessary to eliminate noise on the control voltage, as this will be represented as jitter on the PLL output signal. Higher order filters provide greater attenuation of this jitter. For the purpose of low noise operation, passive filters are preferred to active filters, however this adds some restriction on the choice of filter transfer function.

The DPLL is a highly non-linear system and is further complicated by the fact that the variable of interest around the loop changes from phase to voltage, in the PFD, CP, and LF, and back to phase in the VCO. The DPLL can be approximated to a linear transfer function by replacing the CP-PFD block in Fig. 1 with a multiplier and gain component (K_P), and replacing the VCO block with an integrator and a gain component (K_V), as in [1]. The closed loop transfer function, $H_{CL}(s)$, is expressed as in (1).

$$H_{CL}(s) = \frac{NK_V I_P F(s)}{2\pi N s + K_V I_P F(s)} \tag{1}$$

The 4th order DPLL loop filter F(s), has a structure as in Fig. 2, and is expressed as in (2) below. The passive filter structure of Fig. 2 is designed by choosing a ω_c, of approximately $1/10^{th}$ the reference frequency, ω_R, this is a rule of thumb based on recommendations and empirical results of [1]. Knowing ω_c the components R_1 and C_1 are chosen from the solution to $\omega_c = 1/R_1C_1$, and C_2 is chosen to be $1/10^{th}$ of C_1. The VCO and CP gains are then chosen using rule of thumb or a design criterion such as [1] to assure the system stability.

$$F(s) = \frac{C_1R_1s + 1}{C_1C_2C_3R_1R_3s^3 + (C_1C_2R_1 + C_1C_3R_3 + C_2C_3R_3 + C_1C_3R_1)s^2 + (C_1 + C_2 + C_3)s} \tag{2}$$

Once the low order filter components are chosen, high order elements are added to attenuate out-of-band noise. This paper uses the piecewise linear method (PWL) of [2], along with common filter prototypes to design stable 4th order DPLLs with optimum stability, lock time, and ω_c characteristics. In section II filter prototypes, as an alternative to traditional loop filters, and their adaptability to the DPLL are discussed. In section III a novel design technique is proposed. The proposed technique uses filter prototypes to place filter poles in-band to give optimum noise attenuation. In section IV the optimum filter prototype are considered, and an example of a design is given. Finally in section V conclusions are presented.

II. Filter Prototype and System Equations

In [3] the Bessel filter prototype has been used to design the 3rd order DPLL. Bessel prototypes are specifically chosen due to its linear phase offset in the filter pass-band. This however is an unnecessary requirement as the DPLL reference frequency is constant, and any phase offset is corrected during the operation of the DPLL. This is verified by comparing the phase offset of the traditional DPLL to filter prototype phase offsets in the pass-band, as in Fig. 3 for a cut-off frequency of 10 MHz. It is clear that the traditional DPLL has a phase offset that is much more non-linear in the pass-band then the selected prototypes. For this reason the design method need not be restricted to the Bessel prototype but may also include frequency selective prototypes such as Butterworth and Chebyshev. The application of each of these filter prototypes is considered and compared in this section.

The DPLL filter prototype design method determines component values of the filter by equating the prototype transfer function denominator with the denominator of $H_{CL}(s)$ in (1). $H_{CL}(s)$ has one zero located at $s = -1/R_1C_1$ and in the case of a forth order DPLL it has four poles. Because only the prototype and $H_{CL}(s)$ denominators are equated, and not the numerators, the filter prototype is required to be an all pole system with no zeros; the prototypes that match this criterion are the Bessel, Butterworth and Chebyshev type 1 prototypes.

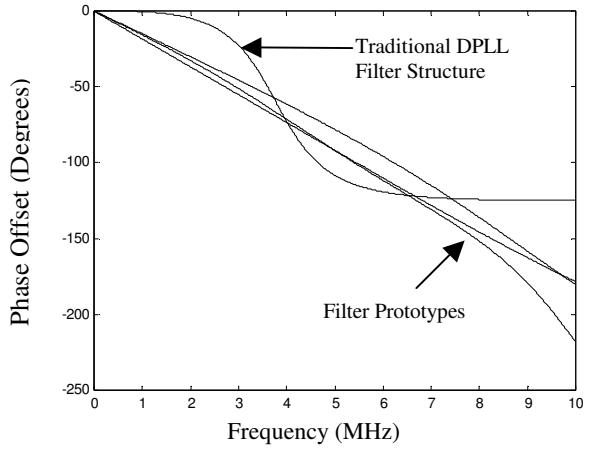

Fig 3: Phase offset for Traditional DPLL and Filter Prototypes

TABLE 1:
NORMALISED FILTER PROTOTYPE COEFFICIENTS

Prototype	Bessel	Butter	Cheby R=0.1	Cheby R=0.5	Cheby R=0.969
α	3.124	2.6131	1.804	1.197	0.9637
β	4.392	3.4142	2.627	1.717	1.464
δ	3.201	2.6131	2.026	1.025	0.7541
ε	1	1	0.8285	0.3791	0.2795
χ	1	1	0.819	0.3578	0.25

The transfer function of these prototypes is given in (3), where α, β, δ, and ε are the normalised coefficients from Table 1 above.

$$H_{BESSEL}(s) = \frac{\chi\omega_C^4}{s^4 + \alpha\omega_C s^3 + \beta\omega_C^2 s^2 + \delta\omega_C^3 s + \varepsilon\omega_C^4} \tag{3}$$

The component values of the DPLL are calculated using (4-8). These component values produce optimum cut-off characteristics for the DPLL filter structure.

$$C_1 = \frac{\beta\delta K(M_1M_2+1) - \alpha\varepsilon M_1M_2K}{N\delta\varepsilon\omega_C^2(M_1M_2 + \frac{1}{M_1})} \tag{4}$$

$$C_2 = \frac{\frac{\alpha M_1M_2K}{N\delta\omega_C^2} - C_1M_2 - C_1}{M_1M_2+1} \tag{5}$$

$$R_1 = \frac{\delta}{\varepsilon C_1\omega_C} \tag{6}$$

$$R_3 = \frac{R_1}{M_2} \tag{7}$$

$$C_3 = \frac{C_1}{M_1} \tag{8}$$

To solve (4-8) there are four unknown parameters that need to be considered, K, M_1, M_2, and ω_c. Each of these will be considered in the next section.

III. Proposed Design Technique

In this section the PWL method of [2] is used to determine the optimum choice of K, M_1, M_2 and ω_c, from the previous section, where K is equal to K_PK_V. Using the above techniques and optimised parameters, an optimum DPLL system is designed, simulated, and shown to be an improvement over existing techniques.

The forth order DPLL has six unknown component values yet the filter prototype provides only four equations, the solution to this is to introduce two ratios M_1 and M_2 (7-8). These parameters define the location of the filter pole P_4 in Fig. 4. Ideally we require that the $H_{CL}(s)$ poles be located at the same point as the prototype poles, however this is not feasible for the passive loop filter structure of Fig. 2. The poles are placed as close to the ideal location as possible.

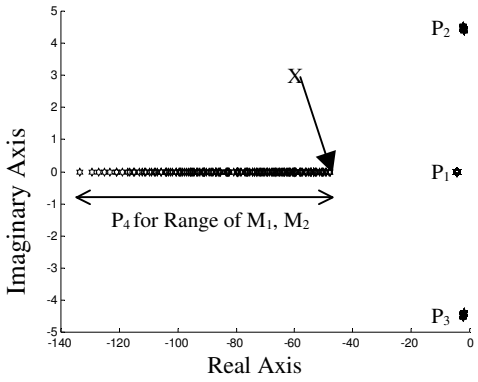

Fig. 4. Pole Locations for range of M_1 and M_2

Fig. 4 shows that increasing M_1 and M_2 causes pole P_4 to move and P_1, P_2 and P_3 to remain constant. Similarly Fig. 5 shows that varying M_1 and M_2 affects the roll-off of the system magnitude. Ideally we require a value of M_1 and M_2 that will produce the sharpest roll-off and therefore best filter cut-off characteristics. This occurs at the point where P_4 is closest to P_1. The trajectory of P_4 as M_1 and M_2 change is irregular, it initially moves closer to P_1 for increasing M_1 and M_2. When P_4 reaches the point X, in Fig. 4, the pole turns and moves away from P_1. The optimum choice of M_1 and M_2 is the point where P_4 lies at X. The optimum location is determined from the denominator of $H_{CL}(s)$. If the denominator of $H_{CL}(s)$ is D(s), as in (9), then the minimum value of P_4 occurs at a minimum value of A, where A is shown in (10) below.

$$D(s) = s^4 + As^3 + Bs^2 + Cs + D \tag{9}$$

The minimum point can be determined by solving A for all M_1 and M_2. Equations (4-8) are dependent on the choice of gain K. If we solve $H_{CL}(s)$ in (1) using (4-8) we find that

$$H_{CL}(s) = \frac{NKnum}{NKden + Knum} \tag{11}$$

The K's in (11) all cancel, so $H_{CL}(s)$ is independent of K, any change in K is reflected by a proportionate change in the component values.

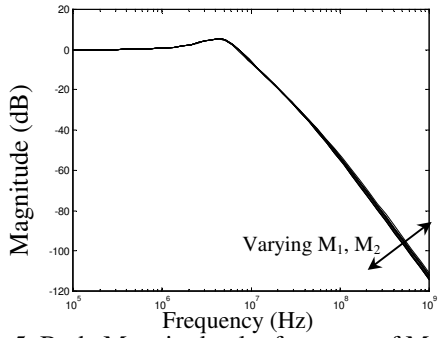

Fig. 5. Bode Magnitude plot for range of M_1 and M_2

This has the effect of keeping the system poles in their optimum location making K insignificant with respect to the system response. However K has an effect on the filter component values (4-8) and is chosen solely to achieve realisable values.

The choice of ω_C is crucial for a stable DPLL system design. Traditionally it was suggested to choose ω_C to be at least $1/10^{th}$ of ω_R, otherwise the CTA would become invalid and the loop filter would pass large amounts of in-band noise causing instability in the DPLL. The traditional choice of ω_C, from [3,4,5] is plotted against the normalised system lock time ($t_{LCK}F_R$), as dots in Fig. 6, and has a minimum ω_C/ω_R ratio of $1/13^{th}$. Ideally we require a ω_C close to ω_R, to reduce out-of-band noise, but the CTA must still be valid. Using the PWL method we can determine the DPLL lock time as ω_C approaches ω_R. This is shown in Fig. 6 as a line for a range of ω_C/ω_F. In Fig. 6 the CTA begins to break down at ω_C/ω_R greater then 0.1. The system lock time is also reduced as ω_C approaches ω_R. Also we know that the out-of-band noise attenuation will be greater the closer ω_C is to ω_R. Therefore we require ω_C to be as close to ω_R as possible, but avoiding the CTA break down point. Identification of the breakdown point can improve the design process. This is achieved using the PWL numerical solution method of [2].

Using (4-8), choosing the optimum ω_C close to ω_R for minimum lock time, and finally choosing optimum M_1 and M_2 for the sharpest roll-off, an optimum, stable, and realizable 4^{th} order DPLL is designed. This is demonstrated in the next section.

IV. Optimum Filter Prototype and Design Example

In this section each filter prototype from Table 1 is considered. The best filter prototype is then applied to the design method of the previous section. In Fig. 7 the lock time (dashed line) and steady state error (continuous line) for each prototype is shown.

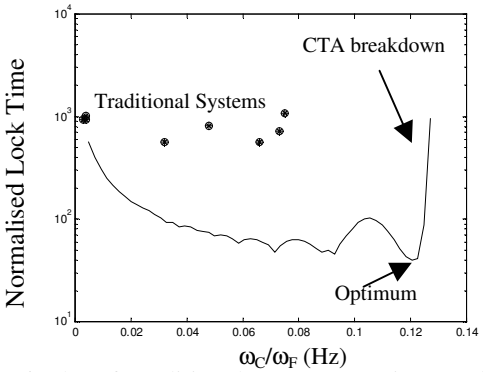

Fig. 6. Plot of Traditional DPLL ω_C against Lock Time

$$A = \frac{\omega_C\left(M_1M_2+1\right)}{\delta}\left[\frac{\left(M_2+1\right)\left(\beta\delta\left(M_1M_2+1\right)-\alpha\varepsilon M_1M_2\right)}{\alpha\varepsilon\left(M_1^2M_2^2+M_2\right)-\left(M_2+1\right)\left(\beta\delta\left(M_1M_2+1\right)-\alpha\varepsilon M_1M_2\right)}\right] \tag{10}$$

It is clear from both plots that the Chebyshev filter returns the best results for both lock time and steady state error for all Chebyshev ripple parameters, R. As discussed earlier the value of K is insignificant in terms of the system response and is chosen here using traditional rule-of-thumb, the values are K_V = 62.8MHz/V and I_P = 10μA. The filter ratios M_1 and M_2 are chosen to produce the lowest possible lock time and optimum location of P_4. The value of R allows the designer to trade-off between faster lock time and better steady state error. As R is increased ω_C approaches ω_R, this is illustrated in Fig. 8. The lock time and steady state error can be varied by optimally choosing R. Fig. 9 shows the lock time (dashed line) and steady state error (continuous line) for a range of R. The minimum lock time and steady state error is found to occur at a value of R equal to 0.707.

Consider the design of a 20MHz DPLL system using the proposed design method. This system has a feedback divide ratio of 10, and gains K_V = 300 MHz/V and I_P = 10μA. A Chebyshev filter prototype with an R of 0.707 is used. The optimum choice of M_1 and M_2 are found using the PWL method to give optimum lock time and optimum location of P_4. For this particular system M_1 is chosen to be 12, and M_2 is 1.4. From these chosen parameter values the filter components are calculated to be C_1 =12.4pF, C_2 = 1.98pF, C_3=1.04pF, R_1=17.3kΩ and R_2=12.4kΩ. The response of this system is demonstrated in Fig. 10.

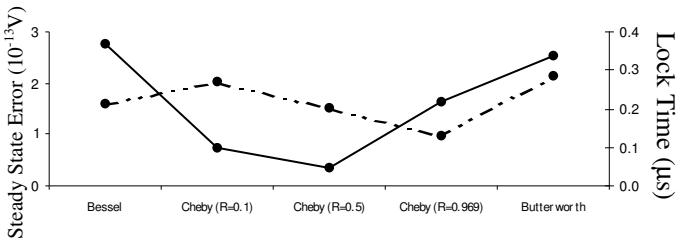

Fig. 7. Lock Time and steady state error for Filter Prototypes

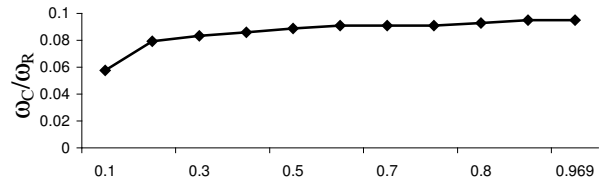

Fig. 8. ω_C/ω_R for range of R parameter

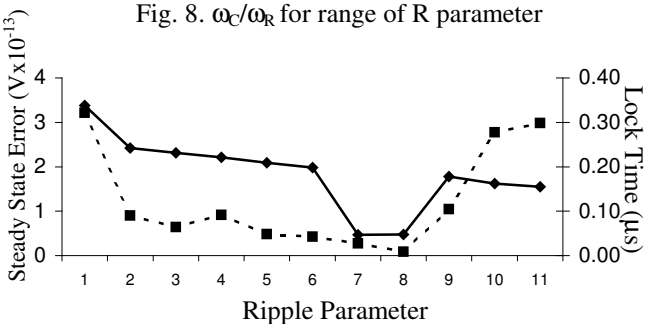

Fig. 9. Lock Time (dashed line) and steady state error (continuous) for Chebyshev filters

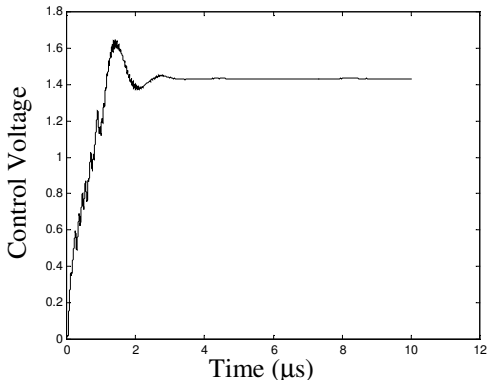

Fig. 10. System Response of a 20MHz 4th order DPLL

V. CONCLUSION

In this paper filter prototypes are used to design a 4th order DPLL. The system components are found by the optimum choice of ω_C and filter ratios M_1 and M_2. The optimum values for steady state error, lock time and sharp filter roll-off are found through the numerical of (10) and the PWL model of [2]. The Chebyshev, Bessel, and Butterworth filter prototypes are each considered and the best filter prototype is found to be the Chebyshev with a ripple value of 0.707. Using this Chebyshev filter and the optimum ω_C, M_1 and M_2, a stable, fast locking, low noise 4th order DPLL is demonstrated.

ACKNOWLEDGEMENTS

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