AN ARCHITECTURE FOR A RECONFIGURABLE CHARGE-SUMMATION BASED ADC

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Abstract

Presented in this paper is a low power, area efficient reconfigurable analog-to-digital (ADC) converter, utilising a charge-summation technique with a switched-capacitor implementation. Using a non-inverting switched-capacitor integrator a staircase ramp is produced using switching capacitors and a fixed reference voltage, as opposed to a linear ramp. The advantage of the charge summation technique is the reduction in power usage as the charging time of the capacitors is small so for most of the sample period the circuit is quiescent. The paper presents the use of this architecture as a reconfigurable ADC for use in a reconfigurable radio.

1 Introduction

High speed, low-power and high resolution are the desired characteristics of modern ADCs for communications and signal processing systems. Resolutions of fourteen bits or greater at MHz sampling rates have proven difficult to design. Pipelining, which involves the cascading of several lower resolution ADCs was introduced to address this problem. Most modern pipeline ADCs are comprised of flash type sub ADCs. Though SAR and ramp type pipeline ADCs exist, they are usually not chosen due to either the faster performance of flash type ADCs [1,2] or the higher resolutions of sigma delta converters [3,4]. Usually the type of ADC chosen is dependent on the application requirements.

For example, video applications require 6-bits of resolution at speeds of 200MHz. For such an application a flash ADC is chosen. An ADC, which can be easily reconfigured to provide either higher resolution or higher speed, is therefore desirable.

This paper presents an ADC architecture, which has the potential to operate at sampling rates in the MHz range and can achieve resolutions of up to 14-bits. The architecture of the ADC is easily reconfigurable which makes it useful for implementation in such areas as reconfigurable radio. The simplicity of the design ensures a relatively low component count, thus savings in terms of area and power are achievable. Attempts to scale ADCs in accordance with technology often encounter limitations in the analog sections. For conventional architectures, one of the main scaling limitations arises from the need for high gain op-amps or precisely matched components. Our final charge summation circuit displays good robustness to such limiting factors.

Another big problem faced by high-resolution data converters is that of thermal noise, which becomes the dominant noise source. To increase the resolution even further requires an exponential increase in power consumption. To increase the resolution by 1 bit and maintain the same SNR requires the noise power to be reduced by 6dB. This means that the sampling capacitor size needs to be increased by a factor of four. This issue of thermal noise is addressed in this paper using a proposed technique for sampling noise reduction [5].

Section 2 of this paper discusses the basics of charge summation ADCs and the novelty of the proposed design. Section 3 covers the implementation of the basic charge summation ADC into different multi-stage configurations. An example ADC with its specifications is shown in section 4 followed by conclusions.

2 Single Stage Charge-Summation ADC

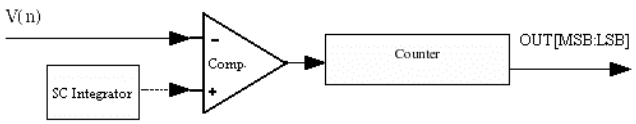

Figure 1: Single Stage SCCS ADC

2.1 Charge Summation ADC

Charge summation based ADCs are similar to more traditional ramp-based converters, except the ramp is generated by the discrete accumulation of charge on a capacitor. Charge summation is performed through using a switched-capacitor integrator to produce a stepped ramp. This ramp forms one input to a comparator, which compares the ramp voltage to that of a sampled signal as shown in figure 1. The number of clock periods required by the ramp to trigger the comparator is proportional to the amplitude of the input signal. The resolution of the converter is dependent on the step size of the ramp and the performance of the

comparator. The reference voltage controlling the ramp step size can be digitally controlled, providing an easy mechanism for calibrating the ramp for offset and gain errors.

Switched-capacitor charge-summation (SCCS) based converters were proposed in the late 1980's [6] but never gained acceptance due to the more robust performance of sigma-delta modulators. However SCCS converters have several advantages over other converters. They have high linearity, monotonicity, simplicity of design, and have inherent self-test capabilities. In addition, many of the design challenges that restricted performance in the past have been overcome due to improvements in process technology and design techniques over the past fifteen years. For example, a major challenge in the past in SCCS systems was maintaining the linearity of the staircase due to finite amplifier gain in switched capacitor circuits [7]. This problem has been addressed by using a finite gain and offset compensated SC integrator, such as proposed by Ki [8]. Switched-Capacitor Charge Summation Circuit

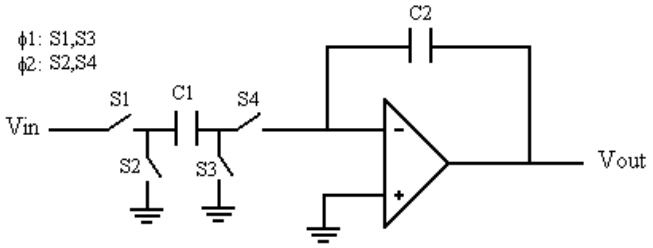

Figure 2: A switched capacitor integrator

Switched-capacitor charge summation utilises a low performance amplifier and a reference voltage source to create a staircase ramp with regular step size and spacing as shown in figure 2. The architecture shown is that of a parasitic-insensitive non-inverting switched-capacitor integrator. This ensures that a positive input control voltage will result in a staircase with positive slope. The advantage of this architecture is that the parasitic capacitances don't affect the charge transfer between the integrating capacitors; they affect the settling time behaviour of the circuit. Ideally the input/output characteristic of the SC integrator may be represented by

$$V_{out}(n) = \left(\frac{C_1}{C_2}\right) V_{in} + V_{out}(n-1) \qquad (1)$$

The z-domain equivalent of the circuit is

$$V_{out}(z) = \left(\frac{C_1}{C_2}\right) z^{-1} V_{in}(z) + z^{-1} V_{out}(z) \qquad (2)$$

giving the transfer function:

$$H(z) = \frac{V_{out}(z)}{V_{\text{in}}(z)} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1} \qquad (3)$$

The step size is dependant only on the capacitor ratio and the value of the input control voltage. A valuable advantage is that if the capacitors are mismatched, the gain offset can be corrected by altering the control voltage, ensuring performance. In a single-stage design, the required step size for 14-bits of resolution and a 1V power supply would be 61μV. Achieving this degree of resolution would be difficult due to noise. This can be simplified by using a large capacitor ratio on the integrator, for example a capacitor ratio for C1/C2 of 100, would allow a 6.1mV control voltage to be used.

2.1 Finite Gain

The main limitation, affecting a 14-bit switched-capacitor integrator is the effect of a finite op-amp dc gain and offset. Though the offset can easily be cancelled, the effect of the gain can only be reduced. Equation (4) shows the effect of finite op-amp gain on the output characteristic of the integrator

$$V_{out}(n) = \left(\left(\frac{C_1}{C_2}\right) \times V_{in} + V_{out}(n-1)\right)\left(\frac{1}{\left(1+\frac{1}{A}\times\beta\right)}\right) \qquad (4)$$

where β is the feedback ratio defined as 1+C1/C2 and A is the amplifier dc gain. Finite gain has the effect of reducing the influence of the previous steps, such that the ramp deviates from the ideal linear ramp as shown in figure 4, where the gain is 80 dB for a 14-bit ramp. Using a finite gain compensated circuit (figure 3) such as the one proposed in [8] equation (4) becomes:

$$V_{out}(n) = \left(\left(\frac{C_1}{C_2}\right) \times V_{in}\right)\left(\frac{1}{1+\frac{1}{A}\times\beta}\right) + V_{out}(n-1)\left(\frac{1}{1+\frac{2}{A^2}\times\beta}\right) \qquad (5)$$

This shows that the effect of the finite gain on the input value remains the same, but it's effect on the stored voltage is reduced to $2/A^2$ as opposed to just 1/A. The finite gain compensated ramp is superimposed on figure 4 to show the improvement in linearity.

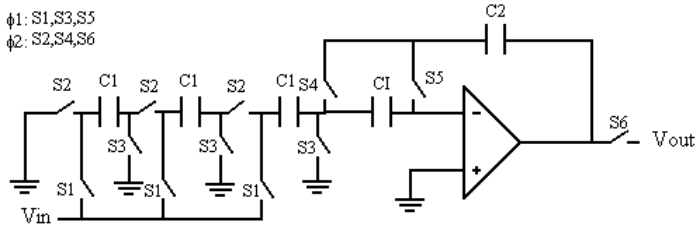

Figure 3: Finite gain and offset compensated SC integrator with thermal noise reduction

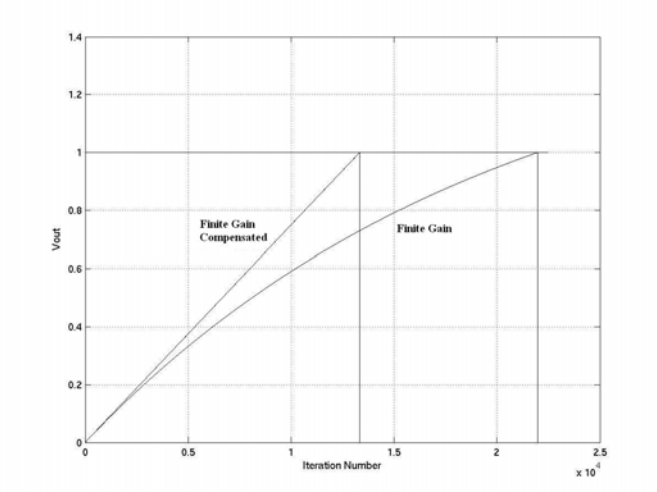

Figure 4: Effect of finite gain on ramp's linearity

2.2.1 Noise

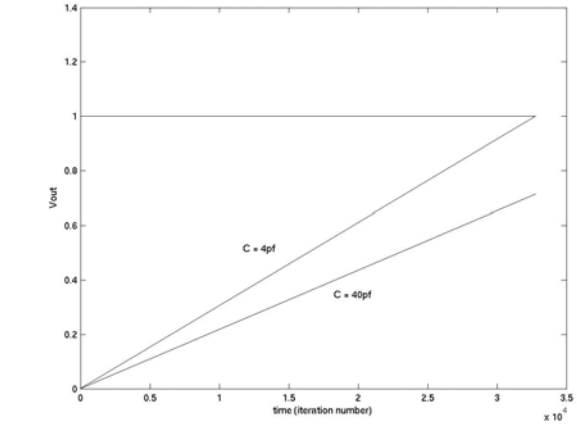

Figure 5: Effect of capacitor size being too large

The choice of capacitor values in the SC circuit has implications for the thermal noise, which is the dominant noise source, as well as for the speed of operation. The relationship between the noise and the speed is an inverse one. Clock jitter manifests itself as noise on the output of the pipeline stages. However, with current values for clock jitter in the range of pico seconds it does not become evident in this design. The same argument can be made for clock feed through errors, which are greatly reduced through the use of transmission gates. As stated in [6] thermal noise arising from sampling and storing the control voltage 2^p times, where p is the resolution of a certain stage is given as

$$V_{Noise} = \sqrt{\left(\frac{2^p kTC_1}{C_2^{\,2}} \times \frac{1}{OSR}\right)} \qquad (6)$$

where OSR is the oversampling ratio. Choosing to C_2/C_1 ratio to be equal to 2^p, this equation simplifies to

$$V_{Noise} = \sqrt{\left(\frac{kT}{C2} \times \frac{1}{OSR}\right)} \qquad (7)$$

The smaller the capacitor used here, the larger the noise. For the case of the circuit presented in figure 2 the OSR = 1 thus we have:

$$V_N = \sqrt{\left(\frac{kT}{C2}\right)} \qquad (8)$$

The speed at which the SC integrator can operate is also determined by the size of the capacitor used i.e. the time required for the capacitor to achieve almost complete charge transfer. The problem with using too large a capacitor for a speed of 1Msps is depicted in figure 5. For a 1Msps sample rate and a maximum stage resolution of 6 bits, for the capacitor to charge to 95% of the input voltage requires a charge period of T = 8ns. This means that the capacitor value is governed by the inequality (assuming a switch resistance of R = 300Ohms):

$$C < -\frac{T}{\ln(1-0.95)\cdot R} \Rightarrow C < 9\,pF \qquad (9)$$

Choosing C1 and C2 to be 0.4pF and 3.2pF respectively creates a 3-bit ramp, while 0.2pF and 3.2pF yield a four-bit ramp. The thermal noise experienced using such capacitor values works out to be .03598mV, which is less than the LSB step size of 0.1526mV ($2.5/2^{14}$), so the noise isn't larger than the resolution of the ADC. The effect of thermal noise can be reduced even further through the use of spatial time oversampling as proposed in [5]. Spatial oversampling reduces the noise power by a factor of n i.e.

$$V_N^{\,2} = \frac{kT}{nC} \qquad (10)$$

where n is the number of sample capacitors used. Say n = 3 the thermal noise is reduced to .02077mV, thus improving the ADCs performance The modified SC integrator circuit, which uses spatial time oversampling and is compensated for finite op-gain and offset effects is shown in figure 3.

As demonstrated, the SCCS circuit has improved robustness to finite gain and noise. The need for precisely matched components in this circuit is also reduced as any mismatch between the capacitors can be easily compensated for through varying the input control voltage. These common problems involved with scaling technology are therefore reduced.

3 Multi-Stage Charge-Summation ADC

3.1 Scalability

One of the main advantages of the proposed charge-summation ADC is its scalability. The resolution and particularly the speed can be improved through creating multi-stage ADCs such as pipelined and time-interleaved architectures. A multi-stage implementation means that a lower resolution ramp can be used. Since the finite gain effect is proportional to the amount of steps in the ramp, its influence can be reduced even further through using such architectures.

The simplicity of the design ensures a small overhead for implementing these architectures. Due to the nature of the steady-state value for the analog signal, it is possible to easily share the reference signal between the various stages. In other words, if stages are of the same resolution then they can all utilise the one SC integrator output. The only additional circuitry per stage is one comparator, along with sample and holds and the standard pipeline residue calculation and amplification circuitry.

3.2 Pipelining

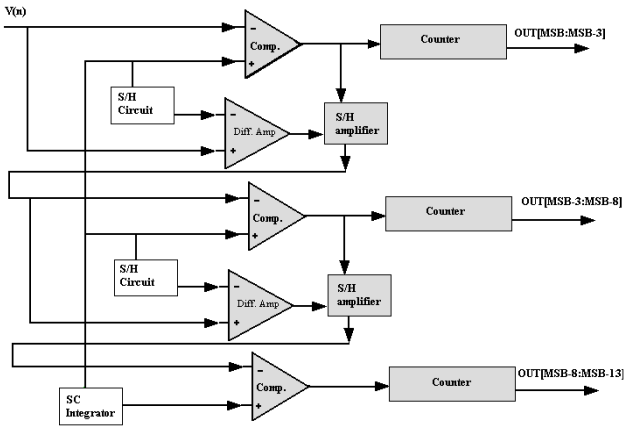

Figure 6: The pipeline SCCS ADC architecture

The available resolution of a charge summation ADC is proportional to the speed at which it can operate. The resolution in a charge summation based converter is dependent on the step size of the ramp. As this is reduced, the number of steps required to reach full scale is increased, providing increased resolution. Sigma-delta technology replaced charge-summation techniques in the late 1980's due to higher resolution available through oversampling and their more complex architectures. However this increased complexity comes at a cost, and sigma-delta architectures are less suitable to pipelined implementations. Sigma-delta modulator based converters require significant oversampling and are unsuitable for pipelining. This has tended to reduce their application to lower frequency or baseband applications. A pipelined SCCS-based converter should provide a superior combination of power; sampling rates and resolution with less latency than experienced in sigma-delta modulator based systems. A diagram of a pipelined SCCS converter is shown in Figure 6.

Pipelining several lower resolution SCCS converters provides many key advantages, which combine to make it a feasible alternative to present ADC architectures. Large savings in power and area are made if the design requires that the pipeline stages have the same resolution (e.g. three five-bit stages). The stages can therefore utilise the same ramp and so only one SCCS integrator is required. This improves matching between stages. The only additional circuitry required for pipelining is a stage comparator and the standard residue calculation/amplification blocks. The actual pipeline architecture that is used is slightly varied from that of general pipelines. The nature of the sub ADC with it's analog ramp output makes it unnecessary to employ a sub DAC, thus eliminating what is a common source of error in conventional pipelines. The ramp output can simply be subtracted from the input signal to obtain the residue of a particular stage.

A direct result of pipelining is the reduction in the required resolution of each ramp and thus the influence of finite op-amp gain. This contributes to a low power and area efficient pipeline architecture.

3.3 Time-Interleaving

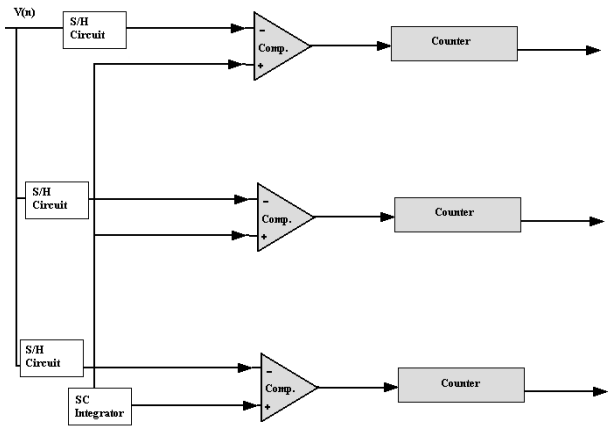

Figure 7: Time-interleaving ADC architecture

Using time interleaving in A/D conversion allows for an increase in the sampling rate. Time-interleaved ADC systems are an effective way to implement a high sampling rate ADC with relatively slow circuits. One way in which time interleaving can be used is to oversample a signal, so an average value can be obtained and so reduce the effect of noise on the input signal, thus increasing the accuracy of the overall ADC. The other main use is that each channel takes a sample during periods defined by the overall system clock. Comparing the sampling rate of a time-interleaved converter with that of a single converter, the number (N) of ADCs in parallel increases the sampling rate by approximately a factor of N. Writing this mathematically:

$$F_{SYSTEM-CLK} \approx \sum_{n=1}^{N} f_{ADC}(n) \qquad (11)$$

So, basically, the converters are operated at a frequency of

$$f_{ADC} = \frac{F_{SYSTEM-CLK}}{N} \qquad (12)$$

The speed requirements of the converters are relaxed by a factor of N but at the same time the number of converters increases. Figure 7 shows a time-interleaved configuration. This diagram differs from a typical time-interleaved ADC as it can share the same ramp between the various channels. This again saves die area but also means that each channel should display the same accuracy if the comparators are closely matched. The only additional circuitry required for increasing the number of ADCs is 1 sample and hold and 1 comparator per channel. This greatly reduces the problem of mismatch (such as gain and offset) between the channels though they are still present in the channel sample and holds. The other problem associated with time interleaving is the delay skews between the clock signals to the S/H circuits of the different channels.

3.3.1 Offset Mismatch

This mismatch causes a fixed pattern noise in the ADC. With offset mismatch a DC input on each channel could produce a different output code from each one. The effect on the S/N ratio of the ADC due to offset is independent of the input frequency but is related to the sample frequency. From [9]

$$f_{noise} = \frac{k \times f_s}{M} \qquad (13)$$

Where M is the number of channels and k = 0,1…M-1.

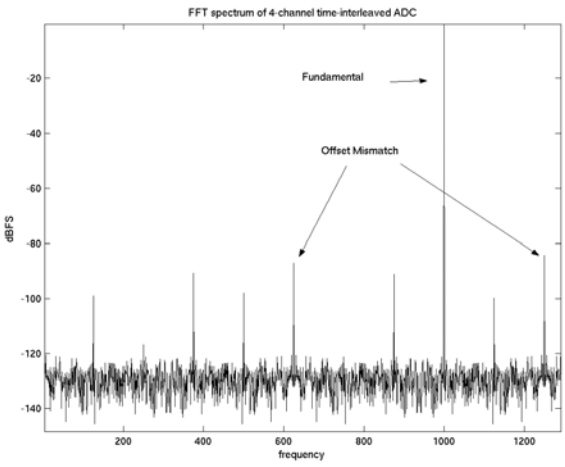

Figure 8: The effect of offset mismatch

3.3.2 Gain Mismatch

Unlike the offset mismatch effect, gain mismatch doesn't produce a fixed pattern noise, the resultant noise is highly dependent on the input frequency. The pattern noise caused by gain mismatch is given by [9]

$$f_{noise} = -f_{in} + \frac{k \times f_s}{M} \quad (k = 1,2,3,...) \qquad (14)$$

Where M is the number of channels and k = 1,2…M-1.

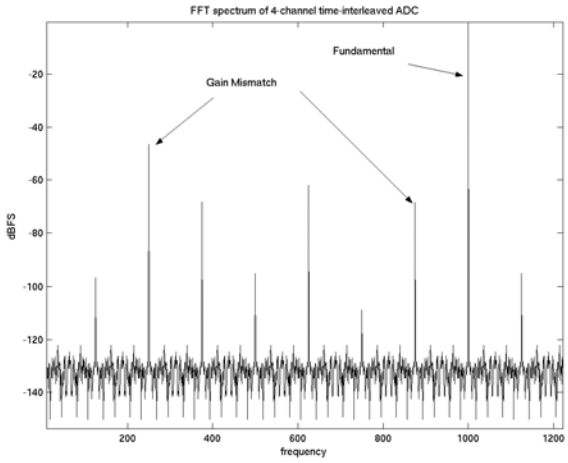

Figure 9: The effect of gain mismatch

3.3.3 Sample-time Error

Deterministic sample-time errors between time-interleaved channels generate nonlinear distortion and degrade SFDR [10]. There are two types of timing errors in time-interleaved ADCs, clock jitter and clock skew. Clock jitter effects cannot be compensated for, as its presence is totally random. Clock skew error on the other hand occurs because of imperfections in sampling circuits or because of other factors such as circuit temperature. The resulting sampling instances differ from the ideal ones. This results in noise in the ADC, and for obvious reasons this error is largest when the signal crosses zero. So the overall effect of sample-time is to raise to noise floor in the frequency domain.

3.3.4 Noise Shaping

As stated above the effects of gain and offset mismatch between the channels manifests itself in the frequency domain as spurious peaks that are related to the sample frequency as shown in equations (13) and (14). Degradation of the SFDR through these distortions reduces the accuracy of the ADC, to a greater extent than noise. What is proposed is a noise-shaping modulation sequence for the order in which the channels are used. This has the effect of removing gain and offset mismatch from the band of interest, and simplifying the matching constraints on the channel sample and holds and comparators. Figure 10 shows the effect of employing such a technique to a four-channel time interleaved architecture. We

can see that the spurious peaks present in figures 8 and 9 have been virtually eliminated, though the noise floor has clearly been increased. This is the trade off with employing such a technique.

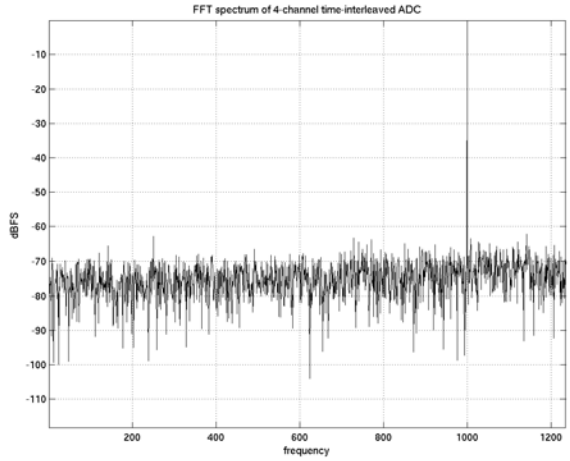

Figure 10: Noise shaping removes spurious peaks from band of interest

3.4 Reconfigurable Ability

It has been shown that the proposed ADC architecture is easily scalable through either pipelining or time interleaving. These configurations provide the opportunity to increase resolution, accuracy or sampling speed. Trade offs can be made to suit the type of standard in which the ADC will be used, at a low overhead cost. For example the speed can be increased through reducing the resolution of the ramp if that is required. Increasing the speed will obviously increase the switching and so the power requirements of the ADC will be increased. The resolution can be increased through lowering the speed requirements on the SC integrator circuit and thus allow the ramp more time to step up. This demonstrates reconfigurable ability of the architecture.

Alternating between a pipeline and a time-interleaved setup means that the resolution is reduced to improve the sampling speed. So, reconfiguring the ADC is simply a case of altering the circuit surrounding the comparators. Reconfiguring the ADC can be achieved simply through switching between the configuration of figure 6 (pipeline) to that of figure 7 (time-interleaved). The SC circuit and comparators remain unchanged; it's only the peripheral circuitry that is turned on or off.

4 Example

The circuit for a 12-bit four-channel time-interleaved pipelined ADC, which can operate at a sample speed of over 50Msps, is shown in figure 11. Each channel is a pipeline ADC with sample rate of 25Msps. Combined this gives 100Msps. The channel ADCs are four stage pipelines with stage resolutions of 3-bits, 4-bits, 4-bits and 4-bits (extra bits for digital correction). A simplified circuit layout is shown, which only shows the circuitry of stage one for illustration purposes. We can see that two-separate ramp generators are needed to due to the different stage resolutions; this does not lead to a large circuit overhead.

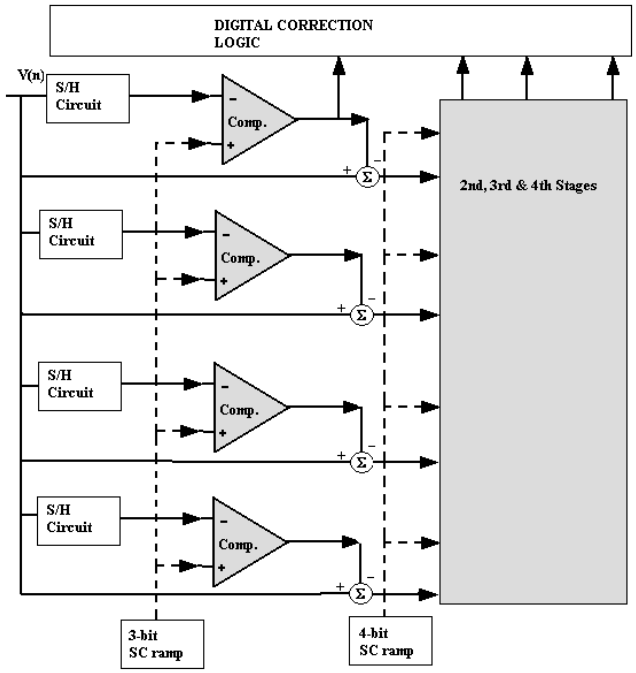

Figure 11: Architecture for a 12-bit 100Msps ADC

This converter was modelled in Matlab$_{TM}$ at 1Msps with an input signal frequency of 300kHz. The converter has the ability to operate faster but due to memory requirements only 1 million samples were simulated. The noise shaping modulation sequence as discussed in section 3.3.4 is used. The 4-bit and 6-bit ramps are produced using the finite gain compensated and noise-reduced circuit as shown in figure 3, with a finite gain of 75dB. The capacitor values chosen for the stages were C_1 = 0.4pF, 0.2pF and C_2 = 3.2pF. Other non-idealities such as comparator offset, thermal noise and clock jitter have also been added. Simulation results for DNL and INL are shown in figure 12 and figure 13 respectively. The FFT spectrum is shown in figure 14.

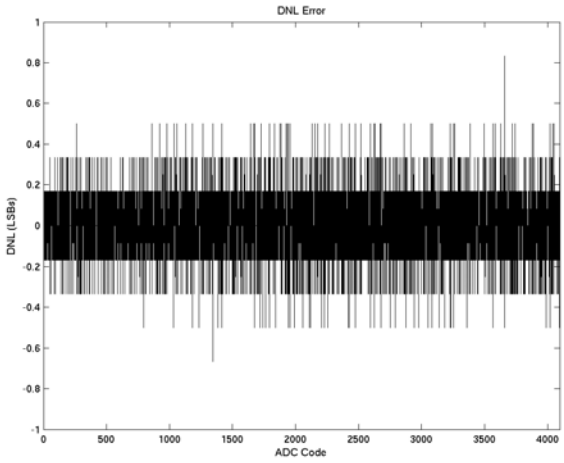

Figure 12: DNL plot for 12-bit ADC

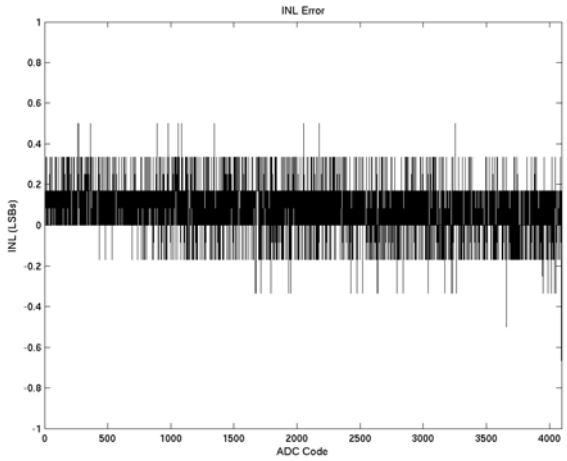

Figure 13: INL plot for 12-bit ADC

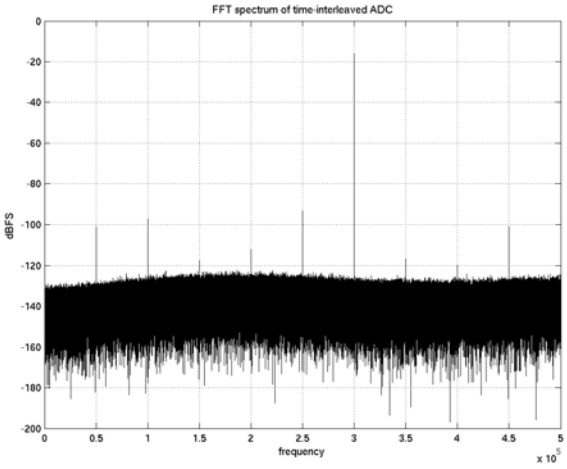

Figure 14: FFT spectrum for a 300kHz input signal.

5 Conclusion

In this paper a charge summation based ADC has been used as the key feature in a reconfigurable ADC architecture. Its ability to be reconfigured means that its operation can easily be changed between a high sample rate, low resolution ADC to a lower sampling rate and higher resolution one. This is a strong advantage other ADC architectures. For example, although it cannot achieve the same resolutions than SC sigma delta converters it can achieve higher sampling rates due to its adaptability to pipelining and time interleaving.

The component sharing aspect of the design it results in a low value for power dissipation.

Simulations show that the modelled ADC remains linear over its entire input range as shown in the INL and DNL plots. In the time-interleaved case, if the mismatch between the channels is sufficiently large, it can cause non-linearities of greater than 1 LSB on the ADC transfer function.

Acknowledgements

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