ARBITRARY ORDER CHARGE APPROXIMATION EVENT DRIVEN PHASE LOCK LOOP MODEL

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Abstract – **An alternative technique for the derivation of an event driven phase lock loop (PLL) model is presented enabling the modelling of higher order PLLs. Event driven models have previously been developed for 2nd, and 3rd order PLLs [1,2,3], however for higher order systems (5th, 6th etc.) the derivation of the loop filter difference equations are not amenable. This paper introduces a technique to model PLLs with arbitrary order filters that removes the restriction on the loop order.**

Keywords – **Phase Lock Loop, Event Driven Modelling.**

I INTRODUCTION

PLLs find widespread use in many areas of modern electronics such as disk drive electronics, telecommunications, wireless systems and digital circuits. A PLL is a closed loop feedback system where the phase of an output signal tracks the phase of an input signal. A typical Digital PLL consists of a charge pump phase frequency detector (CP-PFD), a low pass filter, a voltage controlled oscillator (VCO) and a frequency divider. Modelling these systems can be a slow, challenging process due to the combination of discrete and continuous time components and long settling times.

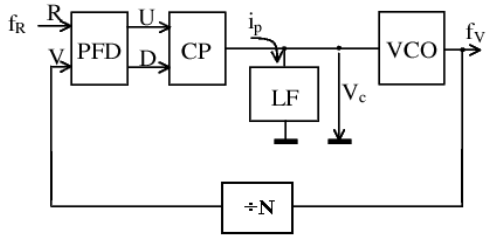

Figure 1 – CP-PLL

This work has been funded through the Enterprise Ireland, Advanced Technology Research Fund.

Hedayat et al. [1,2] and Van Paemel [3] have developed fast and accurate PLL models for 2nd and 3rd order systems. However no event driven PLL model for higher order systems (4th, 5th, 6th etc.) exists.

The event driven PLL model developed by Hedayat et al. [1, 2], provides a fast, efficient, accurate means of modelling 2nd and 3rd order systems. The advantage of such an event driven model over a circuit level simulation model such as Spice is the time taken to run one simulation. For example a full Spice circuit simulation of a PLL for 20 μs requires up to 24 hours of CPU processing time. The event driven model is approximately three orders of magnitude faster.

For higher order PLLs the derivation of the model difference equations become less amenable as the order of the loop filter is increased. In this paper an alternative technique is proposed. This uses the event driven technique, but removes the restriction on the order of the system.

In section 2 an overview of event driven modelling of the PLL is given, explaining the purpose and the advantage of using an event driven model over a circuit simulation such as SPICE. In section 3 this alternative technique to modelling is given, examples of this model are presented and verified in section 4.

II EVENT DRIVEN MODELLING

The PLL is a non-linear system. The non-linearities lie in the CP-PFD and the VCO (Figure 2). These non-linearities require modelling in the system. One such technique is to linearise. This can provide an accurate linearization of the VCO but is insufficient for the CP-PFD, particularly at higher orders.

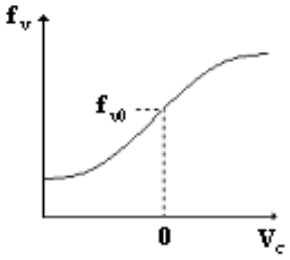

Figure 2: VCO non-linear Characteristic response

The VCO can be linearised as shown below in Figure 2, the linearization (equation (1)) will be accurate as long as the control voltage operates within the linear constraints of V_{c_MIN} and V_{c_MAX},.

$$f_v(V_c) = K_v V_c + f_{v0} \qquad (1)$$

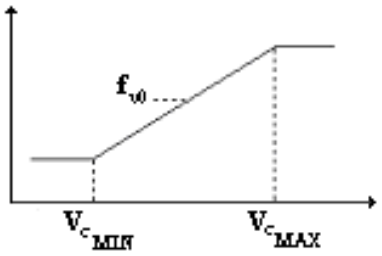

Figure 3: Linear approximation of the VCO system response

Linearising the CP-PFD introduces unacceptable inaccuracies in the model and is therefore not a viable solution [4]. However the non-linear nature of the CP-PFD can be accurately modeled using an event driven state machine as shown in Figure 4. This assumes that the PFD will always operate in one of the following three states:

1. Up (Reference Phase leads the VCO Phase)
2. Down (VCO Phase leads the Reference Phase)
3. Null (Neutral)

If the CP-PFD is in the Up state then there is a $+I_p$ current out from the CP-PFD, likewise if the state is Down there is a $-I_p$ current out, finally if the state is Null there is no current out from the CP-PFD.

The state changes after each new event detected in the system. The relevant events are the falling edges of the reference and VCO signals (Figure 4). This 'event driven' modelling technique has being previously pioneered for PLL's by [1,2,3].

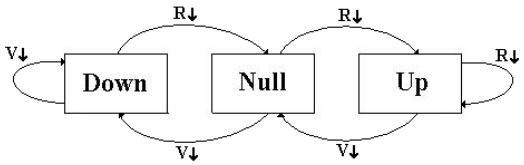

Figure 4: PFD State Diagram

An important parameter of this event driven model is the phase of the VCO and reference signals. These parameters determine the instant at which events occur in the PFD. The phase of the reference signal is calculated using equation (2) below.

$$\varphi_r(t_{n+1}) = \varphi_r(t_n) + 2\pi f_r \Delta t \qquad (2)$$

Where f_r is the reference frequency. Similarly the phase of the VCO is calculated using equation (3).

$$\varphi_v(t_{n+1}) = \varphi_v(t_n) + 2\pi\left(K_v \int_0^{\Delta t} V_c(t')dt + \Delta t f_{v0}\right) \qquad (3)$$

Where K_v is the VCO gain and f_{v0} is the VCO free running frequency. All of the parameters in equation (3), can be calculated except for the integration shown in equation (4).

$$\int_0^{\Delta t} V_c(t')dt \qquad (4)$$

For high order PLLs this cannot be solved in closed form. The technique suggested by Van Paemel [3], to solve this is a first order numerical integration approximation, equation (5).

$$\int_0^{\Delta t} V_c(t')dt = \Delta t V_c(t_n) + \frac{\Delta t\left(V_c(t_{n+1}) - V_c(t_n)\right)}{2} \qquad (5)$$

This introduces an approximation error into the model. This error can be minimized by using a small value of the time step Δt. The VCO and reference phase are calculated using the difference equations (6) and (7) below.

$$\varphi_v(t_{n+1}) = \varphi_v(t_n) + 2\pi\left(K_v\left(\Delta t V_c(t_n) + \frac{\Delta t\left(V_c(t_{n+1}) - V_c(t_n)\right)}{2}\right) + \Delta t f_{v0}\right) \qquad (6)$$

$$\varphi_r(t_{n+1}) = \varphi_r(t_n) + 2\pi f_r \Delta t \qquad (7)$$

The CP-PFD detects falling edge events of the VCO and reference signals. The VCO signal falling edge occurs when the VCO phase is equal to 2π, similarly the reference falling edge occurs when the reference phase is equal to 2π. Note that if a frequency divider is included in the feedback loop of the PLL, then the VCO signal falling edge will not occur at 2π but at 2πN, where N is the feedback divider ratio, as shown in Figure 1 earlier.

III ARBITRARY ORDER TECHNIQUE

Current event driven PLL models [2,3] determine the control voltage by iterating a difference equation over a period of time. A unique difference equation is derived for each type of filter architecture or order. These difference equations contain differential terms and become increasingly complex as the order of the loop filter increases. For filter orders of higher then 4th there is no closed form solution for the difference equation of the over all system. In this section a new model is proposed, this technique uses the charge on the capacitors, rather then the voltages at the nodes (used in [2,3]) as the state variables.

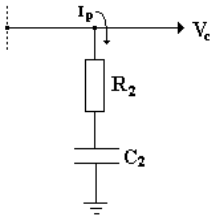

Figure 5: First order filter

For a first order RC filter the ideal response, shown in Figure 5, can be easily derived, as shown in Figure 6.

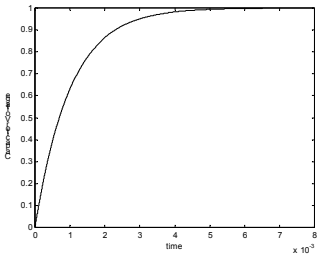

Figure 6: Ideal RC filter response

There is an alternative technique to determine the RC filter response by numerically integrating the current using the rectangular rule to determine the charge at time t+1.

In Figure 7 below, the current, I through the capacitor C at time t+1 is required, while the current at time t is known. We know that the voltage on the capacitor V_{t+1} is equal to the change in charge over time period Δt divided by the capacitance, equation (8).

$$V_C(t+1) = \frac{\Delta Q_C}{C} = \frac{Q_C(t) + I_{ave}\Delta t}{C} \qquad (8)$$

For a fixed Δt step size, all parameters on the right hand side of equation (8) are known except $I_{ave.}$ If I_{ave} can be approximated then $V_c(t+1)$, the control Voltage, can be found.

The assumption made is that the average current I_{ave} through a capacitor during the period Δt is equal to the current at time t (Figure 7).

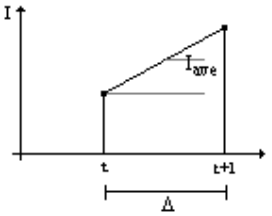

Figure 7: Assumption that current at time t is equal to the average current during Δt

This simplifies the calculation of the V_c, as there are no differential terms, making it significantly easier to increment the model to any arbitrary order. The error introduced through the model is bounded, it tends to zero as the time interval Δt tends to zero as shown in Figure 8a and 8b.

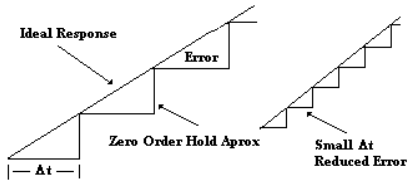

Figure 8: (a) Zero order hold approximation with large Δt, (b) smaller Δt smaller Error

In Figure 9, the error between the ideal and approximated response of an RC filter is calculated at three different capacitor voltages for a range of step sizes. It can be seen that the error introduced due to the charge approximation on the RC filter reduces to zero as the step size is reduced.

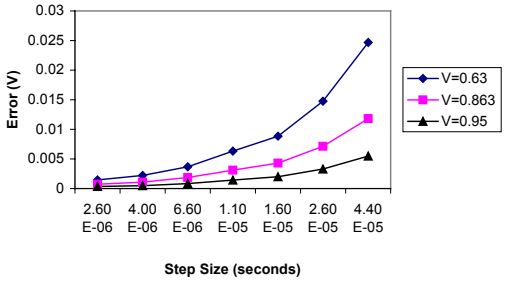

Figure 9: Increasing Error with Increasing Step Size at Three different Voltages

In the PLL model proposed here the set of difference equations used to calculate of the control voltage V_c, are derived using this technique to approximate the charge on the filter capacitors. For example, a PLL with a first order filter, as in Figure 5 has the set of difference equations as shown in equations (9) and (10).

$$Q_2(t+1) = Q_2(t) + I_p\Delta t \qquad (9)$$

$$V_c(t+1) = I_p R_2 + \frac{Q_2(t+1)}{C_2} \quad (10)$$

Where Δt is the time step, and Q_2 is the charge on the capacitor C_2.

Higher order filters can be easily accommodated using this technique, as demonstrated by the second order filter shown in Figure 10.

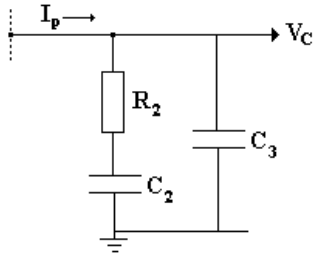

Figure 10: Second order filter

For this 2nd order filter, the control voltage V_c can be found similarly for any time t_n using equations (11)-(15).

$$I_2(t_{n+1}) = \frac{\Delta t C_2 I_p - C_2 C_3 \left(\frac{Q_2}{C_2} - \frac{Q_3}{C_3} \right)}{\Delta t (C_2 + C_3) + R_2 C_2 C_3} \quad (11)$$

$$I_3(t_{n+1}) = I_p - I_2(t_{n+1}) \quad (12)$$

$$Q_2(t_{n+1}) = Q_2(t_n) + I_2(t_{n+1})\Delta t \quad (13)$$

$$Q_3(t_{n+1}) = Q_3(t_n) + I_3(t_{n+1})\Delta t \quad (14)$$

$$V_c(t_{n+1}) = \frac{Q_3(t_{n+1})}{C_3} \quad (15)$$

Similarly, the difference equations for any order of filter can be easily derived.

For example, a third order PLL system with the set of system parameters R_2 = 16kΩ; C_2 = 200pF; C_3 = 100pF; I_p = 10μA; $K_v = 30x10^6$; Δ = 0.3nS; N = 1, is modelled using both the proposed charge approximation model, and the hedayat et al. model. The transient responses of both models are shown in Figure 11, they produce similar frequency responses.

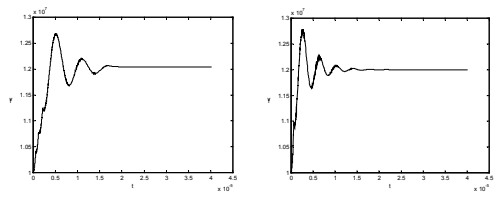

Figure 11: Frequency response of (a) Charge approximation model on the left and (b) Equivalent Hedayat et al.

The error between the two signals is found to be small, Figure 12. It can be seen that the error introduced by the charge approximation, is reduced as value of the time step is decreased.

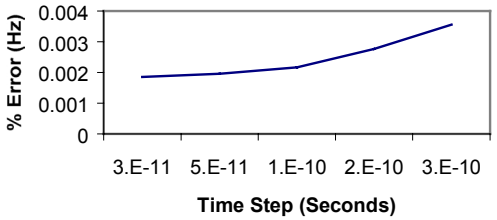

Figure 12: Plot showing decreasing error as Δt is reduced

The selection of Δt introduces a trade off between the error and the simulation time. As Δt reduces, the error reduces correspondingly, with an increase in the simulation time as shown in Figure 13.

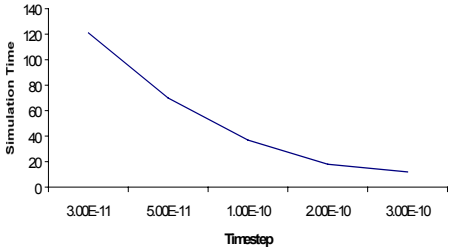

Figure 13: Plot showing decreasing simulation time as the step size is increased

IV MODEL VERIFICATION

In the following section the frequency response of three example PLLs are modelled using the proposed charge approximation model. Firstly a marginally stable PLL is considered and compared to Simulink PLL simulation. In the next example a frequency divider is included in the feedback of the PLL, this is compared to the equivalent Hedayat et al. model. Finally the frequency response of a fifth order PLL model is and compared to the Simulink model.

a) Example 1 – Marginally Stable Third Order

The following set of PLL parameters for a third order PLL are considered in this case, R_2 = 9kΩ; C_2 = 200pF; C_3 = 200pF; I_p = 30μA; $K_v = 200x10^6$; Δt = 0.3nS; N = 1. In Figure 14 the transient response of the charge approximation model and the equivalent Simulink models are shown, again they produce similar transients.

The charge Approximation model took approximately 2 seconds to complete the 35μS, while the Simulink took approximately 10 minutes.

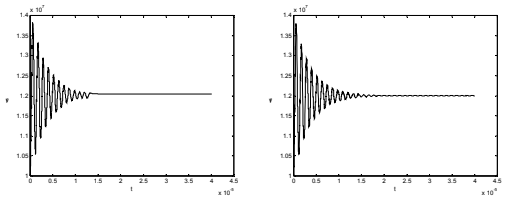

Figure 14: Plot of frequency responses of (a) the Charge approximation model and (b) the Equivalent Simulink for example 2

b) Example 2 – Third Order Using a Feedback Divider.

In this example a 3rd order PLL is again considered, however this time a divider is included in the PLL system with a value of N = 4560. The other parameters are a reference frequency of 500 KHz and a VCO free running frequency of 2.33 GHz, R_2 = 0.4kΩ; C_2 = 55nF; C_3 = 4.6nF; I_p = 5mA; K_v = 200x10^6; Δt = 0.5nS. The transient responses of the charge approximation model and the Hedayat et al. event driven model [2] are plotted in Figure 15 below.

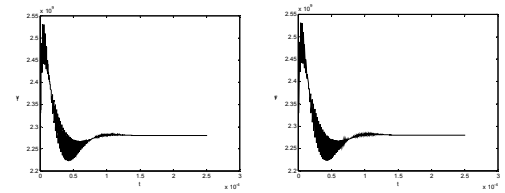

Figure 15: Plot of the Frequency Responses of (a) the Charge approximation model and (b) the Equivalent Hedayat et al. model for example 3

c) Example 3 – Fifth Order PLL

Finally a 5th order PLL is considered, the parameters for this model are N = 1, R_2 = R_3 = R_4 = 16kΩ, C_2 = 100pF, C_3 = 200pF, C_4 = 100pF, C_5 = 100pF, Ip = 10μA, K_v = 30x10^6, Δt = 0.1ns. Again the transient response of the system is shown in Figure 16 as modelled by the charge approximation and the Simulink models.

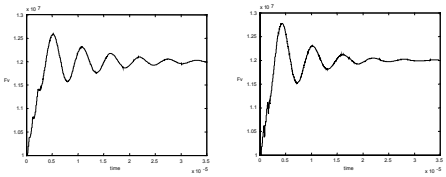

Figure 16: Plot of the frequency response of (a) the charge approximation model and (b) the equivalent Simulink model for example 4

VI CONCLUSION

It has been shown in this paper that a PLL of arbitrary order can be modelled using the event driven modelling technique. The strength of this technique is the speed of transient simulations. The frequency response of the PLL can be easily found using the filter difference equations, derived using the charge approximation, for any order of filter. It is shown that the charge approximation error that is introduced to simplify the difference equation derivation is bounded. Finally, numerous examples are given comparing the charge approximation event driven model to the Simulink model and the Hedayat et al. model.

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