Reconfigurable Radio Testbed

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Abstract — **In this paper a model of a reconfigurable radio testbed is presented. The hardware requirements utilized for a software defined transceiver which covers a wide band of communication standards such as : 2G/3G mobile, IEEE802.11x, IEE802.16x and IEE802.20x are detailed. Specific details for the analog digital conversion are given. The system uses a direct conversion architecture for both up-conversion and down-conversion. Receiver and transmitter features are detailed, and early performance results are shown in this paper.**

Keywords — **SNR, ADC, DAC, BER, Direct-conversion.**

I Introduction

The next generation of wireless communication will demand the use of software radio technologies to support multi-standard, multi-mode and future proof radio designs. Based on this idea, radio technology will be required which will connect any time any where using a single radio platform which can be integrated into any device. This paper details the radio hardware performance, and the requirements needed for this technology. The testbed is in development at the Institute of Microelectronic and Wireless systems at the Department of Electronic Engineering, National University of Ireland Maynooth.

Analog to Digital conversion and Digital to Analog conversion are the two most difficult operations to perform in software defined radio because both ADC and DAC must be able to support the bandwidth, dynamic range, and sampling range required. For this reason simulations using Matlab have been carried out to calculate the dynamic range of the ADC's while trying to keep the best SNR (Signal to noise ratio) as possible.

In order to supply each block with the correct parameters for its frequency band the reconfigurable radio has been divided into 3 blocks: BB (baseband); RF Rx (radio-frequency receiver) and RF Tx (radio-frequency transmitter). Figure 1 illustrates a block diagram of the system.

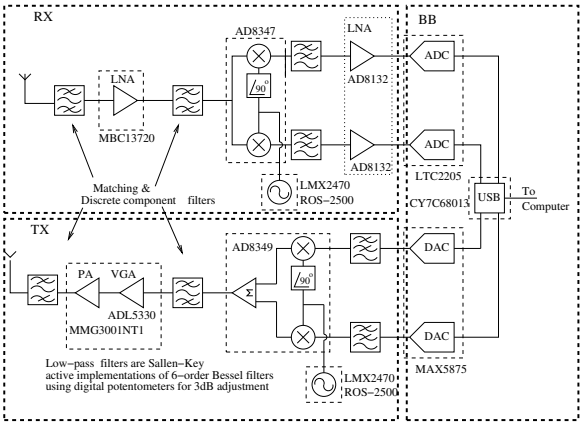

Fig. 1: Block diagram of the system.

II Base Band

a) Simulations

Since data conversion is one of the key features in reconfigurable radio, it is the first block to be simulated, built and tested. The resolution of the high speed ADC is calculated using Matlab. Figure 2 shows some of the parameters which have been taken into consideration while carrying out these simulations. For the BB system simulation an OFDM signal is employed, which can be varied by changing two parameters: modulation scheme and number of carriers. These parameters are modified during the simulation in order to cover several kinds of transmission performances. This technique is used because it is employed on

Multiple access	OFDM						
Modulation scheme	BPSK	QPSK	8QAM	16QAM	32QAM	64QAM	256 QAM
Number of bits	4, 5, 6, 7, 8						
Number of carriers	2-52	2-52	2-52	2-52	2-52	2-52	2-52
SNR_channel	array[dB]= 20 ,40, 60, 80, 100						
Input Power	1W; 0dBW						

Fig. 2: Simulation Parameters.

communications standards like IEEE 802.11g and IEEE 802.16. A transmission channel is simulated with the addition of white Gaussian noise into the system. The receiver is modeled as well. In this case the cyclic prefix of the OFDM signal, which is used to combat ISI in order to avoid including an equalizer[1], is removed before reaching the uniform quantizer, which adds quantization noise to the signal. At the output of the system the BER(bit error ratio) is calculated. The best trade-off between BER and the number of bits is sought. The whole process is shown in the Figure 3. The

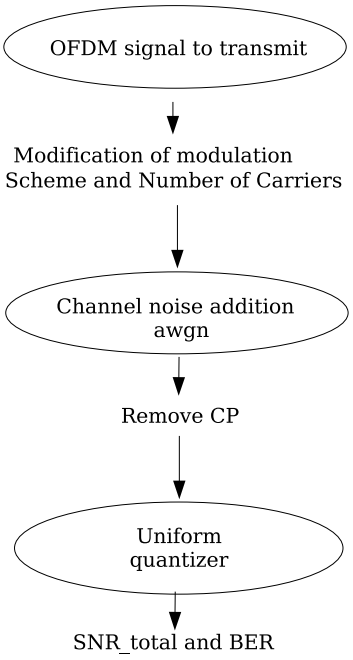

Fig. 3: Flow chart of BB simulation.

total noise is calculated based on the difference between the output and the input signals into the system. Obviously, this noise is formed by white Gaussian noise added in the transmission channel, and the quantization noise added by the uniform quantizer which is described in the equation(1).

$$N_q = 10 \cdot \log_{10} \frac{\Delta^2}{12} \tag{1}$$

N_q is the quantization noise and Δ is the step size of our quantizer. For a uniform quantizer the step size is described as following:

$$\Delta = \frac{2FE}{2^n} \qquad \text{FE: full scale} \tag{2}$$

Since the OFDM signal is a random signal, the total signal to noise ratio of the system is calculated through the variances of both total noise and information signal. The converging variances of both signals, showed in Figure 4, are simulated using equations (5) to (8). Equations (3) and (4) present the expected value or mean (μ) of both noise and information signal.

$$\mu_n = \frac{\sum_{i=1}^{l_{noise}} n_i}{l_{noise}} \qquad l_{noise} : \text{noise length} \tag{3}$$

$$\mu_{ofdm} = \frac{\sum_{i=1}^{l_{ofdm}} ofdm_i}{l_{ofdm}} \qquad l_{ofdm} : \text{ofdm length} \tag{4}$$

Where n is the system noise and ofdm is the information signal. In the following equations k is a variable which counts from 2 to number of samples used for the simulation.

$$\lambda_n^2 = \sum_{i=1}^{k} (n_i - \mu_n)^2 \tag{5}$$

$$\lambda_{ofdm}^2 = \sum_{i=1}^{k} (ofdm_i - \mu_{ofdm})^2 \tag{6}$$

$$\xi_n^2 = \frac{\lambda_n^2}{k-1} \tag{7}$$

$$\xi_{ofdm}^2 = \frac{\lambda_{ofdm}^2}{k-1} \tag{8}$$

$$\sigma_n^2 = \frac{1}{samples^{\,2}} \cdot \sum_{i=1}^{k} \xi_{n_i}^2 \tag{9}$$

$$\sigma_{ofdm}^2 = \frac{1}{samples^{\,2}} \cdot \sum_{i=1}^{k} \xi_{ofdm_i}^2 \tag{10}$$

In the previous equations λ^2 is the temporary variance of both signals; ξ^2 is the sample variance, which is a variance estimate and is based on a finite sample; σ^2 is the total variance for both signals.

Figure 4 present the converging variance and shows how the larger sample we have the more

the noise is constant. However, observing the information signal and considering that variance is the square of the standard deviation, the points from the information signal are highly variable, it is because of the OFDM signal is a random signal.

Equations (9) and (10) are used to calculate the signal to noise ratio (11) of our system which is modeled with Matlab as described in the following equation:

$$SNR = 10 \cdot \log_{10}(\frac{S_\sigma}{N_\sigma}) \tag{11}$$

In order to calculate the BER with the SNR

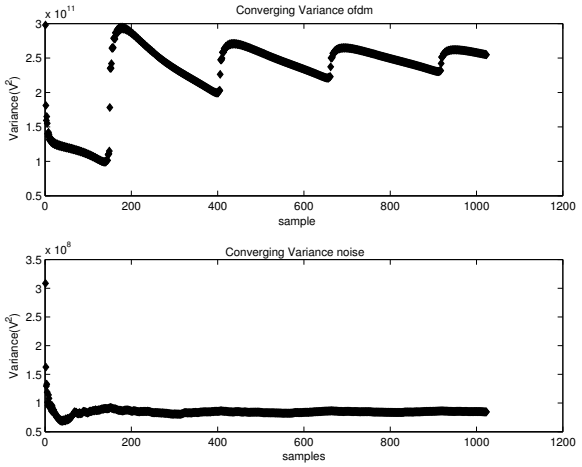

Fig. 4: Converging Variance.

obtained previously, different formulas must be used for each modulation scheme. These equations are related to their constellation characteristics. BPSK and QPSK :

$$Pe = 0.5 \cdot erfc(\sqrt{SNR}) \tag{12}$$

QAM with square constellation (M: 16, 64, 256):

$$Pe = 2 \cdot (1 - \frac{1}{\sqrt{M}}) \cdot erfc \sqrt{\frac{3}{2 \cdot (M-1)} \cdot SNR} \tag{13}$$

QAM with cross constellation (M: 8, 32):

$$Pe = 2 \cdot (1 - \frac{1}{\sqrt{2 \cdot M}}) \cdot erfc \sqrt{\frac{3}{2 \cdot (M-1)} \cdot SNR} \tag{14}$$

where erfc is the complementary error function

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-u^2} du \tag{15}$$

Figures 5, 6 and 7 are showing BER function of SNR for three different types of modulation scheme: QPSK, 256 QAM, 32 QAM. These results are a function of the number of quantization bits. By considering these graphs we obtaine an approximate idea of the best modulation scheme to use. If we focus on these examples, keeping the number of bits and SNR fixed, the best modulation scheme to use would be QPSK. A maximum

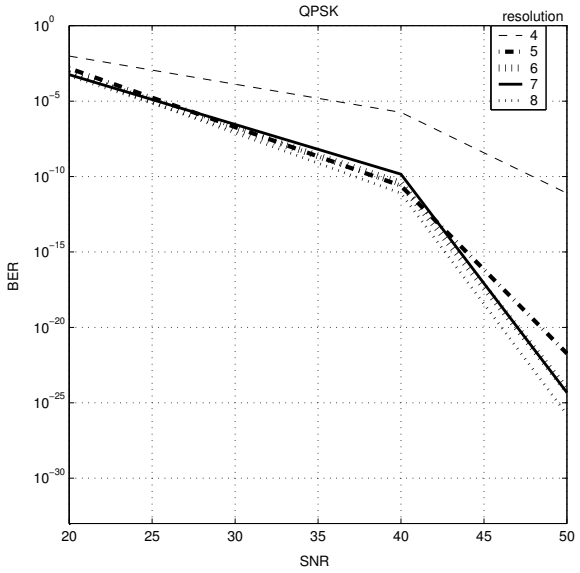

Fig. 5: BER vs SNR with QPSK modulation.

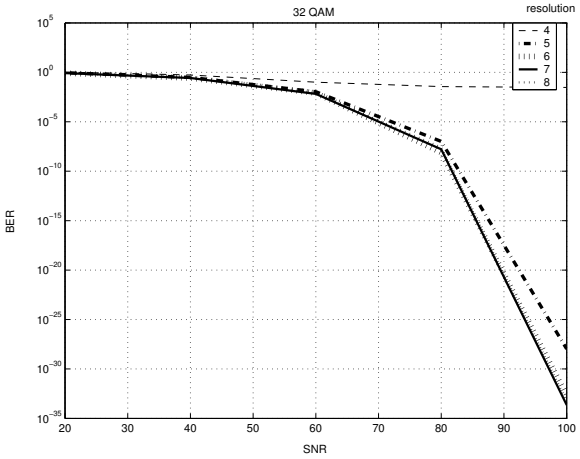

Fig. 6: BER vs SNR with 32QAM modulation.

number of 8 bits is used in order to keep our BER much lower than 10^{-3}, considering a low dynamic range on the ADC's. After, in order to guarantee 8 bits, we use a 16-bits ADC which gives us 8 bits of dynamic range to allow for amplitude variation for the incoming signal.

b) Implementation

For the implementation of the baseband section the following devices are used:

ADC– The Analog to Digital converter is a 16 bit ADC designed by Linear Technology, with

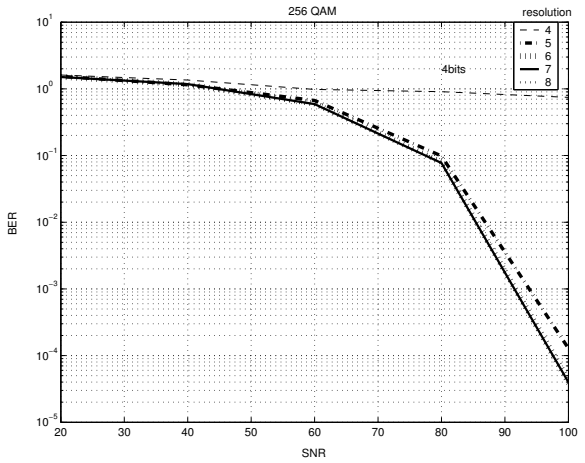

Fig. 7: BER vs SNR with 256QAM modulation.

speed up to 40 Msps. This device can digitize high frequency signals up to input frequencies of 700 MHz. It works with a SNR of 79 dB and 100 dB SFDR. Its analog input is differential to improve common noise mode immunity and to maximize the input range. Moreover, the differential input drive reduces even order harmonics of the sample and hold circuit. The input range selected was 2.25 Vp-p instead 1.5 Vp-p to take advantage of the best SNR related to the operational characteristics of the device.

DAC– The high speed 16-bit digital to analog converter chosen is the semiconductor MAX5875 from Maxim Integrated Products. This advanced device is able to support update rates of 200 Msps. It features an integrated +1.2 V bandgap reference and control amplifier to ensure high accuracy and low noise performance. It has a flexible input data bus that allows for dual port input or single intervaled data port, this last one permits to reduce the size of the system.

USB interface– The Cypress Semiconductor part used for the implementation of this interface is CY7C68013A. This component is capable of operating up to 480 Mbps, the device provides the connection between the host computer and the ADC and DAC. It features a micro-controller, which is used to provide control signals for the rest of devices in the system such as: demodulator, PLL, ADC's, DAC's, modulator, gain control amplifiers and channel selected filters.

III Radio Frequency Receiver

The RF section performs preliminary filtering and amplification of the desired signal, minimising noise and interference. This is then converted to baseband by the demodulator, forming its in-phase (I) and quadrature (Q) components. A local oscillator (LO), from the selected PLL, is used to generate sine and cosine components at radio frequency f_r, tunable within the receiver frequency range from 500 MHz to 2.6 GHz.

a) Direct Conversion Architecture

A DCA, Direct-conversion architecture (also known as zero-IF) is used for our receiver model because of the low power dissipation, easier tunning across large frequency bands, easier design, and the low cost associated with the reduced number of components, which guarantees a higher level of integration than with another architectures[2]. This down-conversion technique directly transforms the RF signal to base band. This approach has image suppression properties. Since DCA does not have problems with image signals, the preselection filter specifications can be relaxed. However in our model it has been used to reject out-of-band interfering signals that could create distortion due to the intermodulation products generated after the mixer. Even though this architecture has many advantages compared to other ones, it has to deal with serious problems such as direct-current offset noise and I/Q mismatch[5]. However the devices for the system have been chosen in order to fulfill the requirements associated with these problems. Figure 8 illustrates an example of drawbacks and requirements of the direct converter receiver.

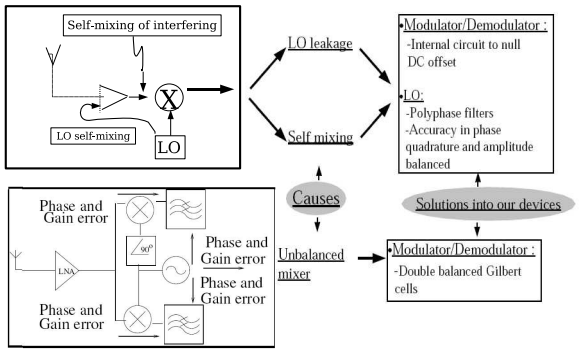

Fig. 8: Direct converter receiver requirements.

b) Devices characteristics

With reference to the Figure 1 the different parts in the system are described as following:

BPF– Baseband filtering is performed by discrete component, broadband matching circuits, which are used to match the LNA to the antenna and the following demodulator.

RF LNA– The device chosen for the preliminary amplification is the Freescale IC MBC13720. This part is a low noise amplifier with bypass switch. It generates a gain of 12 dB and noise figure of 1.55 dB with a working frequency of 2.4 GHz. The LNA is able to operate in a frequency range from 400 MHz to 2.4 GHz. It features two enable pins to control the amplification stage which are controled from the control interface in the USB chip.

Demodulator– The downconverter chosen is the AD8347 device, from Analog Devices. It is a direct quadrature demodulator with RF and baseband Automatic Gain Control(AGC) amplifiers. Its Noise Figure, working at maximum gain, is 11dB. It provides a quadrature phase accuracy of 1^o and I/Q amplitude balance of 0.3 dB. This high accuracy is achieved by the polyphase filters employed by the LO quadrature phase splitter. The dc offset problem is minimized by an internal feedback loop. Channel selection filters are implemented by inserting the LPF, before the amplification of the baseband signal.

PLL– The Phase-locked loop employed in the system is the National Semiconductor LMX2470. This low power Delta-Sigma Fractional-N PLL operates with an auxiliary 800 MHz integer-N PLL. This device has the property to drive close in spur and phase noise energy to higher frequencies. The modulator order is programmable up to fourth order, permitting us to select the optimum modulation order. It works in the frequency range of 500 MHz to 2.6 GHz with phase noise of -200 dBc/Hz. This PLL uses the Mini Circuit VCO ROS-2500.

BB LNA– The low noise amplifier is implemented using a high quality operational amplifier to reduce offset voltage and noise. This device is the Analog Devices part AD8132, which can increase the gain of the mixer output signals by 20 dB.

The calculation of the gain that must be generated by the LNA have taken place here:

Gain– For the calculation of the correct gain on the operational amplifier we take the input characteristics of our ADC device into consideration for best noise performance. We require the gain control of the downconverter to maximise the output in order to minimise the gain needed from thr following opamp. In this way the amplifier is able to work in the linear region within the selected frequency range of operation. All the decisions and calculation taken refer to the following graphs:"Gain vs Frequency" [3] in Figure 9 from the opamp specifications, and"Mixer Output Voltage vs RF input Power"[4] in Figure 10 from the demodulator specifications.

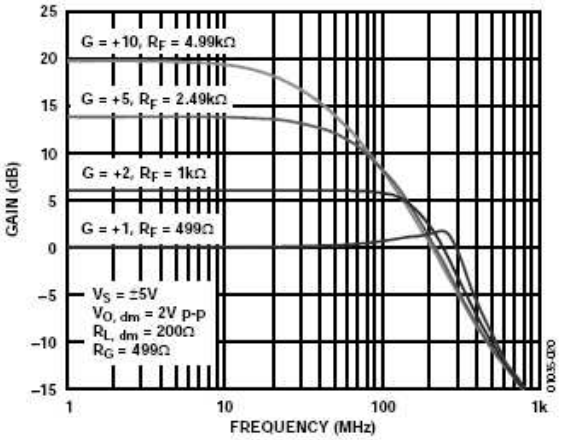

Fig. 9: Gain vs Frequency.

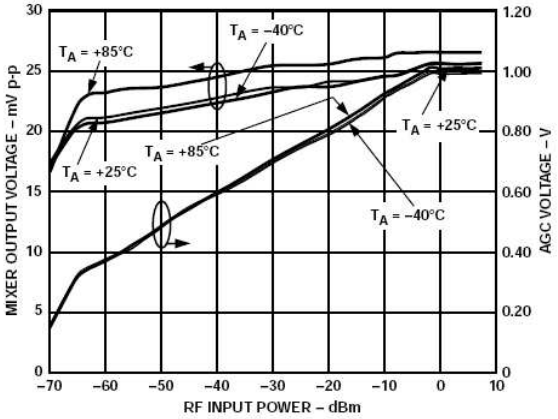

Fig. 10: Mixer Output Voltage vs RF input Power.

Considering our output amplitude of 500 mVp-p, 250 mVp or 23 dBm, we obtain a gain for the amplifier of aproximately 13.1 dB. With these values the AGC voltage on the down converter becomes 1.09 V, which implies a voltage gain inside the device of 3.5 dB. So with these values we are able to calculate the control resistors for the AGC.

LPF– Low pass filters are employed to suppress out of channel interference. Analog filters are used because of their low power consumption. They have been implemented using a Sallen Key architecture which gives better linearity, less noise, simple design and easier selection of components than others architectures. A 6th

order Bessel filter has been chosen because of the flat delay response and the minimum distorsion. The Analog Devices opamp AD8132 is used once again.

IV Radio Frequency Transmitter

a) Up-conversion

The baseband signal from the DAC reachs the upconverter after being filtered by two low pass filters on I and Q channels respectively. These reconstruction filters limit the bandwidth at the input of the modulator. Both I and Q signals are up converted to the carrier frequencies and summed together. Finally the signal is amplified to generate a maximum output power at the antenna of 1 W or 0 dBW. The transmission section has very similar characteristics to the receiver since it uses the direct conversion architecture to upconvert the baseband signal. This implementation eliminates the need for IF stages and increases the reliability of the system.

b) Devices characteristics

With reference to Figure 1 the different parts in the system are described as following:

Modulator– The up-converter chosen is the Analog Devices part AD8349 . It is a quadrature modulator that is able to operate with an output frequency range from 700 MHz to 2700 MHz. It features a modulation bandwidth from dc to 160 MHz and a Noise Floor of -156 dBm/Hz. I and Q inputs from the DAC are driven differentially. To improve the noise performance the local oscillator (LO) drive level is -6 dBm. LO feedthrough is reduced by changing the differential offset voltage on I and Q inputs. The output power generated by the modulator is within the range of -2 dBm and 5.1 dBm.

PLL– Since a direct conversion architecture is implemented the Phase-locked loop employed in this section is the National Semiconductor part LMX2470 as for the radio receiver.

PA– For the amplification stage two amplifiers are employed, because of the necessity to control the output power to transmit to the antenna. The PA used is the MMG3001NT part, which is a broadband high linearity amplifier. It works in the frequency range of 40 to 3600 MHz and achieves a small signal gain of 20 dB with a noise figure of 4.1 dB. However, since this device does not have any gain control input, a voltage controlled amplifier is applied. This VGA is the ADL5330 part which operates from 10 MHz to 3 GHz frequencies, with a gain control range of 60 dB. The gain is controlled through an enable control pin which drives a control signal originating from the micro controller featured in the USB interface chip. In order to control the VGA output voltage a DAC is implemented through a R/2R ladder.

Considering that the maximum output power at the mixer is 5 dBm (with a $f_LO = 2140MHz$), and that the desired transmited signal level is 0 dBW, the minimum gain power between the two amplification stages must be 25 dB. The minimum output power at the mixer is -4 dBm, yielding a power gain between the two stages of 34 dB. With these parameters and knowing that the maximum input power on the MMG3001NT is 10 dBm, the gain range in the VGA is to be from 5 dB to 16 dB.

BPF– Baseband filtering is performed by discrete component broadband matching circuits, which are used to match the power amplifier to the antenna and to the previous modulator.

V Conclusion

In this paper a reconfigurable radio system using direct-conversion architecture has been presented. The system has a certain level of flexibility for channel bandwidth, bit rates, IP3, and sensitivity within the group of standards which it is working with. It is concerned with achieving many of the air-interface specifications which have compatible requirements providing the capability to operate across a width range of applications.

VI Acknowledgments

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References

[1] R.van Nee and R.Prasad. "Wireless Multimedia Communications".2000

[2] Tuttlebee,Walter "Software defined radio:enabling technologies"2002.

[3] Analog Devices "Low Cost,High Speed Differential Amplifier". *Math. Computation*, 12/32–21/32.

[4] Analog Devices "Direct Conversion Quadrature Demodulator". *Graphics TCP 30*,12/20.

[5] B .Ravazi "RF Microelectronics"1998.