FPGA SerDes Capability as Switch mode PA Modulator

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***Abstract*— This paper demonstrates the ability of current commercially available FPGA hardware to generate radio frequency pulsed modulated signals. This work is carried out to determine the suitability of integrated SerDes devices for use in frequency flexible transmitters capable of modulating switch mode power amplifiers (SMPA's). The paper shows that it is possible to meet spectral mask requirements of -50dBc for WCDMA signals at carrier frequencies in digital dividend from 750MHz to 1GHz.**

Keywords – Switch mode power amplifiers; Sigma delta; Class-S; FPGA.

I INTRODUCTION

The fundamental structure of radio transceiver architecture has not experienced radical change over the past 100 years. The radio frequency (RF) frontend of modern transmitters uses a similar architecture to the heterodyne and super-heterodyne radio conceived in 1901 and 1918 respectively. These radio architectures consist of a series of up-converting and filtering stages before amplification that are designed to operate at set frequencies due to bandwidth limitations of analogue components and fixed frequencies of oscillators.

Conversely in the field of IC's, modern silicon processes have increased transistor count and operating frequencies and reduced power consumption. Increased transistor count and reduced power consumption have obvious advantages but coupled with field programmable gate array device architectures this enables increased versatility in reprogrammable hardware for RF systems. FPGA's are therefore found in modern communications systems due to their ability for re-programmability. FPGA's currently are being used for baseband processing of wireless signals and in many high speed optical routing systems. This paper aims to demonstrate how these modern improvements can be used to implement a flexible radio transmitter that is capable of driving a power amplification stage, which is flexible across carrier frequency and modulation standards.

Class-S power amplifiers, outlined in Figure 1, are a combination of a switch mode power amplifier (Class-D), driven by either a pulse width modulator [1] or a sigma delta modulator (SDM) [2]. Pulse width modulators can provide lower in band and out of band noise floors compared to SDM, however it requires analogue implementation to achieve this, resulting in a costly, dedicated design.

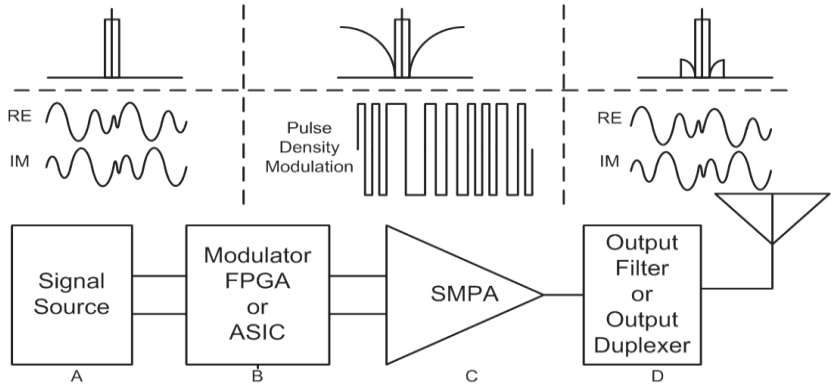

Figure 1 Class S Amplification System

SDM's provide a Pulse Density Modulated (PDM) signal at radio frequency (RF) to drive the switch mode power amplifier. A pulse density modulated signal operates with a fixed minimum pulse width, therefore it can be implemented in digital logic. Increasing operating frequency of modern FPGA's not only enables the prototyping of high speed digital logic designs, but enough processing power is also available to implement more complicated processing tasks at higher frequencies. As indicated by block 'B' in Figure 1 an SDM may be implemented directly on an FPGA board.

Class D power amplifiers are particularly suited to a reconfigurable platform as it consists of a pair of transistors that are driven by a differential signal, alternately switched. In comparison to Class E, F and other harmonic switching amplifiers the class D amplifier can be designed with a wide pass band while maintain efficiency. Class-D amplifiers have a theoretical drain efficiency of 100%, practical demonstrations of between 85% - 90% have been realized [3]. For this reason a class D switch-mode PA can be used to realize the power amplification stage corresponding to block 'C' in Figure 1.

In a Class-S system the SMPA will output the desired signal at the carrier frequency and the quantisation noise that is within the pass band of the amplifier. Filtering of the output is required in order to remove this unwanted noise. This function is performed by block 'D' in Figure 1. In certain cases it has been shown that the pass band of the output duplexer can be used as final stage filtering depending on the modulator that is implemented[6]. If the order of the loop filter is less than the roll off factor of the duplexer we can be confident that the out of band noise will be attenuated sufficiently.

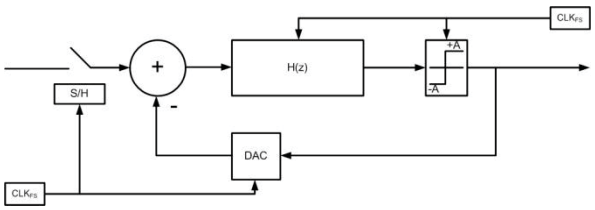

Figure 2 Sigma Delta Modulator

An SDM operates by taking a high resolution baseband input and converting it to a low resolution high frequency output. Because of the reduction in resolution to the input signal there is a large amount of quantization noise which is pushed out of the wanted signal band by the loop filter. The noise is spread across the remaining frequency spectrum up to the sample frequency, therefore the greater the operating frequency or oversampling frequency (OSR) the lower the out of band noise power. The shape of the spectral output of the SDM characterizes the system as either Low pass, Band pass or High pass. Previous papers have demonstrated the operation of modulator structures in FPGA logic such as [4-6]. In these papers it can be seen that there is a loss of dynamic range when comparing simulation results with measurements. This paper demonstrates the high speed capability of FPGA's to generate pulsed density modulated signals through the use of an onboard serial/de-serial module (SerDes). Analysis is carried out to outline the mechanisms that result in lower dynamic range being achieved in practice compared to simulation.

In section II the theory of analogue pulsed signal generation is applied to an ideal pulse density modulated signal and from this a limit of maximum achievable SNR is calculated. In section III this theory is tested with measured signals from different FPGA SerDes modules. Section IV presents the conclusions drawn from this work.

II THEORY

Implementation of a discrete time (DT) SDM in an ASIC or FPGA logic has an advantage of reduced component count compared with discrete implementations as the feedback DAC is inherent in digital implementation. The output of the modulator is then translated from digital to analogue domain through the use of a SerDes. In this paper we will concentrate on two level SDM's. The binary output is translated from digital to analogue drive signal using the FPGA SerDes. SerDes Modules are available on many current FPGA development boards, the two level output combined with the SDM can generate a drive signal for a class D amplifier capable of transmitting a carrier signal at one quarter of the output switching frequency. This platform pushes the digital boundary of the transmitter closer to the antenna.

The DT SDM when fully implemented in digital logic for example on an FPGA will not suffer from clock jitter associated with output quantizer, DAC and loop filter. Therefore the output from the modulator from within the FPGA structure will be almost ideal, aside from quantization error associated with fixed point calculation. The output from the SerDes is an analogue representation of a digital signal and as such will only approximate the digital signal. The analogue output will have a finite rising and falling slope, and jitter about the transition points of the signal. These are two important factors when generating a pulsed driven signal for a digital PA.

In the Xilinx Virtex 6 FPGA family there are three classes of transceiver, each designed for specific frequency ranges of operation and cost. In this paper we will analyze two of these namely: GTX and GTH, which can operate at 6Gb/s and 11Gb/s respectively. The transceivers are designed for digital wired communication standards and as such their figure of performance is bit error rate (BER), they must comply with the specified bit error rate of each standard.

For SMPA operation a delay between transition of on/off state can introduce dead time in the

amplifier output, this is undesirable as it can lead to a distorted output, and also reduce the efficiency of the amplifier. It is important that the FPGA output has a sufficiently fast rise and fall period to avoid this occurring. In the discrete time to continuous time transformation that is carried out in the FPGA SerDes, the rise time of the signal will affect the sinc shaping that is applied to the spectrum of the output as can be seen in Figure 2. The result as stated in [7] is the reduction of power in higher frequency signal component's as they approach the sample frequency.

$$\eta_p(CT) = \eta_p(DT) * (sinc(F_c T_s) * sinc(F_c T_e))^2 \quad (1)$$

Where η_p is the relative signal power, F_c is the frequency at which the power transformation is being performed, T_s is the period of the square waves and T_e is the rise time of the square wave. Using our test case for a band pass SDM operating at 3Gbps and a carrier frequency of approximately 750MHz, a GTX with a typical rise time of 120ps will attenuate the carrier by approximately 1.02dB and a GTH with a typical rise time of 50ps will attenuate the carrier by 0.91dB. These losses are minor in comparison to matching and coupling losses, however from Figure 3 it is apparent that these losses will have a greater impact as frequency increases.

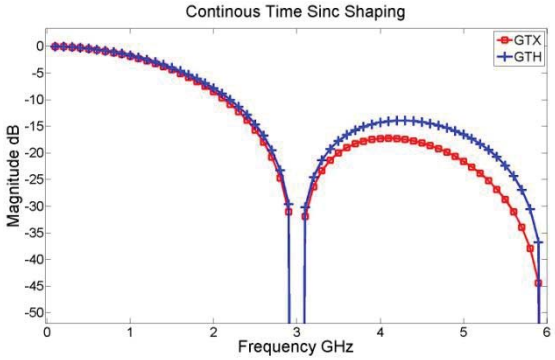

Figure 3 Effects of Sinc Shaping

The increased jitter in the output will increase the noise in the output of the signal across the band. However due to the existing high noise level present from the output of a sigma delta modulator the only area this additional noise will effect is the depth of the notch of the in band signal. In [8] an analysis of both CT and DT sigma delta modulator's is carried out. The following equation derives a figure for the pulse width jitter of the output from a pulsed signal modulator.

$$SNR = 10 * \log_{10} \frac{(T_s)^2}{(2 * \delta_{j\_rms})^2} \quad (2)$$

Where T_s is the clock cycle of the output signal and δ_{j_rms} is the RMS jitter applied to the signal. A SDM has a varying output pulse width period however the formula only uses a fixed pulse width period. It will provide an approximate figure for the jitter noise. The jitter in any SerDes device can be classified as random jitter introduced by the clock and its supporting circuitry and deterministic jitter introduced by the transceiver circuitry its self. Therefore the quality of the input clock and PLL directly effects the jitter performance of the device. For the measurements a ML605 development board with GTX and ML628 development board with a GTH were used, with a figure of total jitter of 50ps and 22ps respectively [9]. Using equation 2 we can simulate a theoretical noise floor for the transceivers.

From Figure 3 it can be seen that for a carrier frequency of 750Mhz the theoretical SNR is 47dB and 38.5 dB for the GTH and GTX transceivers respectively. It is apparent from the graph that the impact of jitter on the output signal quality is quite large, however the GTH transceiver has the ability to meet the required spectral mask noise floor for both LTE and UMTS signals at frequencies below 1GHz.

The main difference between the transceiver structures which impacts on jitter performance is the tuneable (PLL). The lower frequency GTX transceiver can tolerate more jitter due to its lower operating frequency and still achieve the required bit error rate (BER) for the standards targeted by the GTX. Therefore two separate PLL architectures are implemented, the GTX uses a ring oscillator structures. This is a frequency flexible design that consists of cascaded inverters that operate at a resonant frequency dependent on the input reference signal. This structure is compact, requiring only capacitive and logic components which can be easily achieved in CMOS circuitry.

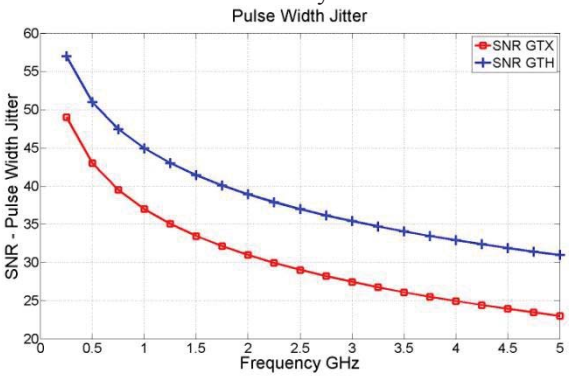

Figure 4 SNR - Pulse Width Jitter

The GTH on the other hand uses an LC tank PLL[10], that offers reduced output jitter at the cost of frequency flexibility. The LC tank PLL structure can offer up to an order of magnitude reduction in RMS jitter compared with a ring oscillator design. However the inclusion of a inductor in the design increases the die area of the PLL making it expensive.

III. MEASUREMENTS

Measurements were carried out using Xilinx ML628 and ML605 development boards. The SDM

bit stream was generated in Matlab using quadrature modulator structure [6] and a memory stream provided the multi gigabit transceivers with the digital signal. The input to the modulator is a single carrier WCDMA signal at baseband. The amplitude of the output waveform was kept constant across transceiver outputs at 200mV. For the purposes of the measurements a single ended output from the transceivers was measured, its complementary port from the transceiver was terminated with a 50 ohm load. The output from the ML605 was a 30cm SMA cable, the ML628 uses a bull's-eye test port with 30cm cables. A differential 150MHz reference clock was supplied to the transceivers directly and the internal PLL multiplied this to the required operating frequency to obtain a 3Gb/s bit stream.

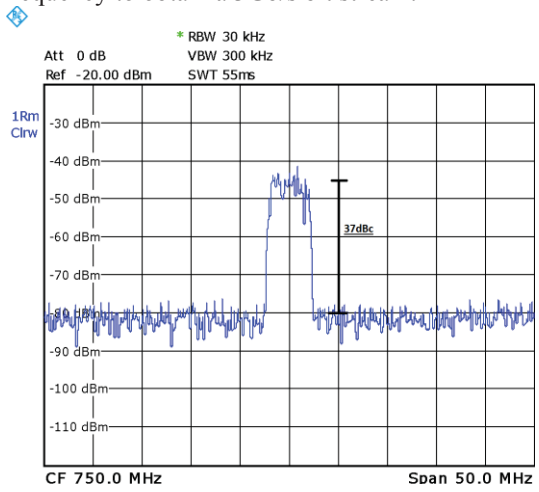

Figure 4 WCDMA 5 MHz Signal at 750MHz GTX Transceiver

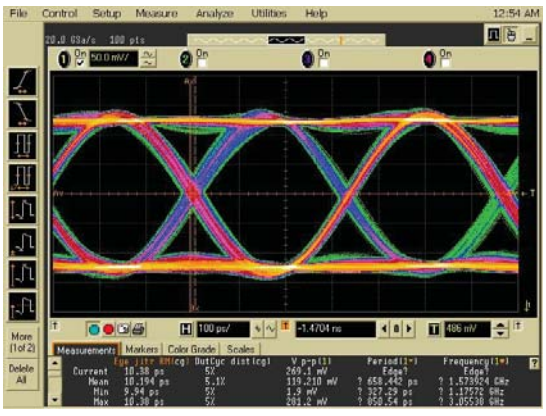

Figure 5 GTX RMS Jitter PDM Signal

Figure 4 shows the spectral performance of the GTX output, using an adjacent channel power ratio (ACPR) measurement on the frequency analyzer a value of -37dBc was calculated for the noise floor from the transceiver at the 750MHz carrier frequency. Figure 5 shows an eye diagram for the GTX output at 3Gb/s, amplitude of the eye is approximately 220mV. The eye is clearly visible and the RMS jitter was calculated at 10ps. Using equation (1) a theoretical value for the noise floor was calculated as 39dBc. Simulation and measurement are in good agreement.

Figure 6 shows the spectral performance of a GTH transceiver transmitting the same bit stream. The reduced jitter from the transceiver lowers the noise floor. The ACPR measurement was increased to 50dBc, which is enough to meet ACPR requirements for a 5MHz WCDMA single carrier or 5MHz LTE signal. The RMS jitter measurement in Figure 7 gives 4ps of jitter. The ACPR and the noise floor of 47dBc calculated with equation 1 also closely agree. The reduced rise and fall time from the GTH transceiver will also provide a better switching signal to the PA.

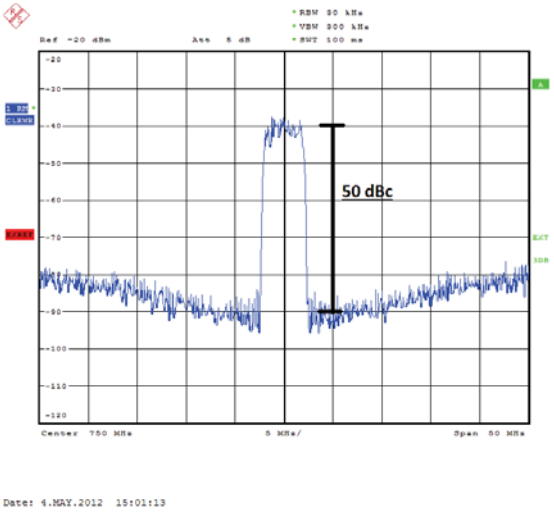

Figure 6 WCDMA 5 MHz Signal at 750MHz GTH Tranciever

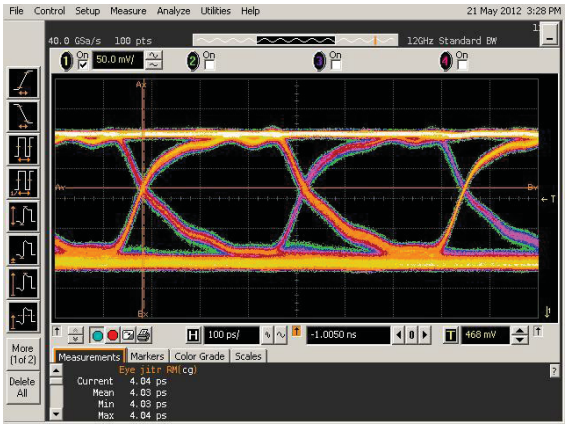

Figure 7 GTH RMS Jitter PDM Signal

IV. CONCLUSIONS

This paper presents the effect of jitter from commercial FPGA boards on PDM signals and demonstrates that it is possible to meet the spectral mask requirements of modulation schemes such as UMTS and LTE. The signal exits the FPGA at RF

frequency, moving the digital boundary right up to the amplifier input. Hardware limitations prevented measurements above 750MHz carrier, from the theory we should expect a 3dB rise in jitter noise from 750MHz to 1GHz, future work will test this. The results show that FPGA's can provide a frequency flexible modulator for RF PA's which can meet spectral mask performance requirements up to 1GHz.

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