Linear Operation of Switch-Mode Outphasing Power Amplifiers

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Deceleration

I hereby certify that this thesis, which I now submit for assessment on the programme of study leading to the award of PhD has not been submitted, in whole or part, to this or any other University for any degree and is, except where otherwise stated the original work of the author.

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January 27, 2016

Abstract

Radio transceivers are playing an increasingly important role in modern society. The ”connected” lifestyle has been enabled by modern wireless communications. The demand that has been placed on current wireless and cellular infrastructure requires increased spectral efficiency however this has come at the cost of power efficiency. This work investigates methods of improving wireless transceiver efficiency by enabling more efficient power amplifier architectures, specifically examining the role of switch-mode power amplifiers in macro cell scenarios. Our research focuses on the mechanisms within outphasing power amplifiers which prevent linear amplification. From the analysis it was clear that high power non-linear effects are correctable with currently available techniques however non-linear effects around the zero crossing point are not. As a result signal processing techniques for suppressing and avoiding non-linear operation in low power regions are explored. A novel method of digital pre-distortion is presented, and conventional techniques for linearisation are adapted for the particular needs of the outphasing power amplifier. More unconventional signal processing techniques are presented to aid linearisation of the outphasing power amplifier, both zero crossing and bandwidth expansion reduction methods are designed to avoid operation in non-linear regions of the amplifiers. In combination with digital pre-distortion the techniques will improve linearisation efforts on outphasing systems with dynamic range and bandwidth constraints respectively.

Our collaboration with NXP provided access to a digital outphasing power amplifier, enabling empirical analysis of non-linear behaviour and comparative analysis of behavioural modelling and linearisation efforts. The collaboration resulted in a bench mark for linear wideband operation of a digital outphasing power amplifier. The complimentary linearisation techniques, bandwidth expansion reduction and zero crossing reduction have been evaluated in both simulated and practical outphasing test benches. Initial results are promising and indicate that the benefits they provide are not limited to the outphasing amplifier architecture alone.

Overall this thesis presents innovative analysis of the distortion mechanisms of the outphasing power amplifier, highlighting the sensitivity of the system to environmental effects. Practical and novel linearisation techniques are presented, with a focus on enabling wide band operation for modern communications standards.

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List of Publications

- K. Finnerty, J. Dooley, and R. Farrell, "Analytical investigation of thermal effects on outphasing power amplifiers," in *Irish Signal and Systems Conference 2015*, June 2015
- K. Finnerty, R. Wesson, J. Dooley, M. Acar, M. van der Heijden, and R. Farrell, "Linearization of an outphasing amplifier for wide-band multi-carrier signals," *Microwave and Wireless Components Letters, IEEE*, vol. 25, pp. 139–141, Feb 2015
- K. Finnerty, J. Dooley, and R. Farrell, "Utilizing sparse-aware volterra for power amplifier behavioral modeling," in *17th Research Colloquium on Communications and Radio Science into the 21st Century, Dublin, Ireland*, March 2014
- K. Finnerty, J. Dooley, and R. Farrell, "Patent application: A signal processing stage for an amplifier, uk application no : 1422097.4," December 2014
- K. Finnerty, J. Dooley, , M. Wesson, R. Acar, M. van der Heijden, and R. Farrell, "Behavioural modeling of outphasing amplification systems," *accepted for publicaion, Microwave Theory and Techniques, IEEE Transactions on*, 2015
- K. Finnerty, J. Dooley, and R. Farrell, "Fpga serdes capability as switch mode pa modulator," in *Irish Signals Systems Conference 2014 and 2014 China-Ireland International Conference on Information and Communications Technologies (ISSC 2014/CIICT 2014). 25th IET*, pp. 118–122, June 2014
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- J. Dooley, B. O'Brien, K. Finnerty, and R. Farrell, "Estimation of sparse memory taps for rf power amplifier behavioral models," *Microwave and Wireless Components Letters, IEEE*, vol. 25, pp. 64–66, Jan 2015
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- J. Dooley, K. Finnerty, and R. Farrell, "Comparison of models for multiple nonlinear power amplifiers in active antenna arrays," *Proceedings of the 43rd European Microwave Conference*, 2013

- S. Farsi, J. Dooley, K. Finnerty, D. Schreurs, B. Nauwelaers, and R. Farrell, "Behavioral modeling approach for array of amplifiers in active antenna array system," in *Power Amplifiers for Wireless and Radio Applications (PAWR), 2013 IEEE Topical Conference on*, pp. 73–75, Jan 2013

- S. Farsi, J. Dooley, K. Finnerty, D. Schreurs, B. Nauwelaers, and R. Farrell, "Cross-memory polynomial modeling for rf circuits," in *Microwave Integrated Circuits Conference (EuMIC), 2012 7th European*, pp. 262–265, Oct 2012

List of Acronyms

2G Second generation mobile communications standard

3G Thrid generation mobile communications standard

ACEPR Adjacent Channel Error Power Ratio

ACP Adjacent Channel Power

ACPR Adjacent Channel Power Ratio

ADC Analogue to Digital Converter

ADS Advanced Design Systems

AM Amplitude Modulation

AMPS Advanced Mobile Phone Service

ANN Artificial Neural Networks

CDMA Code Division Multiple Access

CFR Crest Factor Reduction

CORDIC COordinate Rotation DIgital Computer

CSCD Current Switching Class D

DAC Digital to Analogue Converter

DC Direct Current

DPD Digital PreDistortion

DSP Digital Signal Processor

DUT Device Under Test

EER Envelope Elimination Restoration

ET Envelope Tracking

EVM Error Vector Magnitude

FFT Fast Fourier Transform

FIR Finite Impulse Response

FPGA Field Programmable Gate Arrays

FSK Frequency Shift Keying

GaN Gallium Nitride

GMSK Gaussian Mean Shift Keying

HEMT High-Electron-Mobility Transistor

HSDPA High Speed Downlink Packet Access

ICT Information and Communications Technology

IIR infinite Impulse Response

IM Inter Modulation

IQ In phase Quadrature phase

LINC LIner operation using Non-linear Components

LMS Least Mean Squares

LNA Low Noise Amplifier

LO Local Oscillator

LS Least Squares

LTI Linear Time Invariant

LUT Look Up Table

MLP Multi-Layer Perceptron

MMSE Minimum Mean Squared Error

MOSFET MetalOxideSemiconductor Field-Effect Transistor

MSE Mean Squared Error

NMSE Normalised Mean Squared Error

NMT Nordic Mobile Telephone

OFDM Orthogonal Frequency Division Multiplexing

OSR Over Sample Ratio

PA Power Amplifier

PAE Power Added Efficiency

PAPR Peak to Average Power Ratio

PDM Pulse Density Modulation

PLL Phase Lock Loop

PM Phase Modulation

PMPR Peak to Minimum Power Ratio

PWM Pulse Width Modulation

QAM Quadrature Amplitude Modulation

QPSK Quadrature Phase Shift Keying

RAM Random Access Memory

RBNN Radial Bias Neural Networks

RF Radio Frequency

RLS Recursive Least Squares

RVTDNN Real Valued Time Delay Neural Networks

SCS Signal Component Separator

SOM Self Organising Maps

TACS Total Access Communications System

TDNN Time Delay Neural Networks

TWT Travelling Wave Tube

VGA Variable Gain Amplifier

VI Virtual Instrument

VNA Vector Network Analyser

VSCD Voltage Switching Class D

VSV Vector Switch Volterra

WCDMA Wideband Code Division Multiple Access

WH Weiner Hammerstein

ZCR Zero Crossing Reduction

ZCS Zero Current Switching

ZVS Zero Voltage Switching

Contents

List of Figures

List of Tables

CHAPTER 1

Introduction

Modern society has become heavily reliant upon instantaneous communications in many forms, wireless cellular networks in particular have contributed to this as ubiquitous coverage ensures constant connectivity. This has been furthered by the advancements in information and communications technology (ICT). The advent of the smart phones has enabled instantaneous access to the wealth of information available on the world wide web at an time the user desires. These advancements have modified the traditional forms of mobile communications to include richer forms of multimedia. Pictures and videos are now intertwined with text and speech bites, forming the basis for modern multimedia communications. The evolution in communications increases the load on the cellular networks when compared with the traditional voice and text interfaces. This has lead to an exponential increase in user data rates. Typically when additional data rates are required the signal bandwidth must be increased, however given the restricted quantity of spectrum for consumer mobile communications [16] alternative methods must be implemented. Operators are meeting these demands through more efficient spectral modulations schemes[17], increased number of network base stations and advances in spatial diversity [18].

Each of these methods impacts the hardware requirements for the base-station and the properties of the communications signals. In modern communications networks an increase

in spectral efficiency has been achieved through increasing the complexity of the modulation schemes. This complexity effects the characteristics of the transmitted signal, which in turn impacts negatively on system efficiency. The increased number of network base stations or nodes and the reduced cell size directly impacts the requirements of the base station hardware. The overall cost of the system and the running cost of the systems needs to be reduced in order to achieve an economically viable solution. To achieve these goals advancements in both RF electronics and signal processing techniques must first take place.

A radio frequency (RF) transceiver is a system that consists of both a transmitter and receiver. RF transceivers are common to almost all types of bi-directional communication systems, ranging from satellite communications to low power Bluetooth devices. They are found in many every day devices and as the world becomes more connected this array of devices is ever expanding. RF transceiver efficiency is dependant on the system operational requirement, of the many requirements the two that impact this the most are the distance of transmission and data throughput. As either of these requirements increase the transmit power of the transceiver must increase. However due to the inefficiencies of the RF transceiver the power consumption of the base-station increases rapidly. This is a growing issue for cellular communications as the demand for both constant connectivity coupled with growing demand on data rates is impacting both base station and handset efficiency. Studies have shown that typical efficiency figures for cellular base stations range from 3-12% [19] and in some cases even less. In [20] the author presents the requirements for long term evolution (LTE) base stations configured for 2x2 Multi input - Multi output (MIMO) transmission-reception communications providing less than 2% efficiency. MIMO is a multiple antenna transceiver topology which enhances data throughput under conditions of interference, signal fading and multipath environments [21].

Ignoring the cost of the network on the operators for a moment, such massive inefficiencies lead to excessive power consumption for a single unit, when analysed as a network level problem it is a significant contributor to the universal power consumption within ICT. It is estimated that by 2020 cellular networks will be responsible for approximately 0.5% of the total global carbon dioxide emissions [22, 14]. This is a growing concern, as user demand increases, service providers are forced to expand their infrastructure to meet demand, resulting in increased operational cost and also a growing environmental impact.

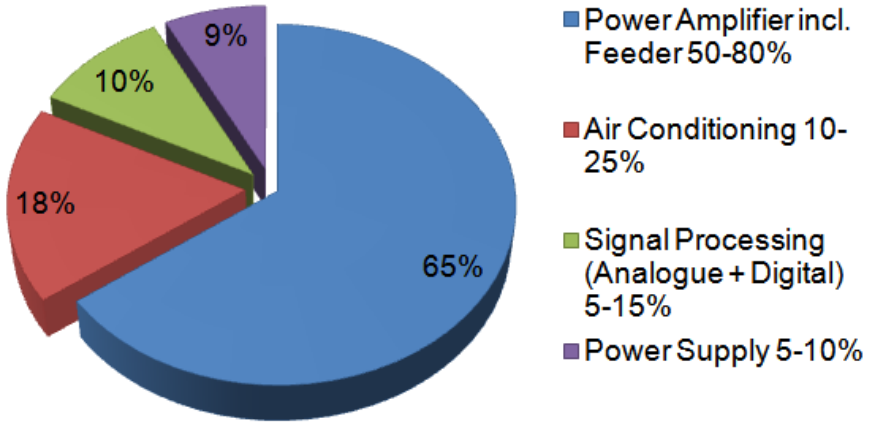


Figure 1.1: Base Station Power Distribution [14]

1.1 Motivation

It is evident that reducing power consumption is not only desirable from an operator's point of view but a requirement from an environmental stand point. Reducing the number of nodes and the power that they transmit is not an option, therefore the efficiency of the base-stations must be improved. Optimum efficiency will be achieved through refinement of each component within the base-station. Optimisation of a full system is outside the scope of this work, therefore this work is focused on the subsystem which can provide the most benefit to the overall system.

Analysis carried out in [14] is visualised in Figure 1.1 which demonstrates that the power consumption of the base station is heavily dependent on the power amplifier and antenna feed network. Increased power amplifier efficiency will lead to a reduction in not only the amplifier and feed network power consumption, it will reduce the power consumed by supporting systems, specifically air conditioning and DC power supplies. Improvements in base station architecture have lead to some reductions, currently remote radio heads have dramatically reduced the impact of the antenna feed network. Research into more efficient amplifier topologies has yielded some promising results. Recent Doherty power amplifiers [23] have improved efficiency when compared with traditional amplifiers topologies [24].

More efficient amplifier architectures are under development, however the topologies and operation required have a negative impact on the power amplifiers ability to reconstruct the input signal. As such they require additional digital signal processing and advanced modulation techniques in order to maintain accurate amplification and efficient operation.

While some advancements have been made, linear performance equivalent to commercial power amplifier solutions is still difficult to achieve [25, 26, 27, 28, 29]. This is mainly due non-linearity and bandwidth limitations associated with these topologies. Enabling linear operation for switch-mode amplifier topologies presents the potential for highly efficient power amplifiers. To achieve this, further advancements in linearisation techniques in combination with improvements in amplifier design are required.

1.2 Thesis Summary

The remainder to this thesis is organised as follows:

Chapter 2 : A comparison of amplifier structures is presented, comparing amplifier efficiency and linearity. Analysing the potential of current switch-mode amplifier topologies demonstrates that the outphasing amplifier is a realisable option, capable of linear operation while maintaining switch-mode operational efficiencies. A comprehensive overview of the impact of non-linear operation is presented, these effects must be quantified in order to characterise or linearise a non-linear amplifier.

Chapter 3 : An in-depth overview of the outphasing power amplifier topology is presented with a focus on the non-linear operation. The outphasing power amplifier is thought of as a system in which the signal generation and all RF components up to the amplifier input are a source of non-linear behaviour. Additionally, analysis on the impact of thermal variation on the outphasing amplifier is carried out focusing on system linearity.

Chapter 4 : The test bench developed for the dynamic operation of a digital outphasing power amplifier is presented. Initial measurements are demonstrated, with baseband time domain signals used to evaluate existing behavioural modelling techniques.

Chapter 5 : In this chapter alternative modelling algorithms to the currently published techniques are presented. The presentation of three novel modelling techniques: Dual path neural network; Dual path Volterra; and Multi-segment Volterra, are evaluated and determined

to be valid techniques for outphasing power amplifier characterisation.

Chapter 6 : The source of memory effects at low output powers is investigated, highlighting the frequency dependant nature of the entire system and the role that the outphasing signal plays in this. The viable models from the previous section are examined as a possible linearisation technique. An additional technique is proposed which is developed to target the frequency effects which the outphasing amplifier experiences at low power. The result is a linearisation technique which enables the amplifier to achieve spectral mask requirements for a multi-carrier 3G 3GPP signal.

Chapter 7 : In this chapter an analysis is carried out on bandwidth expansion. Identifying the main contributors to bandwidth expansion in the outphasing signals. The impact of imposing a bandwidth constraint on the outphasing signal is demonstrated using the output signal linearity as a figure of merit. In addition a novel method of reducing bandwidth expansion is proposed which concentrates the signal processing on the input modulated signal only resulting in a bandwidth reduction in the outphasing signal while maintaining constant envelope input to the amplifier.

Chapter 8 : One of the highlighted requirements of the outphasing amplifier is capability of achieving sufficient dynamic range to fully describe the modulated signal as a continuous function. Failing to achieve this results in a dramatic impact on system linearity. This chapter performs analysis on the importance of system dynamic range and proposes a technique which can reduce the non-linear impact on the output signal for certain dynamic range limited systems.

Chapter 9 : Presenting an overview of the work carried out in this thesis with discussion on the outcomes achieved. The contributions of this work are highlighted, providing a platform to discuss future work in the area of outphasing power amplifier linear operation.

CHAPTER 2

Overview of Power Amplifiers, Non-linear effects and Correction Strategies

Modern communications signals standards are shaping the hardware required in communications systems. This chapter offers a brief overview of the evolution of mobile communications standards, focusing on the impact they have had on power amplifiers, driving development for a more efficient and linear solution. An introduction to power amplifiers, their place in the communications transceiver and the impact communications signals have on their operation will help to frame the work carried out in the subsequent chapters. Section 2.1 provides a brief overview of the evolution of communications signals. Section 2.2 evaluates the operational parameters of power amplifiers which are relevent to transmission of wideband communications signals. Included in this is the basic operation of the Classes of transistor amplifiers, outlining the benefits and drawbacks associated with each. More advanced amplifier topologies, designed to enable efficient operation of linear mode classes and linear operation of switch mode classes are presented in Section 2.3. These designs are targeted at improving system efficiency with the characteristics of communications signals in mind. Linearity is one of the limiting factors in achieving maximum efficiency for an amplifier design, therefore amplifier distortion is discussed and the main sources are outlined in Section 2.4. Since the work in this thesis aims to enable and enhance high efficiency amplifier performance through

the use of digital signal processing, an overview of current techniques will be introduced in Sections 2.5 and 2.7.

2.1 Evolution of Mobile and Radio Communications Signals

Radio communications is essentially a method of encoding information on to electromagnetic signals. Electromagnetic signals are the components of electromagnetic radiation. Electromagnetic radiation covers a range of frequencies called the electromagnetic spectrum which consists of long-wave signals greater than 0 Hz to gamma radiation up to 10^{24} Hz. Radio waves are a subset of this spectrum, ranging from 10^{6} Hz to 10^{13} Hz. The information must be encoded onto a physical property of the analogue electromagnetic signals, initially signal amplitude was modulated in spark gap and amplitude modulation (AM) radio circuits. The information can be easily deciphered as either a binary signal (Morse code) or directly modulating a speaker with sound. This is the simplest from of modulation and demodulation circuity, providing cheap and versatile communications systems. External sources of noise can greatly impact the information of AM modulation signals. Further advancements were made in communications when frequency modulated (FM) radio was introduced. In FM modulation the information is encoded using frequency changes in the signal. FM modulation is more robust to signal amplitude variations and therefore became more popular. A comparison of AM and FM is presented in Figure 2.1.

The first wireless mobile telecommunications standard was an analogue implementation similar to AM or FM radio. As the popularity of mobile communications increased, analogue communications schemes were not capable of supporting the larger number of users, given the limitations of the radio spectrum [30]. Digital communications schemes offered increased spectral efficiency, better signal to noise performance and the ability to encrypt communications, enabling security and privacy to individual users over a single shared channel. To achieve high spectral efficiency communications schemes use both amplitude and phase modulation. Phase modulation is the integral of frequency modulation, resulting in temporary frequency shift. Digital modulation schemes use amplitude and phase modulation to generate a Cartesian constellation diagram, visualising the signals amplitude and phase in a coupled two dimensional plane, demonstrated in Figure 2.2. The location of the data points and pulse

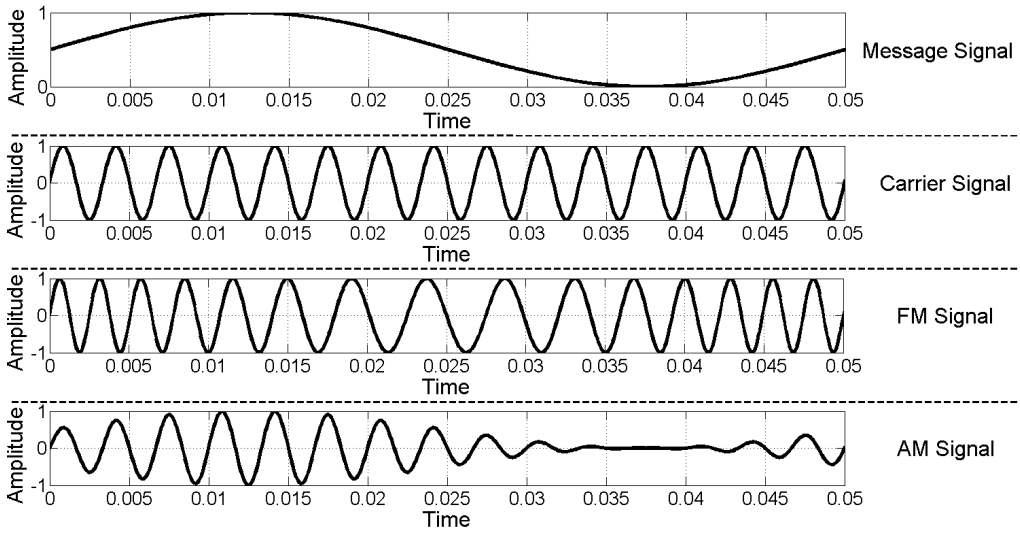


Figure 2.1: Amplitude and Frequency modulation.

shaping [31] that is employed to constrain the transition between the data points will determine the signals characteristics such as bandwidth, data rate and average signal power.

The evolution of the mobile communications schemes has served to increase spectral efficiency, reliability and security over time. The next sections will outline the main communications standards which have been developed over the past 30 years and how they have impacted modern communications systems.

2.1.1 First generation - Analogue cellular telephony

While their have been many variations on mobile telephony dating back to the early 1950's, these systems were more closely related to two way radio than our current infrastructure. The first commercial cellular system went into operation in 1983 in north America [32]. This was the first system to use the concept of spatial diversity, dividing the desired area of coverage into individual regions called cells. Spatial diversity greatly increased network capacity by enabling frequency reuse. This service is very closely related to traditional wired telephony as voice signals were encoded with FM modulation, and analogue transmission was used. Several communications standards existed within the first generation of mobile communications, the most popular were: Advanced Mobile Phone Service (AMPS); Nordic Mobile Telephone (NMT); and Total Access Communication System (TACS). Several issues existed, analogue

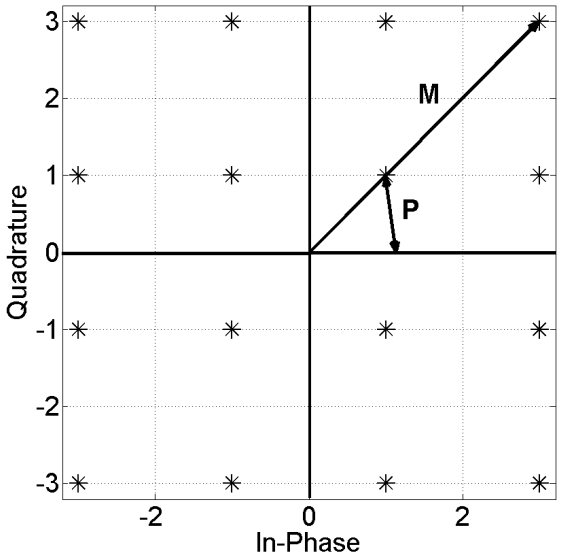


Figure 2.2: Digital constellation diagram, M is the magnitude of the signal amplitude and P is the phase angle of the signal.

signalling does not allow for advanced encryption techniques to be applied. Therefore the identity of the individual handsets could be easily cloned and the communications monitored. Analogue communications are not as robust as digital communications, while FM is more robust when compared with AM, the signals were still easily affected by interference or external noise sources. As the need for mobile communications grew the disadvantages of these standards became limitations. Due to the poor spectral efficiency of the modulation scheme the number of subscribers was limited. These issues would be addressed in the subsequent generation as digital modulation schemes were implemented.

2.1.2 Second generation - GMSK, EDGE

The Global System of Mobile communications (GSM) was the first digital mobile communications standard. The lengthy process of standards definition began in the 1980's, however the first commercial implementations are not available until July 1992. The specification was designed with the limitations of available radio frequency hardware in mind. As such the first release used a GMSK modulation scheme, capable of 270.0833 kilo-symbols-per-second, encoding data at a rate of 1 bit per symbol, resulting in a data rate of 270.0833 kbps. Once a Gaussian pulse shaping filter is applied a signal bandwidth of 200 kHz is achieved. The

modulation scheme uses phase only modulation, signal amplitude remains constant. This offers certain benefits for both amplifier efficiency and linearity. The system is capable of operating the amplifier in its most efficient region constantly. The modulation scheme used time division multiplexing to handle multiple users on a single channel. The standard was initially designed for digitally encoded speech data which only achieved a maximum of 22.8 kbps downlink data rate per user [33].

Mobile communications later transferred from mainly voice communications to a mixture of voice and data communications, beginning with Short Message Service (SMS). As technology improved an increasing number of data only applications were introduced, but the GSM data rates presented a bottleneck. The standard grew to include General Packet Radio Service (GPRS), by aggregating the downlink time slots, data rates improved to a maximum 171 kbps [34]. The introduction of Enhanced Data rates for Global Evolution (EDGE) moved the modulation scheme from GMSK phase only modulation to 8-PSK, improving the bits per-symbol to 3 and the maximum theoretical data rate to 473.6 kbps [35], which is four times the data rate of GPRS alone. While the 8-PSK is still a phase only modulation scheme, the pulse shaping applied and the spectral constraints mean that some amplitude modulation occurs as the signal transitions between data symbols. A measure of this amplitude modulation is the peak to average ratio (PAPR), with the amplitude now varying the amplifier efficiency becomes less optimal.

2.1.3 Third generation - UMTS

Universal Mobile Telecommunications System (UMTS) is the third generation of mobile communications standards. The standard definition process began in the 1990's and the first commercial network was ready for operation in 2002. UMTS is designed for data communications from the ground up, enabling users constant access to the internet over a wide range of devices, not limited to handsets. UMTS uses Wideband Code Division Multiple Access (WCDMA) which enables multiple users to access the same RF carrier. WCDMA is a spread spectrum multiplexing communications scheme, using a data channel multiple times the width of any single users data allocation, individual orthogonal spreading codes are used to overlay the data over the same channel. The access scheme requires users to know the RF carrier and spreading code to retrieve the information, data belonging to other users appears as

noise. The WCDMA signal consists of a 5 MHz channel, the data rate for the channel is 3.84 Mega-chips-per-second. Each individual user inputs or receives data using a IQ constellation mapping which can be QPSK, 16 QAM or 64 QAM depending on the channel. The spreading codes expand the signals which vary up to a maximum of 2 Mbit/s to the required chip rate [36].

The specification later evolved into High Speed Downlink Packet Access (HSDPA) which offers higher spectral efficiency, resulting in increased user data rates [37]. Achieving maximum data rates of 42 Mbps for HSDPA+, a dramatic improvement over GSM data rates. The characteristics of the signal are defined by the modulation scheme that the user data is encoded with. QAM signals will increase the signals PAPR resulting in lower amplifier efficiency's. The increased signal bandwidths also introduce additional linearity challenges which will be discussed later in this chapter.

2.1.4 Fourth generation - LTE Advanced

Long Term Evolution (LTE) was proposed in 2004 as a successor to the UMTS signal standard [38]. The initial specifications required 100 Mbps of downlink data and 50 Mbps of uplink data. This was later exceeded to a peak possible data rate of 300 Mbps downlink and 75 Mbps uplink [39], offering between 5-7 times the capability of the UMTS standard. LTE achieves the increased data rates through higher spectral efficiency of Orthogonal Frequency Division Multiplexing (OFDM) and increased channel bandwidth, up to a maximum of 20 MHz for a single channel. OFDM is comprised of multiple sub carriers, each is capable of implementing individual modulation schemes, increasing the flexibility of the standard. QPSK, 16QAM, and 64QAM are used with trade-off's between data rate and signal to noise ratio, the choice is depending on the channel quality between the user and the base station. The structure of OFDM means that both time and frequency division multiple access schemes are possible as well as dynamic allocation between downlink and uplink channels. The multiple sub carriers within OFDM significantly increase the signals peak to average power ratio and together with increased signal bandwidth will further impact the linearity and efficiency of the communications system.

A comparison of the three generations of communications signals is presented in Table 2.1. The main characteristics that concern the power amplifier have been listed and in the following

section the impact they have will be discussed further.

Table 2.1: Comparison of mobile communications signal standards.

Signal Standard	Analogue FM	GSM	WCDMA	LTE
Bandwidth [MHz]	0.025-0.030	0.2	5	1.4 - 20
Data Rate [Mbps]	NA	0.0224 - 0.48	2 - 48	100-300
Modulation Schemes	FM	BPSK - 8 PSK	QPSK 16 QAM 64 QAM	QPSK 16 QAM 64 QAM
PAPR [dB]	0	0-3 d	6-8	6-12
Spectral Efficiency [(bits/s)/Hz]	0.0015-0.064	0.1-2.4	0.2-9	15+

2.2 Power Amplifiers

An amplifier is an active circuit which increases a signals voltage or current above the levels of the input signal. However an amplifier can have many forms, as they are used in many different applications. The focus of this work is Power Amplifiers (PA's), a circuit that is typically found as the final component in a signal chain and designed to boost signal power for transmission. This work concentrates on improved efficiency of power amplifier circuits, this is a colloquial term which describes the output power of the amplifier. Some of the applications where power amplifiers are used include audio amplification, wired and wireless signal transmission. In this work radio frequency PA's for mobile communications are examined.

An active circuit is one which generates power, the amplifier circuit consists of a transistor or vacuum tube that regulates power from a DC power source, therefore it appears as the power generating component to the load at the output. Figure 2.3 outlines the topology of a single device amplifier. The device can be any controllable current source, suitable circuit components that have been commonly used are vacuum tubes [40], the BJT transistor [41] or the MOSFET transistor [42]. While each of these devices have different operational requirements and constructions they all appear to operate the same in an amplifier circuit, as a voltage controlled current source. The design parameters of the circuit will determine the choice of active component. On of the major design choices is the output power required. The output power is determined by the predicted losses in transmission and the power required at the receiver, in most cases a buffer or amplifier circuit. For the purposes of the work outlined in this

thesis the power amplifier will refer to the final amplification stage before signal transmission, as it has the greatest impact on system efficiency. Currently, high frequency power amplifier circuits are targeting Gallium Nitride (GaN) High-electron-mobility Transistor (HEMT) as the active device, a type of MOSFET that offers the optimum compromise between output power and efficiency for high frequency PA architectures [43].

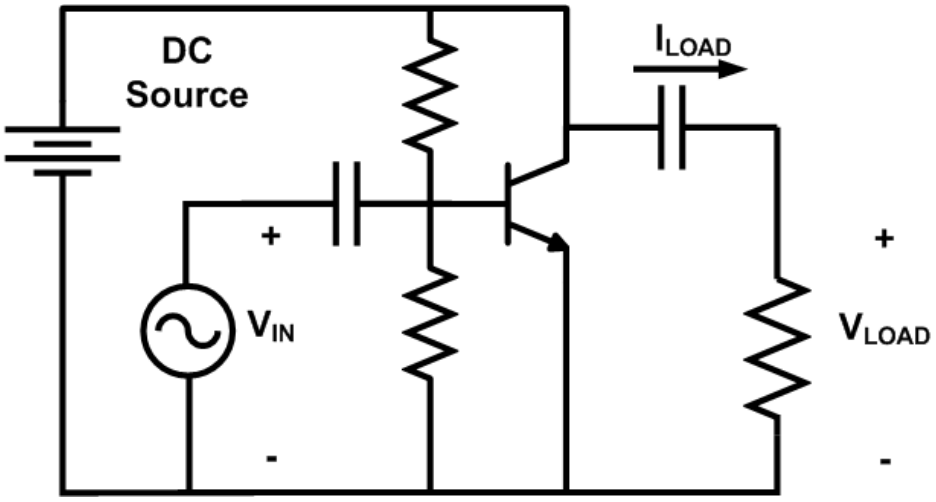


Figure 2.3: Simple BJT amplifier - Class A amplification.

The goal of the amplifier circuit is to transfer the maximum available power from the transistor to the load. This is achieved by matching the output impedance of the transistor to the impedance of the load. This is particularly important at RF frequencies where parasitics that exist within the transistor package and the external bias circuit will influence the impedance seen by the load, which is typically a fixed value. To compensate for this a matching circuit is implemented between the transistor and the load. A matching circuit is essentially a 2 port filter designed to compensate for a given impedance at port one for the fixed impedance on port two. The radio frequency of operation is chosen as the centre frequency of the design. Further information on matching circuits can be found in *"RF circuit design"* [44] and will be presented in Section 3.5.2.1. The impedance of the transistor is defined not only by the device structure but also by the biasing point. This will be explored further in section 2.2.4.

An overview of an RF transceiver is outlined in Figure 2.4. There are five amplifiers in this representation, two variable gain amplifiers (VGA), a driver amplifier, a low noise amplifier (LNA) and the power amplifier (PA). All of the amplifiers in Figure 2.4 impact system efficiency, having equal or in most cases far worse efficiency than the PA. However in many

cases the power consumption is dramatically lower therefore the impact is negligible when compared with the PA.

When analysing the performance of an amplifier, the following parameters should be evaluated:

- Linearity.
- Efficiency.
- Operational bandwidth.
- Gain.

The following section will evaluate each of the above parameters in relation to different power amplifier circuits. An overview of popular amplifier topologies is outlined in Figure 2.5, each of these will be evaluated in the following sections in relation to linear mode and switch mode operation.

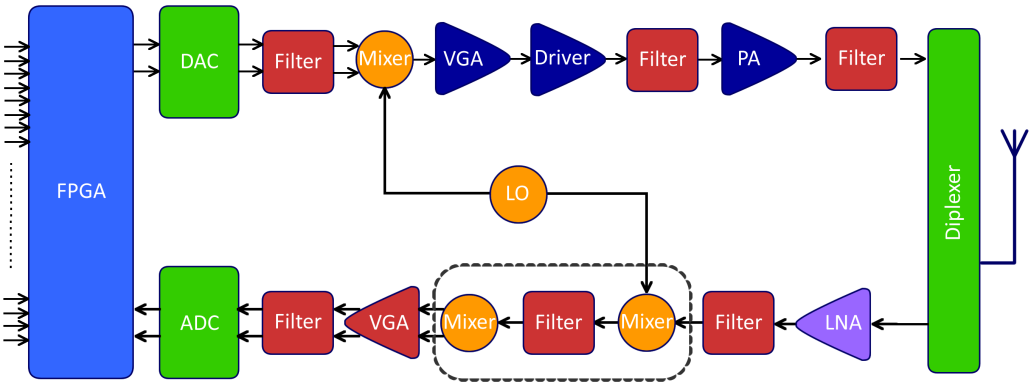


Figure 2.4: Block diagram of RF Transceiver

2.2.1 Linearity

The linearity of a system is dependant on its input - output function. If this can be described by a single straight line then the system is linear. Often this is not the case, it is therefore more common to analyse linearity as the amount the system deviates from the ideal. Communications systems must meet linearity specifications for two main reasons: spectral

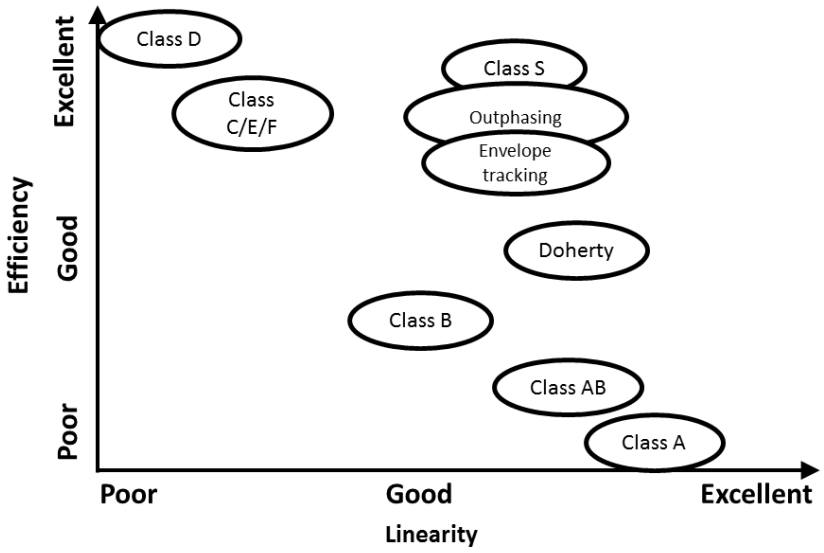


Figure 2.5: An illustrated overview of current known amplifier configurations. The power amplifier classes of operation degrade in linearity with an increase in efficiency. The amplifier topologies are to the top right, break this relationship and are an area of current exploration for expanding operational efficiency of transistor amplifiers.

requirements; and information error. The spectral output of the transceiver must comply with the specification set out in the 3GPP signals standards [33, 39]. This ensures that the transmitter will not interfere with adjacent channel signals, this is termed illegal operation and will be shut down by the appropriate communications regulatory body. The introduction of non-linearity will affect the information that is contained within the signal, this can result in bit errors in extreme cases. Bit errors will reduce the maximum achievable data rates. A transistor is a non-linear circuit component. Its function can be represented by an infinite series of non-linear products of the input demonstrated by equation 2.1. The non-linear function typically will have a pseudo-linear region where the non-linear products do not greatly impact the output. The typical response of a transistor amplifier is presented in Figure 2.6, the linear response is the dotted black line, as the amplifier deviated from this it enters a non-linear region of operation.

$$f(x) = \sum_{n=0}^{\infty} a_n x^n = a_0 + a_1 x^1 + a_2 x^2 + a_3 x^3 \ldots \tag{2.1}$$

The coefficients of the power series $a_2, a_3, a_4...$ result in non-linear products, which can be directly related to harmonics in the frequency domain. Spectral non-linearity is a result of addition and subtraction of the odd order harmonics with the fundamental frequency. This is described further in Section 2.4.5. Similarly the non-linear region will change the input - output data, if the magnitude of the non-linearity is sufficiently large, errors can be introduced. The impact on both time domain and spectral domain information is expanded upon in Section 2.4.

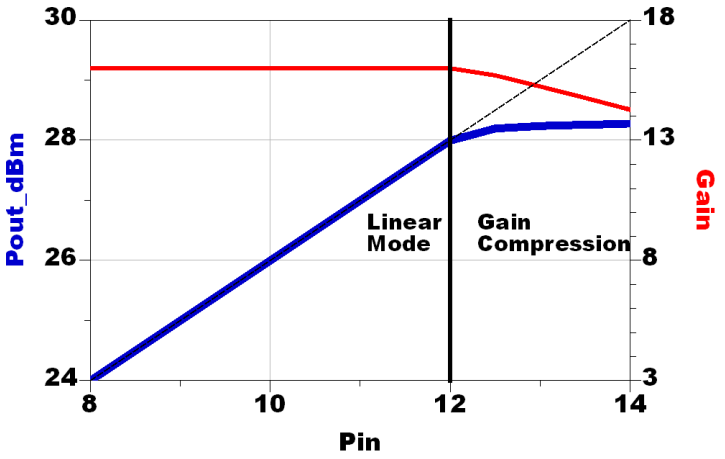


Figure 2.6: Output power of a transistor amplifier. The solid black line indicates the transition from linear to non-linear operation. The black dashed line is the linear output of the PA.

2.2.2 Efficiency and Gain

Power amplifier efficiency is the percentage of output power compared with total power input from DC and RF sources. The power that is *"consumed"* in the amplifier is dissipated as heat. In order for power to be dissipated in the transistor the voltage across the device and the current through it must overlap, the area in which they overlap will determine the amount of power the transistor has to dissipate. An example of a Class A power amplifier characteristic voltage and current waveform across the drain - source terminals is presented in Figure 2.7. The area highlighted in orange under the voltage and current waveforms demonstrates the power dissipated through the device.

There are three definitions of amplifier efficiency that are commonly used. Overall power efficiency [45] is the ratio of output power to the sum of the input power and RF drive power presented in equation 2.2. This is the most versatile efficiency figure of merit as it can be

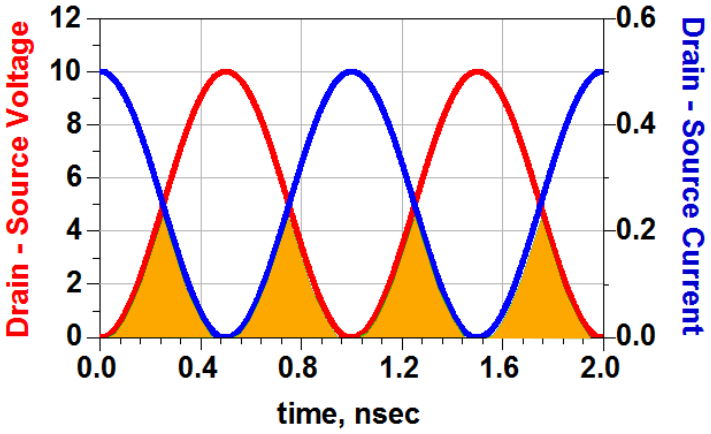


Figure 2.7: Power is dissipated in the highlighted region under the voltage and current waveforms.

modified to include driver DC power as well as power consumed by supporting circuits.

$$\text{Overall Efficiency} = \frac{P_{out}}{P_{dc} + P_{in}} \tag{2.2}$$

Drain efficiency is the ratio of RF power to DC power and is described in equation 2.3, conditions for achieving a drain efficiency of 100% in equation 2.4 occur when the current and voltage waveforms do not overlap i.e. $[i_D v_{DS} = 0]$

$$\text{Drain Efficiency} = \frac{P_{out}}{P_{dc}} \tag{2.3}$$

$$P_D = \frac{1}{T}\int_0^T i_D v_{DS}\, dt = 0 \tag{2.4}$$

Drain efficiency P_D is the ratio of DC power consumed at the drain of the amplifier compared with the RF output energy generated by the amplifier. It can be useful when analysing the efficiency of the final stage of amplification or as a comparison of output matching techniques. Power added efficiency (PAE) is the third measure of amplifier efficiency, it is the ratio of RF drive power and output power to the input DC power, outlined in equation 2.5. This figure of merit is a good indication of PA performance, including the DC to RF power conversion and power consumed in the amplifiers gate biasing network. It is an important measure of amplifier performance considering the entire system, for example, a low gain final

stage's can be very efficient however require a larger power driver stage or stages which are less efficient. This will impact the overall system efficiency.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{in}(G-1)}{P_{dc}} \tag{2.5}$$

Where G is the gain of the amplifier, gain is the ratio between output power vs input power.

2.2.2.1 Back-off efficiency

Amplifier circuits achieve peak efficiency at maximum output power. This is a misleading figure of merit when evaluating systems for modern communications standards (2.5G +) which require amplitude modulation. The system efficiency varies proportionally with signals amplitude. The reason for this is the biasing point of the amplifier holds the average voltage of the signal about a mean operating point. Increasing the overlap of the voltage and current waveforms in the device results in an additional percentage power loss for a given output power. Figure 2.8 illustrates this, the input power has been reduced by 3 dB and the resulting overlap is much larger when compared with Figure 2.7.

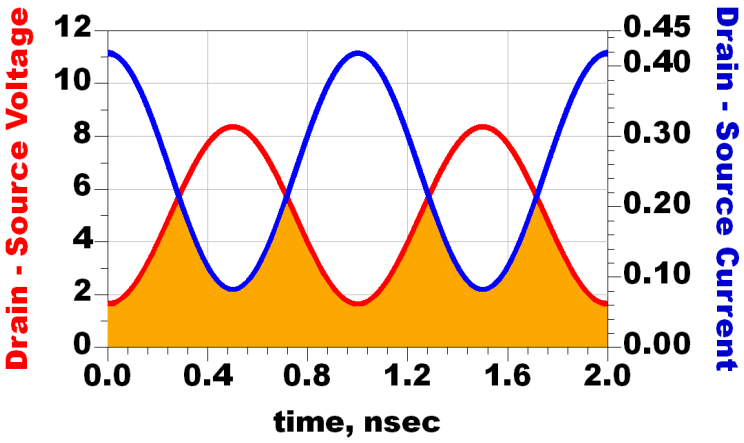


Figure 2.8: Power dissipated in an amplifier in back-off operation. Power is dissipated in the highlighted region under the voltage and current waveforms.

The operational efficiency of the amplifier can be equated to the average output power of the signals compared with the maximum output power. Figure 2.9 demonstrates the impact of modern communication signals introduced in Section 2.1 on the efficiency of the power amplifier. The average power of the signal will be used to estimate the average efficiency of the

power amplifier when operating with the desired communications signals. The calculation of PAPR using signal magnitude is outlined in equation 2.6, giving $-2.6dB$, $-8.9dB$ and $-12dB$ for EDGE, WCDMA and LTE respectively, resulting in amplifier efficiencies of 52%, 33% and 28% for an ideal Class AB amplifier.

$$PAPR = 20log_{10}\frac{mean}{max} \tag{2.6}$$

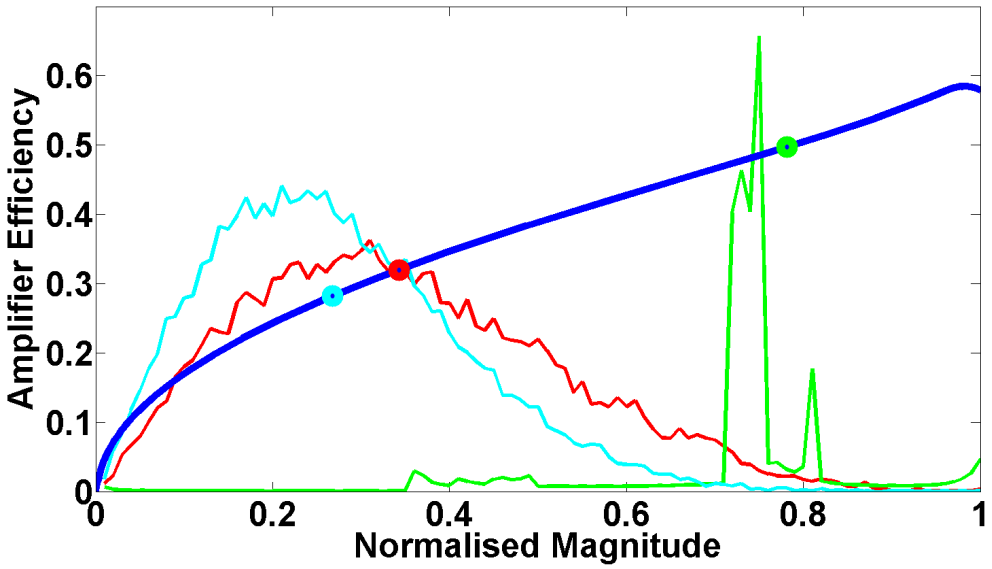


Figure 2.9: Distribution of signal magnitude for the three generations of signal standards. Green = EDGE 2G signal, 200 kHz. Red = WCDMA 3G signal, 5 MHz. Cyan = LTE 4G signal, 20 MHz. The theoretical efficiency for a Class AB amplifier operated in saturation is presented in blue. The average efficiency of the amplifier for each signal standard is estimated by the average power in the signal and marked on the efficiency curve with a circle corresponding to the signal standard. The increase in spectral efficiency has increased the PAPR of communications signals the resulting impact on efficiency is demonstrate.

2.2.3 Operational Bandwidth

Power amplifiers are typically designed to achieve maximum power transfer at a specific frequency or frequency range. This is referred to as the operational bandwidth of the amplifier. Wideband amplifier design requires compromise in other areas, such as maximum power transfer, gain or efficiency over the bandwidth of operation. Typically amplifiers are designed to have a flat passband for a given communications band. A communications band is a range of

frequencies designated by the 3GPP specifications assigned to a communications standard. LTE for example has 44 bands assigned to it, with bandwidths of between 5 - 200 MHz [46]. Outside of this bandwidth an amplifier is typically designed to have a sharp roll off where possible to attenuate any out of band signals generated by either the amplifier or the communications system.

2.2.4 Linear mode operation

The structure of a single transistor amplifier is outlined in Figure 2.10. The input and output matching networks provide impedance matching to the transistor for maximum power transfer. The bias supply voltage and the structure of the matching networks will define the operation of the amplifier. Figure 2.11 provides an overview of biasing for linear power amplifier classes of operation that are expanded upon in the following sections.

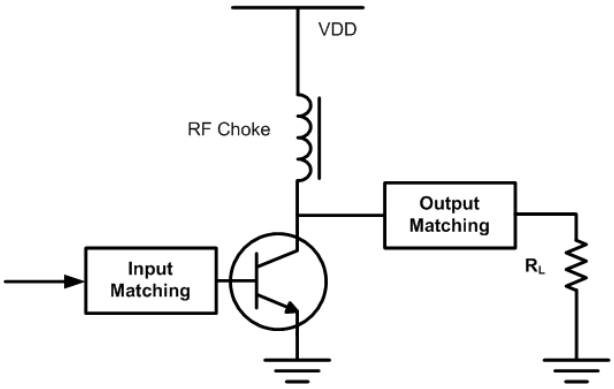


Figure 2.10: Layout of power amplifiers operating in the linear region a transistors.

2.2.4.1 Class A amplifier

Class A power amplifiers are the simplest amplifier circuit, introducing a minimum amount of distortion. The bias point, as outlined in Figure 2.11, is set to half the maximum input voltage this is to ensure that full peak to peak voltage can be achieved without clipping. This ensures that only the fundamental output frequency is generated in the transistor. Due to the lack of harmonics the output matching circuit can be wide-band as the higher harmonics do not need to be attenuated. Class A power amplifiers conduct for all values of the input signal, 360° and achieve the highest possible output power for linear mode transistors [24], as the output signal is not clipped during minimum output power or maximum output power. High output power

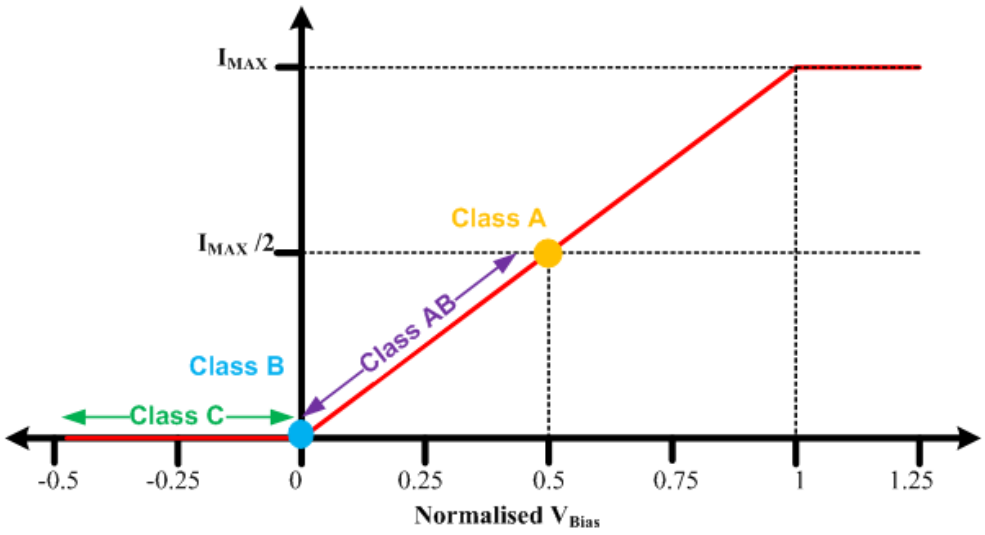


Figure 2.11: The biasing points which correspond to operation in the linear region of the transistor.

and wide band operation mean that Class A amplifiers are typically used as driver and bench top amplifiers. This flexibility and linearity comes at the cost of efficiency. The maximum theoretical output efficiency is demonstrated in equation 2.7. The biasing voltage ensures that the transistor is operated half way between maximum output current and switching off. As such half the maximum output current is always flowing through the transistor to ground, therefore the maximum theoretical efficiency is 50%. Significant heat is generated during operation, as such sufficient active cooling is generally required. Figure 2.12 outlines the voltage and current waveforms across the transistor amplifier.

$$\eta_{Dmax} = \frac{1}{2}\left(1 - \frac{V_{DS\,min}}{V_{DS}}\right) < 0.5 \tag{2.7}$$

2.2.4.2 Class B amplifier

The Class B amplifier is biased on the edge of transistor conduction, the output is driven by the input for half of the duty cycle [180°] [47]. It will not conduct for the negative portion of the input signal. Operating the amplifier circuit in this way has benefits and disadvantages over the Class A amplifier. The efficiency of the amplifier is increased compared with the Class A amplifier, biased in such a way that no current will flow through the transistor unless the input signal is positive, greatly reducing power loss. Therefore by modifying equation 2.7,

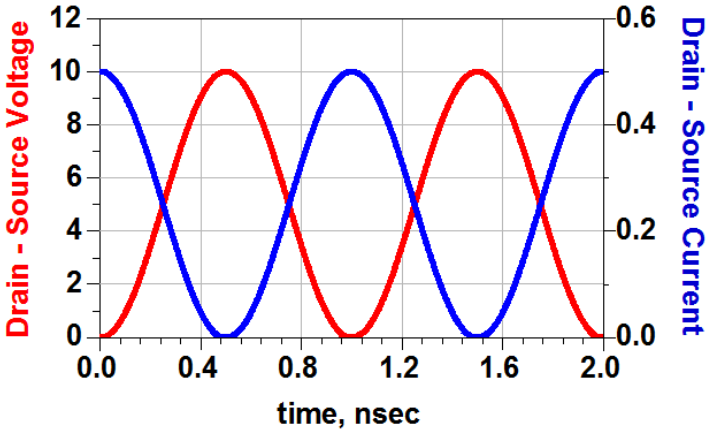


Figure 2.12: Drain - source current and voltage waveforms for a Class A power amplifier.

changing the scaling factor from $\frac{1}{2}$ to $\frac{\pi}{4}$ we can describe the amplifier operation. The amplifier has a maximum theoretical efficiency of 78.4%, given by equation 2.8. The amplifier will only conduct for half the input cycle, we can assume that the input is a sinusoidal signal, therefore the amplifier is only operating for half its period. Figure 2.13 demonstrates the voltage and current waveforms across the transistor. The reduced conductance angle results in a discontinuous waveform of drain - source current. In order to reduce the transmission of harmonics, we ensure power will only be constructed at the fundamental frequency. This is achieved by a resonance circuit that is introduced into the output matching network. As a result the bandwidth of the output is somewhat limited when compared with Class A operation. Furthermore due to the amplifier only conducting for 50% of a complete cycle the amplifiers gain is reduced by 6 dB.

$$\eta_{Dmax} = \frac{\pi}{4}\left(1 - \frac{V_{DS\,min}}{V_{DS}}\right) \approx 0.7854 \tag{2.8}$$

2.2.4.3 Class AB amplifier

The Class AB amplifier is a popular design in communications system [48]. The biasing point is chosen between Class B and Class A resulting in a conductance angle of $180° < \theta < 360°$. This approach achieves improved efficiency compared with Class A and reduced the harmonic non-linearity when compared with Class B. The reduced quiescent current will offer better efficiency as demonstrated by equation 2.9, however some of the non-linear effects associated with Class B operation still remain. The resonance circuit is not as narrow band as with a

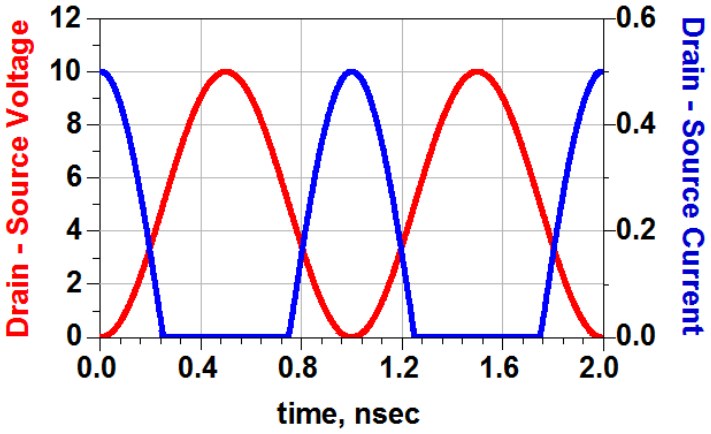


Figure 2.13: Drain - source current and voltage waveforms for a Class B power amplifier.

Class B amplifier resulting in a more flexible amplifier for communications systems. Gain is also improved compared with Class B amplification as the angle of conduction increases, gain reduction is between 6 - 0 dB compared with the Class A amplifier.

$$\eta_D = \frac{\theta - sin\theta cos\theta}{2sin\theta - \theta cos\theta}\left(1 - \frac{V_{DS\,min}}{V_{DS}}\right) < 0.7854 \qquad where \quad 180^\circ < \theta < 360^\circ \qquad (2.9)$$

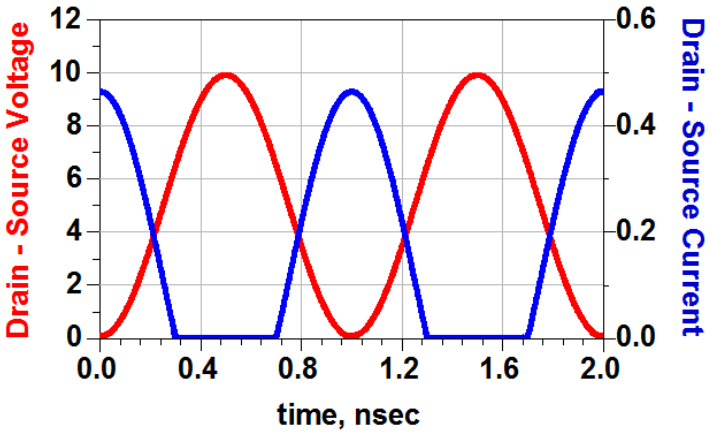


Figure 2.14: Drain - source current and voltage waveforms for a Class AB power amplifier.

2.2.4.4 Class C amplifier

Class C amplifiers conduct for less than a Class B amplifier between $0^\circ < \theta < 180^\circ$ of the input signal and as such the output is highly distorted [49]. The reduction in conductance angle dramatically reduces the overlap between voltage and current waveforms, resulting in higher

efficiencies, in some applications efficiencies of up to 90% have been recorded. The voltage and current waveforms are outlined in Figure 2.15. The penalty for such operation is an increase in higher order harmonics and further reduction in amplifier gain. The resonant circuit in the matching network will have a narrower pass band in order to achieve a linear output. Typically the amplifier structure is only suitable for low bandwidth applications, one such example is FM radio transmission.

$$\eta_D = \frac{\theta - sin\theta cos\theta}{2sin\theta - \theta cos\theta}\left(1 - \frac{V_{DS\,min}}{V_{DS}}\right) > 0.7854 \qquad where \quad 0^\circ < \theta < 180^\circ \tag{2.10}$$

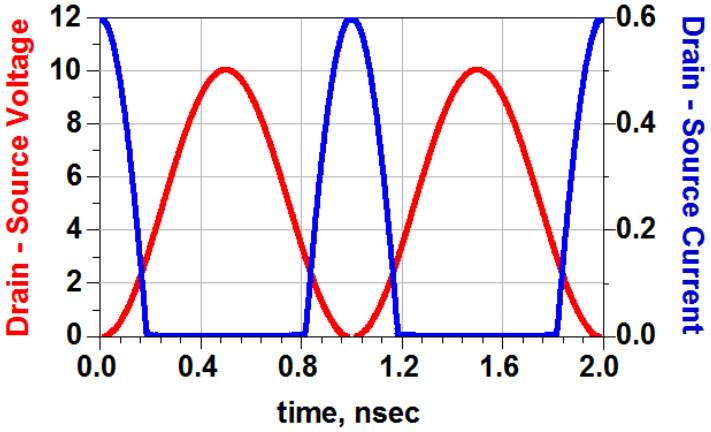


Figure 2.15: Drain - source current and voltage waveforms for a Class C power amplifier.

2.2.5 Switched mode operation

Switch mode operation biases the amplifier circuit in Class B at the edge of conductance or light Class C. However unlike the linear modes the input is hard switched, operating on the linear region of the amplifier for as short a period as possible. The equivalent circuits of switch mode power amplifiers commonly replaces the transistor with a switch, when closed current flows through and when open a voltage is present across the drain - source terminals. Theoretically the voltage and current waveforms will not overlap, eliminating power loss in the transistor. As a result some forms of switched mode PA's of operation having a theoretical maximum efficiency of up to 100%. There are two distinctions to be made in switch mode power amplifiers, Class D amplifiers are fully digital amplifier. The higher harmonics that the

switching generates either output directly to the load or terminate in a resonance circuit. Classes E and F are harmonic switch mode power amplifiers - controlling the harmonic termination of the amplifiers output enables benefits from switch mode operation while achieving an output similar to the linear model amplifiers. These structures are further explored in the following sections.

2.2.5.1 Class D amplifier

Class D power amplifiers consist of a pair of complementary transistors that operate together. Complementary switching ensures that a path to ground is never presented to the DC source, all currents must pass through the load. Switch mode operation requires a square wave to be presented as an input to drive the transistors. In Figure 2.16 a Voltage Switching Class D (VSCD) amplifier is illustrated, It is so named because the voltage across the transistors is a square wave, the current waveform of the amplifier is dependant on the output resonant circuit. The waveforms for the ideal VSCD operation are presented in Figure 2.17, the resonant circuit is tuned for the fundamental operating frequency f_0.

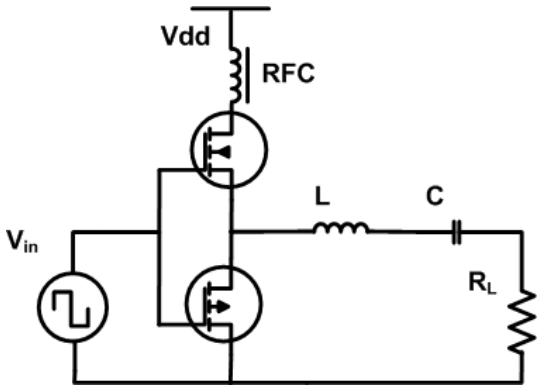


Figure 2.16: Class D Amplifier Voltage Switching

The Current Switching Class D (CSCD) architecture in Figure 2.18 is fed by a DC voltage source and an RF choke which form a DC current source. The CSCD or Class D^{-1} waveforms are presented in Figure 2.19. The waveforms have been inverted, as the current through the switches is now a square wave and the voltage across them is sinusoidal. Like the VSCD the resonant circuit is tuned to achieve a voltage waveform at the fundamental f_0.

The VSCD [50] and the CSCD [51] power amplifier have been realised for both low frequency and high frequency applications. They are popular in low frequency applications

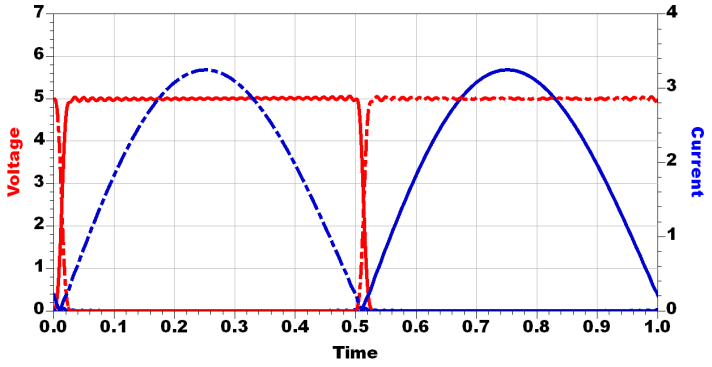


Figure 2.17: Drain - source current and voltage waveforms for a Voltage Switching Class D (VSCD) power amplifier. Solid line represents the waveforms for switch one, the broken lines represents the waveforms for switch two.

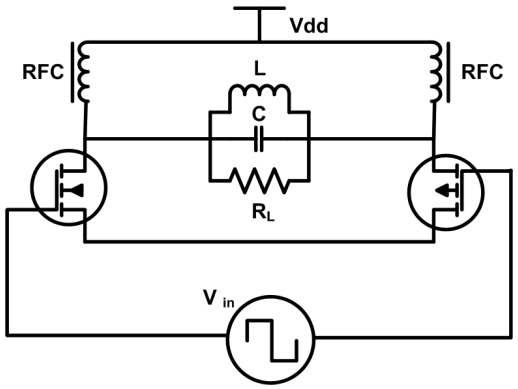


Figure 2.18: Class D Amplifier Current Switching

particularly audio amplifiers and switch mode power supplies. At RF frequencies the CSCD amplifier is generally found more suitable. The sinusoidal voltage across the device ensures zero voltage switching can be achieved, easing the design process by reducing the effects of parasitics of the transistor and surrounding circuitry [24]. Additional work on the generation of a suitable drive signal needs to be carried out before they are suitable for communications signal amplification. This will be discussed further in Section 2.3.0.5 with additional information provided in Appendix B.

2.2.5.2 Class E amplifier

The Class E amplifier is a single transistor structure which conducts for 180^o of the waveform. There is a parallel capacitor that discharges for the other 180^o of the waveform to complete the signal period and provide a linear output. The Class E amplifier also has a theoretical

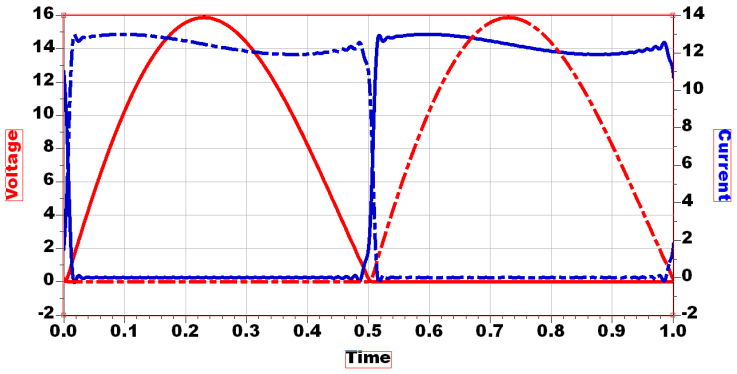


Figure 2.19: Drain - source current and voltage waveforms for a Current Switching Class D (CSCD) power amplifier, the waveforms are the inverse of the VSCD. Solid line represents the waveforms for switch one, the broken lines represents the waveforms for switch two.

maximum efficiency of 100% provided the voltage and current waveforms do not overlap during operation. Typically this is only the case at or near the fundamental design frequency, with a duty cycle of 50% To ensure that there are no switching losses the amplifier must satisfy the switching conditions in equation 2.11 that state that the voltage and the derivative of the voltage must be zero when the switch closes. The zero voltage switching (ZVC) amplifier structure can be seen in Figure 2.20, the capacitor C_p charges while the switch is open and discharges to complete the output wave cycle when the switch is closed. The waveforms for Class E operation are presented in Figure 2.21.

$$ClassE \Leftrightarrow \left\{ \begin{array}{l} v_{sw}(t_1) = 0 \\ \frac{dv_{sw}}{dt}|_{t=t_1} = 0 \end{array} \right\} \tag{2.11}$$

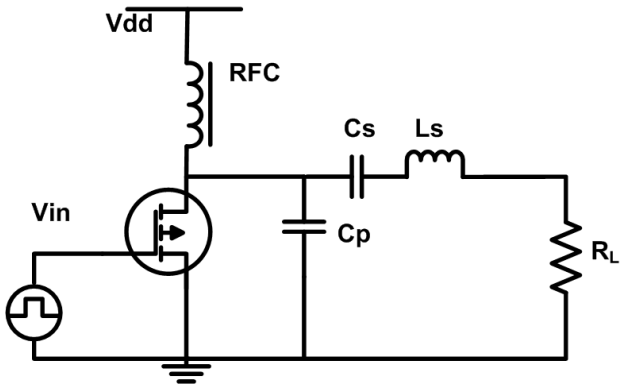


Figure 2.20: Class E Amplifier Zero Voltage Switching

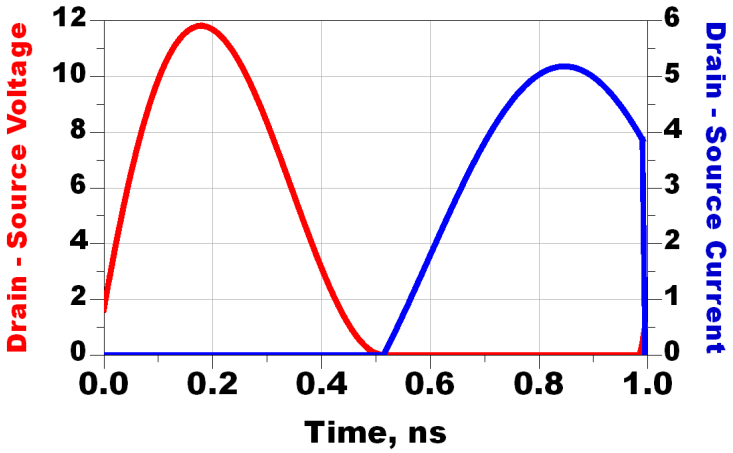


Figure 2.21: Drain - source current and voltage waveforms for a Class E power amplifier.

The complement of this amplifier architecture is a zero current switching variant in Figure 2.22 where the capacitor C_p is replaced with and inductor. The waveforms for the inverse Class E amplifier are presented in Figure 2.23. Similar to the ZVS amplifiers the current and its first derivative must be zero when the switch opens. The series inductor L_s performs the same function as the parallel capacitor in the ZVS amplifier. The advantage of this is that there is zero switching losses, however the power stored in the internal capacitance of the switching device is now dissipated in the switch, reducing overall efficiency. This has the additional effect of lowering the overall operating frequency of the Class E^{-1} compared to a Class E. Inverse Class E has some advantages over standard Class E. The implementation relaxes the peak break down voltage requirement of the drain - source voltage by up to 20%. In addition the feed inductance is lower and therefore can be implemented using lumped elements [52].

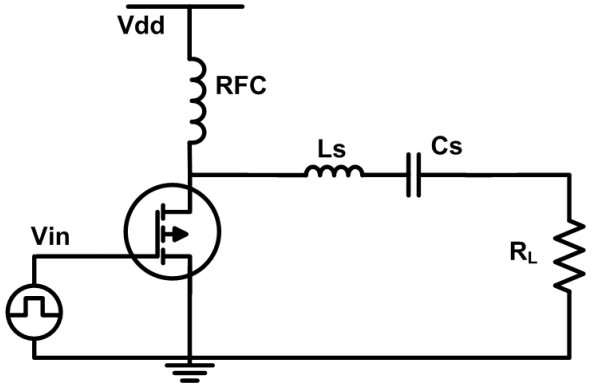


Figure 2.22: Class E Amplifier Zero Current Switching

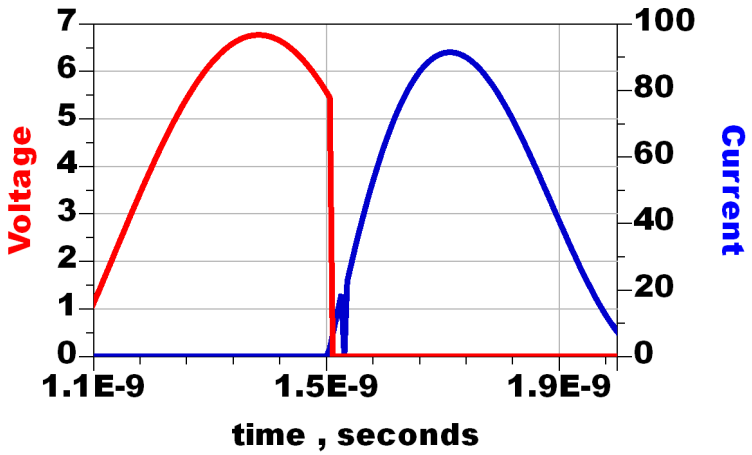


Figure 2.23: Drain - source current and voltage waveforms for an inverse Class E power amplifier.

2.2.5.3 Class F amplifier

The Class F power amplifier is similar in structure to Class E, however the output matching network is comprised of LC tuned harmonic tanks which are used to shape the drain to source voltage across the transistor to reduce losses and increase efficiency. The principle of operation was developed in 1919 by Tyler for AM modulation [53]. In Figure 2.24 the structure of a Class F amplifier with odd harmonic output matching network can be seen. The result of this structure is that the drain-source voltage contains only odd harmonics and the drain current contains only even harmonics. Therefore the input impedance of the load network represents an open circuit at even harmonics and a short circuit at odd harmonics. In this case V_{DS} is symmetrical for the lower and the upper half of the cycle. Increasing the number of harmonic chambers in the matching network will make the drain-source voltage more square, further reducing any the possible overlap of current and voltage waveforms.

A Class F amplifier with an even order harmonic resonant elements in the output is constructed as the circuit in Figure 2.24 with the odd harmonic chambers replaced with even order ones. The drain-source voltage contains only even harmonics and the drain current contains only odd harmonics. Therefore the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics. In this case V_{DS} is not symmetrical for the lower and the upper half of the cycle. The wave forms produced by the voltage and current can be modified by the output matching network and the number of

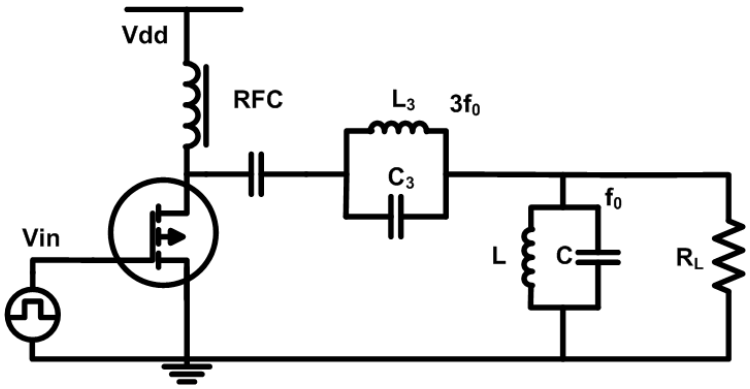


Figure 2.24: Class F Amplifier Odd Harmonic Tuning

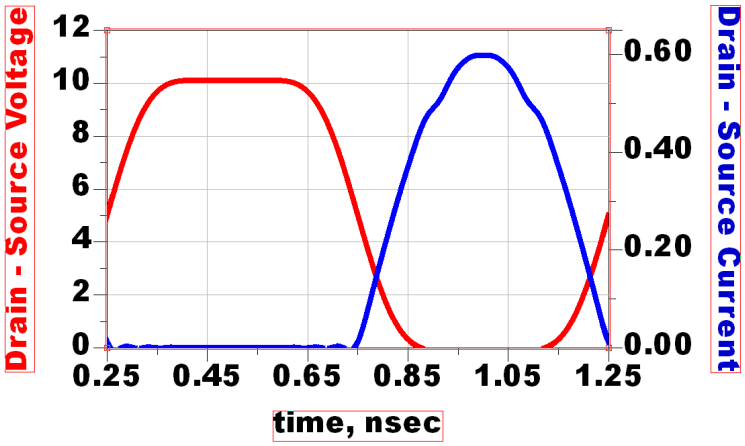


Figure 2.25: Drain - source current and voltage waveforms for a Class F power amplifier.

resonators it contains. Figure 2.25 presents the waveform for a Class F power amplifier with terminations for the 3rd and the 5th harmonic.

2.2.6 An overview of amplifier class of operation

A comparative overview of power amplifier classes of operation is presented for linear mode amplifiers in Table 2.2 and switch mode power amplifiers in Table 2.3. The compromise for linear mode amplifiers is efficiency verses linear operational bandwidth. Of these the Class AB amplifier is typically used for digital communications signals with amplitude and phase modulation, as it presented the best compromise in this respect.

The switched mode classes are capable of extremely high theoretical efficiency, however this is only achievable over a limited range of input signals, as the amplifier is comprised of ideal components. These amplifiers require alternative configurations in order to efficiently

amplify the desired communications signal. A selection of these topologies are outlined in the following section.

Table 2.2: Linear mode amplifier classes of operation

Amplifier	Class A	Class AB	Class B	Class C
Operation	Linear	Linear	Linaer	Linear
Conduction angle (Deg)	$\theta = 360$	$360 < \theta < 180$	$\theta = 180$	$180 < \theta < 0$
Maximum Theoretical Efficiency	50 %	50% - 78.4%	78.4%	78.4% - 100%
Gain (dB)	G_{Max}	$G_{Max} - (G_{Max} - 6)$	$(G_{Max} - 6)$	$(G_{Max} - 6) - 0$
Linearity	Excellent	Excellent - Good	Good	Poor

Table 2.3: Switch mode amplifier classes of operation

Amplifier	Class D	Class E	Class F
Operation	Switching	Harmonic Switching	Harmonic Switching
Conduction angle (Deg)	$\theta = 180$	$\theta = 180$	$\theta = 180$
Maximum Theoretical Efficiency	100%	100%	100%
Gain (dB)		$(G_{Max} - 7.052)$	$(G_{Max} - 4.951)$
Linearity		Good	Good

2.3 Amplifier Topology

Power amplifier topologies are designed to achieve additional efficiency and/or linearity through more advanced modulation techniques. Of these the two most common are load and drain modulation. Load modulation is a technique of modifying the load impedance seen by the amplifier stages. Drain modulation is a technique where the drain voltage is modified, the aim is to have the transistor in the most efficient region of operation for a longer period of time. By applying these methods to the traditional amplifier structures outlined in Section 2.2.4 and Section 2.2.5 additional performance can be achieved. While the benefits of advanced amplifier topologies are very attractive, they are more complex than single stage amplifiers. However with advancements in both transistor technology and digital signal processing these methods are becoming more popular. Firstly in this section two drain modulation techniques will be

introduced, envelope elimination restoration and envelope tracking. The remain amplifier topologies, Doherty, outphasing and Class-S utilize load modulation.

2.3.0.1 Envelope Elimination Restoration

Envelope elimination restoration or polar modulation amplifiers were first introduced in 1952 [54]. An outline of the system is presented in Figure 2.26. The method aims to achieve more efficient operation by having the main amplification stage operate in a saturated or switch mode configuration only amplifying the signal phase. The drain supply to the amplifier is modulated with the baseband envelope of the amplitude modulation component. The architecture shows potential for improved system efficiency, however this is highly dependent on the efficiency of the envelope detector and amplitude modulator circuit. Many techniques such as switch and sigma delta power supplies have been examined, however in each case a trade off between bandwidth, linearity and system efficiency is made. An example of EER is presented in [28] where the authors achieved a system efficiency of 44%. One of the major disadvantages of EER transmitters is the accurate generation of low power signals. Drain supply voltage has a minimum value below which the transistor will not operate. This value will define the minimum linear output power, and as a result the maximum dynamic range associated with the amplifier, severely limiting the amplifier spectral linearity. This topology has been demonstrated for handset specifications, however base station implementations still remain a challenge.

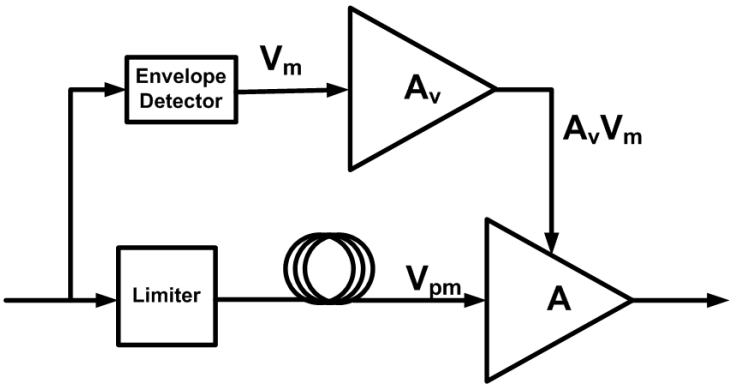


Figure 2.26: Envelope Elimination Restoration

2.3.0.2 Envelope Tracking

The envelope tracking amplifier seen in Figure 2.27 is an extension of the EER transmitter presented in Section 2.3.0.1. However the input to the amplifier is also amplitude modulated, enabling higher efficiency amplifiers to be used for the supply voltage, while maintaining equivalent or better amplifier linearity than the EER topology. A Class-S amplifier in low pass configuration operating as a DC/DC converter modulates the RF amplifier's supply voltage with a pulse width equivalent of the envelope of the input signal. This architecture achieves high efficiency by operating the RF amplification stage close to the 1 dB compression point at all times, increasing efficiency in back off dramatically. The delay block before the amplifier compensates for the delay through the envelope detection path relative to the main amplification path. By enabling linear amplification with switching power amplifier the envelope tracking topology has achieved 70% drain efficiency [55]. As the amplifiers are cascaded this some what limits the maximum achievable output efficiency. In this topology the design of the drain supply network can be difficult, in order to ensure transistor stability some limitations are placed on the bandwidth of the signals amplitude component, limiting overall system bandwidth.

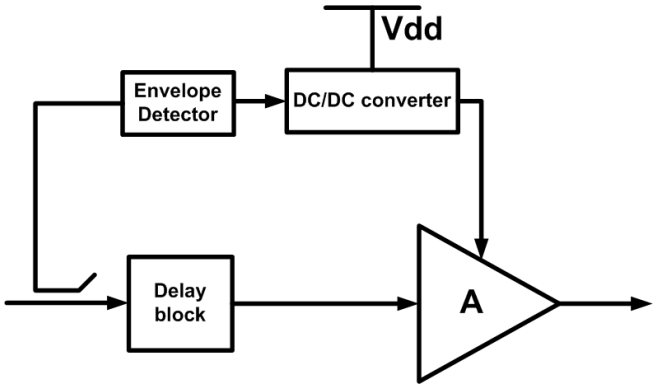


Figure 2.27: Envelope tracking

2.3.0.3 Doherty

The Doherty amplifier was proposed in 1936 [23]. The amplifier achieves increased efficiency at back-off output power through load modulation, by combining the output of two or more linear power amplifiers as seen in Figure 2.28. The topology uses a main amplifier generally a linear amplifier, Class B or AB and a peaking or auxiliary amplifier biased much higher than the

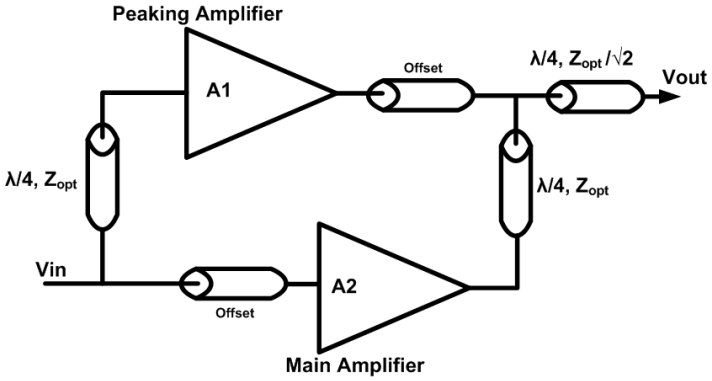


Figure 2.28: Doherty Amplifier

main amplifier into Class C operation. Load modulation requires a quarter wave transformer at the output of the main amplifier as such the input to the peaking amplifier is delayed by an equal amount to align the output signals. For maximum efficiency the peaking amplifier will only turn on when the main amplifier is saturated. Doherty amplifiers are capable of delivering increased efficiency from 6-10 dB into power back off [56], greatly increasing the overall transmitter efficiency. Further efficiency improvements have been demonstrated in Doherty amplifier topologies with three amplifier stages [57] and asymmetric power transistors [58]. Up to 52% PAE has been demonstrated for a symmetrical Doherty amplifier where the output is heavily saturated [59]. The amplifier has some disadvantages, the tuned output combiner, comprising of quarter wavelength transmission lines, and therefore will limit the efficiency across frequency and operational bandwidth. Additionally the amplifier experiences additional memory as both amplifier become active at higher output powers, as such more advanced linearisation techniques are required.

2.3.0.4 Outphasing amplifier

The outphasing power amplifier was first introduced by Henri Chireix in 1935 [60] as a method to improve both efficiency and linearity in amplitude modulation transmitters. In 1974 the concept was later revised by [61] with the concept of LINC (Linear amplification using Non-linear Components). The work by Cox demonstrated how highly non-linear yet efficient devices could be arranged to provide a linear output. The concept of the outphasing amplifier is illustrated in Figure 3.1.

The principle of operation is relatively simple, the amplitude modulated signal is converted

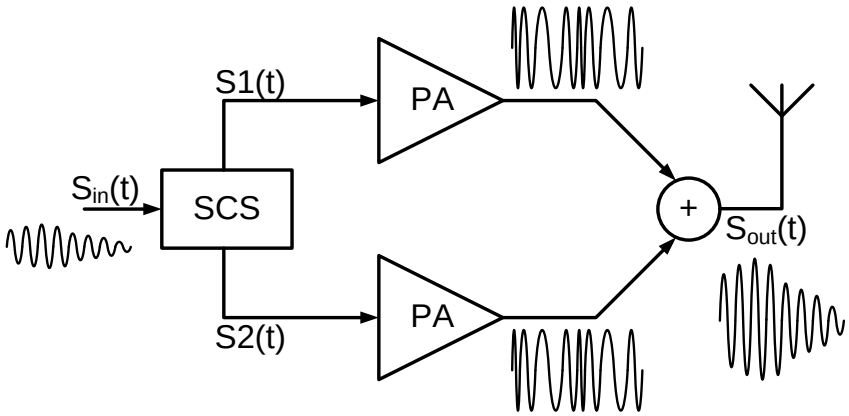


Figure 2.29: Outphasing amplifier

to a pair of phase modulated signals with constant amplitude. These signals are then amplified by identical saturated linear PA's or switch mode PA's. The constant envelope amplified signals are then re-combined in the power combiner stage, resulting in an amplified version of the amplitude modulated input signal. Efficient operation is achieved as both amplifiers are operating with constant output power close to or at peak efficiency, reducing the losses in the transistor. The key to efficient operation is the signal component separator, the amplitude to phase modulation process allows the PA's to operate at a constant output amplitude. Operating the amplifiers at a constant amplitude negates their non-linear input-output power characteristics, this enables the system to employ highly efficient PA architectures while maintaining a linear output, provided the input signal component separator and the output power combiner are linear. Digital implementations have demonstrated greater than 70% drain efficiency with up to 60% drain efficiency at 8dB power back-off [29]. As with the Doherty amplifier the system bandwidth is limited by the design of the output Chiriex combiner. Additionally the constant envelope outphasing signals experience bandwidth expansion when compared with the modulated signals. This increases the bandwidth requirement of all components in the system. Any limitations on the signal bandwidth will severely impact over all linearity of the topology.

2.3.0.5 Class - S amplifier

The Class - S amplifier topology presented in Figure 2.30 differs from the classes of operation outlined in Sections 2.2.4 and 2.2.5 in that it also includes a modulator and output filter.

The amplifier uses switched-mode classes of power amplifiers in conjunction with high speed binary modulators to achieve a highly efficient output [62]. The binary modulator operates at multiples of the base band signal frequency and a bit rate of at least two or more times that of the RF frequency is required. There are several modulation schemes which can be employed such as pulse density modulation, pulse width modulation or pulse position modulation, each with their own benefits and drawbacks. The switching stage, which can be any switching class amplifier, for example Class D/E/F, have the potential to deliver between 90-100% of the DC power to the load as RF power. This has been successfully achieved in low frequency applications such as DC/DC converters and audio amplifiers, however the switching frequencies required for RF modulation and amplification are difficult to achieve. A system has been realised for LTE signal achieving up to 33% efficiency for a modulated output [63].

The upper operating frequency of digital circuits somewhat limits the bandwidth and dynamic range of pulse density implementations for communication signal frequencies. Pulse density modulators can be achieved in a digital logic alone and as such have the potential to offer reduced cost. The pulse width and pulse position require expensive analogue circuitry, in addition the flexibility of these implementations are limited. However the analogue implementation can achieve higher operating frequencies and wider signal bandwidths. Further information on the digital modulator and particularly the pulse density modulator can be found in Appendix B. At the output a reconstructed filter is required to translate the binary amplified signal from the pulsed encoding into an analogue time domain signal. The signal bandwidth of the Class-S amplifier is defined by the reconstruction filter, which is in turn dependant on the capabilities of the digital modulator.

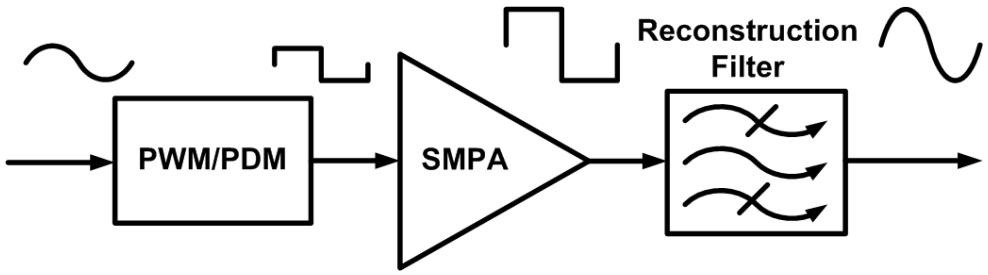


Figure 2.30: Class-S amplifier

2.4 Amplifier Distortion

An ideal amplifier should be 100% efficient, linear and have infinite bandwidth, however due to the constraints of physical systems this is not possible. The linearity of the amplifier depends on both the transistor type and the amplifier structure. As described in Section 2.2 the transistor linearity is dependant on input amplitude, operation frequency, environment temperature and angle of conductance. To avoid interfering with neighbouring transmissions, the amplifier must conform to the legal spectral characteristics associated with the communication standard. The largest generator of out of band signal components is the relationship of input to output signal amplitude. If the relationship is non-linear, a signal that incorporates amplitude modulation will experience spectral spreading, generating unwanted noise in adjacent communications channels. In this section the causes and effects associated with non-linear power amplifiers are outlined.

2.4.1 Clipping

Modern communication modulation schemes achieve high data rates by modulating both amplitude and phase components of the signal. A compromise between linear and efficient operation means the amplifier is operated as close to the saturation point as possible. In the time domain the maximum signal amplitude varies between modulation schemes. If the amplitude of the input signal is too great it will cause the transistor in the amplifier to saturate. Depending on the transistors and the amplifier design, the transition into the saturation region may be gradual or abrupt. If it is abrupt the output signal will be clipped. Clipping is a sharp discontinuity to the output signal, information in the signal is lost and frequency spreading will occur in the output spectrum.

2.4.2 Gain Expansion and Compression

Gain is the ratio of amplitude between an amplifiers input and output signals. In an ideal amplification system the gain should remain constant up to the maximum output power. However this is not the case, in practise amplifiers generally reach a compression point, commonly called 1 dB compression point, demonstrated in Figure 2.31. At this point an increase of input power no longer relates to the same increase in output power. The 1 dB

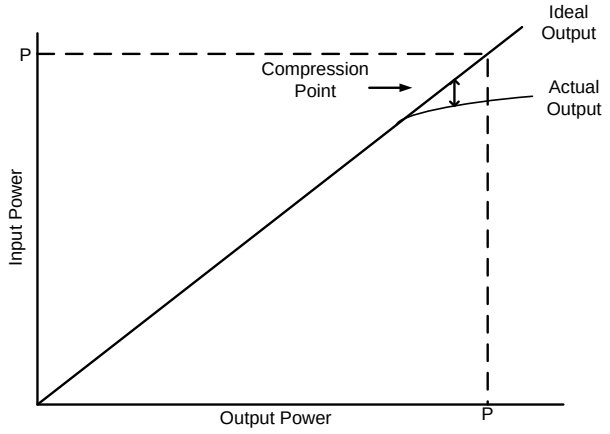


Figure 2.31: Illustration of gain compression which can occurs in amplifier circuits.

compression point commonly marks the beginning of a region of strong non linearity in the amplifier. It is also possible for the opposite to occur, i.e. an increase in the gain can occur [64]. Both gain expansion and compression will cause non-linearity in output amplitude [65].

2.4.3 AM/AM AM/PM distortion

AM/AM is the relationship between the input amplitude to the amplifier and the measured output amplitude. AM/PM is the relationship between the input amplitude to the amplifier and the output deviation in signal phase from the ideal. The amplitude can be affected by device linearity, once the amplifier is operated beyond the 1 dB compression point it will experience strong non-linear amplitude effects. The amplitude of the input signal can also effect the phase of the output, this can occur at any amplitude but is typically more pronounced beyond the 1 dB compression point. The distortion of an amplifier is typically characterised in AM/AM AM/PM scatter plots. These scatter plots can be expressed using the normalised signal magnitudes for the input and output signals or the signals power in log scale (dBm), for the remainder of this work any AMAM/AMPM plots will be presented using normalised signal power. The relationship between input and output signal using these characteristics provide a visual representation of the linear and non-linear regions of operation.

2.4.4 Harmonic Distortion

The generation of additional tones in the frequency spectrum and multiples of the fundamental frequency is described as harmonic distortion. The additional tones are generated through the

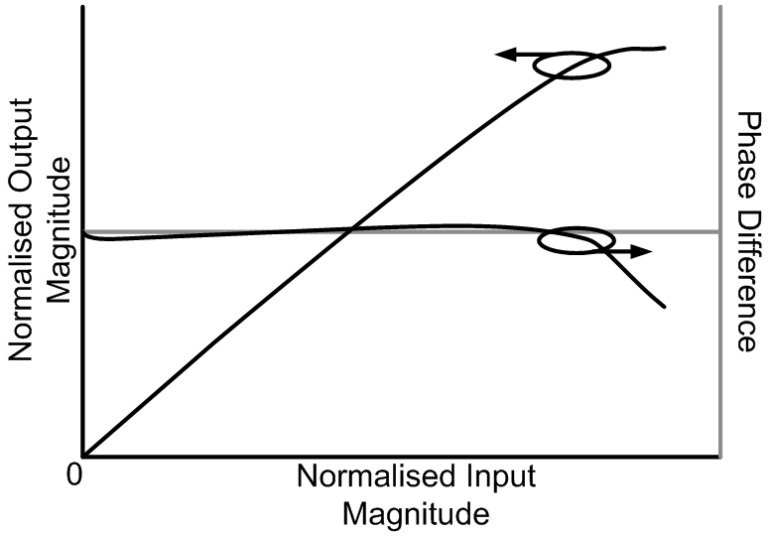


Figure 2.32: Illustration of AMAM AMPM non-linearity that can occur in amplifier circuits.

non-linear polynomial function describing the amplifier as seen in equation 2.12. A single tone input $Xcos(\omega t)$ applied to the amplifier function will return as in equation 2.13.

$$A(x) = a_1 x_i + a_2 x^2 + a_3 x^3 ... a_n x^n. \tag{2.12}$$

$$A(x) = a_1 Xcos(\omega t) + \frac{a_2}{2} Xcos(2\omega t) + \frac{a_3}{4} Xcos(3\omega t) + ... \tag{2.13}$$

The severity of the harmonic distortion is determined by the non-linearity of the amplifier, therefore it is a good figure of merit for the performance of the power amplifier. Harmonic distortion of an amplifier can be described as the power at a multiple of the fundamental frequency compared with the power at the fundamental. This is demonstrated in equation 2.14.

$$HD_{nf} = \frac{Vout,_{nf}}{Vout,_f}. \tag{2.14}$$

Total harmonic distortion is the sum of all of the harmonic distortion components in the output signal. Equation 2.15 demonstrates this.

$$THD = \frac{\sqrt{\sum_{n=2}^{N} Vout,_{nf}}}{Vout,_{1f}} \tag{2.15}$$

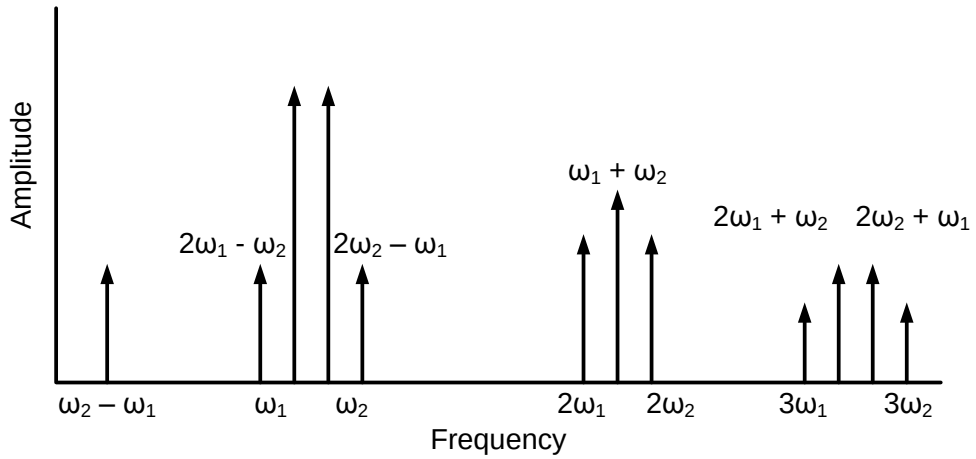


Figure 2.33: Illustration of intermodulation distortion which can occur in amplifier circuits.

2.4.5 Intermodulation Distortion

Intermodulation distortion is the result of two or more frequencies $[\omega_1, \omega_2]$ being passed through a non-linear device. The output of the device includes the original signal and the sum $[\omega_1 + \omega_2]$ and difference $[\omega_1 - \omega_2]$ of the input frequencies. The non-linearity of the device produces harmonics of the input signal at integer multiples of the original signal frequency $2\omega_1, 3\omega_1, 4\omega_1$.... The products for some of these signals is outlined in Figure 2.33. Odd order intermodulation products for example, the third order products $[2\omega_1 \pm \omega_2]$ $[2\omega_2 \pm \omega_1]$ and the fifth order products $[3\omega_1 \pm 2\omega_2]$ $[3\omega_2 \pm 2\omega_1]$ will occur close to the input signals, while even order intermodulation produces occur out of band. If the odd order produces have sufficient power they can interfere with the transmitted signal as well as the frequencies adjacent to it. The results will cause the transmitter to fail the spectral requirements for the transmitter and in sever cases result in bit errors in the transmitted signal. Additionally if the harmonics, both odd and even, are high enough power they will effect transmitter efficiency as DC power is converted into unwanted RF signals.

2.4.6 Cross Modulation Distortion

This is similar to intermodulation distortion described in 2.4.5 however intermodulation distortion refers to two carriers that are either part of the same signal or close to each other for transmission i.e. in the same signal band. Cross modulation distortion however refers to the interference between two carriers that are in different signal bands [66]. In intermodulation distortion, because the signals are relatively close together the odd order harmonics cause

in-band distortion. However with increased spacing between carrier signal IF frequencies, particularly in carrier aggregation systems for fourth generation cellular communications standards, some even order harmonic distortion may fall with one of the desired band of operation. This is an issue that is common in receivers that operate in a dual bands simultaneously, and is an issue of increasing concern in dual band transmitter architectures [67].

2.4.7 Memory Effects

Memory effects are the changes in the power amplifier's output that depend on previous values of the input signal. There are two sub-categories of memory, which are determined by the period of the memory effect. Long term memory effects include temperature fluctuations and ageing, causing variations which may be on the order of milliseconds to years. Long term memory effects are independent of the signal bandwidth. Short term memory effects are due to the storage of energy within the PA structure, drain supply network, gate bias supply network and the frequency response of the amplifier. Short term memory effects are typically on the order of nano to micro seconds. Short term memory effects are directly related to signal bandwidth, depending on the passband of the amplifier and the charge and discharge times of the parasitics that reside within the transistor and the supply networks.

In either case the memory effects are often equated to a filtering effect of the system and can be described by the function in equation 2.16 where n is the current input sample and M is the number of previous input samples which impact the output. The relationship of short term memory effects is easily described by this formula, however the number of samples it would take to describe long term effects makes such a calculation difficult. When examining the time domain relationship between the input and output signals an AMAM AMPM plot are typically used. Memory in the output signal can be identified as a spreading in the sample feature space. In the frequency domain it often causes an imbalance between upper and lower power of the non-linearity [68].

$$y(n) = \sum_{m=0}^{M} f(x(n-m)) \tag{2.16}$$

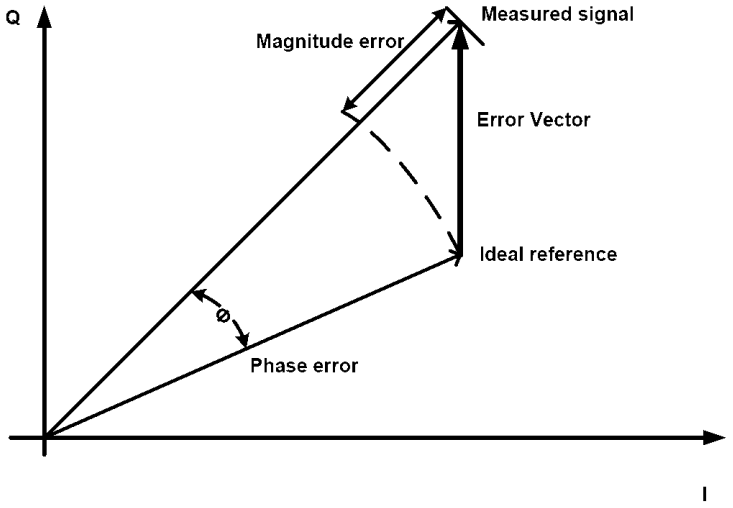


Figure 2.34: An illustration of Error Vector Magnitude(EVM) which can occur in amplifier circuits.

2.4.8 Error Vector Magnitude

Error vector magnitude (EVM) is used to quantify the distortion produced by a non-linear system as seen in Figure 2.34. EVM is determined by the integrity of a digital modulation scheme. Analysing the individual samples and using the difference between the ideal constellation points and the measured signal a calculation of percentage error can be made, the equation of the measurement is outlined in equation 2.17, where P_{error} is the power of the error component of the signals and $P_{referece}$ is the original signal source, this is used to determine the error vector when compared with the measured signal.

$$EVM(dB) = 10log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \tag{2.17}$$

EVM is the figure of merit that incorporates all possible time domain non-ideal effects on the signal data. This figure of merit is used in determining the impact of signal processing techniques, the impact that non-ideal effects in the transmitter and the impact of non-ideal effects introduced by the transmission channel.

2.4.9 Overview of Amplifier Distortion

In this section a brief overview of the effects typically seen during non-linear amplifier operation are outlined in this section. The frequency effects such as harmonic distortion,

intermodulation distortion and cross modulation distortion, result from the non-ideal time domain effects, gain expansion/compression, clipping and AM/AM AM/PM. These non-linear effects are quantified in the frequency domain using adjacent channel power ratio (ACPR), an measure of percentage out of band noise in comparison to signal power. ACPR is therefore a measure of the magnitude of out of band signal components generated through harmonic distortion, intermodulation distortion and cross modulation distortion. All signal standards have a maximum allowable ACPR level that the transmitter must adhere to, this figure of merit will be used extensively in power amplifier analysis during the up coming chapters. The time domain accuracy of the data signal will be impacted again by gain expansion/compression, clipping and AM/AM AM/PM from the power amplifier. Typical figures of merit for time domain data are EVM and a measure of bit error proportional to the number of bits successfully transmitted. Mathematical functions capable of describing these non-linear effects are introduced in the following section.

2.5 Behavioural Modelling

Behavioural modelling, also known as black box modelling, is a method of using mathematical functions to describe a complex system using only the input, output and control signal applied to that system. They have proven to be very useful for modelling of non-linear radio frequency components, particularity when applying modulated signals. Carrying out wide band system characterisation using traditional circuit simulators and circuit solvers such as transient and harmonic balance simulations, is computational expensive. Behavioural models provide a sufficiently accurate system model while greatly reducing the computational overhead. The accuracy of the model is dependant on both model parameters and available system information. To achieve an accurate system model all inputs which affect the system operation must be accounted for. This section will outline some common modelling techniques for RF power amplifier, identifying their strengths and weaknesses. The following functions are derived from baseband signals, and therefore are baseband or envelope equivalent models of the RF system.

2.5.1 Static Modelling functions

Static system models derive the input output relationship of the system using only the current input values. In relation to radio frequency equipment, and more directly power amplifiers, they cannot model frequency effects or dynamic transient effects created due to the parasitics of the device or system. The following are the more common modelling functions associated with power amplifier operation. The Sahel and the Ghorbani models are presented first. These models assume that the order of non-linearity is fixed, using a fixed form equation for the amplitude and phase relationship they were designed to describe the non-linear response of the TWT power amplifiers. More flexible polynomial functions are used to describe the AMAM AMPM response of a non-linear system. Providing a more general model for all amplifier types.

2.5.1.1 Sahel Model

In [69] several frequency dependant and frequency independent models for travelling wave tube (TWT) power amplifiers are presented. A pair of two parameter functions capable of modelling the amplitude and phase relationship and an alternate set capable of modelling the quadrature relationship for a frequency independent TWT amplifier are outlined in equations 2.18 - 2.24 . The benefit of the two parameter model is that it is computationally simple.

$$x(t) = r(t)cos[\omega_0 t + \psi(t)] \tag{2.18}$$

$$A(r) = \frac{a_a r}{(1 + \beta_a r^2)} \tag{2.19}$$

$$\Phi(r) = \frac{a_\Phi r}{(1 + \beta_\Phi r^2)} \tag{2.20}$$

$$I(t) = r(t)cos[\omega_0 t + \psi(t)] \tag{2.21}$$

$$Q(t) = r(t)sin[\omega_0 t + \psi(t)] \tag{2.22}$$

$$I(r) = \frac{a_i r}{(1 + \beta_i r^2)} \tag{2.23}$$

$$Q(r) = \frac{a_q r^3}{(1 + \beta_q r^2)^2} \tag{2.24}$$

2.5.1.2 Ghorbani Model

The Ghorbani model [70] is similar to the previous Saleh model, however in this case, a pair of four parameter functions represent the amplitude and phase response of a given non-linear system. The behaviour of this model is described by equations 2.25 and 2.26, describing the amplitude and phase distortion of an amplifier.

$$A(r) = \frac{X_1 r^{X_2}}{(1 + X_3 r_2^X)} + X_4 r \tag{2.25}$$

$$\Phi(r) = \frac{Y_1 r^{Y_2}}{(1 + Y_3 r_2^Y)} + Y_4 r \tag{2.26}$$

2.5.1.3 Polynomial Model

Polynomial functions are a simple yet robust technique commonly used for both device and system modelling of radio frequency circuits [71]. The system is characterised for a range of input amplitudes, measuring the corresponding output amplitude and phase, the response of the system can be visually illustrated. From this illustration a mathematical model of the system response can be derived. The AMAM AMPM model describes the input-output amplitude and the input amplitude - signal phase deviation. It is possible to describe this relationship using a variable order of polynomial functions.

$$y(n) = \mid y(n) \mid e^{\phi_{x(n)} + \delta\phi_{y(n)}} \tag{2.27}$$

$$\mid y(n) \mid = \sum_{j=0}^{P} a_j \mid x_j(n) \mid^j \tag{2.28}$$

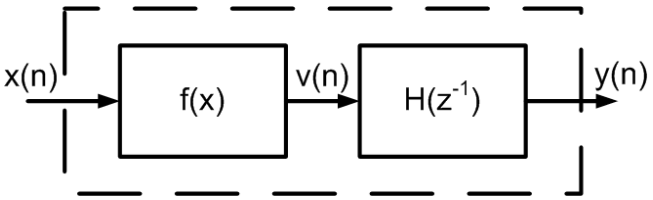


Figure 2.35: Overview of Hammerstein model

$$\delta\phi_{y(n)} = \sum_{j=0}^{P} b_j \mid x_j(n) \mid^j \tag{2.29}$$

2.5.2 Memory capable models

The models outlined in this section are capable of characterising the amplitude dependant non-linear effects in a similar method to the static non-linear models, however they have additional coefficients that are capable of modelling dynamic effects as well. This is achieved by using selected previous samples of the input as well as the current input sample. The resulting models are more complex than the models outlined in Section 2.5.1, however this increase in computation effort enables accurate wide-band characterisation of RF systems.

2.5.2.1 Hammerstein Model

The Hammerstein model outlined in Figure 2.35 is a behavioural model comprising of a static non-linearity $f(x)$ and a linear time invariant (LTI) system $H(z^{-1})$. The inclusion of the linear time invariant system enables frequency dependant or memory effects to be characterised. The block $H(z^{-1})$ can be implemented using a variety of LTI systems however the most common are finite impulse response (FIR) systems or infinite impulse response (IIR) systems. There are benefits to each implementation, for example, the FIR system is more stable while an IIR system is more computationally efficient [72]. Equations 2.30 and 2.31 outline an IIR implementation of a Hammerstein model.

$$v(n) = \sum_{p=0}^{P} \gamma_p x(n) \mid x(n) \mid^P \tag{2.30}$$

$$y(n) = \sum_{d=1}^{D} \alpha_d y(n-d) + \sum_{m=0}^{M} \beta_m v(n-m) \tag{2.31}$$

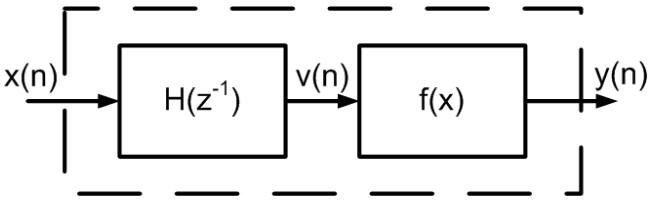


Figure 2.36: Overview of Weiner model

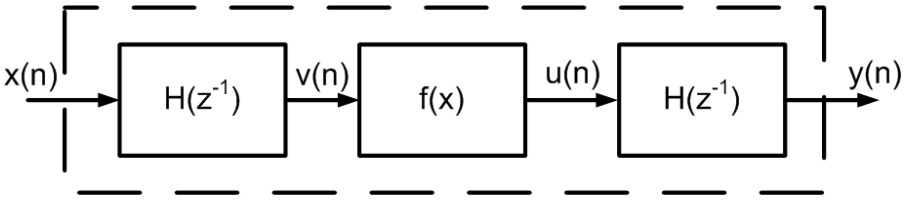


Figure 2.37: Overview of Weiner - Hammerstein model

2.5.2.2 Weiner Model

The Wiener model outlined in Figure 2.36. Operating on a similar principle to the Hammerstein model using static non-linearity with LTI systems to achieve a memory capable model. However the order of implementation has been reversed. Similar to the Hammerstein both FIR and IIR systems are used to implement the LTI block. A complex LTI system can increase the complexity of calculating the non-linear component $f(x)$. Therefore in many cases, particularly in implementations where model inversion is required, an FIR system is used. The equations for the Weiner model with an FIR system are outlined below.

$$v(n) = \sum_{m=0}^{M} \beta_m x(n-m) \tag{2.32}$$

$$y(n) = \sum_{p=0}^{P} \gamma_p v(n) \mid v(n) \mid^P \tag{2.33}$$

2.5.2.3 Weiner-Hammerstein Model

The structure of the Weiner-Hammerstein model is outlined in fig 2.37, it consists of a Weiner model in series with a Hammerstein model. This results in two non-linear blocks being placed in series and therefore can be considered as a single non-linearity.

2.5.2.4 Volterra Series

Volterra series behavioural modelling is a powerful time series estimator for non-linear systems. The model uses every possible combination of terms up to a given order and for a given memory depth. Therefore the Hammerstein, Weiner and Weiner - Hammerstein coefficients are subsets of the Volterra series expansion. It has been extensively used in both biological and financial modelling in both its continuous time and discrete form. To model RF power amplifier we use the discrete time, base-band from the the series [73]. To date it has been successfully used to model various RF power amplification systems. The Volterra series is outlined in equations 2.34.

$$y(n) = \sum_{k} \sum_{l_1} \cdots \sum_{l_{2k+1}} h_{2k+1}(l_1, l_2, \cdots, l_{2k+1}) \prod_{i=1}^{k+1} x(n - l_i) \prod_{i=k+2}^{2k+1} x^*(n - l_i) \tag{2.34}$$

Where y is the output, x is the input, h represents the Volterra coefficients, k is the order of non-linearity and l is the memory depth. The Volterra series is composed of all possible combinations of non-linear order and memory terms and as the terms P and M increase the number of weights increases rapidly. This is undesirable as the purpose of a behavioural model is to reduce the computational complexity therefore several reduced forms of the full Volterra kernel have been presented for power amplifier modelling. In power amplifiers we ideally want to model the non-linear effects that will cause interference with neighbouring transmission. From Section 2.4.5 we know that intermodulation distortion generally results from odd order non-linear harmonics. Therefore a popular model for the Volterra series and indeed many non-linear power amplifier models is to remove the even order terms from the non-linear function. Therefore we are left with a modified Volterra function outlined in 2.35.

$$y(n) = \sum_{k=0}^{P} \sum_{qk=0}^{M} h_k(l_k) x(n - l_1) \prod_{i=1}^{(k-1)/2} x(n - l_{2i}) x^*(n - l_{2i+1}) \tag{2.35}$$

The modified Volterra is useful for standard signal band amplification, however the original or a further modified function must be used in systems where even order harmonics are a concern, for example cross modulation in dual band amplifiers, or wide band amplifiers capable of transmitting at the even order harmonic frequencies.

2.5.2.5 Memory Polynomial

A generalised form of the Hammerstein model, the memory polynomial is formed by selecting individual filters for each non-linear order. Combining the non-linear orders and individual filters associated with them a two dimensional array can be formed, the generalized Hammerstein model in equation 2.36.

$$y(n) = \sum_{k=1}^{K} \sum_{m=0}^{M} -1\alpha_{km} x^k(n-m) \tag{2.36}$$

Taking the narrow band case for band limited operation we choose only the combinations that form $x(n) \mid x(n-m) \mid^k -1$, the resulting function is the memory polynomial, equation 2.37.

$$y(n) = \sum_{k=0}^{K-1} \sum_{m=0}^{M-1} \alpha_{km} x(n-m) \mid x(n-m) \mid^k \tag{2.37}$$

The memory polynomial presented in [74] is a efficient method of modelling non-linear power amplifiers. In comparison to Volterra series the memory polynomial is very efficient however this comes at a cost of reduced generalization. In [75] the authors introduce the generalized memory polynomial, a method of introducing some cross terms to the memory polynomial, by introducing additional polynomial functions which have a delay between the complex signal and the magnitude of the envelope. The generalised memory polynomial is presented in equation 2.38 where $K_a L_a$ are the number of coefficients for the aligned signal and envelope, $K_b L_b M_b$ are the number of coefficients for the signal with lagging envelope and $K_c L_c M_c$ are the number of coefficients for the signal with leading envelope.

$$\begin{aligned} y(n) = & \sum_{k=0}^{K_{a-1}} \sum_{l=0}^{L_{a-1}} \alpha_{kl} x(n-l) \mid x(n-l) \mid^k \\ & + \sum_{k=0}^{K_{b-1}} \sum_{l=0}^{L_{b-1}} \sum_{m=0}^{M_{b-1}} b_{klm} x(n-l) \mid x(n-l-m) \mid^k \\ & + \sum_{k=0}^{K_{c-1}} \sum_{l=0}^{L_{c-1}} \sum_{m=0}^{M_{c-1}} b_{klm} x(n-l) \mid x(n-l+m) \mid^k \end{aligned} \tag{2.38}$$

The memory polynomial and generalised memory polynomial offer a reduced number of non-linear coefficients when compared with the Volterra series, by enabling selection of

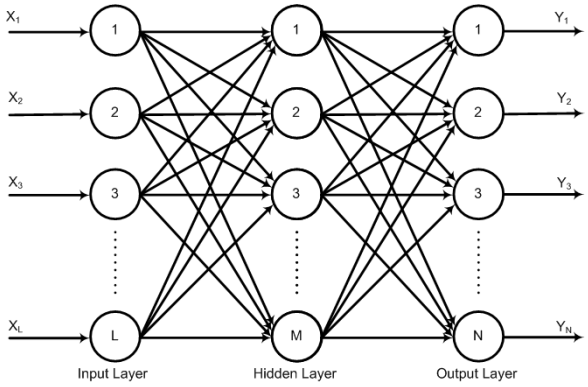


Figure 2.38: Overview of Multi-layer preceptron (MLP)

individual non-linear orders or memory taps. Some of the generality of the model is lost, therefore additional information about the black box system must first be derived before it is possible to implement.

2.5.2.6 Artificial Neural Networks

Based upon the physiological model of the central nervous system, artificial neural networks (ANN) and more specifically the multilayer preceptron (MLP), seen in Figure 2.38 are capable of linear and non-linear behavioural modelling. The MLP is a universal approximator [76], given enough neurons and sufficient training time a MLP system can in theory model any linear or non-linear system.

A MLP consists of three layer types, the input layer arranges input signals X_n for distribution to the following neurons. The hidden layer weights the signal from the input layer and passes the result through an appropriate activation function. The output layer arranges the stimuli from the hidden layer neurons to the required number of outputs signals. Neurons in both the hidden and output layer have the same structure. Neurons in the input layer only accept a single input signal.

$$Y = \sigma \sum_{n=1}^{N} W_n X_n \tag{2.39}$$

Figure 2.39 outlines the structure of a typical neuron. The inputs signals are weighted and summed before being passed through an activation function σ as described in equation 2.39. The activation function can be any linear or non-linear equation. The activation function in the input and output layers of a MLP are commonly linear functions while a non-linear function

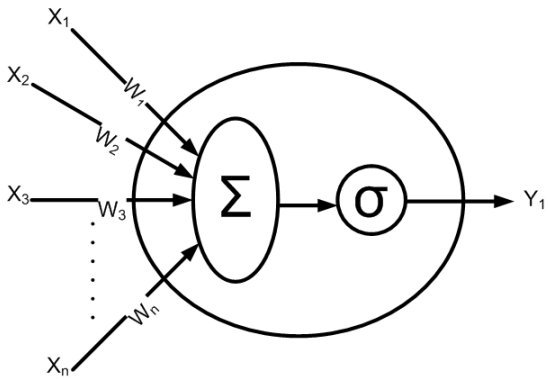


Figure 2.39: Illustration of a single neuron

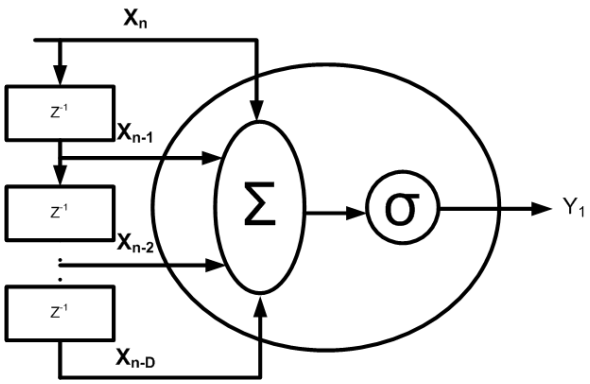


Figure 2.40: Overview of a TDNN input neuron

can be used in the hidden layers. MLP's are capable of modelling linear and non-linear RF circuits as shown in [77]. MLP's as shown in Figure 2.38 have the capability of performing static PA modelling. Neural networks are only capable of real computational operations and therefore to model complex input-output signals a two input-output neural network must be used on the rectangular from of the signal. However by modifying the input neurons a memory capable neural network model can be created.

Time delay neural networks (TDNN) are primarily used to process sequential data and as such are capable of modelling memory effects in a deterministic system [78]. The addition of delay taps within one of the neuron layers, commonly the input layer as seen in Figure 2.40, enables non-linear processing of current and past samples. Equation 2.40 outlines the function of a single input-output TDNN with input A and output B, p is the number of delay taps and z is the number of hidden layer neurons. A bias term b is included in the equation, the bias term allows each neuron to tune the activation function of the hidden layer neurons.

$$B(n) = \sum_{j=1}^{z} w_j \sigma \left(\sum_{i=1}^{p} w_{ij} A(n-i) + b_j \right) + b \tag{2.40}$$

$$Y(x) = \frac{1 - e^{-2x}}{1 + e^{-2x}} \tag{2.41}$$

$$r = \| x - x_i \| \tag{2.42}$$

$$Y(r) = e^{-(\epsilon r)^2} \tag{2.43}$$

As a universal approximator the neural network will use the available neurons to achieve the most accurate behavioural model regardless of model order. This property reduces the number of redundant coefficients that can occur in time series models such as the Volterra series. The flexibility of the neural network structure is highlighted in Chapter 5, providing a unique and accurate multiple input modelling structure for the outphasing power amplifier. Training of the neural network structure must be performed iteratively and is computationally time consuming, this is outlined in the following section.

2.5.3 Overview of Behavioural Modelling

This section offers a brief overview of popular behavioural modelling algorithms for power transistors technology and power amplifier designs. This work will concentrate on the amplifier itself therefore a brief overview of suitable behavioural modelling strategies in relation to amplifier designs will provide context for future work.

Polynomial functions are capable of characterising the magnitude and phase non-linearities that occur in power amplifier structures. The AMAM/AMPM method of characterisation can be applied to many RF active circuits, and is not dependant of the technology that is used. Static algorithms therefore are typically used to model the linear mode of power amplifiers outlined in Section 2.2.4. The simplicity of these designs is limited with the presents of non-linear memory in the majority of cases. However if the transistor has large parasitics they can heavily contribute and a memory approach must be used, for example hysteresis in GaN HMET transistors is prevalent at higher operating powers in any amplifier configuration [79].

Of the memory capable algorithms presented, modified variants of the Volterra series and the generalised memory polynomial are commonly used. Both algorithms offer a combination of linear and non-linear memory taps for wideband characterisation of amplifier effects. Again they can be used for both linear mode and amplifier topologies that include linear and switched mode operation. Amplifier topologies that include strong non-linear memory include Class E/F [80], Doherty [81], EER [82], Envelope tracking [83] and outphasing [84] power amplifiers.

The neural network approach is not as popular as other time series approaches, this may be due to dimensionality or requiring more complex training techniques [85]. In Chapter 5 however a neural network technique will be evaluated. The application of neural networks to this area is relatively new, for traditional amplifier structures, time series have proven to be more computationally efficient. However as the complexity of the transmitter increases there may be a cross over point. Neural networks are a universal approximator, therefore for systems which experience discontinuous non-linearity they may offer a more flexible solution.

2.6 Behavioural Model Training

Parameter estimation or training of the behavioural model can be as important as the capabilities of the model itself. For all of the methods outlined in the static and memory capable modelling sections, the input output relationship can be expressed as the estimated output $\hat{Y}$, the result of a linear convolution between the extracted non-linear values $\overrightarrow{X}$ and the model weights w, this is demonstrated in equation 2.44. Once the kernel values of the model have been extracted the relationship between the kernel, weights and output is linear. Therefore it is possible to use linear parameter estimation functions to extract the model weights. Some popular linear extraction techniques include batch estimation using the least squares algorithm, and adaptive estimation using least mean squares and recursive least squares techniques.

$$\hat{Y} = X^T \overrightarrow{w} \tag{2.44}$$

Neural networks on the other hand require a different approach to parameter estimation. In the neural network structure as outlined in Section 2.5.2.6 there are multiple layers of linear weights and linear or non-linear activation functions, as such the linear extraction techniques cannot be directly applied. The structure requires a back propagation training technique, in this

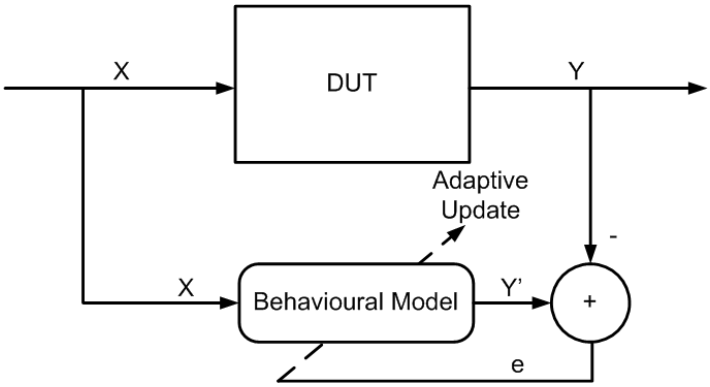


Figure 2.41: Overview of the adaptive training method.

algorithm the error is propagated through the network and a weight update is calculated. The back propagation methods are generally iterative using a gradient descent method to update the individual weights. This section provides a brief overview of the parameter extraction techniques and outlines the strengths and weaknesses with each.

2.6.1 Least Squares Estimation

Least squares estimation is a direct estimation process where the input and output signals are analysed in vector form and an optimal solution can be derived from direct matrix inversion [73]. The least squares solution is identical to that of the minimum mean square error (MMSE) solution however unlike the MMSE solution the least squares solution can be extracted with the input and output sample data alone. The least squares algorithm chooses the weights to minimise the function in equation 2.45. The optimal weight solution is given by

$$J(M) = \frac{1}{M}\sum_{t=1}^{M}\left(y(t) - X^T(t)\overrightarrow{w}\right)^2 \tag{2.45}$$

$$\overrightarrow{w}_{opt} = \hat{R}_{xx}^{-1}\hat{P}_{dx'} \tag{2.46}$$

$$\hat{R}_{xx} = \frac{1}{M}\sum_{t=1}^{M}X(t)X^T(t) \tag{2.47}$$

$$\hat{P}_{dx'} = \frac{1}{M}\sum_{t=1}^{M}y(t)X(t) \tag{2.48}$$

The optimum coefficient set is guaranteed to be extracted as long as the dataset is representative of the device under test (DUT). The main drawback with the least squares approach is the computational complexity in the parameter extraction operation. The size of the matrix X is determined by the number of samples in the input - output data set as well as the number of coefficients in the behavioural model.

2.6.2 Least Mean Squares Estimation

In comparison to the least squares approach the least mean squares algorithm is an adaptive estimation [73]. The adaptive approach evaluates each sample of the input - output dataset individually. The algorithm aims to minimise the cost function defined by the mean-square estimation error in equation 2.49. The algorithm iteratively approaches the optimum solution expressed by the least squares extraction technique, however it cannot extract the optimum set of weights. Instead an approximation is extracted and the algorithm continues with each iteration to try to minimise the error. As a result the sum of errors toggles about the optimum solution, resulting in a residual mean error. The algorithm extraction process is outlined in equations 2.50 and 2.51. The advantage of this approach is the computational complexity of a single update iteration is several orders of magnitude less that the least squares approach. This greatly reduced the system requirements, however the computational complexity expands linearly with the number of iterations required in order to achieve convergence.

$$J(n) = E[e^2(n)] \tag{2.49}$$

$$e(n) = y(n) - X_1^T(n)\overrightarrow{w}(n) \tag{2.50}$$

$$\overrightarrow{w}(n+1) = \overrightarrow{w}(n) + \mu X_1(n)e(n) \tag{2.51}$$

The update process is outlined in equation 2.51 it minimises the error at a controlled rate using a learning factor μ. The learning factor determines the speed of convergence, however a threshold level exist, α, where the learning rate must remain positive but below the threshold to avoid stability issues.

2.6.3 Recursive Least Squares Estimation

Recursive least squares estimation has many advantages over least mean squares estimation outlined in Section 2.6.2. Like the least squares estimation, it can extract the optimal set of coefficients, however this is achieved in an adaptive process. There are several variants of the recursive least squares approach. Each aims to achieve the same solution. For this analysis, the exponentially weighted variant will be presented [73]. The cost function which the algorithm aims to minimise is outlined in equation 2.52 where λ is the convergence control constant which should be a positive real number less than one.

$$J(t) = \sum_{t=1}^{n} \lambda^{n-t}(y(t) - \overrightarrow{w}^{T}(n)X^{T}(t))^{2} \tag{2.52}$$

The solution to the cost function can be determined by differentiating $J(n)$ with respect to the current solution $\overrightarrow{w}(n)$. The conventional recursive least squares adaptive algorithm is outlined in equations 2.53 - 2.57.

$$k(n) = \frac{\lambda^{-1}C^{-1}(n-1)X(n)}{1 + \lambda^{-1}X^{T}(n)C^{-1}(n-1)X(n)} \tag{2.53}$$

$$\varepsilon(n) = y(n) - \overrightarrow{w}^{T}(n-1)X^{T}(n) \tag{2.54}$$

$$\overrightarrow{w}(n) = \overrightarrow{w}(n) + k(n)\varepsilon^{*}(n) \tag{2.55}$$

$$C^{-1}(n) = \lambda^{-1}C^{-1}(n-1) - \lambda^{-1}k(n)X^{T}(n)C^{-1}(n-1) \tag{2.56}$$

$$e(n) = d(n) - \overrightarrow{w}^{T}(n-1)X^{T}(n) \tag{2.57}$$

2.6.4 Back propagation

In comparison to the time series behavioural models outlined, the neural network structure is very different. There are two main properties of the neural network and more specifically the multi-layer preceptron, which require that alternative training methods be employed. As the

name suggests the network generally has two or more layers, weights are applied between these layers and as such the weights are applied in a cascaded fashion. Therefore it is more difficult to determine the direct impact of any one weight. Secondly the activation function of the neuron is after the application of the weights to the input signals, further obscuring the impact of the weights.

In order to extract the update to the weights, the input output signal of each must first be determined. This is achieved through a method called back propagation. As the function of each neuron is known it is therefore possible to apply the inverse and determine the input signals to the neuron. In the same way the error at the output of the network can be back propagated to each neuron. The error is then used to derive an update for the neuron weights. An example of the MLP is outlined in Figure 2.38, the weights for each neuron are applied to the incoming signals $X_1 - X_n$ therefore in this example there are two layers of weights. The example will include a linear input layer, a non-linear hidden layer and a linear output layer. The non-linear hidden layer will use a sigmoidal activation function. The following equations will denote the input, hidden and output layers as I th, J th and K th layers respectively. The neuron outputs with be defined with O and the first order derivative will be denoted with δ The back propagation function minimises the squared error estimation of the output in equation 2.58.

$$E = \frac{1}{2}\sum(O_k - y)^2 \tag{2.58}$$

The following steps are used to compute the back propagation function. The derivatives are a function of the neuron activation function and as such have been derived for each layer.

1. Calculate the output for the current set of weights.

2. For each output node compute the first order derivative of the error (Linear activation function).

$$\delta_k = O_k(1 - O_k)(O_k - y) \tag{2.59}$$

3. For each hidden layer calculate the first derivative of the error into the output layer

(Sigmoid activation function).

$$\delta_j = O_j(1 - O_j) \sum_{k \in K} \delta_k w_{jk}(n) \tag{2.60}$$

4. Update the weights and bias weights using:

$$w(n+1) = w(n) - \eta \delta_{layer} O_{layer-1} \tag{2.61}$$

$$\theta(n+1) = \theta(n) - \eta \delta_{layer} \tag{2.62}$$

Where η is a learning rate similar to the least mean square function used to control the rate of convergence and avoid stability issues.

2.6.5 Genetic algorithms

For models which do not have an obvious convex solution a heuristic search method can be employed. One popular approach for these problems are genetic algorithms [86]. Genetic algorithms are based upon evolutionary theory, whereby repeated modifications of a population of individual solutions are carried out. At each step, the genetic algorithm selects individuals at random from the current population to be parents and uses them to produce the children for the next generation. Within the individual solution there are a number of coefficients called chromosomes. The algorithm will search through the population to find the individual solutions which provide an answer closest to the desired goal. By selecting a group of best solutions and cross sharing their individual chromosome's in multiple arrangements a new population can be formed. This new population is referred to as the preceding generation. In addition to this every population has a subset of individuals which are not formed from the previous generation, but have random chromosome's. This is referred to as mutation. This occurs within the population in order to diversify the chromosomes, preventing the algorithm from settling in a local minimum when a global minimum exists. The steps of the algorithm are summarised in a flow diagram presented in Figure 2.42.

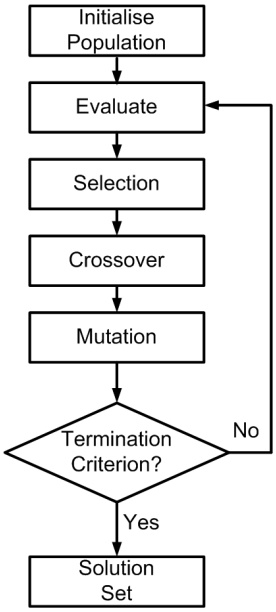


Figure 2.42: Genetic algorithm flow diagram.

2.7 Distortion Correction

Power amplifier design is a balance between three operating parameters, namely operational bandwidth, efficiency and linearity as outlined in Section 2.2. A compromise must be made in either amplifier design or operation to achieve reduced power consumption. System bandwidth is equally as important as efficiency, with the requirements modern communications signals and multi-carrier systems. Therefore the final parameter that can be compromised on is system linearity.

To illustrate this Figure 2.43 presents the characteristics of a simulated Class AB amplifier when input signal power is swept. The graph presents output signal power, system gain, drain and power added efficiency. The amplifier is driven deep into saturation, from this we can see the input power at which the amplifiers linear operation is effected, approximately 18 dBm input power. In a typical amplifier structure to achieve linear operation this would be the peak input power possible resulting in a peak drain efficiency of 40%. For an input signal greater than 18 dBm the output signal will experience gain compression, resulting in some form of non-linear output. For a modern wideband communications signal amplitude modulation will affect the average efficiency of the amplifier. Section 2.2.2.1 demonstrates that a typical modulated signal can expect between 8 - 10 dB peak to average power ratio. From this we can extrapolate

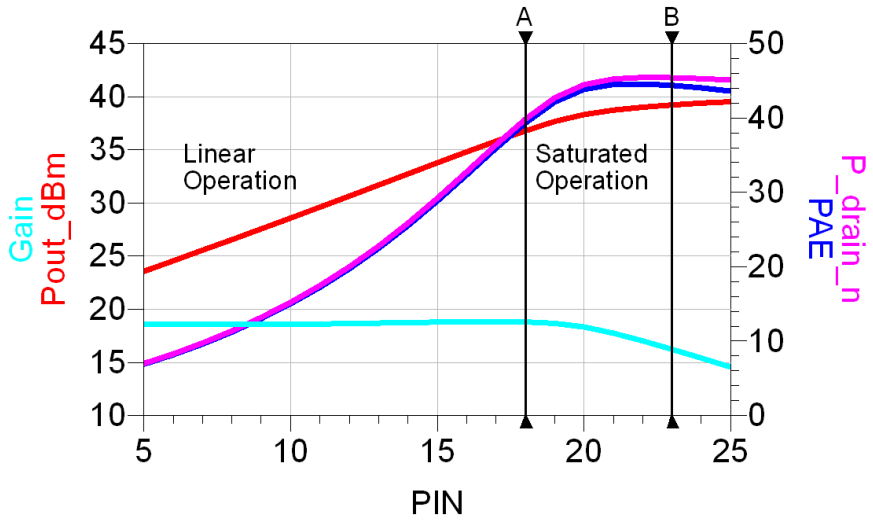


Figure 2.43: Characteristics of a simulated Class AB power amplifier. Point A is the peak input power for linear operation. Point B is the peak input power selected for saturated operation.

the system efficiency for a modulated signal as the efficiency point 8-10 dB from the peak operating power. Given a peak input power of 18 dBm and a signal PAPR of 8 dB the average input power is 10 dBm resulting in an average efficiency of 15%.

If however the amplifier is operated further into the non-linear region the system efficiency can be improved, this can be demonstrated using a thought example with the values presented in Figure 2.43. By operating the amplifier 3 dB into compression, a peak input power of 23 dBm is required, the average input power becomes 15 dBm resulting in an average power of 30%, effectively doubling the amplifiers efficiency. This section will demonstrate methods to negate or correct for the non-linearity that will be experienced by operating in such a high efficiency mode.

2.7.1 Crest factor reduction

The increase in spectral efficiency of modern communications schemes has lead directly to an increase in the peak to average power ratio (PAPR) of these signals. As demonstrated in Section 2.7 this results in greatly reduced efficiency or the generation or non-linear products in the output signal. One solution to this is to implement crest factor reduction, a method of pre-distorting the input signal to reduce the peak signal power relative to the average signal power. Several methods have been proposed for achieving crest factor reduction, from modification to the signal modulation process [87], a clipping and filtering process [88] or a signal cancellation

process [89]. The algorithm increases linear operation by avoiding the region of non-linearity near saturation.

While initially developed as a robust linearisation method in modern communications systems, CFR is more commonly used in conjunction with other linearisation techniques as a method to increase efficiency. It is commonly paired with digital pre-distortion, which can help reduce some of the non-linear out of band effects that CFR can introduce. This has enabled CFR to reduce the signal PAPR by as much as 6dB. The effect of CFR on signal magnitude is presented in Figure 2.44. The modification to the communications signal will involve altering the signal information to a certain extent. Each signal standard will have an EVM limit for the transmitter, this can limit the performance of the CFR algorithm and the robustness to noise of the signal.

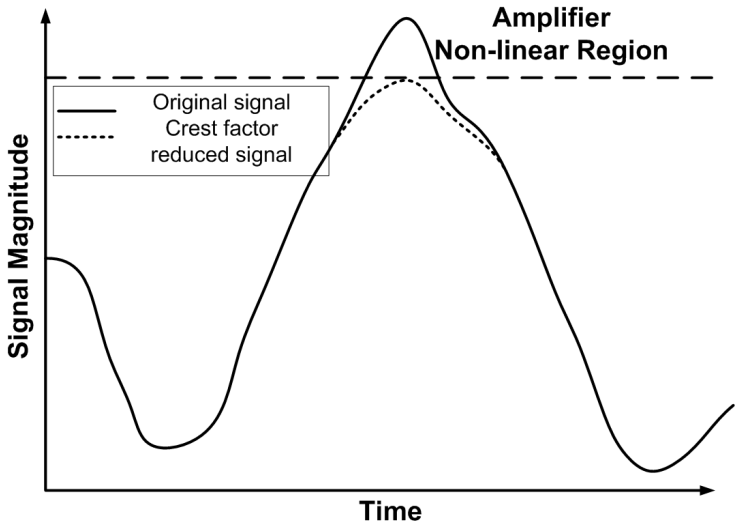


Figure 2.44: Effects of CFR on time domain signal magnitude.

2.7.2 Feed Froward Linearisation

Feed forward linearisation uses the non-linear output of the amplifier to determine the error generated for the main amplification process. This is determined by taking the output signal from the amplifier and subtracting it from the original input signal. The resulting error is then amplified using a lower power linear amplifier. The amplified error can then be subtracted from the output, cancelling the non-linear effects introduced by the main amplifier. This is a comprehensive method of reducing the error generated by the amplifier it takes into account

the changing amplifier characteristics. However there is additional complexity with this design as there is a second amplifier required in the design.

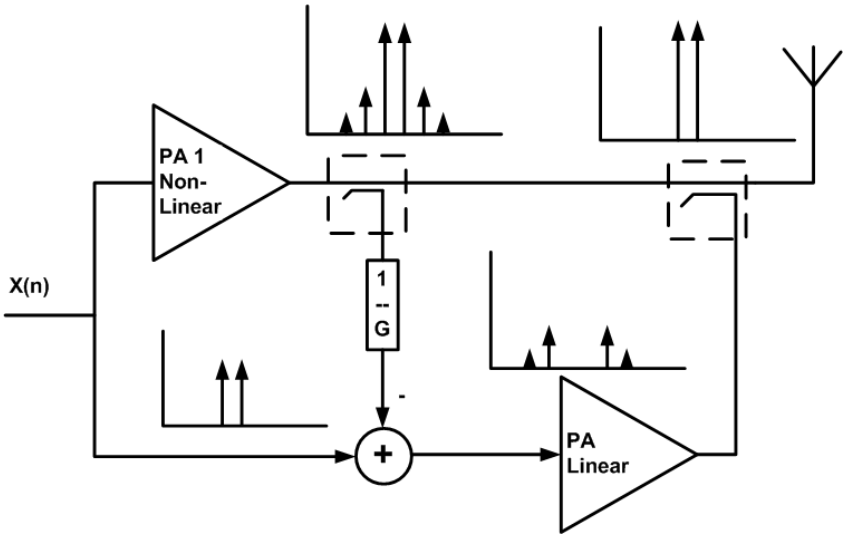


Figure 2.45: Overview of feed forward linearisation

There will also be design considerations for signal couplers that sample the main amplifier output and recombine the output of the error amplifier. These couplers will have to be designed for the specific operating frequency of the amplifier, reducing system flexibility. The system will also consume additional power with the presence of an additional amplifier in the system, the quantity of power consumed by the error amplifier depends on the magnitude of the error generated by the main power amplifier [90]. Using additional logic in the feed forward structure, it is possible to further reduce amplifier error. Techniques such as gain and phase control to allow the system to be more adaptable will be covered in further section on pre-distortion 2.7.4

2.7.3 Cartesian Feedback

Cartesian feedback linearisation is designed to get the output of the amplifier to track the input. This is achieved by comparing the down-converted previous output with the current input value. A loop filter is then used to track the difference between the current update and the previous output. The system then applies an update to the current output to correct for the effects of the previous output. As this happens in analogue or high speed digital circuitry the difference between the time samples will be very small so both should be affected by equivalent non-

linearities. The system offers dynamic error correction, however operation at high frequencies may cause instability in either the feedback path or the loop filter or both. For this reason analogue implementations may be difficult for modern communications schemes, however digital implementation will reduce these effect at the cost of additional hardware (high speed ADC's and DAC's) [91]

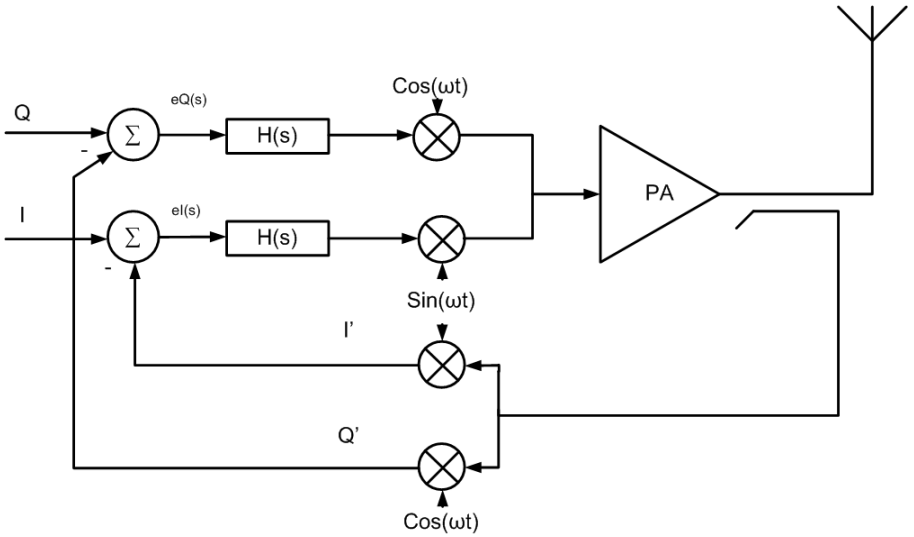


Figure 2.46: Overview of cartesian feedback linearisation

2.7.4 Pre-distortion

Pre-distortion linearisation uses an inverse model of the amplifier circuit, when the inverse model and the amplifier are combined the resulting system output is linearised. Pre-distortion can be implemented at various stages in the signal chain, this results in a distinct divide in pre-distortion methods between analogue and digital implementations. In both cases the objective is the same, an inverse function of the non-linear process must be applied to the input signal prior to the non-linear system component. Both digital and analogue implementations have advantages and disadvantages:

Analogue pre-distortion offers a low power, ultra wide band solution typically used in optoelectronic or satellite links. The solution is bespoke for each system resulting in a costly and inflexible solution, not very suitable for cellular networks.

Digital pre-distortion offers a relatively cheap and flexible method of linearisation. A balance of efficiency increase verses higher implementation cost (in both hardware and power

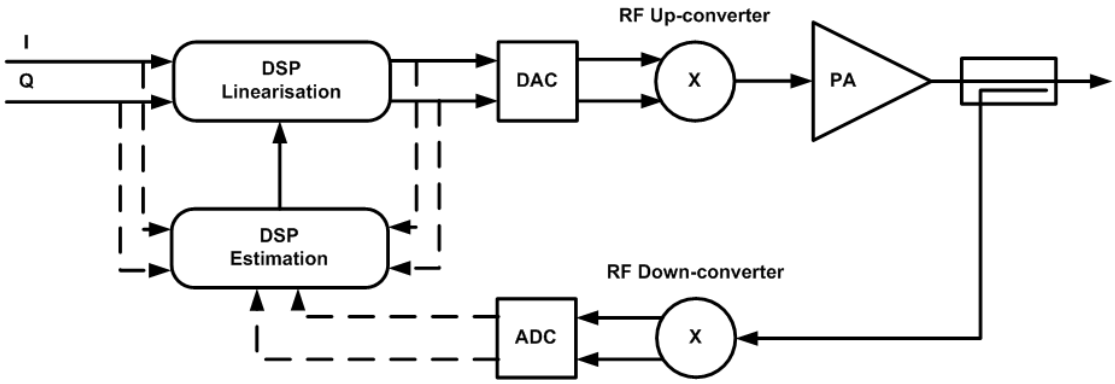


Figure 2.47: Overview of digital system linearisation.

budget) prevents it from being implemented in low power systems. The operational bandwidth is limited to the operational frequency of the DSP. An example of digital pre-distortion is presented in Figure 2.47.

Due to cost and flexibility digital pre-distortion is the commonly chosen method of linearisation for modern communications system base station amplifiers. It will be explored further in this section and indeed in the coming chapters as it is evaluated as a method for enabling the operation of outphasing amplifiers in cellular communications systems.

A popular method of implementing digital pre-distortion is to use an inverse non-linear function on the input of the amplifier. The non-linear function outlined in the behavioural modelling in Section 2.5 are commonly applied as linearisation algorithms. As with behavioural modelling the complexity of the non-linear function will depend on the complexity of the non-linear system that is being linearised. For many high power and efficient amplifier designs such as Class E, F, Doherty, Envelope tracking ect. a non-linear function capable of non-linear memory correction is required. As such the Volterra series and generalised memory polynomial time series demonstrate excellent performance [75] [92].

In comparison to behavioural modelling, digital pre-distortion is performed in real time on DSP or digital logic (FPGA) systems. Therefore the most efficient function which can achieve the required performance is chosen. In addition all calculations are performed in fixed point notation. Extraction of linearisation function weights should be carried out in fixed point to achieve the maximum linearisation performance [93].

There are some downsides to this method. Digital pre-distortion requires an RF and digital down conversion stage to accompany the forward path correction, placing additional cost on

system implementation. Additionally the non-linear signal and the linearisation signal have an increased signal bandwidth requirement. This is dependent on the order of non-linearity however practical systems deal with up to fifth order or five times the original signal bandwidth. The bandwidth expansion requires high speed digital signal programming for the forward path linearisation logic. Wider bandwidth multi-channel 4G communications are becoming increasingly difficult to accommodate [94].

2.7.5 Overview of Distortion Correction Techniques

This section provides a brief overview of some of the more popular linearisation techniques applied to base-station power amplification systems. Currently the most popular method is digital pre-distortion, in comparison to other methods the limited amount of additional hardware and the flexibility of the method offer benefits that far out weigh the negatives. However as outlined above the algorithm that is used to linearise the amplifier is dependent on the amplifier topology and available resources. In modern communications systems digital pre-distortion is used in conjunction with CFR to dramatically improve the amplifier's efficiency [95]. This combination is becoming more popular as the signal standards increase the margin between peak power and average power.

Digital pre-distortion is currently a popular research topic as more unconventional amplifier topologies are being developed to further increase efficiency. The Doherty [58], envelope tracking [96] and outphasing [2] power amplifiers require digital pre-distortion to achieve a linear output.

2.8 Conclusion

In summary RF power amplifiers can achieve efficient conversion of DC to RF power however at the cost of complexity or linearity. Section 2.2 outlines the compromise that amplifier design must make with regards efficiency and linearity. The individual classes of operation can compliment each other in the amplifier topologies, achieving linearity greater than the sum of their parts. While theoretical maximum efficiency demonstrates the abilities of each class of operation, as a figure of merit it does not give the full picture. Efficiency of the amplifier at power back-off is a more accurate representation of amplifier efficiency during operation.

Therefore analysis of PA topologies which have the potential of extending higher operating efficiencies into power back-off are more interesting.

The Doherty implementation demonstrates this using load modulation to increase efficiency in power back-off substantially, as such its popularity has greatly increased in modern communications systems. However the use of linear class of amplifiers does somewhat limit the maximum theoretical efficiency and therefore researchers are actively exploring switching architectures. Class-S power amplifiers potentially demonstrate the ability to achieve a frequency flexible, efficient and linear power amplifier architecture however advancements in both pulse signal generation and transistor technology are required in order to unlock its potential, further information including work carried out at Maynooth university is available in Appendix B. Alternatives to the Class-S amplifier are outphasing power amplifiers and envelope tracking amplifiers, using a combination of two or more switching amplifiers to amplify a complex modulated signal using load modulation. In comparison to the Class-S topology the technology required is currently available. Envelope tracking and outphasing topologies both offer the potential for very high efficiencies at back-off power. Both require additional hardware and a minimum of two active amplification stages. With the improvements of both signal processing and transistor technologies both amplifiers have become more realisable in recent years. However there is a fundamental difference in the amplifier topologies, the outphasing amplifier is a complementary arrangement with both amplifier stages directly contributing to the systems output power. The efficiency of the outphasing amplifier is dependent on the maximum efficiency of the amplification stages. In the envelope tracking amplifier the amplification stages are cascaded, the RF amplifier modulates the signal supplied from the baseband drain supply. Therefore the efficiency is dependant on the efficiency of both stages with losses in each. In theory the outphasing amplifier offers the potential for higher absolute efficiency, this is one reason that the work that will be presented in the future chapters will concentrate on the outphasing amplifier.

Advancements in signal generation and transistor technology have enabled efficient operation of the outphasing topology for communications signals however linear operation with wide band communication signals still pose a challenge. Evaluating the output of the topologies power combiner and the individual amplifier stages using the non-linear function outlined in this chapter will provide an improved understanding of the outphasing topology.

To characterise these non-linearities the Volterra series is often applied. The Volterra model consisting of every combination of non-linear orders and memory taps up to the defined limits, it provides the best possible characterising of the non-ideal effects which have yet to be fully defined.

Artificial neural networks, the universal approximator, will also be evaluated for non-ideal effects which are not directly related to polynomial non-linearity. With further development the optimum behavioural function will be applied as a linearisation function using digital pre-distortion, a flexible and rapid linearisation method is perfect for evaluating and optimising correction functions.

In short the technology and techniques outlined in this chapter will form the basis for the work carried out in the subsequent chapters, in which novel characterisation and correction functions are presented as well as alternative signal processing techniques. The following chapter will outline the investigation into outphasing amplifiers and sources of non-linear operation.

CHAPTER 3

Outphasing Power Amplifiers

The outphasing power amplifier was first introduced by Henri Chireix in 1935 [60] as a method to improve both efficiency and linearity in amplitude modulation transmitters. In 1974 the concept was later revised by Cox with the introduction of LINC (Linear amplification using Non-linear Components)[61]. The work by Cox demonstrated how highly non-linear yet efficient devices could be arranged to provide a linear output. The concept of the outphasing amplifier is illustrated in Figure 3.1.

The principle of operation is relatively simple, the amplitude modulated signals is converted to a pair of phase modulated signals with constant amplitude. These signals are then amplified

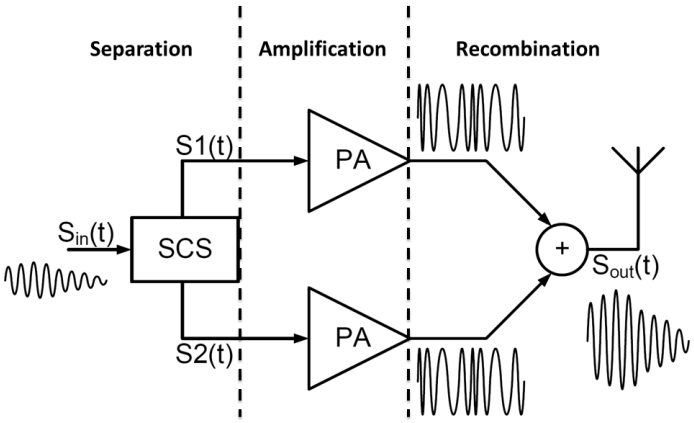


Figure 3.1: Overview of the Outphasing amplifier

by identical PA's. The constant envelope amplified signals are then re-combined in the power combiner stage, resulting in an amplified version of the amplitude modulated input signal. Efficient operation is achieved as both amplifiers are operating with constant output power close to or at peak efficiency of the amplification stages, reducing the losses in the transistor. Furthermore non-linear and switch-mode classes of amplifier can be used, providing higher system efficiency. The key to efficient operation is the signal component separator which translates the amplitude to phase modulation allowing the PA's to operate at a constant output amplitude. Operating the amplifiers at a constant amplitude negates their non-linear input-output power characteristics, this enables the system to employ highly efficient PA architectures while maintaining a linear output, provided the input signal component separator and the output power combiner are also linear.

3.1 Basic Operation of an Outphasing PA

The outphasing power amplifier consists of three distinct sections, the signal component separator (SCS), the amplification stage and the output power combiner. The topology achieves efficient linear operation by generating constant envelope operation of high efficiency amplifications stages. Figure 3.2 demonstrates how the constant envelope signals recombine to form an amplitude and phase modulated output signal. The output power combiner design will determine the overall efficiency of the amplifier. The following sections will provide an overview of each of the signal conversion stages in the outphasing power amplifier.

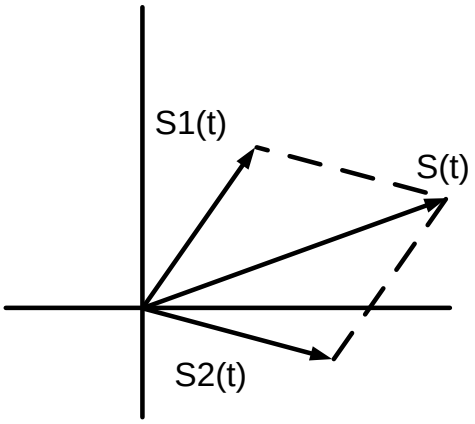


Figure 3.2: Signal recombination of LINC and Outphasing topologies.

3.1.1 Separation

The signal component separation involves de-constructing an amplitude or quadrature modulated signal, transforming it to a pair of complementary constant envelope signals with the amplitude information encoded as a phase difference.

$$S(t) = A(t)cos[\omega t + \phi(t)] \quad 0 \leq A(t) \leq A_{max} \tag{3.1}$$

The equation 3.1 outlines the composition of a quadrature modulated signal where $A(t)$ is the amplitude modulated component of the signal and $\phi(t)$ is the phase modulated component of the signal. The input signal processed by the SCS now consists of two constant amplitude signals on to which an additional phase modulation component $\rho(t)$ is used to encode the amplitude $A(t)$.

$$S_1(t) = \frac{A_{max}}{2} exp[j\omega t + \phi(t) + \rho(t)] \tag{3.2}$$

$$S_2(t) = \frac{A_{max}}{2} exp[j\omega t + \phi(t) - \rho(t)] \tag{3.3}$$

The outphasing angle $\rho(t)$ is a function of the recombining circuit, for ideal outphasing recombination the SCS function is denoted as

$$\rho(t) = arc - sine(\frac{A(t)}{A_{max}}) \quad 0 \leq \rho(t) \leq \frac{\pi}{2} \tag{3.4}$$

In a practical implementation the SCS will use an amplitude to phase conversion function capable of describing the output power combiners phasing function. Many alternative functions have been proposed including, arc-sine, arc-cosine, stretched arc-cosine and fully custom look up tables. The stretched arc-cosine function is a modification of the trigonometric arc-cosine function, however where a typical arc-cosine function has a maximum angle of $\frac{\pi}{2}$, the modified arc-cosine function has a maximum angle of $\frac{\pi}{2}A$, where A is a positive real number. Research has been carried out on dedicated SCS circuitry [97], however it is also possible to implement a custom functions on digital logic or DSP. This allows for integration into existing digital signal processing techniques [98]. Encoding band-limited, amplitude and phase information into a pair of constant envelope, phase only modulated signals alters the spectral characteristics of

the information. A comparison of outphasing techniques are discussed in [99].

The authors also presented a novel method of increasing the efficiency of the outphasing load modulation technique through mixed mode linear operation. An additional consequence of the mixed mode operation is a reduction in the bandwidth expansion experienced by the signal component separation process. The authors demonstrate that during typical outphasing operation the bandwidth expansion experienced is 10-12 times the original signal bandwidth. Through mixed mode operation this can be reduced to a factor of 8 times. The principle of operation of the outphasing system requires symmetry in the signal generation and amplification paths to achieve linear operation. For modern wideband communications systems bandwidth expansion of up to 12 times will require wide band high precision signal chain.

3.1.2 Amplification

Constant envelope operation negates the non-linear AM effects of saturated or switch mode amplifier operation. The class of amplifier chosen will depend on the desired modes of operation, however high efficiency implementations have been demonstrated using saturated Class B and switch mode Class D, E and F [99, 100, 29, 101]. Trade-off's between output power of the choices must be made such as output power, frequency of operation and method of implementation. For optimum implementation the choice of amplifier should also consider the variance between amplifier characteristics due to manufacturing tolerances. Any imbalance introduced at the amplification stage may hinder linear operation.

3.1.3 Recombination

The power combiner is a fundamental component in the outphasing technology. The efficiency gains from operating the amplifiers at their most efficient levels must be converted into the load with minimal losses. For linear operation we ideally want to isolate the amplification stages from one and other. However for most efficient operation non-isolating power combiners are most advantageous. This is discussed further in the following sections.

3.1.3.1 Isolating power combiner

The Wilkinson power combiner proposed in [102] offers high output linearity due to the isolation between input ports. The Wilkinson combiner shown in Figure 3.3 achieves isolation

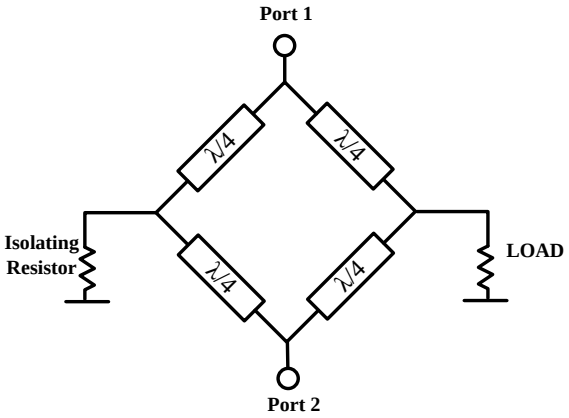


Figure 3.3: Wilkinson Combiner

through the use of a balance resistor between the input ports, the output port is the sum of the input signals, while the difference is consumed by the isolation resistor. The combiner is at maximum efficiency when both input signals are in-phase. However as the signal deviates away from this efficiency drops as the isolating resistor begins to consume power. From this characteristic of the combiner we can determine the system to be lossy, impacts the back off efficiency of the outphasing amplifier.

Modifications to the architecture have been proposed in order to reduce the impact on the efficiency. In [103] a multilevel LINC amplifier is proposed. This method is a hybrid design between envelope elimination- restoration and outphasing topologies. Coarse amplitude modulation is applied to the drain of each of the amplifiers in the topologies while finer amplitude modulation steps are achieved by changes in the outphasing angle. This operation reduces the efficiency losses during back off when compared with traditional Wilkinson outphasing amplifiers, yet maintains the isolation required for linear operation. Total system efficiency will be dependent on the combined efficiency function for the envelope modulator circuit and the amplification stages.

An alternative method was proposed in [104] where a tuned rectification stage is used to recover the power dissipated in the isolating resistor and then convert it to DC power, feeding back into the amplifier's drain supply, this reduces the power lost during back off operation. However the efficiency of the rectifier stage will greatly impact any possible efficiency improvements. As the power rectification circuit will experience an impedance change when the input current changes, this will in turn affect the outphasing angle of the

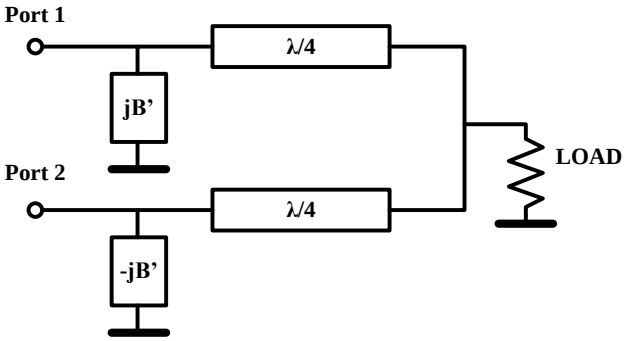


Figure 3.4: Chireix Combiner

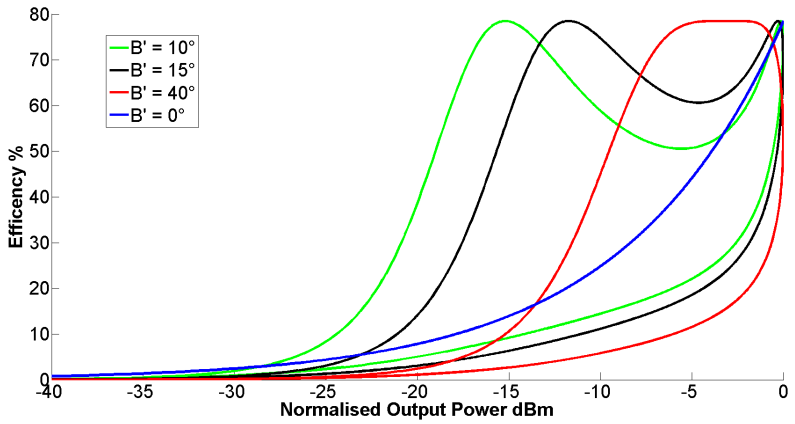


Figure 3.5: Chireix Combiner Power Efficiency With Amplifier

combiner, directly affecting the linear operation of the amplifier.

3.1.3.2 Non-isolating power combiner

The Chiriex combiner consists of a pair of quarter wavelength transmission lines in combination with shunt reactances as seen in Figure 3.4. A simple matched Chireix combiner without the shunt reactances has equivalent efficiency to that of an isolated combiner. The cause of the efficiency loss is the susceptance that the amplifier experiences as the outphasing angle changes. By equating the load compensation reactances to cancel the susceptance that the amplifier experiences at an outphasing angle the efficiency loss can be cancelled out. This results in a secondary maximum efficiency peak. Generally the amplifier is designed in such a way that the secondary peak is approximately the peak to average power value of the desired modulated signal.

3.1.3.3 Theoretical Efficiency

A brief analytical analysis of the outphasing amplifier structure can lead to a simplified set of equations for maximum theoretical efficiency. The Wilkinson power combiner and the Cheriex power combiner without load compensation have similar operation. Therefore it is possible to analyse an ideal outphasing system and derive a single equation for both systems. In [105] the author presents a detailed analysis of the combiner operation. To calculate the efficiency of the combiner, it is assumed that the inputs to the combiner are ideal voltage sources $S_1(\Theta)$ and $S_2(-\Theta)$ which provide a constant voltage signal with a phase modulation of Θ. The output voltage across the load is $V_o(\Theta)$ and the current through the load is $I_o(\Theta)$.

$$S_1(\Theta) = e^{j\Theta}; S_2(\Theta) = e^{-j\Theta} \tag{3.5}$$

$$i_{out}(\Theta) = \frac{S_1(\Theta) + S_2(\Theta)}{Z_L} = \frac{e^{j\Theta}e^{j\Theta} + e^{-j\Theta}}{Z_L} = \frac{2cos\Theta}{Z_L} \tag{3.6}$$

A simpler method of calculating the impedance seen by each voltage source is to analyse the Norton equivalent circuit of the combiner. This enables the calculation of the circuit admittance which can later be inverted.

$$Y_{S_1} = \frac{i_{out}}{S_1} = \frac{2cos\Theta}{Z_L e^{j\Theta}} \tag{3.7}$$

$$Y_{S_2} = \frac{i_{out}}{S_2} = \frac{2cos\Theta}{Z_L e^{-j\Theta}} \tag{3.8}$$

Therefore the impedances that equate to Y_{S_1} and Y_{S_2} are,

$$Z_{S_1} = \frac{2cos\Theta}{Z_L e^{j\Theta}} = \frac{Z_L}{2}(1 + jtan\Theta) \tag{3.9}$$

$$Z_{S_1} = \frac{2cos\Theta}{Z_L e^{-j\Theta}} = \frac{Z_L}{2}(1 - jtan\Theta) \tag{3.10}$$

By adding load compensation to the circuit in the form of a negative supseptance to S_1 and

S_2 the load admittance changes to,

$$Y_{S_1} = \frac{2cos\Theta}{Z_L e^{j\Theta}} - jB \tag{3.11}$$

$$Y_{S_2} = \frac{2cos\Theta}{Z_L e^{-j\Theta}} - jB \tag{3.12}$$

where the compensation supseptance B is calculated as $sin2\Theta/Z_L$. The efficiency is then derived as

$$\eta(\Theta) = \frac{Re[Z_{S_1}(B,\Theta)]}{\| Z_{S_1}(B,\Theta) \|} \tag{3.13}$$

$$Z_{S_1} = \frac{1}{Y_{S_1}} = \frac{cos\Theta + jsin\Theta}{\left[\frac{2cos\Theta}{Z_L} - Bsin\Theta\right] + jBcos\Theta} \tag{3.14}$$

Figure 3.5 demonstrates the theoretical efficiency curves that can be achieved by altering the reactances of the load compensation network. A *B'* of zero degrees is equivalent to an unmatched Chireix combiner or Wilkinson combiner. The calculations assume that the signals are provided from an ideal saturated Class-B amplifier and therefore the peak efficiency is 78.5%. The increased efficiency in back-off make the Cheriex outphasing power amplifier an attractive option, no additional hardware or circuitry is required to extract the efficiency from the saturated amplifiers. This comes at a cost, the additional load matching reactances result in reflections between the amplifier and the combiner, these result in a non-linear operation. These effects along with additional sources of non-linearity will be investigated in Section 3.3.

3.2 Different Modes of Outphasing PA Operation

In addition to the power combiner circuits outlined in Section 3.1.3, the outphasing amplifier can be configured using the classes of amplification outlined in Sections 2.2.4 and 2.2.5. Non-linear analysis will be carried out on the saturated linear outphasing amplifier implementation and the digital switch mode outphasing amplifier, as they are the two most common forms of efficient outphasing amplifier implementations. For completeness alternative high efficiency implementations will also be introduced, these hybrid outphasing amplifiers will suffer from

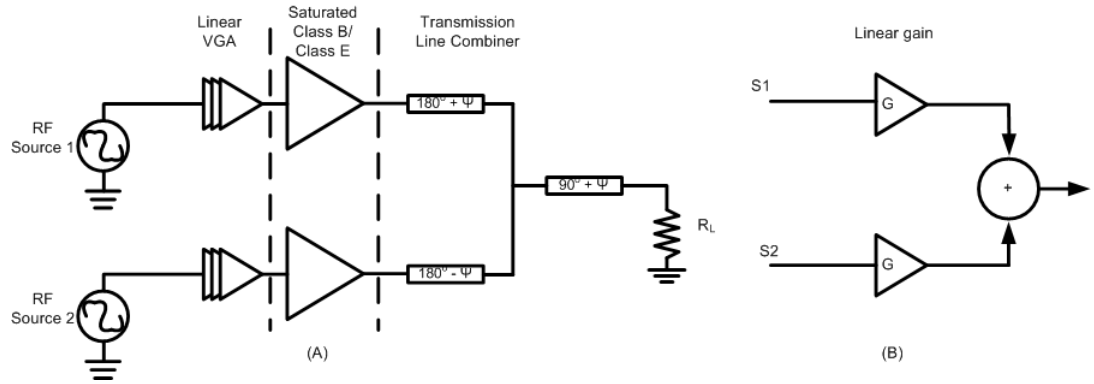


Figure 3.6: Saturated linear amplifier outphasing system, (A) high level circuit diagram, (B) low level model used for simple linearity analysis.

the same non-linear effects. Research into outphasing amplifiers with additional modulation functions has yielded additional efficiency at the cost of increased system complexity [106, 100, 29, 99, 107, 108].

3.2.1 Saturated Outphasing Amplifier

The outphasing amplifier topology negates the amplitude non-linearities associated with saturated amplifier operation. Therefore Class B and C amplifiers can be operated in saturation to achieve maximum system efficiency. This implementation is chosen due to the fact that existing linear mode amplifier designs could be used. These designs have advantages at higher output powers, where parasitics associated with larger transistors can impact efficient switch-mode operation. In [106] the author presents the efficiency of a saturated amplifier implementation. The theoretical maximum efficiency of the system is equal to the maximum efficiency of the chosen class of amplifier, in the case of Class B amplifier that is 78.5%, however higher efficiencies have been demonstrated for Class E implementations [109]. Depending on the frequency of operation the combiner is typically a lumped element design for lower frequency or transmission line design for higher frequency, as compromise between size, accuracy and parasitic effects are made.

3.2.2 Digital Outphasing Amplifier

Digital outphasing amplification is implemented with switch mode classes of amplifiers such as Class D [100], E [29], and F [101] to achieve increased system efficiency. As outlined in

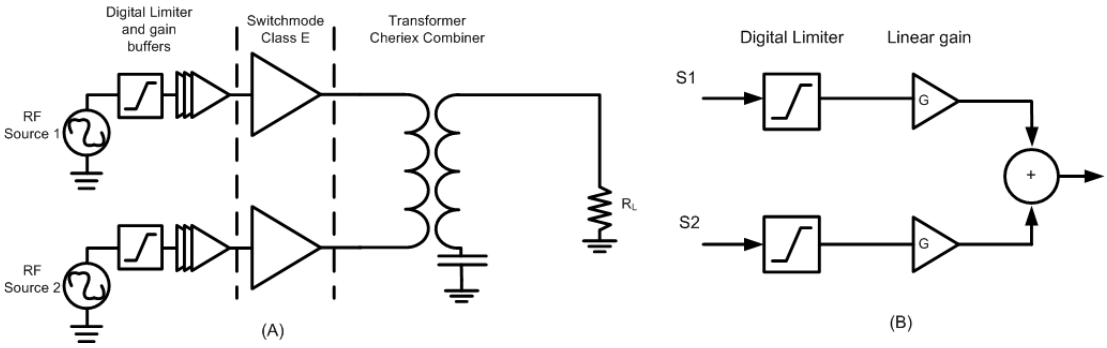


Figure 3.7: Digital outphasing system, (A) high level circuit diagram, (B) low level model used for simple linearity analysis.

Section 2.2.5 switch mode operation offers increased efficiency, and is ideally suited to constant amplitude operation. Switch mode amplifiers have become increasingly popular in part due to improvements in transistor technologies and also due to improved analytical design and implementation techniques. In particular the widespread availability of Gallium Nitride (GaN) transistors with reduced output parasitics and increasing the switching frequency has enabled development of Class D, E and F amplifiers at cellular frequencies (2 GHz +). In Figure 3.7 a digital outphasing amplifier is outlined showing a transformer based combiner as presented in [29]. For higher operating frequencies the transformer based power combiner has demonstrated wider operating frequency band when compared with transmission line implementations, while maintaining a compact and efficient implementation.

3.2.3 Linear back-off outphasing amplifier

Linear back-off or mixed-mode outphasing uses the topology of the saturated linear outphasing system outlined in Figure 3.6. Signal separation and recombination are carried out in the same method. However as the name suggests at a chosen threshold the signal modulation is modified and the outphasing signal amplitude is also modulated. The topology has two major benefits when compared with traditional outphasing, it offers increased efficiency in the amplifier back off power region and additional reduction of the non-linear effects associated with achieving a high dynamic range. An additional benefit is the reduction in bandwidth expansion which occurs during the signal component separation process. In [99] the authors presented a reduction in bandwidth from 10 times the original signal bandwidth to 8 times. The efficiency of the system is presented in equation 3.15, where the outphasing efficiency is

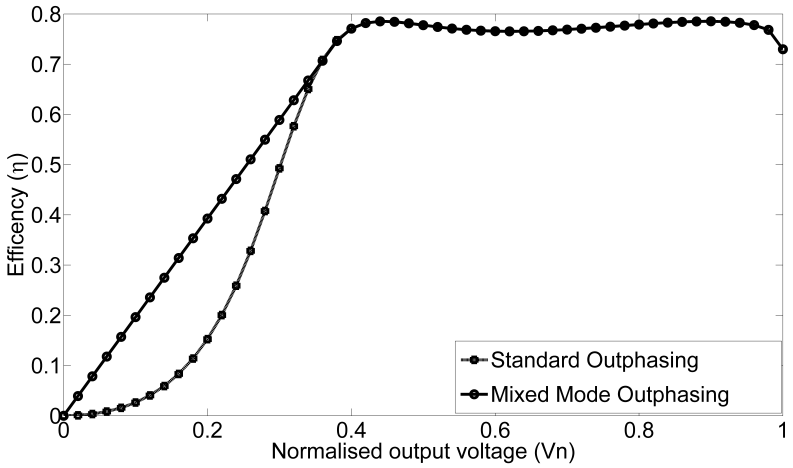


Figure 3.8: Theoretical efficiency of a saturated linear back-off or mixed-mode outphasing amplifier vs. a saturated Class B pure outphasing amplifier

calculated using the theory presented in Section 3.1. The efficiency of the saturated Class B amplifier is linear with respect to output voltage and therefore can be described as $\eta = V_n * \eta_{max}$ where the maximum theoretical efficiency of a Class B amplifier is 78.5% as shown in Section 2.2.4.2.

$$H = \begin{cases} \eta = \eta_{classB}, V_n < V_{th} \\ \eta = \eta_{outphasing}, V_n > V_{th} \end{cases} \tag{3.15}$$

This technique is further explored in [110] the authors characterise the behaviour of the amplifier to outphasing at various input power levels. The results extracted additional efficiency from the amplifier through optimised input amplitude and outphasing angle for a given output power. There are some drawbacks to the linear back off topology. A linear driver stage is required to provide input power to the amplifier, reducing overall system efficiency. While negating the non-linear effects at lower output powers the amplifier's amplitude modulation results in large memory effects as it enters and exits saturated operation. These can prove to be more complex than with traditional saturated amplifier operation as the resulting memory and non-linear effects are not equal in each path and are additive.

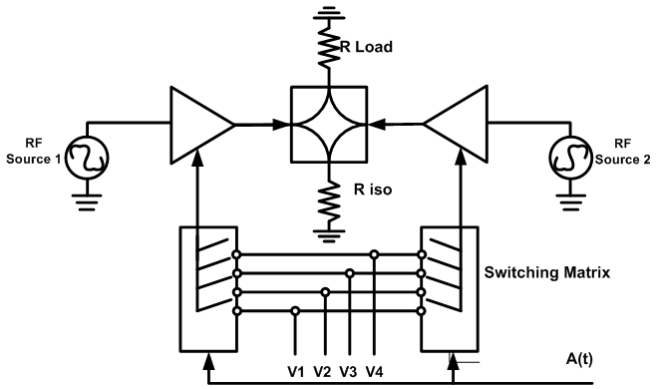


Figure 3.9: Asymmetric multi-level outphasing amplifier

3.2.4 Asymmetric Multi-level Outphasing Amplifier

LINC power amplifiers enable the linear amplification of amplitude modulation signals with non-linear components, namely power amplifiers. This is achieved with an isolating power combiner demonstrated in Section 3.3. The benefit of the LINC system is increased linearity at the cost of sub-optimal efficiency, the system achieves a similar efficiency curve to that of a saturated Class B amplifier. In [107] the authors present a hybrid envelope tracking / LINC amplifier. The envelope tracking is achieved through a multi-level switching matrix which controls the DC power supplied to the amplifiers drain. The coarse switching on its own results in large amplitude errors and limited dynamic range. However when combined with an outphasing action the system is capable of achieving far higher levels of accuracy. The modulation of the supply voltage reduces the power sent to the isolating resistor and therefore increases efficiency. The system topology is presented in Figure 3.9 in this example the supply voltage ranges in values $(1-4) * A_{max}(t)$ and the switching matrix chooses a value based upon the signal amplitude $A(t)$. This method has demonstrated linear performance for a wireless LAN signal with efficiencies up to 35.5%. The output power and efficiency is determined by the DC/DC converter, as such the topology experiences some of the down sides associated with envelope tracking amplification outlined in Section 2.3.0.2.

3.2.5 Outphasing Amplifier with RF to DC Power Recovery

RF to DC power recovery or power recycling was proposed in [108] for LINC power amplifier's which use the Wilkinson power combiner. The technique aims to recover the power which is

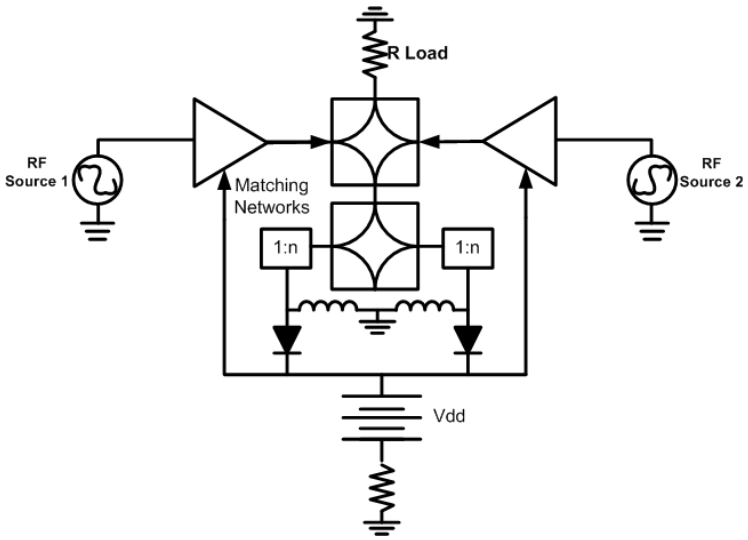


Figure 3.10: Outphasing amplifier with RF to DC power recovery.

normally dissipated in the isolating resistor. This is achieved with an RF to DC converter which injects the recovered power back into the amplifier supply rail. Additional isolation can be added between the non-outphasing output and the RF to DC converter at the expense of a loss of efficiency. The structure can cause additional distortion as the energy recovery system will cause some variance in its impedance causing a phase shift in the combiner outputs. An overview of the system is presented in Figure 3.10. In [104] a prototype demonstrated the principle of operation, the system was capable of 42% efficiency for a 50 kHz QAM signal.

3.3 Visualizing and Quantifying non-ideal Outphasing Behaviour

There are many methods of implementing the outphasing architecture as demonstrated in Section 3.2. While each introduces additional signal modulation or circuity to enhance efficiency, the fundamental operation of the amplifier does not change. To achieve a linear amplified output the input signal must be separated, amplified and combined in a linear, continuous function, however this is often not the case. By examining the output of an outphasing amplifier in different signal domains, the non-ideal effects can be visualised. Using this method the causes of non-ideal effects will be classified into sub-sections.

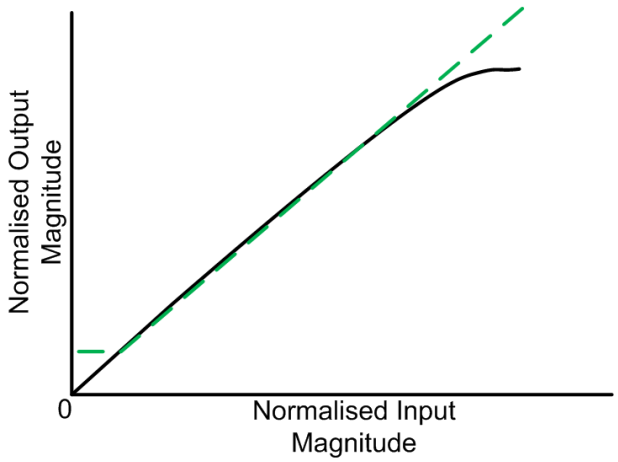


Figure 3.11: The amplitude effects of non-ideal behaviour in outphasing power amplifiers. AMAM a non-linear relationship between input and output amplitude is presented in **Black**. The discontinuous amplitude function in **Green** is a result of an inability to achieve sufficient dynamic range.

3.3.1 AMAM AMPM Non-linearity of an Outphasing PA

Like traditional amplifier structures the outphasing power amplifier will experience some AMAM AMPM non-linear behaviour. As described in Section 2.4.3 AMAM and AMPM are amplitude dependent non-linear functions, in the majority of amplifier structures these functions are continuous and for the most part this is similar in the outphasing amplifier. However in some cases the non-linear function at lower output power can be discontinuous. There are a range of factors which will impact upon these functions including outphasing system design and operation. Figure 3.11 demonstrates the possible non-linear functions in the outphasing amplifier AMAM response.

3.3.2 Frequency Domain Effects

The frequency domain is often the most informative when inspecting the performance of any amplifier. In the case of the outphasing power amplifier, several overlapping effects can contribute to either a raised out-of-band noise floor or an increased ACPR level. Figure 3.12 highlights three of the most common and distinctive effects.

An increase in side-band power points to a non-linear function within the amplified signal. This would typically be continuous in nature and occur at higher output power. When visualising the output signal in the frequency domain the intermodulation produced will

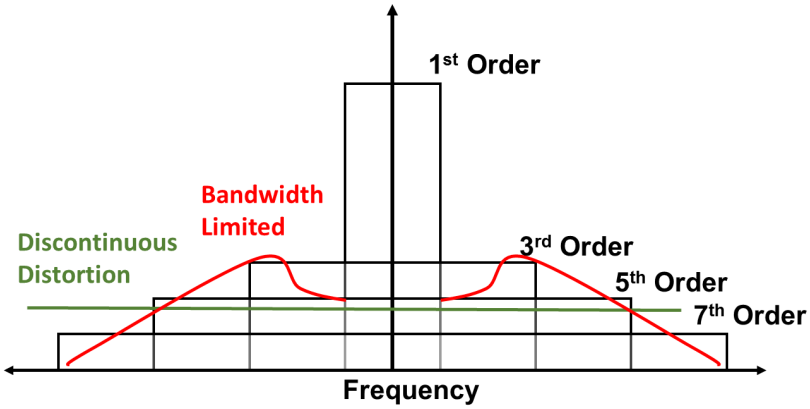


Figure 3.12: The frequency effects of non-ideal behaviour in outphasing power amplifiers. Intermodulation in **Black** is the result of amplitude dependent non-linear effects. The discontinuous in **Green** is a train of infinite harmonics which result from discontinuous effects. The bandwidth limitations in **Red** is a result of an insufficient frequency passband available within the RF components.

typically appear above other contributions to out-of-band noise.

Raised out-of-band noise several channels from the desired output signal indicates a limitation on outphasing signal bandwidth, this can be attributed to any component in the outphasing signal up to and including the output combiner. The increased bandwidth requirement can often be too much for general RF components and amplifier design techniques. If the outphasing signal exceeds the operational bandwidth of the system an out-of-band response as shown in red will occur.

The green infinitely flat out-of-band noise floor is typically the lowest of the three in terms of the maximum signal amplitude, however it is the hardest to eliminate. Resulting from a discontinuity in the time domain signal it will result in an infinite number of harmonics with equal power. In reality the noise will be the shape of the pass band of the output combiner. The only method of reducing this noise floor is to remove the discontinuities. The discontinuous behaviour is further examined in the next section using time domain signals.

3.3.3 Time Domain Effects

Dynamic range is defined as the ratio between the largest and the smallest possible output signal power. Within the outphasing topology there are many properties which can limit this value, effects from the signal generation hardware and the amplifier circuity must be taken into

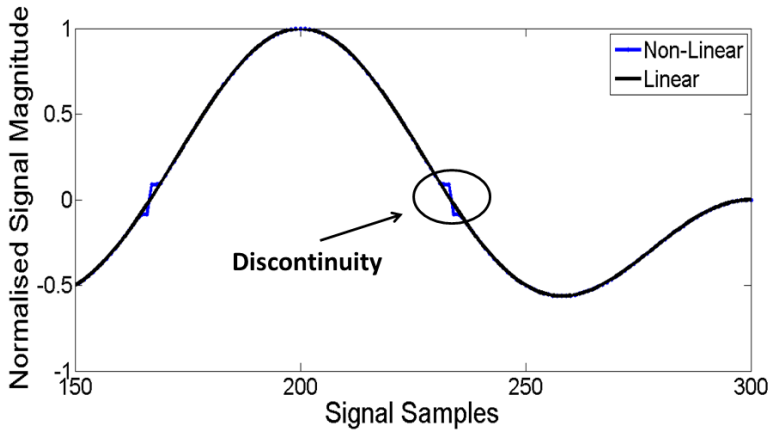


Figure 3.13: The Effects of limited dynamic range on time domain signal. The in-phase component of the two tone signal, hard limiting causes a discontinuous signal component at low output power.

account. This results in non-linear operation as the range of outputs from the amplifier is not capable of representing the modulated signal, particularly at low output powers. The effect of this is visible as wideband noise in the frequency domain, if the noise is large enough the amplifier will not be capable of meeting the spectral requirements for the signal standard.

A hard limit is applied to a two tone signal using the function described in equation 3.16 where $A(t)$ is the signal magnitude and M is the hard limit. In this example M is chosen to be 0.05 of the maximum signal magnitude. The effect of the limited dynamic range is an infinite number of low power harmonics. Figure 3.13 demonstrates the effect of limited dynamic range on the time domain signal. Examining the in-phase component of the signal, the source of the infinite number of harmonics is apparent. A discontinuity occurs as the original "linear" signal has a rapid phase change close to zero output power. While the step function is an unrealistic function in the physical amplifier system, a band limited version will be generated, resulting in unwanted, wideband noise.

$$\hat{A} = \begin{cases} A(t) \leqslant M, \hat{A} = M \\ A(t) > M, \hat{A} = A(t) \end{cases} \tag{3.16}$$

3.4 Sources of Non-ideal behaviour

Having highlighted the effects that can be expected from non-ideal behaviour of the outphasing power amplifier, this section will outline the sources of these non-ideal effects and quantify the non-linear impact of each. By analysing the individual components of the outphasing system the main factors contributing to the the non-linear effects outlined in Section 3.3 will be outlined.

3.4.1 Signal Component Separator and Combiner Mismatch

The theoretical direct analysis thus far has been carried out assuming the combiner is ideal and therefore the signal component separator function is also described by an ideal trigonometric function. In the case of load modulated amplifiers this is often not the case, complex functions are required in order to achieve a linear output and maximum system dynamic range simultaneously. In some cases a modified arc-cosine function or LUT's are used in order to reduce this mismatch. The mismatch can affect the output of the amplifier in two ways. First the AM/AM function can be altered introducing a continuous non-linear output resulting in severe intermodulation distortion. Secondly, any phase offset that exists between the outphasing paths will limit the dynamic range of the amplifiers output. This can affect the amplifier at both maximum and minimum output powers. The effect at lower output powers can introduce a discontinuous function, which has been highlighted in Section 3.3.

3.4.2 Static Offsets

Signal imbalance between the outphasing paths can be introduced by both amplification stages of the small signal generation hardware. In most cases these effects can be removed through a calibration process. In a well designed outphasing amplifier these offsets are confined to the small signal generation stages. The following section will introduce the main imbalances which occur in small signal generation.

3.4.2.1 Quadrature Imbalance

As with all quadrature transmitters both signal paths need to be calibrated to remove quadrature offsets which result from gain and phase offsets between the real and imaginary paths in the

transceiver. Furthermore any DC offset which occurs will result in the local oscillator feeding through the system and therefore also needs to be accounted for. Quadrature imbalance will be generated in the signal generation hardware only, specifically the digital to analogue converters and the quadrature modulators.

In an outphasing system these effects will alter the characteristics of the outphasing signals. Any asymmetric changes to the outphasing signal will affect the signal recombination. Quadrature imbalance can manifest itself in the frequency domain if sufficiently large in comparison to the outphasing amplifier noise floor.

3.4.2.2 Gain imbalance between outphasing paths

Gain imbalance is an amplitude imbalance between the outphasing paths G_n. Gain imbalance can occur at any stage in the outphasing system. In the amplification stages it can be attributed to device gain or amplifier input/output matching and is heavily dependent on power combiner design and frequency of operation. In the earlier stages it is most likely caused by the digital to analogue conversion or due to varying impedances in the transmission path.

This imbalance will occur at all output powers however it will cause the largest percentage error at lower output powers. This is further examined in the following section on outphasing amplifier simulations, Section 3.5. The offset will prevent the outphasing power amplifier achieving zero output power, limiting dynamic range.

3.4.2.3 Phase imbalance between outphasing paths

Phase imbalance is a shift between the outphasing paths δp_n. This can be introduced at any stage in the outphasing system, attributed to the signal generation and amplification stages equally. The design of the power combiner is crucial in determining the phase shift of the system, the values of the load compensation network will greatly impact this value.

The result is a shift in the relationship between the amplitude to phase function of the SCS, potentially limiting the maximum or minimum output power of the system.

3.4.2.4 Time delays imbalance between outphasing paths

Delays between the outphasing paths τ can greatly impact the output linearity, and result in reduced operational bandwidth if not characterised properly. They can occur in both the digital

and analogue small signal generation however delays are typically due to timing errors in the digital to analogue conversion and therefore primarily confined to the signal generation portion of the system.

A delay offset will cause visible wideband noise in the frequency domain and severe spreading in the AM/AM characterisation of the system. The effects will greatly increase as the bandwidth of the system increases. While software solutions can reduce the impact to a degree it is generally better to resolve these issues in hardware as much as possible from the outset.

3.4.3 System Bandwidth

The outphasing power amplifier achieves efficient amplification through the use of constant envelope phase modulated signals. To achieve maximum efficiency the amplification stages use either switch mode or deeply saturated operation as outlined in Section 3.2. Passing a constant envelope signal through a band-limited system will modify the phase information and introduce amplitude modulation. The amplification stages will strip the amplitude information from the input signals. As a result any information that was transcoded during the band limiting will be lost. The modified constant envelope signals will not linearly recombine. Pass band limitations can occur at any point in the outphasing system, from the baseband signal generation to the RF passband of the modulators and the amplifiers matching networks.

The non-ideal effects are most apparent in the frequency domain with an increased out-of-band noise floor. The largest non-ideal out-of-band spectral noise generated by bandwidth limitation occurs at the transition point between the pass-band and stop-band of the system. The rate of change of this transition and the magnitude of the attenuation will determine the magnitude of the out of band noise.

3.4.4 Frequency Passband Ripple

The frequency response of the baseband and RF components of the outphasing system will each have a frequency response and ripple across the passband. A frequency response will alter the outphasing signals amplitude and phase. Gain and phase ripple will be limited in the passband however any variation will induce non-ideal behaviour similar to the static offsets outlined in Section 3.4.2.2 and 3.4.2.3. The offset is not constant therefore the noise floor will

not be raised as much as a static offset.

3.5 Outphasing PA simulations

This section will demonstrate the sensitivity of the digital outphasing topology to signal imbalance. The outphasing amplifier requires digital signal processing in the form of a signal component separator to enable linear amplification. As such the entire signal generation and RF hardware up to the amplifiers input should be considered as part of the outphasing system. To evaluate the sources of non-ideal behaviour outlined in Section 3.4, simulations will be carried out in both Matlab and Agilents Advanced Design Systems (ADS) Circuit simulator. In Matlab a general model will be built using an ideal formula of the outphasing signals. The circuit simulator will help demonstrate the extent of the effects which are dependent on to the amplifiers design such as SCS and combiner mismatch and amplifier passband ripple.

3.5.1 System simulation

The system simulation is carried out in Matlab using equations to describe the effects outlined in the previous sections. Static offsets will be incorporated into a Cartesian description of the outphasing signals prior to recombination. This enables the sensitivity of the individual offsets to be compared using signal error and ACPR.

3.5.1.1 Quadrature imbalance

Using the rectangular representation of a quadrature signal we can examine the effects of quadrature imbalance.

$$S(t) = A(t)exp(j\phi(t)) \tag{3.17}$$

$$Re(t) = A(t)cos(\phi(t)) \tag{3.18}$$

$$Im(t) = A(t)sin(\phi(t)) \tag{3.19}$$

$$S(t) = Re(t) + jIm(t) \tag{3.20}$$

$$S(t) = A(t)cos(\phi(t)) + jA(t)sin(\phi(t)) \tag{3.21}$$

$$S'(t) = [(G + G\Delta)A(t)cos(\phi(t) + \psi) + DC1] + j[(G - G\Delta)jA(t)sin(\phi(t) - \psi) + DC2] \tag{3.22}$$

Equation 3.22 is a modified version of the ideal rectangular case in equation 3.21. The inclusion of gain error ($G\Delta$), phase error (ψ) and DC offsets (*DC1* and *DC2*) provide a direct model for path mismatch within a quadrature signal. Using this model we can simulate the effects and sensitivity of the quadrature transmitter to IQ mismatch. Figure 3.14 demonstrates the effects of 0.1% mismatch to gain, phase and DC offset. A single tone at an intermediate frequency(IF) is unconverted to its final frequency and can be seen at the intermediate frequency plus the local oscillator frequency ($fLO + fIF$). LO feed through due to the DC offsets can clearly be seen at the up conversion centre frequency. The IQ image, a result of gain and phase mismatch, a mirror image of the wanted signal appears on the lower side of the up conversion frequency ($fLO - fIF$). Both LO feed through and IQ mismatch will introduce additional frequency components to the individual outphasing signals, given the sensitivity of the combiner structure at lower output powers, the additive effect to each path will cause linearity issues.

3.5.1.2 Effects of offsets on outphasing recombination

Expanding equations 3.2 and 3.3 to include the quadrature and outphasing path mismatch parameters that are outlined above, we can evaluate the sensitivity and linearity of an ideal outphasing structure. Equations 3.24 and 3.25 outline the contributions of outphasing mismatch to the signals S_1 and S_2, including the effects of quadrature mismatch results in equations 3.26 and 3.27

$$S'(t) = S'1(t) + S'2(t) \tag{3.23}$$

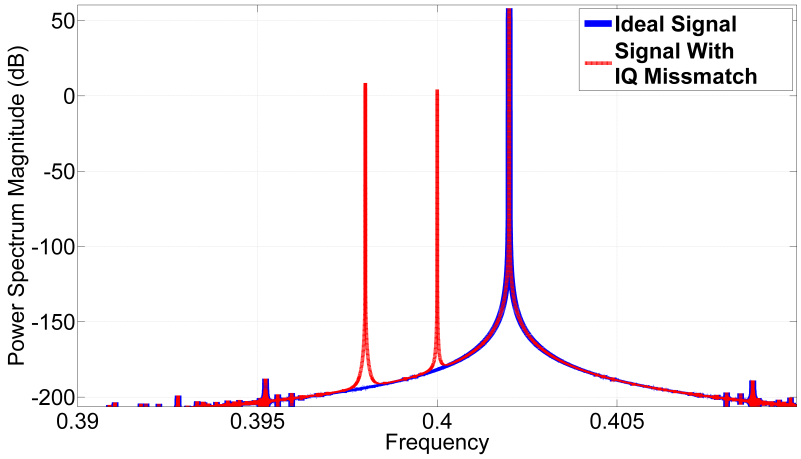


Figure 3.14: Quadrature signal with 0.1% mismatch on gain, phase and DC offset

$$S_1'(t) = 0.5(G_1(exp[j(\omega(t+\tau) + \phi(t+\tau) + \rho(t+\tau) + \Delta p)])) \tag{3.24}$$

$$S_2'(t) = 0.5(G_2(exp[j(\omega(t-\tau) + \phi(t-\tau) + \rho(t-\tau) - \Delta p)])) \tag{3.25}$$

$$\begin{aligned} S_1'(t) = 0.5 * ([(G_1 + G\Delta_1)cos(\omega(t+\tau)(\phi(t+\tau) + \psi_1 + \rho(t+\tau)) + \Delta p) + DC_{I1}] \\ + j[(G_1 - G\Delta_1)jsin(\omega(t+\tau)(\phi(t+\tau) - \psi_1 + \rho(t+\tau)) + \Delta p) + DC_{Q1}]) \end{aligned} \tag{3.26}$$

$$\begin{aligned} S_2'(t) = 0.5 * ([(G_2 + G\Delta_2)cos(\omega(t-\tau)(\phi(t-\tau) + \psi_2 - \rho(t-\tau)) - \Delta p) + DC_{I2}] \\ + j[(G_2 - G\Delta_2)jsin(\omega(t-\tau)(\phi(t-\tau) - \psi_2 - \rho(t-\tau)) - \Delta p) + DC_{Q2}]) \end{aligned} \tag{3.27}$$

Examining equations 3.26 and 3.27, we can determine the sensitivity of the overall system to the various types of mismatch. Each channel has individual quadrature mismatch, outphasing mismatch is common to both channels. Outphasing gain mismatch is represented by the ratio of G_1 and G_2, phase mismatch is represented by Δp and delay mismatch is represented by τ. Individually sweeping both outphasing and quadrature mismatch the effects on signal error vector magnitude(EVM) and signal linearity in the form of adjacent channel power ratio (ACPR) can be represented.

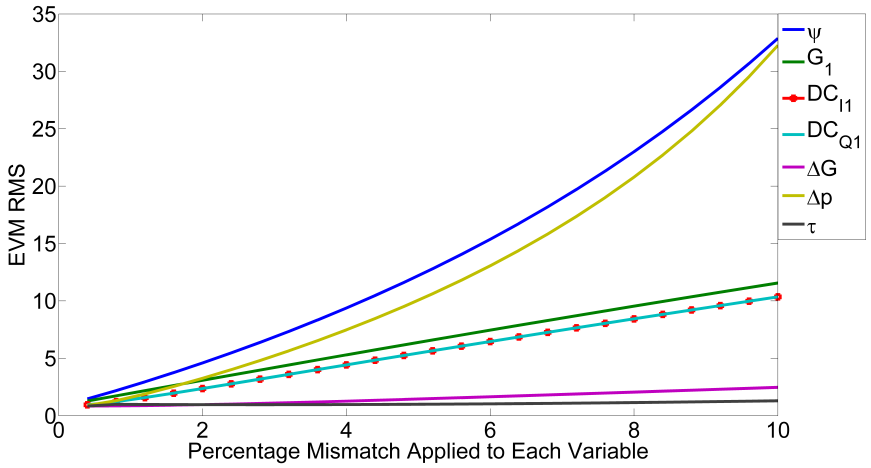


Figure 3.15: The effect of mismatch on outphasing system comparing signal EVM. The model of the outphasing system is outlined in equations 3.26 and 3.27.

Figures 3.15 and 3.16 demonstrate the sensitivity of the outphasing architecture to the various forms of path mismatch. Simulation results demonstrate the sensitivity of the outphasing architectures to phase mismatch. Deviations in IQ phase mismatch and outphasing phase result in the largest signal EVM values. In terms of ACPR the outphasing path mismatch have the most impact reducing ACPR to a little as -20 dBc. Even 0.25% outphasing phase mismatch will result in a 20 dB reduction in ACPR. Examining the outphasing functions in equations 3.2 and 3.3 it is clear that simulation results are as expected. Any deviation in the phase of S_1 and S_2 will effect both output signal amplitude and phase, the impact of which is an increase in out of band power.

While path mismatch will cause error at all output powers, the largest relative errors occur at output powers close to zero magnitude, in general this is a function of the outphasing topology. Mismatch is most apparent at lower output powers where the signals must cancel exactly to achieve the required magnitude and phase output. This is demonstrated in Figure 3.17, the error is normalised for each magnitude, as we approach zero error approaches 100% and in some cases can exceed the magnitude of the signal. This can create issues when standard linearisation techniques are used, which will be evaluated in later sections.

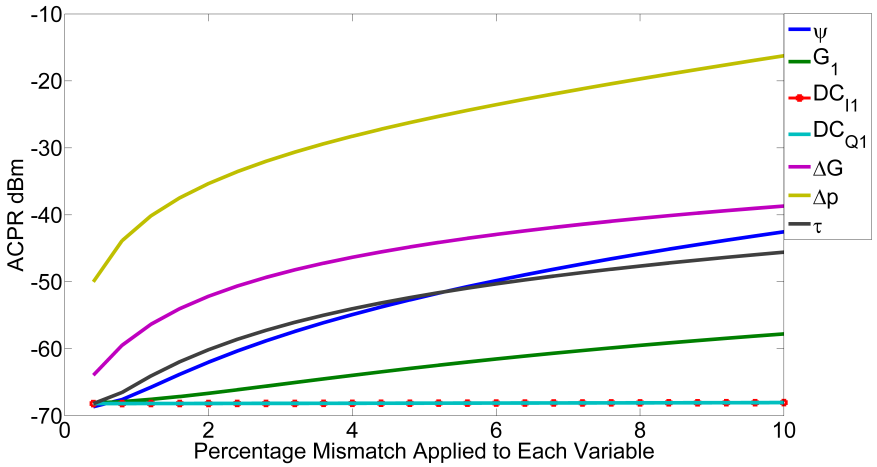


Figure 3.16: The effect of mismatch on outphasing system comparing signal ACPR. The model of the outphasing system is outlined in equations 3.26 and 3.27.

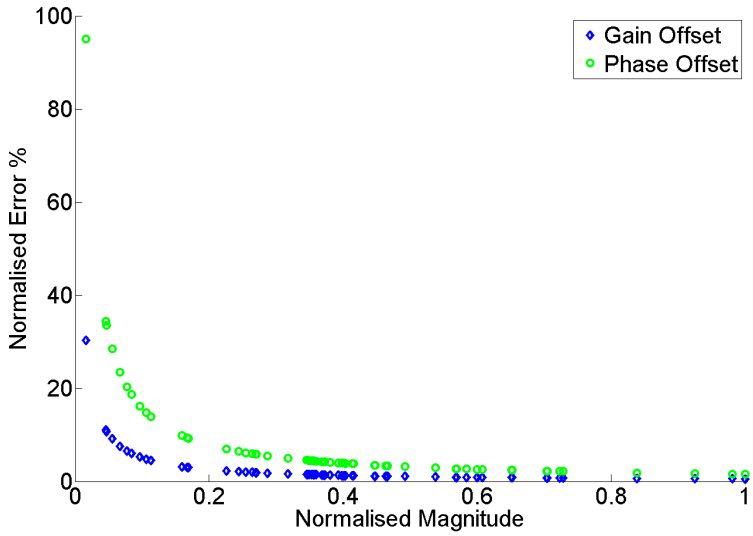


Figure 3.17: Normalised error for a range of magnitudes, Offset is constant at 0.1%

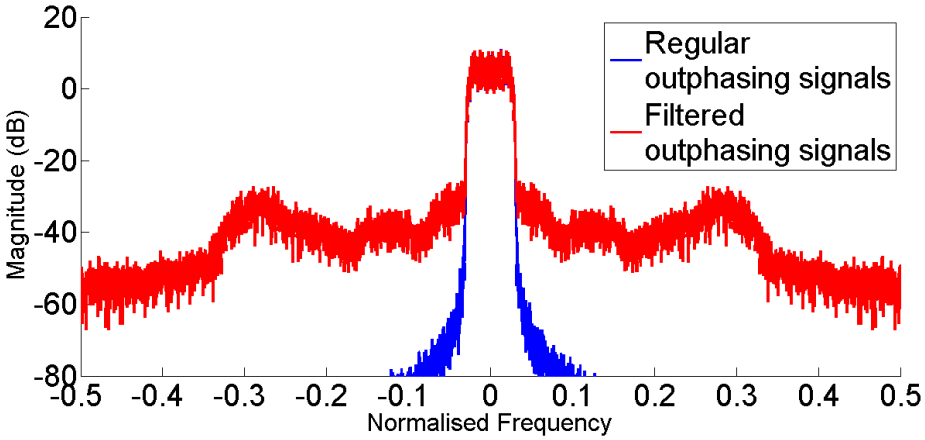


Figure 3.18: Effects of band limitation on out phasing signals.

3.5.1.3 Limited outphasing passband

Bandwidth expansion of the outphasing signals increases the pass band requirement of every component in the signal generation and RF signal chain. This includes the amplifier itself, both the amplification stages and the combiner itself must achieve a sufficient passband to enable linear operation. This can be difficult to achieve given the tuned nature of the amplifiers input and output matching networks and the combiner itself. Failure to achieve the required passband generates an increased out of band noise floor and a dramatic impact on ACPR levels. Figure 3.18 demonstrates the effects of a band-limiting filter applied to an outphasing signal before recombination. An IIR filter with a passband of 25 MHz is applied to the outphasing signal of a 5 MHz QAM signal, this is approximately half the predicted required pass band. Simulating the effects of a digital or saturated outphasing amplifier the amplitude information is stripped from the signals and then recombined. The out of band level is significantly increased when compared with the ideal recombined signal in blue.

3.5.2 Circuit simulation

Not all of the effects outlined in Section 3.4 can be simulated using an ideal model, or ideal filters. The SCS and re-combiner mismatch is an amplitude dependent effect, and the passband ripple is a frequency dependent effect. Moreover each of these non-ideal behaviours are system dependent. Evaluating a simulation of an outphasing power amplifier will demonstrate more realistic characterisation of these effects. To this end an amplifier is designed in ADS. The

design process is outlined below. Using the characteristics of the amplifier, equivalent functions in Matlab are developed. By applying these functions to a modulated signal the extent of the amplitude dependent and frequency dependent effects can be independently explored.

3.5.2.1 Class B Saturated Amplifier

To analyse the Chireix combiner linearity a saturated Class B amplifier was designed in simulation. A GaN HEMT 10 Watt transistor from Cree (CGH40010) is chosen for the amplifier structure. The transistor is capable of broadband operation and can achieve a saturated efficiency of greater than 65% for linear operation in Class AB biasing of -2.7 V. The Class B amplifier will have a lower bias point than the reference design and as such greater efficiency can be expected, as a trade off however a loss of amplifier gain is expected. From the data sheet a threshold biasing gate voltage of $-3V$ will be used. This provides Class B operation with a 180 degrees conduction angle, for a drain voltage of 28 V. The reference amplifier circuit is capable of 16 dB gain at 2 GHz. The saturated Class B amplifier will target a gain of 14 dB.

The design will match the transistor input and output impedances to 50 ohms. Load pull analysis was carried out on the transistor in order to determined the optimum load impedance, a balance between maximum output power and maximum power added efficiency was chosen. The results from load pull can be seen in Figure 3.19, the load impedance chosen delivered a 42 dBm of power to the load an a power added efficiency of 75.6% at a saturated input power of 27 dBm. Input and output matching circuits were designed using single poll stub matching. The biasing network was also included in the matching circuit. The source impedance of the amplifier was measured at $5 + 0j$ ohms, therefore a real impedance transformation is required to match a 50 ohm input, the chosen network can be seen in Figure 3.20. As an impedance transformation does not require any reactive components the circuit is designed without any stubs. The load impedance chosen was $20 + 23j$, a single pole L matching network performs the impedance transformation to a 50 ohm output as seen in Figure 3.21.

The initial input and output networks are designed independently using s-parameter simulations to evaluate the networks passband and return loss. Finally a harmonic balance simulation is carried out to optimise the design for output power and power added efficiency. The performance following the tuning process is displayed in Figure 3.22. The design satisfies the design targets set out in this section.

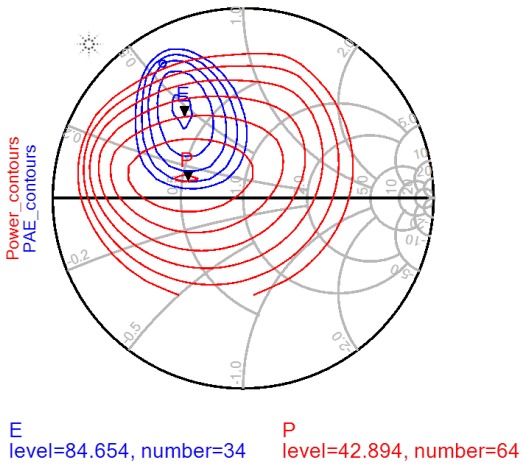


Figure 3.19: Simulated Load pull analysis, maximum power analysis in red, maximum power added efficiency analysis in blue.

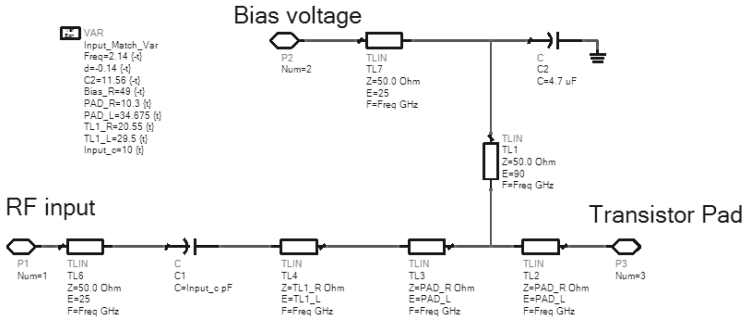


Figure 3.20: Class B input match

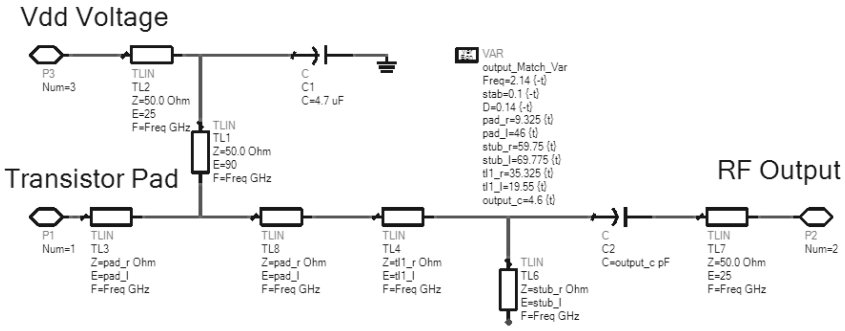


Figure 3.21: Class B output match

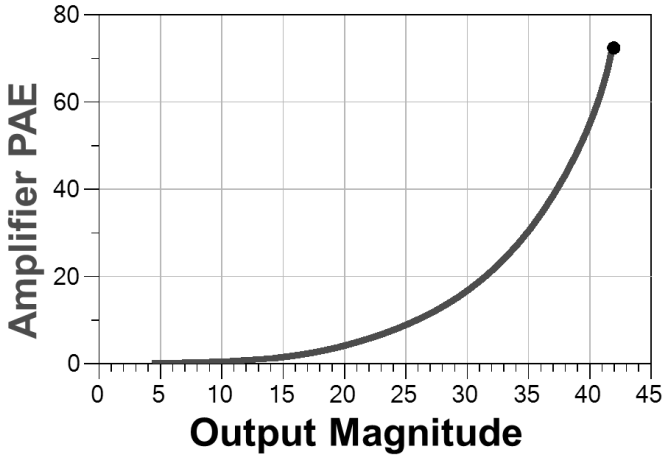


Figure 3.22: Power added efficiency of simulated GaN Class B power amplifier. PAE = 75%, output power of 41.9 dBm and a gain of 14.9 dB @ 27 dBm input power

3.5.2.2 Outphasing amplifier design

The key to the outphasing amplifier's efficiency is the combiner circuit as outlined in Section 3.1.3. The Chireix combiner is chosen for its efficiency at back-off output power. The topology of the combiner is outlined in Figure 3.23. The combiner consists of three quarter wavelength transmission lines. Ideal admittances are used to provide load compensation, enabling the efficiency gains at lower output powers. Choosing 50 ohm impedance for load matching for both the Class B amplifier and the output of the combiner greatly reduces the complexity of the combiner design. Equation 3.28 describes the relationship between the branch transmission line impedance's $Z1$ and the output impedance and characteristic impedance $Z0$ when the inputs and output of the combiner are the same.

$$Z1 = Z0\sqrt{2} \tag{3.28}$$

Load compensation is calculated using equation 3.29, where the impedance Z_L is the load impedance of the amplifier input to the combiner circuit and the outphasing angle is ϕ. The design optimises the outphasing angle to achieve a maximum drain efficiency at 6 dB power back off. Following some system tuning an outphasing angle of 22.5 degrees is chosen. The resulting amplifier performance is presented in Figure 3.24. The resulting peak efficiency is equivalent to the saturated Class B amplifier at 75%. However the efficiency in back off is

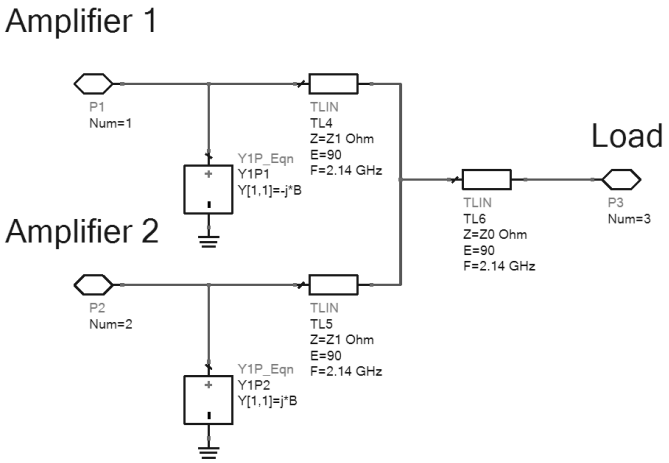


Figure 3.23: Outphasing amplifier Chiriex combiner. A two stage transmission line output combiner with ideal load compensation supectances.

improved by 30% at 6 dB back off and 20% at 10 dB back off power, in both cases this represents double the efficiency of the Class B amplifier alone while enabling saturated or switch mode operation.

$$B = \frac{sin(2\pi\phi)}{2Z_L} \tag{3.29}$$

3.5.2.3 Combiner Passband

There are three main causes for limited dynamic range: imbalance occurring in small signal generation; and amplification stages and the design of the combiner itself. The majority of small signal and amplifier imbalance can be offset with static calibration, an important step in initialising a two path amplification system. However care must be taken when designing the amplifier and combiner that the required dynamic range is achievable at the centre frequency, of course wide-band operation is more desirable. The main cause of limitations from the amplifier design is in the unmatched combiner case where load compensation occurs. Ideally both amplifiers experience identical loading at all output ranges in order to achieve a linear output, for load compensation this is not the case. Each amplifier experiences an alternate reactance, either capacitive or inductive. For a balanced output these reactance values are required to be equal but opposite. For reactive components this typically only occurs at a single

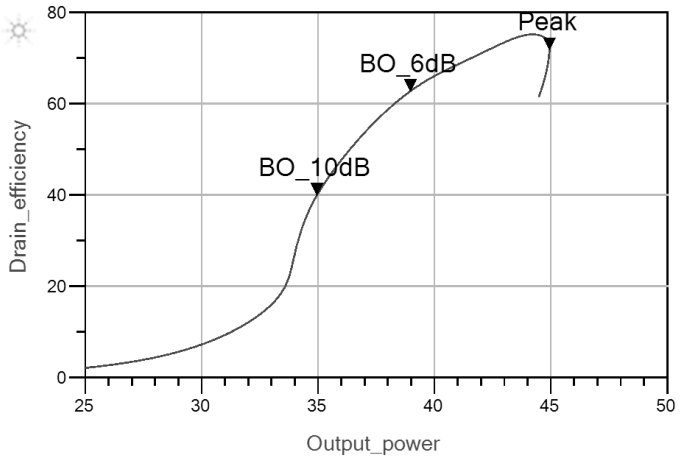


Figure 3.24: Outphasing amplifier drain efficiency. Peak power 44.9 dBm, Peak efficiency 75%, efficiency at 6 dB back off 64%, efficiency at 10 dB back off 40%, dynamic range 69dB

frequency, and for maximum efficiency these paired reactances must match the susceptance for the amplifier. Any deviations from this will result in either a limited dynamic range or a sub-optimal efficiency from the output. An example of limited dynamic range due to variation in the load compensation value can be seen in Figure 3.26, and due to change in frequency of operation in Figure 3.25.

3.5.2.4 Combiner compensation angle

For ideal recombination an arc-cosine function provides a linear amplitude to phase mapping. However for a Chireix combiner this is not always the case, specifically in the case of a load compensated Chierix combiner. The additional reactive components generally change the phase angle at which minimum and maximum magnitude is achieved. In some cases this can be described with a stretched arc-cosine function. In real world systems this is not always the case, a more effective method is to characterise the outphasing angle to amplifier magnitude relationship directly, using a look up table to implement the function. An example of the variation of the phase to magnitude function for different load compensation values can be seen in Figure 3.26. The LUT thus ensures linear amplitude modulation. The most important points to find for any combiner structure are the phase angles that correspond to the minimum and maximum output amplitudes. These points will determine the maximum dynamic range of

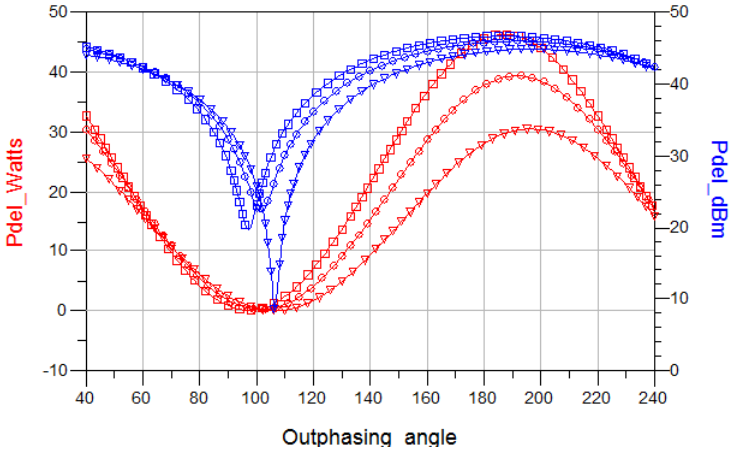


Figure 3.25: Outphasing frequency of operation - square = 1.8GHz, circle = 2.1GHz, triangle = 2.4GHz

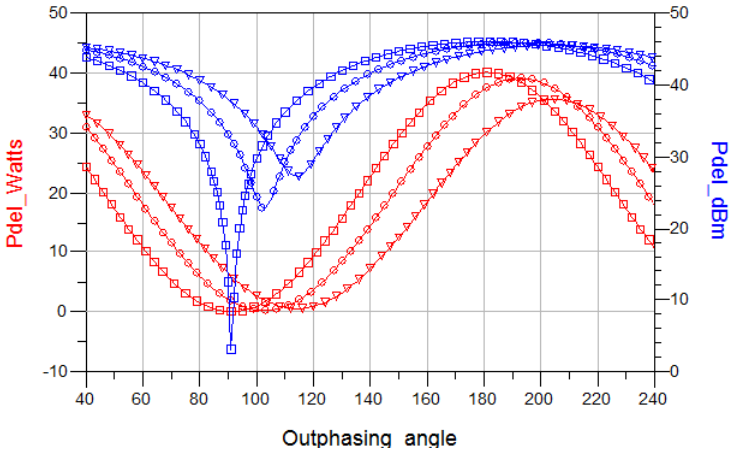


Figure 3.26: Outphasing angle - square = compensation angle of 0, circle = compensation angle of 10, triangle = compensation angle of 20

the system.

3.5.2.5 AMAM AMPM Linearity

For analytical purposes in the previous sections an ideal signal component separator and combiner functions were considered. However in practical implementations this is not the case, especially considering the case of non-isolating power combiners. Furthermore the implementation of load compensation can introduce further non-ideal effects, the two issues with the greatest impact is the amplitude imbalance between input branches and the phase shift and distortion to the characteristic recombining function. The amplifier characterisation sweep

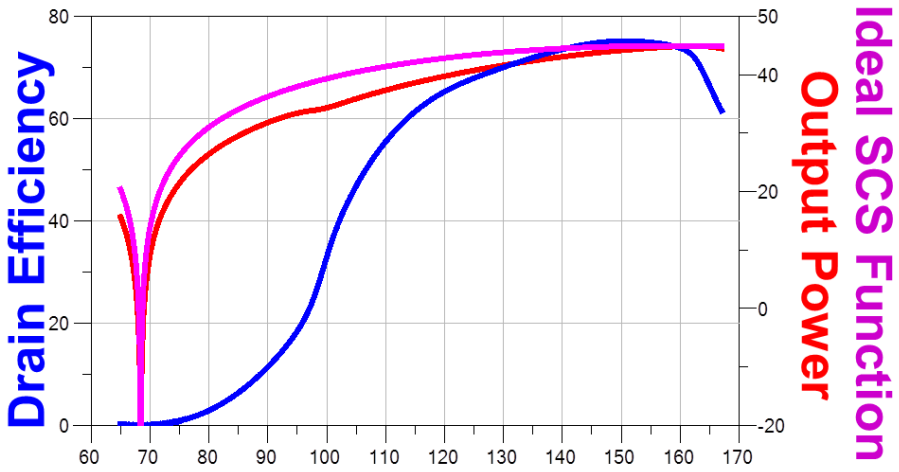


Figure 3.27: Outphasing amplifier characterisation sweeps, output magnitude is compared to an ideal arc cosine function with a phase shift to illustrate the deviation between ideal and practical outphasing system output.

is presented in Figure 3.27, the figure demonstrates amplitude and efficiency functions with respect to outphasing angle.

The introduction of load modulation can introduce amplitude imbalance between outphasing paths, in the design outlined in Section 3.5.2.2 ideal components are used, the amplifiers in path one and two are identical and even so some limitations of dynamic range were observed. To alleviate these and maximise dynamic range an imbalance is introduced to the drain supply voltage (VDD), the value of which can be determined analytically using the S-parameters of the combiner with compensation elements in place. Alternatively it can be determined empirically by sweeping through a range of offset values, a method that is commonly used in practical implementations [111]. The offset required for the proposed simulation was an additional 0.05 volts on the drain of amplifier 2. The results demonstrated an increase of $20dB$, resulting in a dynamic range of almost $70dB$. This adjustment highlights the sensitivity of the outphasing system to imbalance.

An incorrect signal component separator function while capable of achieving the maximum system dynamic range, can still introduce distortion which can be compared to AMAM

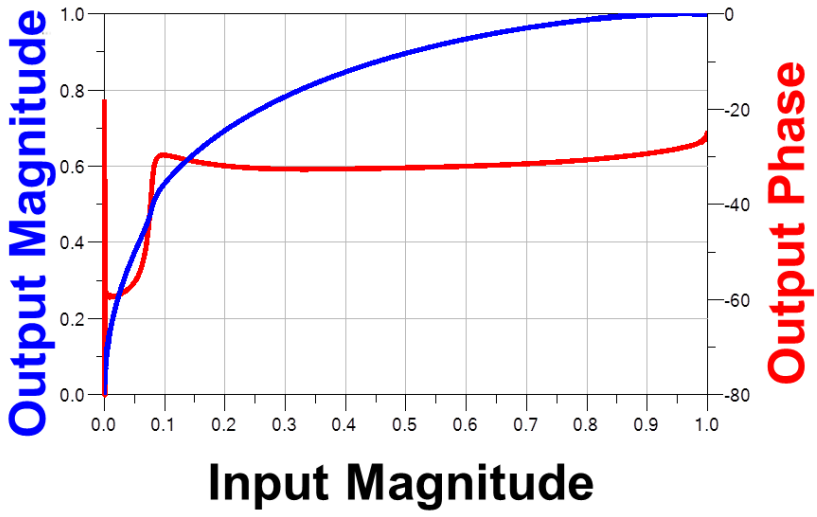


Figure 3.28: AMAM AMPM of simulated outphasing amplifier.

distortion in standard amplification systems. Gain expansion, gain compression and AMAM distortion will result in harmonic distortion occurring as described in Section 2.4. The AMAM AMPM function of the outphasing amplifier is demonstrated in Figure 3.28. The ideal linear input function is an arc-cosine function which included a phase shift to account for the cancellation offset introduced by load compensation elements. An example of the stretched arc-cosine function is presented in equation 3.30, where ϕ is the outphasing angle, $\mid S(t) \mid$ is the magnitude of the input signal S, H is the scaling factor to stretch the arc-cosine function and υ_{comp} is the phase deviation introduced by the load compensation technique.

$$\phi = arc - cosineine(\mid S(t) \mid) * H + \upsilon_{comp} \tag{3.30}$$

In practical systems, and as demonstrated in simulations, the stretched arc-cosine is not capable of capturing the non-linear effects associated with the outphasing angle to output magnitude relationship. Additionally an amplitude to common phase deviation may also exist [112]. The effects of the non-linear response are presented in Figure 3.29. The AMAM AMPM response is imported into Matlab and applied to a QAM signal. A significant increase in ACPR levels due to the severity of the mismatch between SCS and power combiner amplitude

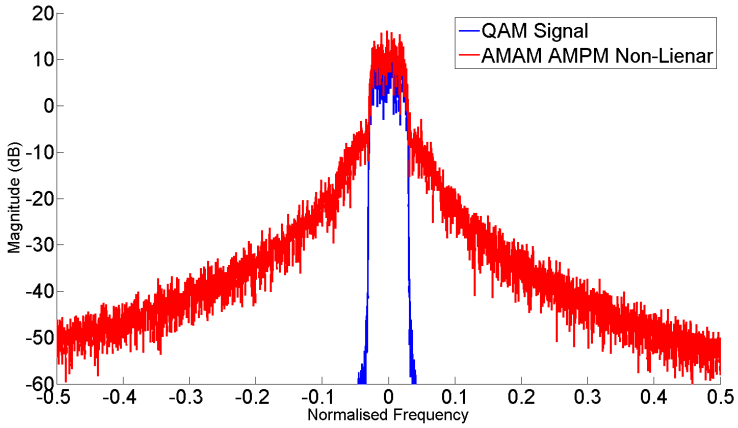


Figure 3.29: AMAM AMPM effects on QAM modulated signal. Blue shows the original signal, Red presents the non-linear mismatch between SCS and power combiner. ACRP of -22dBc

functions is observed.

3.5.3 Frequency dependent non-linearity

The circuit simulation of the amplifier implementation has validated the existence of frequency dependent effects on the outphasing system. To demonstrate the effect on amplifier linearity the amplitude and phase offsets are imported into Matlab and applied to a modulated signal. The results are plotted in Figure 3.30. By asymmetrically applying amplitude and phase offsets to the outphasing signals before re-combination, an analysis can be carried out on the importance of wideband systems and therefore the consequence of bandwidth expansion on outphasing signals. Simulations carried out with a multi-tone sinusoidal signal demonstrates the out-of-band, non-ideal effects on a wideband amplitude and phase modulated signal. The non-linear effects are introduced in the frequency domain, the signals are then translated back to the time domain for recombination.

Given the wideband nature of the outphasing signals it is conceivable that the transmitter system will impose a frequency imbalance across the band of operation. The effects of applying a $1dB$ mismatch to single path of an outphasing system has been simulated in Figure 3.31. A QAM signal is used to demonstrate the impact of this non-linearity is a slightly increased noise floor across the band. However in comparison to the static offsets, frequency dependent offsets on a system which is calibrated at the centre frequency will not result in as much non-

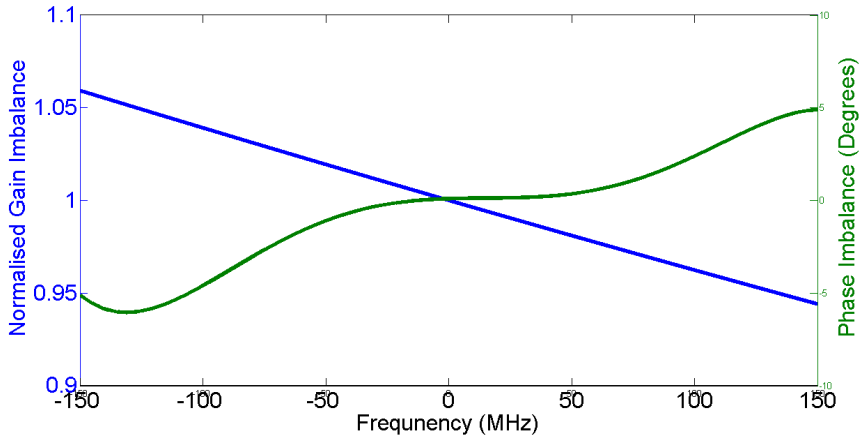


Figure 3.30: The frequency imbalance of the outphasing amplifier.

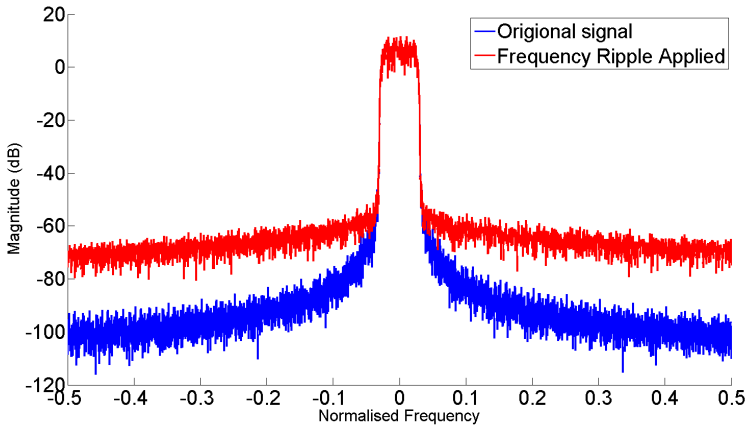


Figure 3.31: Frequency ripple offset applied to modulated signal.

linear frequency effects. The ACPR and noise floor are still within acceptable levels. If signal bandwidth increases we can expect an increase in the noise floor and ACPR. These effects have not yet been published for an outphasing topology.

3.6 Effects of thermal variation on outphasing topology

While the thermal effects on power transistors are highly characterised in their documentation and the thermal effects of a LDMOS power amplifier have been examined for pulsed operation in [113], the thermal effect on the outphasing topology has not yet been explored. Using the circuit simulation of an outphasing amplifier designed in section 3.5.2.2 it is possible to adjust the junction tempetrature of the device to analyse gain and phase shifts from the amplifiers

and their effect on the linearity of the topology. First the impact of thermal changes on the saturated Class B power amplifier is evaluated in section 3.6.0.1, providing an approximation of the thermal effects that will be present in the outphasing topology presented in 3.6.0.2. As we have shown previously the outphasing topology is sensitive to amplitude and phase shifts. The outphasing power amplifier using a isolating power combiner is robust to offsets applied to both amplification paths simultaneously, However given that the Chiriex topology is differential, phase offsets due to thermal variations on both amplifiers will sum rather than being cancelled, and therefore impact the amplifiers linearity.

Power amplifier thermal stability impacts not only device longevity, it significantly contributes to the non-linear operation of the amplification circuit. Variations in transistor temperature affect the internal resistance (Rth_{on}). This effect can result in a memory effect which is referred to as an electro-thermal memory effect. The effect is dependent on the method of amplifier operation, either pulsed power operation or carrier wave operation. In [113] the authors present an analysis and subsequently a thermal model for a generic power amplifier which experience both long and short term thermal memory effects. The model accounts for the variation in output gain and absolute phase shift with a shift in device temperature.

3.6.0.1 Class B PA Thermal Characteristics

Thermal variations are simulated through modifying the transistor package temperature of the device model. Harmonic balance analysis is carried out, demonstrating the relative effects on the amplifiers operation. Figure 3.32 demonstrates the impact of a 10 degree swing above and below the nominal operating value. In a typical amplifier structure the variance demonstrated will almost be undetectable, as our simulations demonstrate the output gain is reduced by 0.15 dB for each 10 degree step. While the amplitude difference is apparent in a variation of output power, it will not result in a significant non-linearity unless the amplifier is operating close to the 1 dB compression point. The phase shift with temperature appears to be not dependent on amplifier output power therefore should not impact on amplifier linearity. These variations will have a greater impact on the outphasing structure which depends on constant branch gain and phase for a linear output.

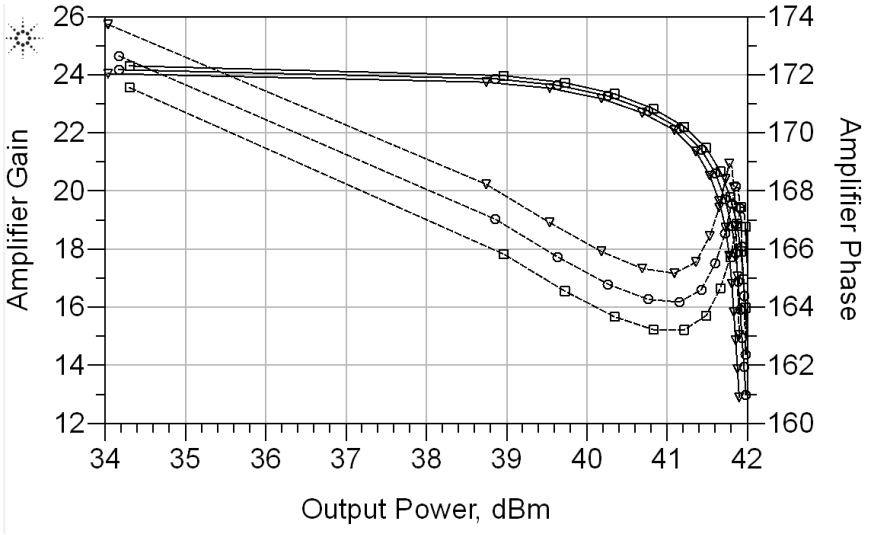


Figure 3.32: Effect of thermal variations an a Class B amplifier. Solid line = amplifier gain, Dashed line = amplifier phase. Square delta temp -10 degrees C, Circle delta temp 0 degrees C, Triangle delta temp +10 degrees C.

3.6.0.2 Outphasing Amplifier Thermal Considerations

As demonstrated in Section 3.3 the linearity of the outphasing amplifier is effected by the slightest variation of either the gain or phase. The thermal variation effectively results in an impedance change at the output of the amplifier. The load impedance of the outphasing amplifier is fixed and the output impedance of the amplification stage has been modified, therefore the load compensation applied to the combiner is no longer optimal. The outphasing phase angle experiences a shift in accordance with the variation demonstrated in Figure 3.32. The effect on the relationship between outphasing angle and output power is demonstrated in Figure 3.33. The most notable impact is on the dynamic range achievable by the outphasing amplifier. The results presented in this work cause a reduction of greater than 20 dB. In comparison to the Class B amplifier the thermal effects have a dramatic impact on outphasing amplifier linearity. The effect of the limited dynamic range has been explored in Section 3.3.3.

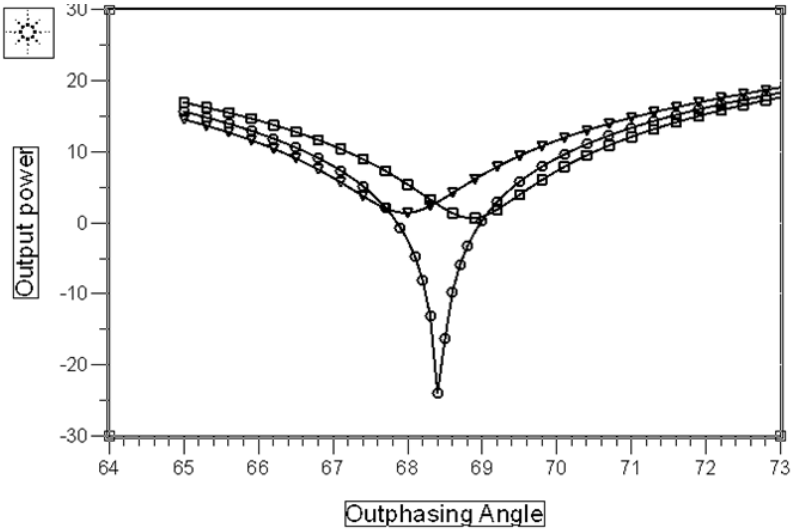


Figure 3.33: Effect of thermal variation on minimum achievable output power. Square delta temp -10 degrees C, Circle delta temp 0 degrees C, Triangle delta temp +10 degrees C

3.7 Conclusion

This chapter presents the basic operation of the outphasing amplifier highlighting the operational differences between isolating and non-isolating power combiners. Various implementations of the outphasing PA have been investigated to enhance both efficiency and linearity. The relative simplicity and potential efficiency of the digital outphasing power amplifier is the reason that it has been chosen for further linearisation studies in this work.

The sensitivity of the amplifier topology to amplitude and phase imbalances is discussed, including an analysis of the impact to a communications signal in both the time and frequency domain. All offsets will impact operational linearity however the gain and phase offsets between the outphasing paths will be the greatest contributors. From this it was determined that a broadband and balanced transmission system is essential to enable wideband operation of the outphasing amplifier. This will be discussed more in the following chapter.

Further analysis of the outphasing topology was carried out to determine the effects of thermal variation on the design, an analysis that to the authors knowledge has not been considered to date. The results demonstrate that to ensure linear operation a thermal equilibrium must be achieved before characterisation and linearisation can be carried out. This requirement will be observed for all measurements carried out in the following chapters. These results have been published in [1]. Future work will be carried out to determine the sensitivity

of high power outphasing amplifier designs to asymmetric thermal effects.

Circuit simulations demonstrate the practical considerations that must be taken into account when designing an efficient, non-isolating outphasing amplifier design. This demonstrates the occurrence of AMAM AMPM non-linearity and frequency dependent effects which are not output power dependent. It is this property that must be further understood in order to develop more accurate behavioural models and in turn linearisation algorithms.

Bandwidth expansion of the outphasing signal increases the requirements on not only the signal generation and RF subsystems but also the amplifier design. Further analysis on bandwidth expansion in outphasing systems will be carried out. Limiting this side affect of phase only signal modulation could reduce the cost of the outphasing hardware and ease linearisation efforts.

The circuit simulations highlighted the effects that mismatch can have on the amplifier dynamic range. The dynamic range required to fully reconstruct a modulated signal will be investigated with a view to finding a possible method to negate the non-linear output of a system incapable of accurately generating the modulated signals at low output powers.

It is these three main areas of non-linearity: memory effects; bandwidth expansion; and limited dynamic range that will be further investigated in the upcoming chapters.

CHAPTER 4

Outphasing test bench and characterisation

To achieve maximum linearity from the outphasing power amplifier all possible non-ideal effects from the amplifier and the signal generation system must be considered. As such the amplifier is a part of a larger outphasing amplification system which includes signal generation and all radio frequency equipment up to the input of the amplifier. The outphasing signals experience bandwidth expansion when compared to the modulated communication signals. The bandwidth requirement for outphasing amplification systems is therefore an order of magnitude greater than traditional amplification systems.

Chapter 3 provides analysis of the distortion mechanisms in outphasing power amplifiers and highlights the effects of gain, phase and delay mismatch in both static and frequency dependent functions and how each can impact the system linearity. In this chapter an outphasing system is proposed that is capable of the generation and transmission of outphasing signals which relate to a wideband communication signal. A quad carrier WCDMA signal is chosen as the initial target for linear system operation. The system is evaluated with, and without, a device under test. A digital outphasing power amplifier from NXP is chosen to be evaluated, designed with wideband operation in mind, this efficient digital outphasing PA provides an excellent platform to analyse the limitations of the current state of the art.

Increased component count and more complex device models result in the substantial

increase in computational requirement to preform modulated system characterisation for an outphasing amplification system. Behavioural modelling of radio frequency system components aims to provide a computationally efficient yet accurate modelling structure to dramatically decrease simulation time. In this chapter existing behavioural model structures are presented and evaluated with data gathered from the digital outphasing test bed.

4.1 Outphasing Amplifier Test-bench

The requirements for linear operation of an outphasing amplification system have been explored in depth in Chapter 3. From this comparison it is clear the bandwidth requirements far exceed that of a traditional amplification system. For ideal operation a pair of identical RF signal generation paths are required. In this work our target output signal bandwidth is a minimum of 20 MHz. As outlined in Section 3.1.1 outphasing signals experience bandwidth expansion, therefore to achieve linear recombination the passband of the system must be greater than 12 times that of the original signal bandwidth. The target for the system is to have a minimum operating bandwidth of 240 MHz with a centre frequency of 2.14 GHz.

At the beginning of this work such a system was not readily available. The main reason for this was that test equipment did not exist for these operational bandwidths while simultaneously generating four synchronised signals, the I and Q signals for each outphasing signal. Wideband system components were initially targeted for integration into a existing outphasing test bench located at NXP Eindhoven. A comparable system was later developed with the chosen specification at Maynooth University's radio communications laboratory for further experimentation. Figure 4.1 is a block diagram overview of the proposed test bench. Any non-ideal effects which cannot be negated with currently available hardware are compensated for using digital signal processing on the signal generation hardware and will be outlined in future sections. A functional overview of the required test-bench is presented in Figure 4.1, where the signal generation is presented in detail. The impact of each component on the generated signal must be taken into account and the major contributions are highlighted. 1 The DAC can contribute non-linear intermodulation products, gain imbalance and DC offset. 2 The IQ modulators are responsible for the IQ mismatch, some gain imbalance and in some cases gain variance across the frequency band of operation. 3 The driver PA's can be responsible for gain

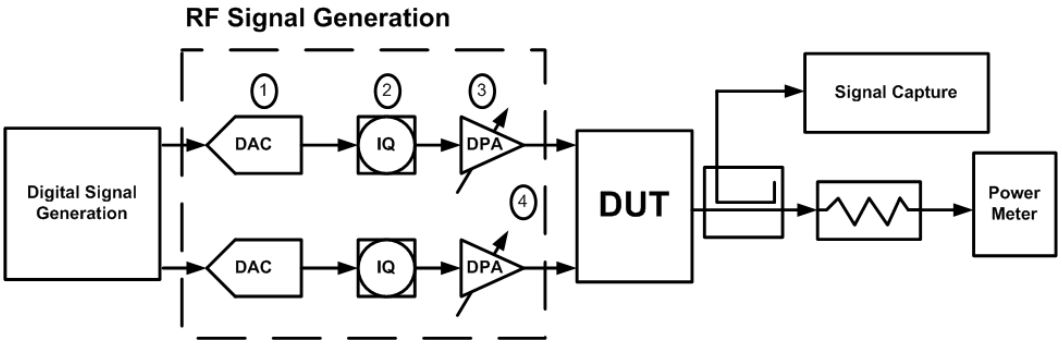


Figure 4.1: A functional overview of the outphasing amplifier test bench consisting of the major active components.

and phase imbalance as well as having a gain and phase imbalance across frequency. 4 Passive components that are not highlighted on the diagram such as power couplers or attenuators also have a frequency response that must be taken into account. The following sections outline the design choices for the test-bench to meet the unique requirements of outphasing operation.

4.1.1 Digital Signal Generation

Both the DAC and ADC require a high speed DDR LVDS interface, with digital logic capable of generating and capturing signals at greater than 500 Msps. The system requirements limit the choices of the digital logic to an FPGA implementation. The Texas instruments TSW 1400 development platform has a Alteara FPGA and 512 MB of random access memory (RAM) designed to either capture or generate a signal for Texas Instruments evaluation modules. It enables a seamless extension of the NXP test-bench to generate arbitrary wideband signals and capture signal bandwidth. Code for the TSW1400 was written in the development of standalone virtual instrument (VI) files to load and save signals in Labview. External data flow is controlled by an FTDI USB interface chip.

4.1.2 Digital to Analogue Signal generation

The use of a single quad DAC chip limits the occurrence of sub-sample delay between the outphasing signals, removing the requirement for sub-sample compensation. The outphasing signals are complex, requiring four signals to be generated; the in-phase and quadrature signals for both signal paths. The system requires a DAC capable of wideband generation of four high resolution signals. The DAC must be capable of a sample rate of a minimum of 240 MHz for

Figure 4.2: Texas Instruments pattern and generation board.

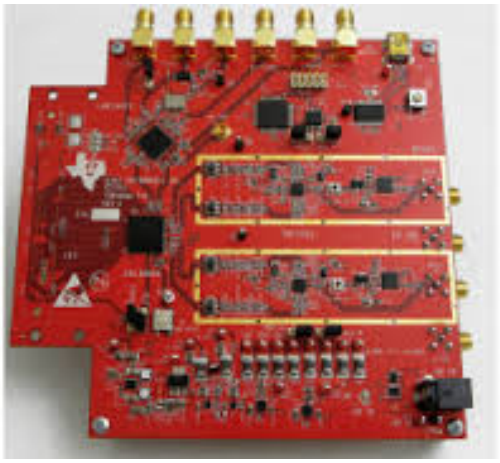


Figure 4.3: Texas Instruments signal generation board.

a 20 MHz signal [99]. One DAC which satisfied our requirements is the Texas Instruments DAC34SH84, capable of generating four 750 Msps signals direct from a digital interface with an FPGA. More specifically Texas Instruments have developed a dual path, signal generation, RF transmitter development board with the DAC34SH84. The TSW30SH84 board also overcomes the issues with path synchronisation as all four DAC's have the same clock sources and the RF paths are fully symmetrical. This dual path direct RF signal generation platform greatly reduced the potential for path mismatch and sub-sample delay between the signal paths. The RF signal chain is capable of RF up-conversion between 400 MHz and 3000 MHz, which complies with the required centre frequency of 2140 MHz.

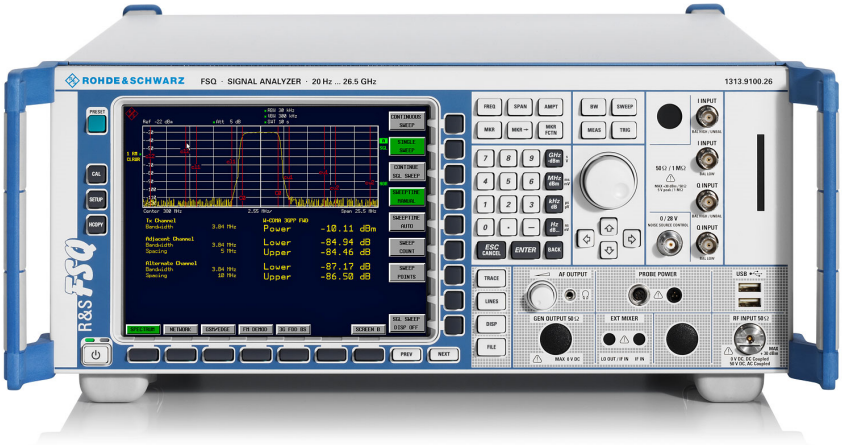


Figure 4.4: Spectrum analysis and signal capture.

4.1.3 Signal capture

A Rohde and Schwarz FSQ has a dual purpose in the outphasing test bench. As a spectrum analyser it can characterise and evaluate the operational performance of the amplifier. Spectrum analysis provides the capability of calibrating the set-up and characterising the amplifier through single and multiple sinusoidal tone sweeps. This will be discussed further in sections 4.1.4.1 and 4.1.5. The spectrum analysis provides adjacent channel power measurements for a variety of signal standards, useful when analysing the system under dynamic operation with a modulated signal. It is also capable of down conversion and signal capture of complex baseband signals. The frequency down conversion stage of the instrument enables the capture of modulated signal from 0-26.5 GHz, the baseband capture frequency is 122.88 MHz. Further baseband capabilities include error vector magnitude (EVM) and complementary cumulative distribution function (CCDF) which will be useful for time domain analysis in future work.

4.1.4 Test-bench Set-up and Qualification

The combined test-bench consists of the signal generation hardware, a signal capture system and ancillary test equipment such as power supplies, power meters and tonal frequency generators. The entire system is controllable with the use of a desktop PC through interfaces such as GPIB and USB. Figure 4.5 provides a picture of the test-bench set-up. An on-board PLL is capable of generating the conversion clock of the DAC's however for best results an independent clock source is used. The clock signal is supplied with HP 8656B signal generator.

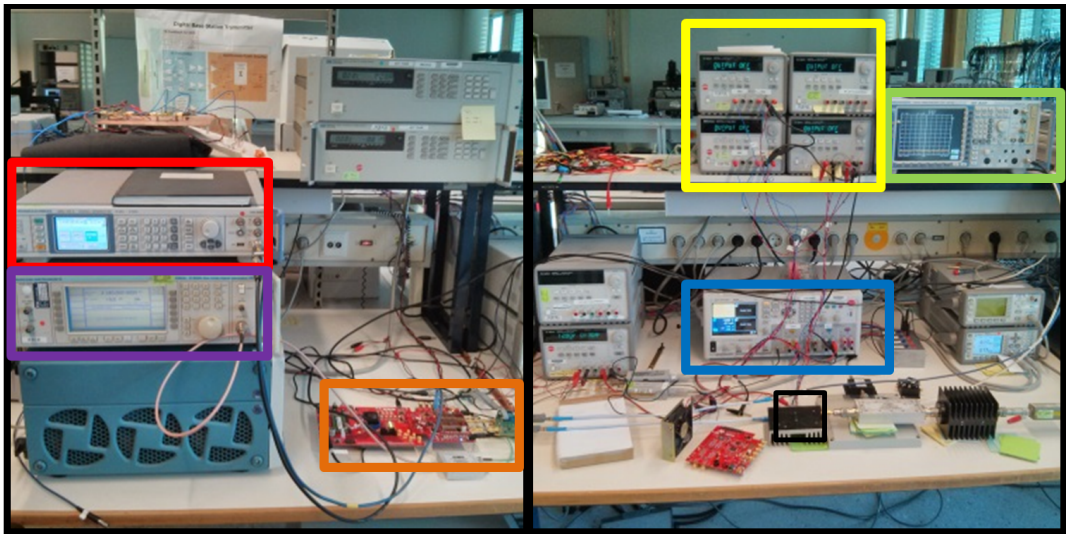


Figure 4.5: Signal generation and capture test bench set-up. Red - transmitter LO. Purple - DAC and ADC clock generator. Orange - TX signal generation. Yellow - CMOS power supply's. Blue - GaN finial stage power supply. Green - Spectral analyser and ADC.

Local oscillator generation is carried out using Agilent E4438B signal generators. To ensure that the signal generation was capable of wide band cancellation an identical signal was output from each channel. An individual LO was supplied to each, by modifying the phase on each LO the signals could be cancelled. The signal generation board demonstrated greater than 300 MHz cancellation bandwidth.

All signal generation, signal capture and support equipment is clocked using a common 10 MHz reference from the FSQ. An array of power supplies are required for the digital driver stage and final amplification stages. In both cases Agilent power supplies are used, the digital drivers use 4 E3600's and the final GaN power stage requires an N6700 Aglient power supply for higher currents at a drain voltage of 28V.

4.1.4.1 Calibration

Calibration is carried out before the device under test is added to the system, a Wilkinson power combiner is used to simulate linear recombination enabling outphasing gain and phase angle to be calibrated. The combiner is fully characterised using a VNA and the results are presented in Figure 4.6. This analysis demonstrates that each input has a linear relationship in gain and phase across our band of interest to the output. Referencing the systems outphasing characteristics to this combiner of a similar component will provide a highly calibrated input

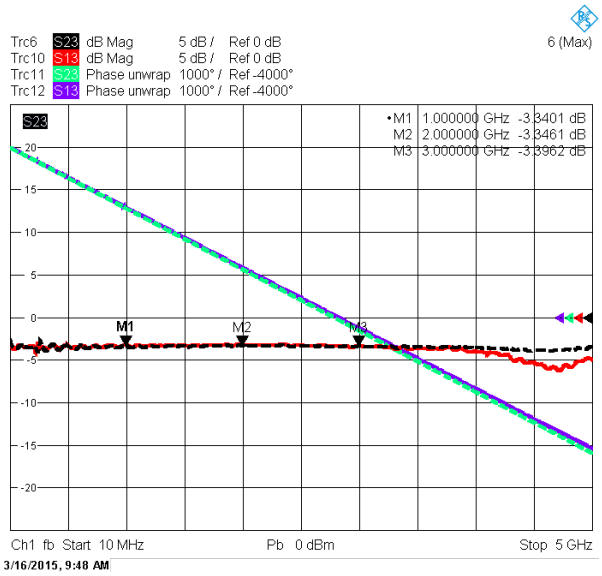


Figure 4.6: A isolating Wilkinson power combiner is used during calibration. The combiner structure is robust to frequency dependent variations to gain and phase.

to the amplification system. As outlined in Section 3.4 various system imbalances must be calculated and corrected for in order to achieve linear outphasing recombination. Using a single tone signal at a predetermined intermediate frequency a series of measurements are carried out until the mismatches have been reduced to a predefined threshold. These mismatches include quadrature mismatch, local oscillator feed through and outphasing gain and phase mismatch. The resulting correction factors are saved, and will be applied to any future outphasing test signals. Calibration must be carried out whenever key system parameters are changed, for example operating frequency and output power. An overview of the digital correction scheme is presented in Figure 4.7, where section A the digital correction is applied to the small signal generation and the system amplifiers, providing the DUT with balanced and linear input signals. Section B applies digital pre-distortion to the system as a whole, it mainly targets the non-linearity introduced by the amplifier module, however it will also try to remove any residual distortion from the signal generation system.

4.1.4.2 Equalisation

Equalisation is a digital signal process where the frequency imbalance within a channel or system is alleviated. The outphasing signal generation and amplification system requires identical components in both paths in order to achieve linear amplification. However

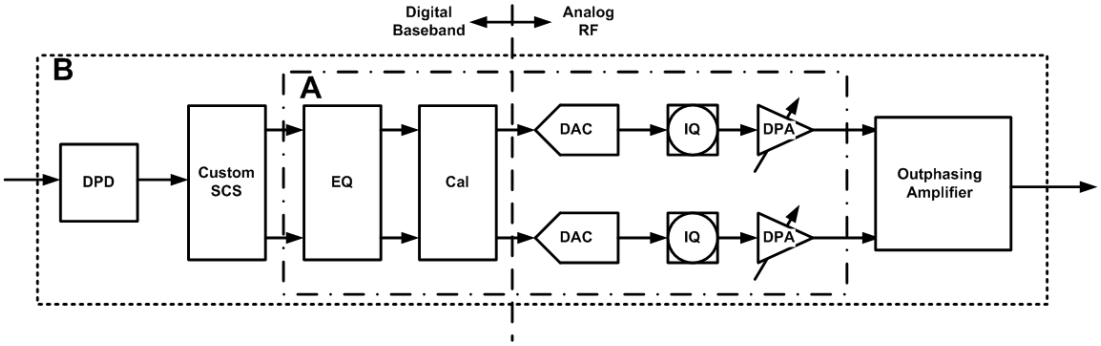


Figure 4.7: Layout of the digital correction applied to the outphasing signals. There are two distinct regions outlined.

due to manufacturing tolerances this is not practical. By using channel equalisation we can characterise the channels and reduce the frequency dependent effects, creating ideal channel pairs. Each channel is characterised using a multi-tone signal, amplitude effects are characterised on a channel by channel basis. The outphasing angle also varies with frequency. Again using a multi-tone signal and a sweep of outphasing angles the relative phase change compared to the center frequency can be determined.

From the characterised channels, the inverse channel correction function can be derived. In a practical system equalisation can be preformed using a filtering function, however in a test bench greater degrees of freedom can be employed. An ideal channel correction was chosen to be implemented using a Fourier transform to convert the time domain signal to the frequency domain. The correction is then applied before the inverse Fourier transform returns the signal to the time domain. With this approach, we obtain an ideal frequency independent dual path transmission system to present to the device under test, ensuring any non-linear effects are only as a result of the device itself.

4.1.4.3 Small signal outphasing performance

Once fully calibrated and characterised the performance of the small signal is checked with a linear isolating power combiner. The combiner is characterised to find the maximum and minimum output power outphasing angles, from this an outphasing LUT can be derived. Using a wide band WCDMA signal the system performance is evaluated. This ensures that the amplifier inputs are fully calibrated and the DUT is the only component being calibrated. The performance of the small signal outphasing system is demonstrated in Figure 4.8. This

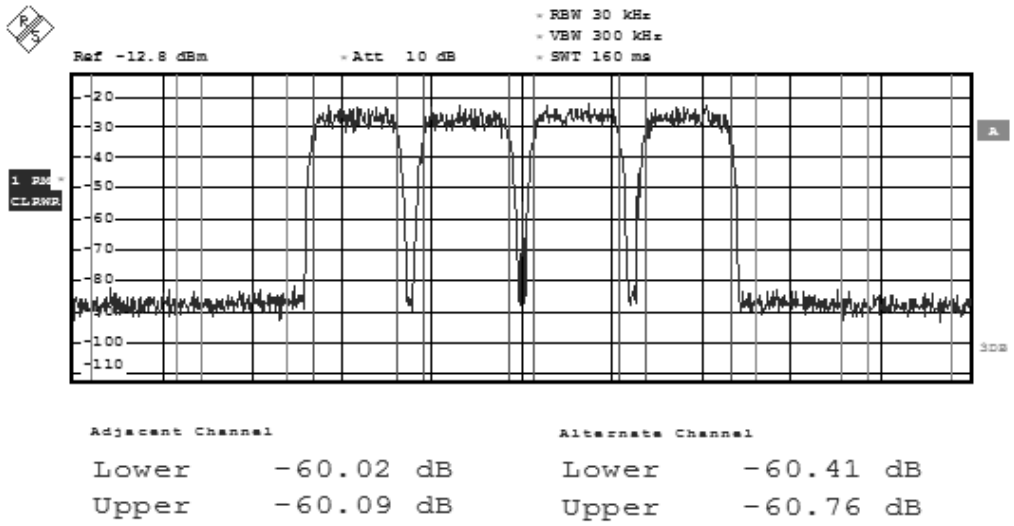


Figure 4.8: Calibrated small signal outphasing performance, approximately -60dBc ACPR performance.

demonstrates that the test-bench is capable of linear outphasing, a 20 MHz modulated signal that can achieve a SNR of 60 dBc. Therefore any non-linear amplitude or frequency effects which will be measured during dynamic amplification can be attributed to the DUT alone.

4.1.5 Characterisation of device under test

As with all amplifier architectures, amplifier characterisation is an important process in determining the operating range for output power, efficiency, bandwidth and stability. It is common practice to present the output power as a function of the input power, as demonstrated in Section 3.1.3. The output power for an outphasing PA's is also a function of the outphasing angle between the input signals. Load compensation dramatically increases amplifier efficiency in back off. This behaviour however, is not symmetric about the nulling outphasing angle. Figure 4.9 is a simulation of the power combiner and demonstrates this asymmetry, in this example higher back off efficiency is achieved by using the outphasing angles between 0 and 180 degrees. The range of angles in which efficient operation occurs is dependent on amplifier design and system configuration. However the relationship is predetermined and can be identified. Efficiency characterisation is necessary to verify the operation of the design, it also gives confirmation of the most efficient outphasing angles.

As described in Section 3.4.1 the Chireix combiner relationship between outphasing angle

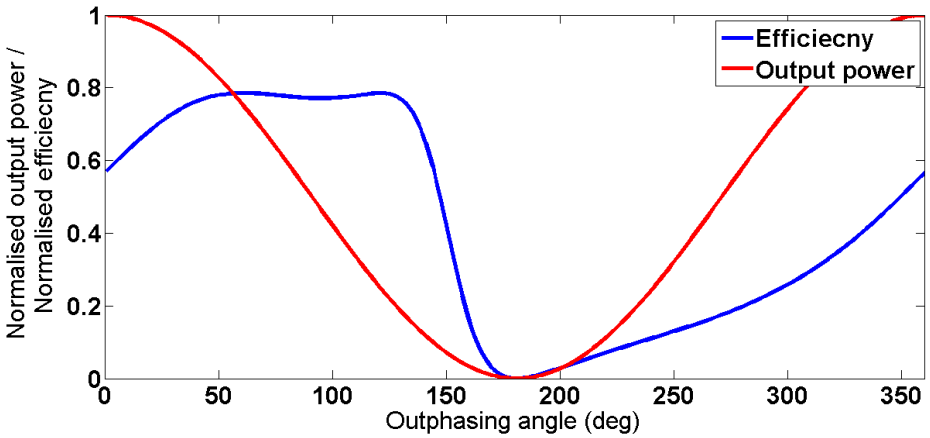


Figure 4.9: Simulated efficiency and normalised output power verses outphasing angle.

and output power cannot be described by a trigonometric function in practice. To determine the optimum outphasing function to use in the signal component separator. The outphasing angle is swept, the resulting power sweep determines the angle at which maximum and minimum output power occurs, and therefore the system dynamic range. This information can in turn be used in the signal component separator to achieve optimum linear operation.

4.2 Measurements

A set of measurements from a practical outphasing system were required in order to verify the performance of the proposed system. A digital outphasing amplifier produced by NXP [29], the topology of which is outlined in Figure 4.10, was chosen for evaluation. The module consists of a novel digital driver amplification circuit in conjunction with final stage GaN amplifiers. The module consists of a pair of GaN Class E PA's with a novel transformer based Chireix combiner, designed for wideband operation. A digital drive signal is provided by a pair of CMOS driver stages. The amplifier produces a 19W peak output power greater than 70% drain efficiency and up to 65% drain efficiency at 10 dB power back off. Total system gain is 24 dB.

The DUT is tunable across frequency through bias control on the input driver stage. The amplifier is tuned for maximum dynamic range at 2140 MHz. A look up table is generated for the signal component separator, mapping the input signal amplitude to outphasing angle, ensuring maximum dynamic range is achieved during operation. The system is equalised and calibrated to provide the DUT with amplitude and phase balanced inputs across frequency.

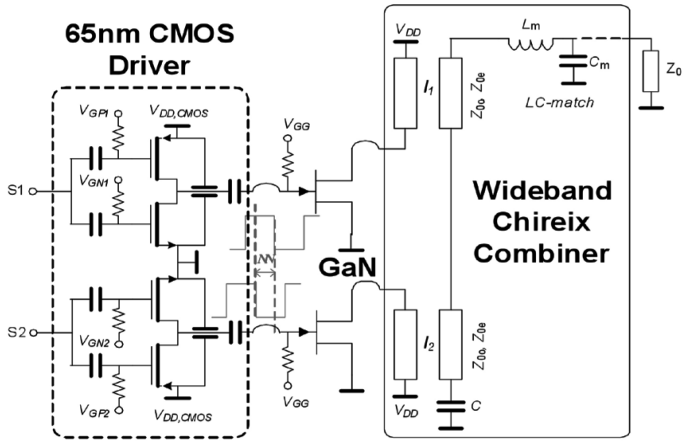


Figure 4.10: NXP Digital outphasing module.

The aim of calibration and equalisation is to ensure the non-linear effects measured are only associated with the DUT and its effect on the system components.

For completeness the stimulus signals applied to the amplifier must conform to current modulation standards. The system is evaluated with wideband code division multiple access (WCDMA) signals, commonly associated with the 3GPP standard [37]. The signals are generated using Agilents Advanced Design Systems (ADS) software, the Ptolomey simulator incorporates signal generation blocks for 3GPP standards for both base station and handset signals. The WCDMA standard utilises a maximum channel bandwidth of 5 MHz, our objective is to analyse the wideband performance of the outphasing amplifier and subsequently developed wideband behavioural models. Therefore a multi-carrier signal is generated combining four base station signals into a single complex signal occupying 20 MHz bandwidth.

The resulting test signal requires some signal conditioning before it can be applied to the amplifier; firstly crest factor reduction is applied, reducing the peak to average power ratio (PAPR): secondly the signal must be conditioned to be cyclical in order to remove the possibility of large discontinuities being introduced to the amplifier. The concept of crest factor reduction is outlined in Section 2.7.1. It was initially developed to reduce the impact of operating the amplifier in a saturated state, but is now a de-facto requirement for efficient operation of modern power amplifiers. As such it must be introduced in order to achieve a representative real world test signal. Doing so reduced the multi carrier signals PAPR from 12.9 dB to 9.8 dB. The test signal is of finite length. In a test system it will experience wrapping as

the signal is continuously streamed out to the amplifier during characterisation and evaluation. Using a windowing process the amplitude of both the real and imaginary components are aligned. Measurements were taken for single and quad carrier WCDMA signals, these signals will be used to evaluate behavioural model performance. The data sets are split into training and test vectors. The training and test vectors have similar characteristics but are independent.

The resulting spectrum for an amplified four carrier WCDMA signal can be seen in Figure 4.11. In Figure 4.12 the input amplitude verses output amplitude (AMAM) and input amplitude verses input-output phase difference (AMPM) are plotted to demonstrate the regions of non-linearity. The spectrum in Figure 4.11 contains significant out of band noise, this is a combination of amplifier non-linearity and memory effects. Memory effects are a result of dynamic operation of the amplifier. In traditional amplifiers this is due to parasitics within the device or biasing networks at high output powers. In an outphasing topology they result from path mismatch. Given the relationship between amplitude and phase in the Chireix combiner the effects are most sensitive at lower output powers. From the AMAM-AMPM plot this is evident, a large proportion of the non-linearity resides at low output powers, as demonstrated in Figure 4.12. The output is relatively linear at higher output powers however at lower output powers non-linear distortion is mainly a memory effect indicated by the spreading in both the AMAM AMPM curves. There is additional phase distortion in the AMPM curve at low power which is not as strong at higher output powers. This is typically the inverse of standard amplifier topologies where memory and polynomial distortion is strongest at higher output powers.

4.2.1 Model performance

Section 2.5 presented an overview of many modelling techniques which can describe the non-linear effects of traditional power amplifier architectures. The Volterra series is the most comprehensive memory capable model, capable of individual non-linear terms for each memory taps as well as all possible cross product combinations as outlined in Section 2.5.2.4. Here it is used as a bench mark in determining model performance before more computationally efficient implementations are considered.

The models are generated for a 245.66 Msps sample rate. The evaluation includes mean squared error in equation 4.1 and normalised mean squared error in equation 4.2 as figures of

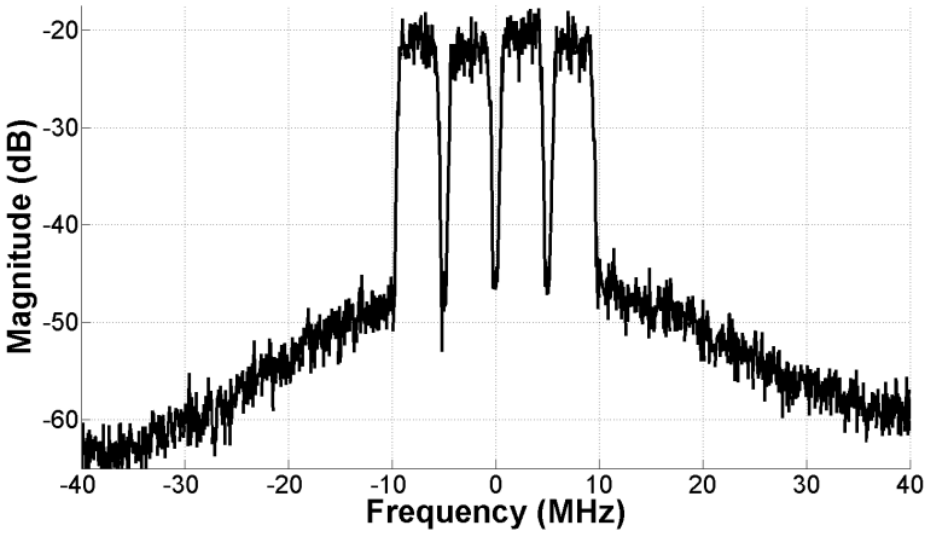


Figure 4.11: NXP Digital outphasing module non-linearity spectrum.

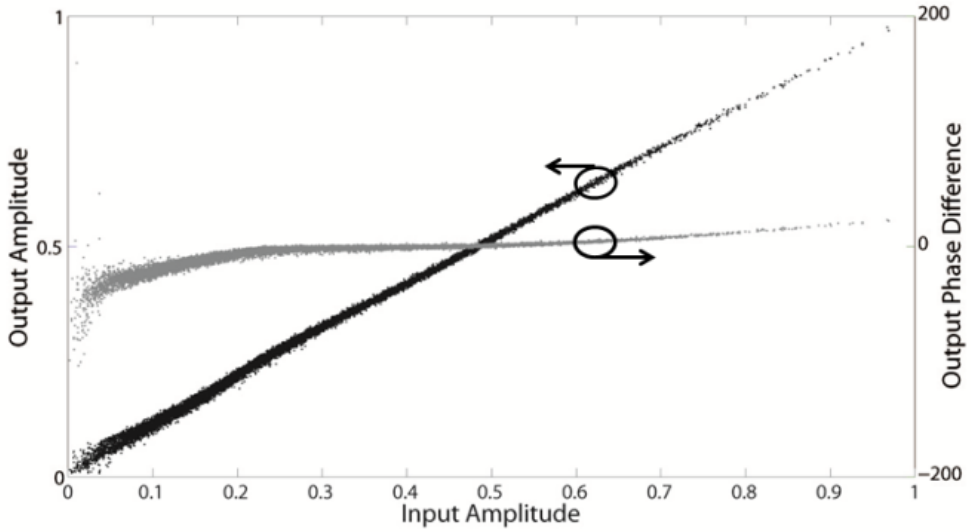


Figure 4.12: NXP Digital outphasing module non-linearity AMAM - AMPM.

merit. Additionally the spectral characteristics are also examined.

$$MSE = \frac{1}{n}\sum_{n}^{t=1} |\hat{y}(t) - y(t)|^2 \tag{4.1}$$

$$NMSE = \frac{1}{n}\sum_{n}^{t=1} \frac{|\hat{y}(t) - y(t)|^2}{|\hat{y}(t)|^2} \tag{4.2}$$

4.2.2 Single input - single output characterisation

Single input - single output non-linear functions, presented in Section 2.5, are commonly used to characterise classical amplifier topologies. As such they were also applied in this work to outphasing amplifier structures. In [114] the author performs an analysis on an ideal Chireix combiner structure. Using simulations it is shown that the load modulation deviates from ideal operation when the amplifiers are introduced as replacements for ideal voltage sources. The resulting non-linear behaviour is then modelled using a single input-output Weiner model as introduced in Section 2.5.2.2. It has been demonstrated in [115] that the reflection coefficient of the combiner inputs is an important analytical parameter. Furthermore the reflection coefficient will increase as the frequency of operation deviates from the designed centre frequency, resulting in a tangible memory effect within the amplifier. The outphasing topology will therefore require a non-linear, memory capable model to fully characterise its behaviour.

The Volterra time series is a single input - single output model, for the outphasing amplifier the input prior to signal component separator is used. While simplifying the implementation, this also limits the ability of the model to account for some elements of path mismatch. It was not obvious from the measurements the required model order or number of memory taps required, therefore these system parameters were swept in order to find the optimum model performance. The models parameters are extracted in an off-line process using the least squares algorithm discussed in Section 2.6.1. The results are presented in Figure 4.13, the model required 7th order non-linear terms and three memory taps to achieve an NMSE of -26dB.

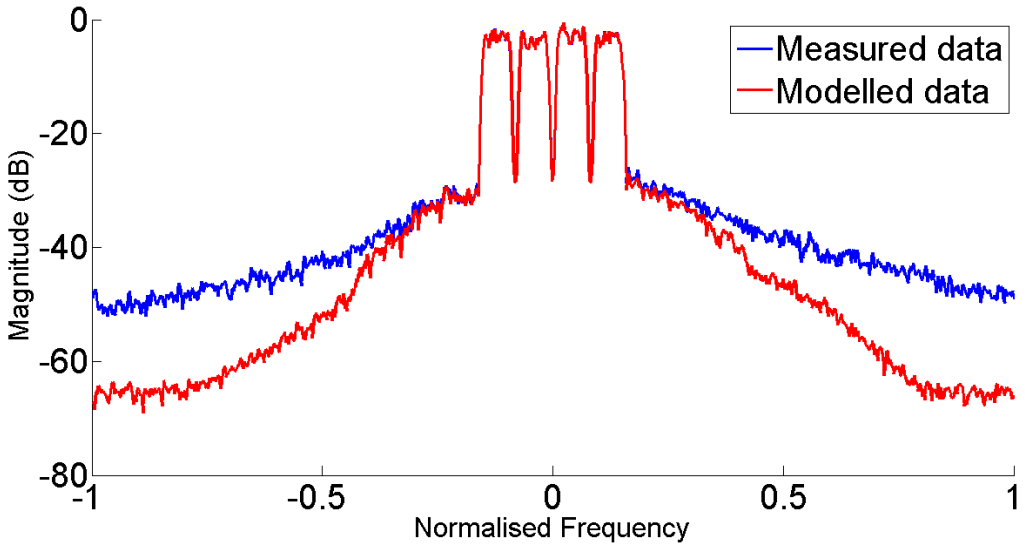


Figure 4.13: Modelling results for the Volterra model - MSE of -38 dB, NMSE of -26 dB

4.2.3 Outphasing angle characterisation

In [116] the amplifier is characterised through a series of measurements. Using outphasing angle sweeps of 1 degree across the operating bandwidth $\pm 20MHz$ a frequency dependent LUT is built up. The results are then processed and a modified signal component separator function is extracted, with amplitude, phase and frequency as inputs. This method is inherently capable of modelling both non-linear and memory effects of the amplifier of infinite order making it extremely flexible. However the method cannot be easily described mathematically and as such the only extraction method is through measurement process, requiring off-line updating. An illustration of a simulated Chireix combiner characterisation is presented in Figure 4.14, the combiner was evaluated in 20 MHz steps either side of the designed combiner centre frequency. The deepest notch and most ideal phase change represent the centre frequency. The combiners performance deviates as we move away from the centre frequency.

4.2.4 Direct model characterisation

In [100] a phase polynomial for each outphasing path is derived, characterizing the amplitude and phase distortion of the amplification system. The amplifier model is described in equation 4.3. where the amplitude imbalance between the outphasing paths is described by the gain terms g_1 and g_2. Distortion in the amplifier is described by a non-linear outphasing

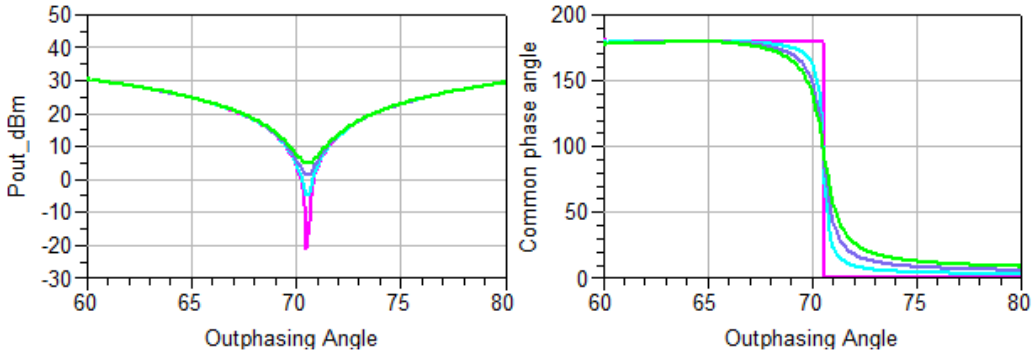


Figure 4.14: Characterisation of Chireix combiner over 100MHz bandwidth. The amplitude and phase deviations are symmetric about the centre frequency.

angle function, a phase polynomial based upon the outphasing angle, it is defined using $p(\eta_i, \Delta\Psi(s_1, s_2))$ where $\Delta\Psi(s_1, s_2)$ is the outphasing angle and η_i are the coefficients of the polynomial.

$$y'(t,\theta) = g_1 s_1(t) e^{jp(\eta_1, \Delta\Psi(s_1,s_2))} + g_2 s_2(t) e^{jp(\eta_2, \Delta\Psi(s_1,s_2))} \tag{4.3}$$

This work is expanded upon in what is referred to as a direct outphasing model [117], a dynamic gain function replaces the static gain parameters g_1 and g_2, and a static time delay parameter τ for each channel is added. The direct outphasing model is presented in equation 4.4 where λ_i is the coefficients of the amplitude correction function. The model accounts for not only the non-linear function of the amplifier, more specifically the combiner stage, it can also model the effects of path mismatch in both the amplifier and system using the zero order terms of the phase and amplitude polynomial functions and the static path mismatch coefficient.

$$\begin{aligned} y'(t,\theta) = {} & g_1(s(t-\tau_1);\lambda_1)(t) e^{jp(s(t-\tau_1);\eta_1)} s_1(t-\tau_1) + \\ & g_2(s(t-\tau_2);\lambda_2)(t) e^{jp(s(t-\tau_2);\eta_2)} s_1(t-\tau_2) \end{aligned} \tag{4.4}$$

The model is derived in a series of steps. First the gain function of the system is initialised. Assuming that the phase distortion is set to zero and the amplitude functions are linear the coefficients can be found by solving the linear least squares problem. An example of which is

outlined in equation 4.5 where the amplitude function is set to constant values.

$$y = [s_1 s_2] \left[\frac{g_1}{g_2} \right] \tag{4.5}$$

Using the extracted gain parameters the modified outphasing signals can be extracted using equations 4.6 and 4.7.

$$\hat{y_1}(t) = \frac{y(t) - g_2(s(t); \lambda_2) s_2(t)}{g_1(s(t); \lambda_1)} \tag{4.6}$$

$$\hat{y_2}(t) = \frac{y(t) - g_1(s(t); \lambda_1) s_1(t)}{g_2(s(t); \lambda_2)} \tag{4.7}$$

The residual error in the signal is now determined to be a function of the phase difference between $\hat{y_i}(t)$ and $s_i(t)$. This difference is approximated by the phase polynomial p_i which is approximated by solving equation 4.8.

$$\sum_{n=0}^{N-1} | \left[\angle \hat{y_i}(t) - \angle s_i(t) \right] - p_i(s(t); \lambda_i) |^2 \tag{4.8}$$

Finally the delay parameter is set to zero and the final values for the coefficients η_i, λ_i and τ_i are found using an optimisation search. The precise optimisation function is not described in the publication, therefore the genetic algorithm was chosen [118]. It is a robust evolutionary search algorithm that mitigates the issue of local minimum solutions through continuous genetic mutation, forcing the search to deviate from the current optimum solution.

The direct model is chosen to have a total of 16 coefficients, each path has a single gain coefficient, a single time delay coefficient and six coefficients for the phase polynomial. Training is carried out as outlined in Section 4.2.4, where the initial system parameters are derived form inversion of the output signal and the outphasing signal. The final optimisation is carried out using a genetic algorithm, the model is then refined over 500 epochs of the genetic algorithm resulting in a final model NMSE of -28 dB. The spectral characteristics are presented in Figure 4.15 for this approach.

The direct outphasing model presents a non-convex optimisation problem [117], as such there exists many local minima within the feature space of possible solutions. The optimisation of this problem must be robust enough to evaluate a local minimum and where required provide

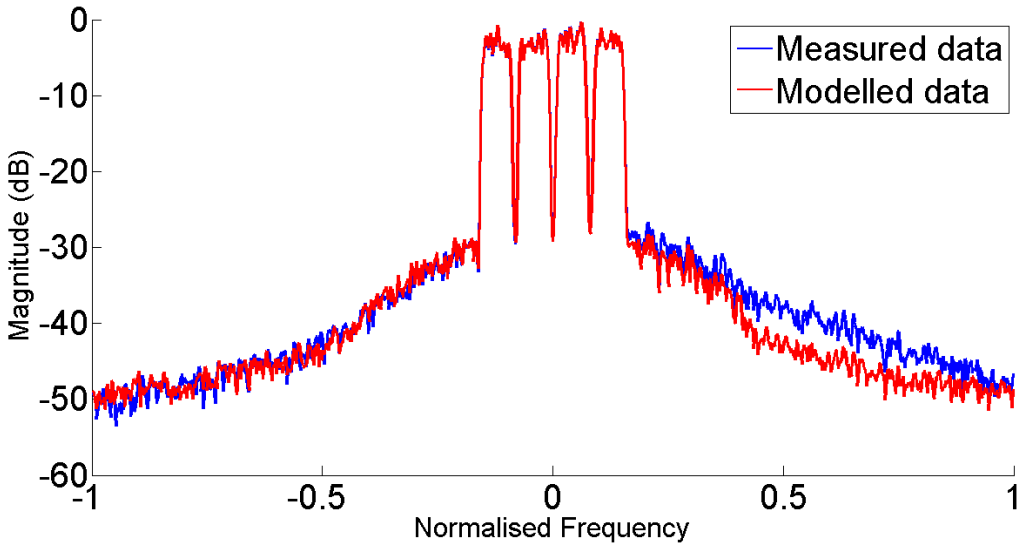


Figure 4.15: Modelling results for the direct outphasing model - MSE of -41 dB, NMSE of -28 dB

enough diversity in proposed solutions to exit the region and evaluate alternative possible minimisation regions. In the case of the direct model the chromosomes are the coefficients of the model. For a bounded mathematical problem a cost function is required in order to evaluate the population. The optimum solution is one that minimises the error in the cost function. The cost function used for parameter optimisation in the direct outphasing model is a function of the error between the measured signal $y(t)$ and the output of the model $\hat{y}(t)$. The normalised mean squared error function is outlined in equation 4.2, and provides a numerical figure of merit upon which the performance of each individual can be determined.

4.2.5 Amplitude model characterisation

Modelling the frequency dependent effects of the outphasing power amplifier can be challenging. The relationship between the non-linear effects at the output and the in channel memory effects is not always direct and therefore can be difficult to model. In [84] the authors present a model developed to characterise the non-linear effects of the outphasing amplifier based upon the signal amplitude. The authors choose the model formed in equation 4.9 as it forms a convex optimisation problem, which can be trained directly. This is in comparison to an amplitude and phase model which will result in an non-convex optimisation problem due to the presence of the exponential function for phase in a complex signal. The individual time series functions

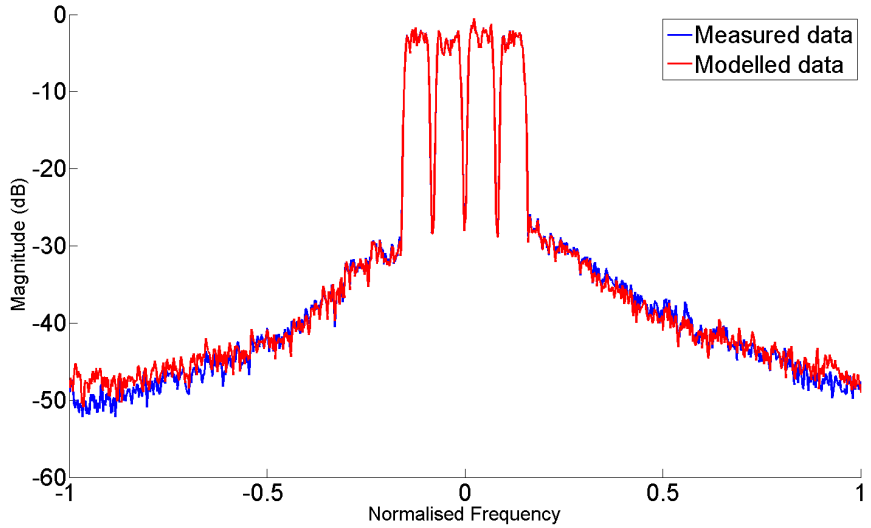


Figure 4.16: Modelling results for the amplitude distortion outphasing model - MSE of -43 dB, NMSE of -31.5 dB

for g_1 and g_2 are outlined in equation 4.10. The model comprised of the outphasing signals s_i and the input signal before outphasing decomposition $s(n)$. The model is comprised similar to a parallel Hammerstein function with the presence of linear and non-linear memory functions.

$$\hat{y_2}(t) = g_1(s(n);\lambda_1)s_1(n) + g_2(s(n);\lambda_1)s_2(n) \tag{4.9}$$

$$g_i(s(n);\lambda_i) = \sum_{m=0}^{M_{lin}} \lambda_{i,0,m} s_i(n-m) + \sum_{p=1}^{P} \sum_{m=1}^{M_{nonlin}} \lambda_{i,p,m} s_i(n-m) \mid s(n-m) \mid^p \tag{4.10}$$

4.2.6 Modelling Performance

The performance of existing behavioural models are summarised in table 4.1. The models which were suitable for off-line behavioural modelling were evaluated and compared, the outphasing look up table method outlined in Section 4.2.3 requires static sweeps therefore it is omitted due to implementation issues. The direct outphasing and amplitude distortion models provide the best characterisation performance and offer comparable flexibility to standard behavioural modelling methods, the Volterra series for example.

Ultimately the goal is to find a non-linear algorithm which can accurately characterise and linearise a digital outphasing amplifier. Of the models presented in this chapter the Volterra

Table 4.1: Power amplifier behavioural model performance compared

Model	Order	Memory depth	Number of coefficients	MSE	NMSE
Direct Model	6	NA	16	-41 dB	-28 dB
Amplitude distortion Model	6	[1Mlin, 4Mnon-lin]	50	-43 dB	-31.5 dB
Volterra	7	3	70	-39 dB	-26 dB

series and the direct outphasing models are possible solutions however additional performance is required. The most accurate model the amplitude distortion algorithm is only capable of modelling in its current form. This is due to the fact that the modified signals S1 and S2 have both amplitude and phase information encoded onto them. For the saturated and digital outphasing amplifier the amplitude information will be striped from the input signal, impacting the algorithms performance, and system efficiency. Therefore further investigation into outphasing behavioural models is required, using the results from Table 4.1 algorithms that provide increased accuracy can be identified and subsequently analysed for linearisation performance.

4.3 Conclusion

The outphasing system developed for wide-band signal generation was successful and is capable of linear recombination of 20 MHz communications signals when analysed with a linear power combiner. This is made possible through a combination of wide-band signal generation and robust calibration and equalisation techniques. The proposed system will ensure that the amplifier will be the only component in the system to be under test. As a result the system non-linearities can be attributed solely to the amplifier. Therefore it can be said that the models presented in Section 4.2.1 are behavioural models of the outphasing amplifier and do not include elements of non-ideal system behaviour. This is an important distinction and enables the behavioural model to evaluate modifications to the outphasing signal generation set-up.

A thorough comparison of outphasing amplifier behavioural modelling is carried out in Section 4.2.1. The models are capable of characterising the outphasing amplifier to a

certain extent however for wide band linearisation further advances are required, namely the development of a memory capable linearisation algorithm. The amplitude distortion behavioural model utilizes linear and non-linear memory to provide the most accurate characterisation of the amplifier. However due to altering the outphasing signals amplitude it cannot be used as a linearisation algorithm for the digital outphasing power amplifier. The direct outphasing model is the next most accurate model however its performance will need to be improved upon for wideband linearisation.

The following chapter will investigate several behavioural models capable of characterising the outphasing power amplifier, with the aim of identifying a subset that are suitable for implementing linearisation.

CHAPTER 5

Behavioural Model Development for Outphasing Systems

5.1 Introduction

Behavioural modelling of RF systems greatly reduces the computational complexity when compared with traditional transient or harmonic balance solvers. An outphasing amplifier can be thought of more as a system than a traditional amplifier block as there are multiple components. As such the computational effort required to model this system is substantial. Furthermore as described in the previous chapter current outphasing amplifier behavioural models are only suitable for narrow band or single carrier signals of the current generation modulation schemes. This chapter explores model development for outphasing systems, using measured data to evaluate and verify the algorithms. The performance of novel dual input models as well as advanced techniques to enhance single input models are evaluated. The aim is to improve the accuracy of the modelling techniques for a 20 MHz quad carrier WCDMA signal when compared with existing outphasing models presented in Chapter 4.

In this chapter two approaches are outlined to achieve this. The outphasing amplification system is a two path structure, analysis in Section 4.2.1 demonstrates that of existing behavioural models the multi - input configuration offers the best performance. This approach is extended using both a Volterra series and a neural network method, capable of being

structured in a similar configuration to the physical amplification system, to examine alternative models for a more accurate solution.

Single input - single output models can describe some of the non-linear effects, as demonstrated with the characterisation using the Volterra series in the previous chapter. However as the outphasing power amplifier experiences both continuous and discontinuous non-linear behaviour standard models have difficulty describing this behaviour accurately. In this chapter segmented non-linear time series is investigated as a method to enable single - input single output models to accurately describe the operation of the outphasing power amplifier.

5.2 Dual path memory models

The analysis of existing behavioural models for outphasing PA's has indicated that a multi input model has added benefits for characterising the non-linear effects associated with outphasing technology. The direct outphasing model requires an individual parameter for each non-linear effect associated with the amplifier. This simplifies the modelling structure however generality is lost, as each effect must be directly described. This section will evaluate two time series models, similar to the amplitude distortion model in the previous chapter. The aim is to accurately describe the outphasing effects as well as the memory effects which can arise. First a two path implementation of the classical Volterra series is presented, derived from continuous time implementation. A variety of neural network structures are also presented modified for multiple inputs and to more closely resemble the outphasing structure. Both have been successful when modelling single input single output power amplifier structures.

Dual path models receive the decomposed outphasing signals as the inputs to the models. As outlined in the measurement set up the output combiner of the outphasing amplifier is fully characterised. The main purpose is to ensure maximum dynamic range during modulated operation, however as the input - output characteristics are linearly mapped an ideal decomposition and recombination can be used for modelling purposes, reducing the overall complexity.

An important aspect in the operation of outphasing amplifiers, and even more so when a Chireix topology is concerned, is the interference between the individual amplification paths before the recombination process. There are two aspects which must be examined: when the

high power devices are operating in close proximity to one another this may result in some non-linear cross products; the reflections between the output of the combiner and the load will generate non-linear memory products in the output signal. In both of these cases the products which are not a function of the current input signal will effect the output, and must be taken into account.

5.2.1 Dual Path Volterra

The standard single input - single output Volterra model is introduced in Section 2.5.2.4 and analysed in Section 4.2.1. The Volterra series has been successfully applied to modelling biological and financial applications and more recently to power amplifiers. The previous chapter demonstrated the benefit of multiple input behavioural modelling of outphasing amplifiers, therefore it is logical to try to extend current non-linear models for multiple input capability to further increase modelling accuracy. In [119] the author presents a multiple input model based upon a modification of the Weiner non-linear model. The author outlines the continuous time Weiner function for the first three kernels where $x(t)$ is the input signal and $y(t)$ is the output signal.

$$y(t) = \sum_{n=0}^{\infty} G_n[h_n, x(t)] \tag{5.1}$$

where the first three terms in the series are:

$$G_0[h_0, x(t)] = h_0 \tag{5.2}$$

$$G_1[h_1, x(t)] = \int_0^{\infty} h_1(\tau)x(t-\tau)d\tau \tag{5.3}$$

$$G_2[h_2, x(t)] = \int \int_0^{\infty} h_2(\tau_1, \tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_2 - P\int_0^{\infty} h_2(\tau, \tau)d\tau \tag{5.4}$$

Adding an additional input *u(t)* to the single input system in equation 5.1 we develop a

mutli-input model as follows.

$$y(t) = \sum_{n=0}^{\infty} G_n[\{h\}_n, x(t), u(t)] \tag{5.5}$$

where the first three terms in the series are:

$$G_0[\{h\}_0, x(t), u(t)] = h_0 \tag{5.6}$$

$$G_1[\{h\}_1, x(t), u(t)] = \int_0^{\infty} h_{1x}(\tau)x(t-\tau)d\tau + \int_0^{\infty} h_{1u}(\tau)u(t-\tau)d\tau \tag{5.7}$$

$$\begin{aligned} G_2[\{h\}_2, x(t), u(t)] = &\int\int_0^{\infty} h_{2xx}(\tau_1, \tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_2 - P_x \int_0^{\infty} h_{2xx}(\tau, \tau)d\tau \\ &+ \int\int_0^{\infty} h_{2uu}(\tau_1, \tau_2)u(t-\tau_1)u(t-\tau_2)d\tau_1 d\tau_2 - P_u \int_0^{\infty} h_2(\tau, \tau)d\tau \\ &+ \int\int_0^{\infty} h_{2xu}(\tau_1, \tau_2)x(t-\tau_1)u(t-\tau_2)d\tau_1 d\tau_2 \end{aligned} \tag{5.8}$$

Analysing the Weiner expansion from a single input - single output model to a multiple input signal output model, a distinct model structure appears. Breaking the expansion in equation 5.5 down it contains the Weiner series, equation 5.1 for $x(t)$ and $u(t)$ plus an additional set of terms, a function which contains the cross terms between *x(t)* and *u(t)*, $\int\int_0^{\infty} h_{2xu}(\tau_1, \tau_2)x(t-\tau_1)u(t-\tau_2)d\tau_1 d\tau_2$. Rewriting equation 5.5 using single path Weiner series it can be rearranged as:

$$y(t) = \sum_{n=0}^{\infty} G_n[h_n, x(t)] + G_n[h_n, u(t)] + G_{n-1}[h_{n-1}, x(t)u(t)] \tag{5.9}$$

Replacing the Weiner series in equation 5.9 with the discrete time Volterra outlined in 2.34 a two path discrete time Volterra series is formed in equation 5.10, where $h_{k,m}$ represents the Volterra kernel for k non-linear order and m the number of memory taps. The discrete form of the Volterra series can then be applied to the baseband time domain signals captured from the

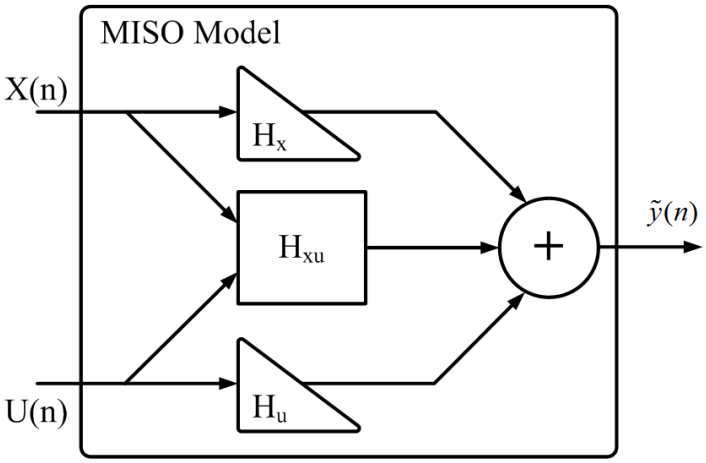


Figure 5.1: Configuration of MISO model

power amplifier.

$$y(n) = \sum_{k}\sum_{m} h_{k,m}x(n) + \sum_{k}\sum_{m} h_{k,m}u(n) + \sum_{k}\sum_{m} h_{k-1,m-1}[x(n), u(n)] \tag{5.10}$$

The layout of the model is represented in Figure 5.1 where the kernels for $x(n)$ and $u(n)$ are represented by a triangular matrix, while the cross terms of $[x(n), u(n)]$ is a square matrix. Some work has been carried out on multi input - single output Volterra for power amplifier structures for both Doherty amplifiers and envelope tracking amplifiers. The capabilities of a non-linear time series, in this case Volterra series, have been extended. A full Volterra kernel is present in each path and non-linear cross interaction between the individual input paths is also accounted for. As described in Section 3.1.3, each amplifier interacts with the load to construct an output signal.

The model is implemented as described in equation 5.10, once the kernels are extracted the least squares function is used to extract the estimation of the coefficients in all three sections at once. The computational complexity of the two path Volterra is on average between 2.5-3 times greater than a single Volterra series for a given order and number of memory taps. As stated in [120] the number of inputs is not limited to a two path system, however the number of computations in the model increases dramatically as the number of inputs are increased. Care must be taken to strike a balance between computational complexity and model performance. As with the standard Volterra series it is not immediately evident what non-linear order or the number of memory taps is required. A search routine can be used and the performance of the

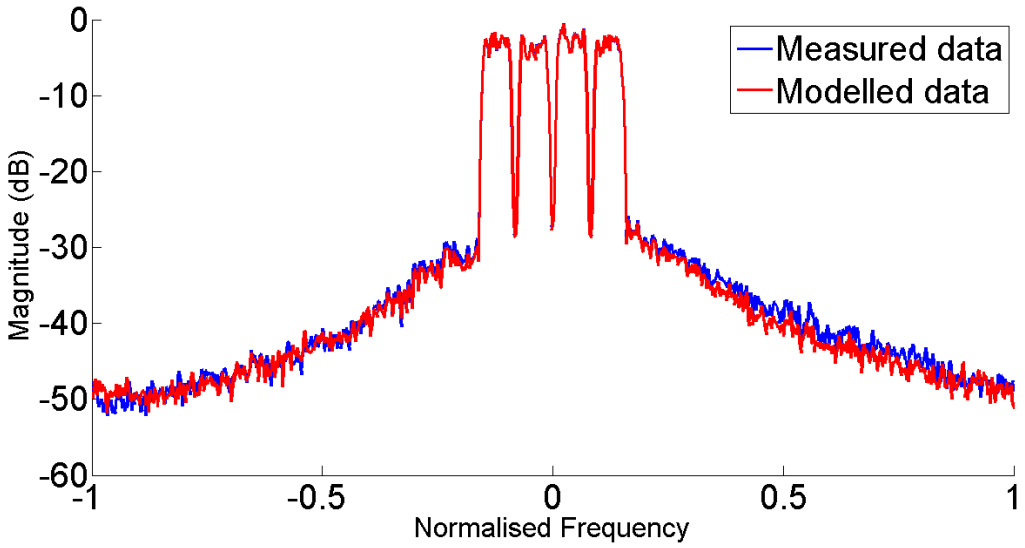


Figure 5.2: Modelling results for the two path Volterra model - MSE of -44 dB, NMSE of -31 dB

model is evaluated to find the optimal solutions. The results for the two path Volterra model are presented in Figure 5.2

5.2.2 Neural Networks

Artificial neural networks, introduced in section 2.5.2.6, are capable of universal approximation of both linear and non-linear systems. The time delay neural networks are capable of modelling non-linear systems with memory effects. Neural network functions only operate on real value signals. However modern communications signals are complex, therefore a two input neural network model is developed in [121]. To capture the real and imaginary parts the rectangular form of the complex signal is used as model inputs and outputs, the complex signal is presented in equation 5.11 and the real and imaginary values are presented in equations 5.12 and 5.13. Therefore the new model is referred to as the real value time delay neural network (RVTDNN). This model is outlined in equations 5.14 and 5.15 where O_i^{ol} is the output of the output neuron i, w_{ji}^1 are the weights of the layer l from neuron i and $w_{j0}^1 = b_j^1$ are the bias values of the layer l from neuron i. This network is a feed forward network with a linear activation function in the output layer, the input and hidden layer have a tangential sigmoid non-linear activation function

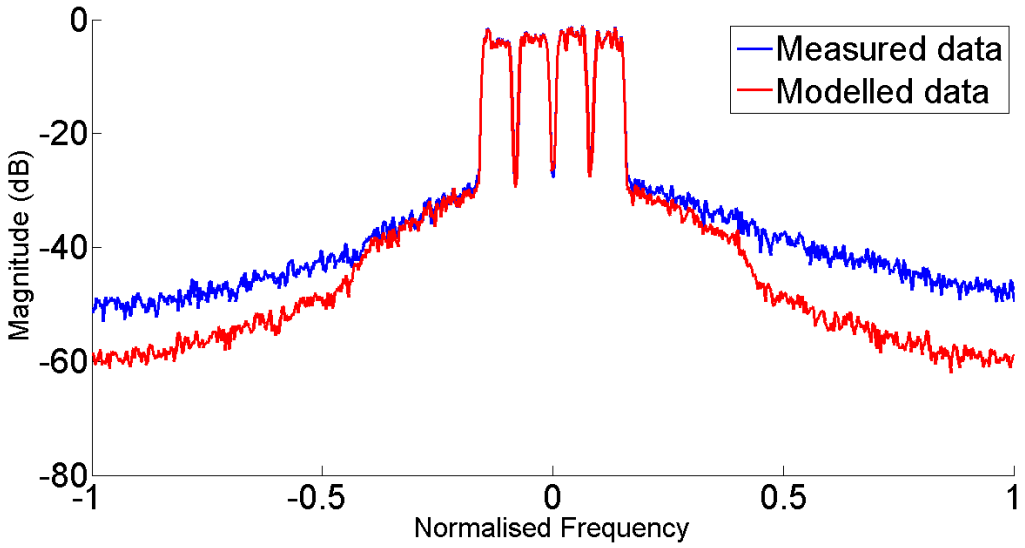


Figure 5.3: Modelling results for the RVTDNN model - MSE of -38 dB, NMSE of -26 dB

as outlined in equation 2.41.

$$s(t) = A(t)e^{j\omega\phi} \tag{5.11}$$

$$RE[s(t)] = A(t)cos(\phi(t)) \tag{5.12}$$

$$IM[s(t)] = A(t)sin(\phi(t)) \tag{5.13}$$

$$I_{out}(n) = O_1^{ol} = \sum_{j=1}^{N_{hl}} w_{1j}^{ol}\sigma\left\{\sum_{d=0}^{q} w_{j1d}^{hl}I_{in}(n-d) + w_{j2d}^{hl}Q_{in}(n-d) + w_{j00}^{hl}\right\} + w_{10}^{ol} \tag{5.14}$$

$$Q_{out}(n) = O_2^{ol} = \sum_{j=1}^{N_{hl}} w_{2j}^{ol}\sigma\left\{\sum_{d=0}^{q} w_{j1d}^{hl}I_{in}(n-d) + w_{j2d}^{hl}Q_{in}(n-d) + w_{j00}^{hl}\right\} + w_{20}^{ol} \tag{5.15}$$

As with the previous models an independent training and test data set are used to evaluate the model performance. A wide verity of supervised training algorithms exist for neural network models. The authors in [122] evaluate a selection of first and second order training

algorithms. From the analysis carried out it is clear that the Levenberg-Marquard training algorithm provides the most efficient method of training while maintaining model accuracy.

An advancement on the back propagation presented in section 2.6, the Levenberg-Marquardt achieves this by approaching second order training speed without having to compute the Hessian matrix, a second order matrix of partial derivatives. This is achieved by approximating the Hessian matrix in equation 5.16 where J is the Jacobian matrix which contains the first derivatives of the network error. The standard second order weight update given from a quasi Newton method is given by equation 5.18, the Levenberg-Marquardt update is given by equation 5.19, where the Hessian approximation is given by equation 5.16 and the gradient is computed by equation 5.17. The results for the single input single output RVTDNN approximation of the outphasing power amplifier is presented in Figure 5.3. In line with the performance of the Volterra series behavioural model presented in Section 4.2.1, it confirms the short comings of standard single input - single output behavioural model configurations. However as with the Volterra series the neural network structure is not limited to this configuration.

$$H \approx J^T J \tag{5.16}$$

$$g = J^T e \tag{5.17}$$

$$W_{n+1} = W_n - (H_n)^{-1} g_n \tag{5.18}$$

$$W_{n+1} = W_n - (J_n^T J_n)^{-1} J_n^T e_n \tag{5.19}$$

5.2.2.1 Multi Input Model

The RVTDNN model is a multi - input/output system. Therefore it can be expanded to a two path model equivalent to the direct model in Section 4.2.1 by using the outputs of the signal component separator as the inputs to the model. The model only accepts real value inputs therefore a total of four inputs are used. The input and output layers use a linear activation

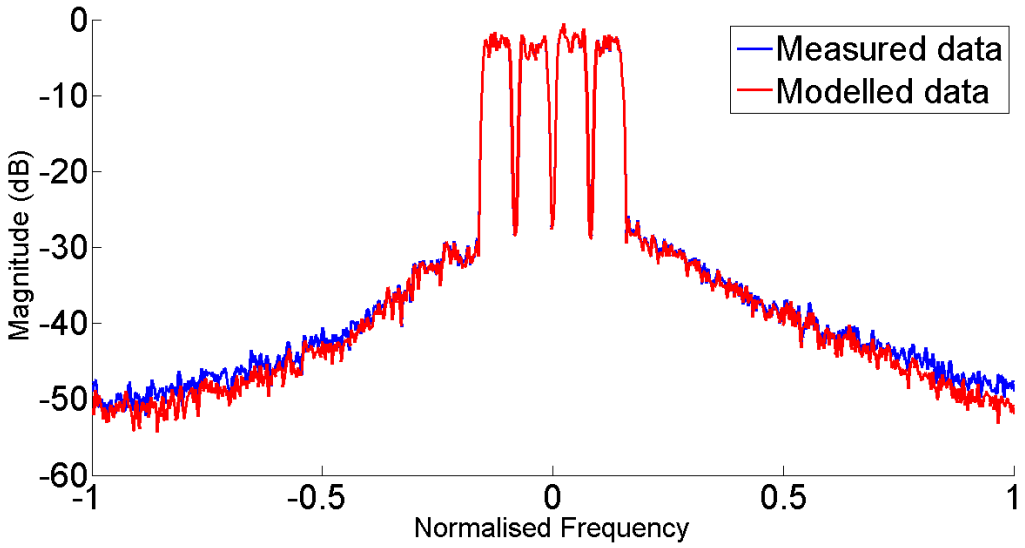


Figure 5.4: Modelling results for the 4 input RVTDNN model - MSE of -46 dB, NMSE of -33 dB

function, while a single hidden layer uses a sigmoidal non-linear function. The structure of the network is outlined in equations 5.20 and 5.21. The performance of the model is outlined in Figure 5.4, there is an improvement in accuracy of the spectral characterisation and the MSE and NMSE figure of merit indicate an improvement in the time domain characterisation.

$$I_{out}(n) = O_1^{ol} = \sum_{j=1}^{N_{hl}} w_{1j}^{ol}\sigma\left\{\sum_{d=0}^{q} w_{j1d}^{hl} I_{V1}(n-d) + w_{j2d}^{hl} Q_{V1}(n-d) + w_{j3d}^{hl} I_{V2}(n-d) + w_{j4d}^{hl} Q_{V2}(n-d) + w_{j00}^{hl}\right\} + w_{10}^{ol} \tag{5.20}$$

$$Q_{out}(n) = O_2^{ol} = \sum_{j=1}^{N_{hl}} w_{2j}^{ol}\sigma\left\{\sum_{d=0}^{q} w_{j1d}^{hl} I_{V1}(n-d) + w_{j2d}^{hl} Q_{V1}(n-d) + w_{j3d}^{hl} I_{V2}(n-d) + w_{j4d}^{hl} Q_{V2}(n-d) + w_{j00}^{hl}\right\} + w_{20}^{ol} \tag{5.21}$$

5.2.2.2 Two path model

It is clear that the mutli-input neural network offers increased modelling accuracy. Expanding upon this in a similar method to the two path Volterra model outlined in Section 5.2.1 the neural

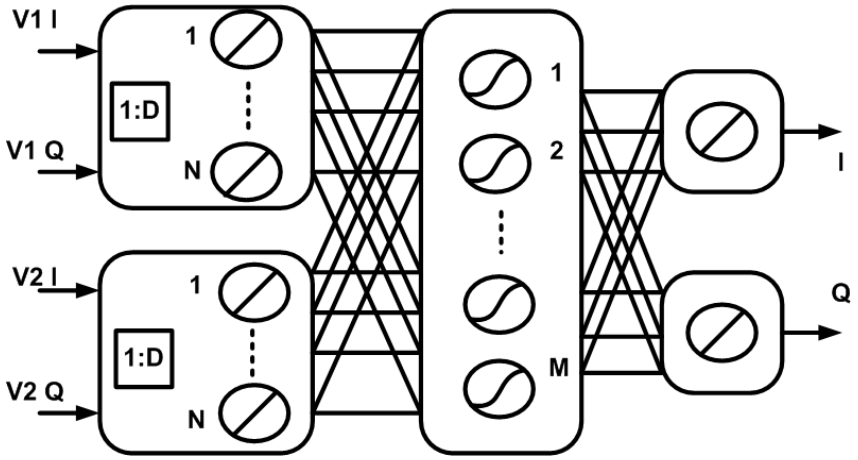


Figure 5.5: Structure of two path neural network designed to mimic the structure of outphasing power amplifier.

network with individual neuron layers for the input paths. The non-linear function is then placed in an additional hidden layer, this arrangement mimics the physical system more closely. The addition of the extra layers increases the number of neurons in the structure compared with the four input model previously examined. The model performance is demonstrated in Figure 5.6, the result is an increase of approximately 2 dB NMSE requiring twice the number of coefficients. The arrangement of the system is visible in Figure 5.5.

$$I_{out}(n) = O_1^{ol} = \sum_{j=1}^{N_{hl}} w_{1j}^{ol}\sigma\left\{\sum_{i=1}^{N_{il}} w_{j1i}^{il}\left[\sum_{d=0}^{q} w_{ji1d}^{il} I_{V1}(n-d) + w_{ji2d}^{il} Q_{V1}(n-d) + w_{ji00}^{il}\right] + \sum_{i=1}^{N_{il}} w_{j1i}^{il}\left[\sum_{d=0}^{q} w_{ji3d}^{il} I_{V1}(n-d) + w_{ji4d}^{il} Q_{V1}(n-d) + w_{ji01}^{il}\right] + w_{j00}^{hl}\right\} + w_{10}^{ol} \tag{5.22}$$

$$Q_{out}(n) = O_2^{ol} = \sum_{j=1}^{N_{hl}} w_{2j}^{ol}\sigma\left\{\sum_{i=1}^{N_{il}} w_{j1i}^{il}\left[\sum_{d=0}^{q} w_{ji1d}^{il} I_{V1}(n-d) + w_{ji2d}^{il} Q_{V1}(n-d) + w_{ji00}^{il}\right] + \sum_{i=1}^{N_{il}} w_{j1i}^{il}\left[\sum_{d=0}^{q} w_{ji3d}^{il} I_{V1}(n-d) + w_{ji4d}^{il} Q_{V1}(n-d) + w_{ji01}^{il}\right] + w_{j00}^{hl}\right\} + w_{20}^{ol} \tag{5.23}$$

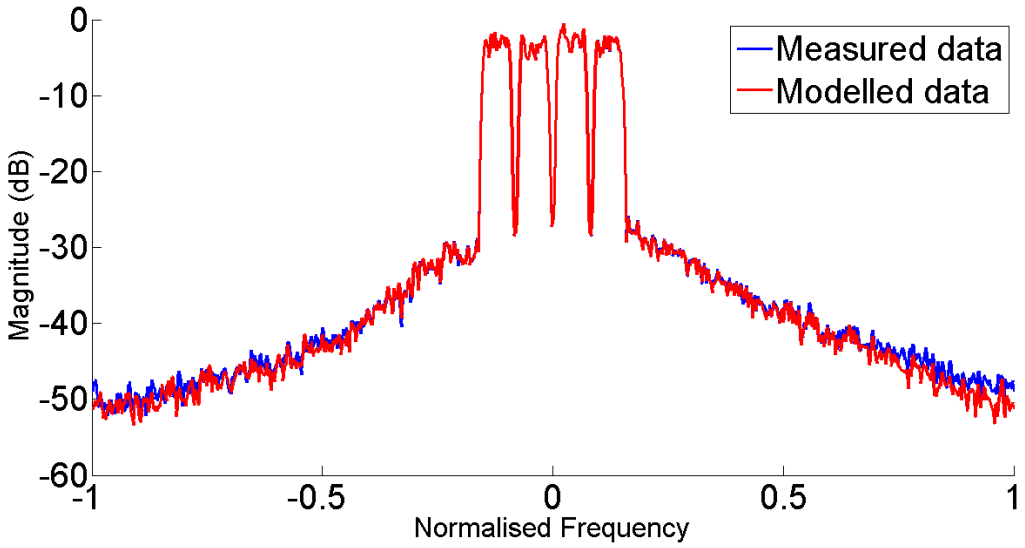


Figure 5.6: Modelling results for the 2 path plus combiner RVTDNN model - MSE of -47 dB, NMSE of -35 dB

5.3 Segmented Single input models

In section 5.2 the performance of two path models is explored. Given the system layout they have a natural advantage over single path models, with the ability to model the individual path mismatch effects and amplifier memory effects. In contrast to single path models additional resources are required in order to achieve an accurate system model. In some cases they can be cumbersome to train as demonstrated in Section 4.2.4. Single input model have a distinct advantage in this case as they require fewer coefficients. In traditional power amplifiers memory effects and non-linearity are more pronounced at higher output powers. In switching amplifier and more specifically the outphasing amplifier this is not the case. Static non-linearity is present for all output powers, however the presence of memory effects is more likely to occur at lower output powers. The memory effects are caused by the frequency dependent mismatch associated with the combiner. Examining the error location between a single path and dual path model in Figure 5.7 the lower power region stands out as the main difference. In order to overcome the inability to model these memory effects with a standard single input output model, segmented implementations are examined. Segmentation has many advantages, enabling accurate estimation of localized non-linear characteristics and also the use of lower order models increases stability when training.

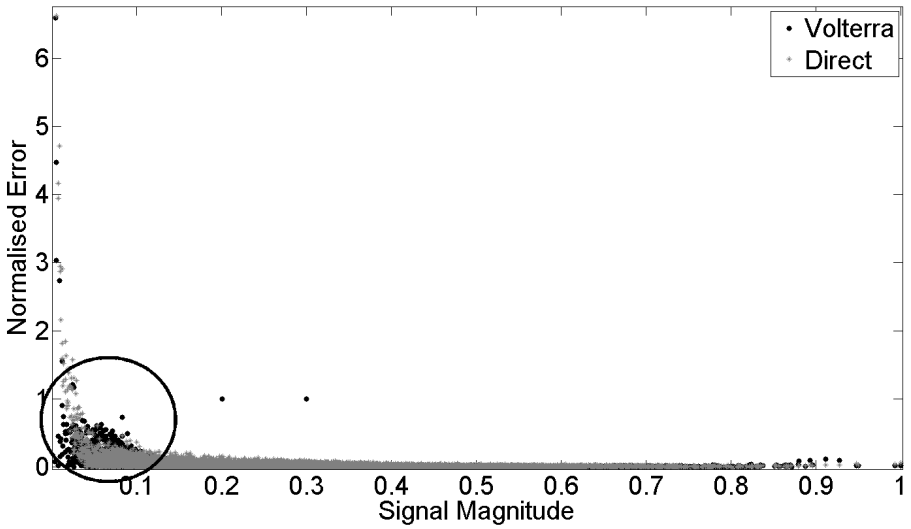


Figure 5.7: Modelling error Single path model vs Dual path model. The single path model evaluated is the Volterra series. The dual path model is the direct model introduced in the previous chapter. The circled area is the dominant difference between the models.

5.3.1 Piecewise polynomial

The piecewise function is a common mathematical method of using multiple sub functions to more accurately describe a more complex function. Each sub function is applied at either predetermined intervals or at distinct transition points, enabling more accurate and less complex mathematical descriptions. Using a single attribute of the input signal $x(n)$ a piecewise decision matrix can be constructed. The magnitude of the input signal is the most commonly used input of the piecewise function, the output is an array of model coefficients h_n.

$$H = \begin{cases} h_1 & \text{if} \quad |x(n)| > d_1 \\ h_2 & \text{if} \quad d_1 > |x(n)| > d_2 \\ & \cdots \\ h_n & \text{if} \quad |x(n)| < d_n \end{cases} \tag{5.24}$$

In [123] a piecewise polynomial is presented as a method of modelling difficult amplifier structures. By applying a unique polynomial function to each piecewise segment, a more accurate model can be extracted. Each sub function of the piecewise structure requires lower order polynomial functions. By designing the piecewise function to mimic the transition points that can occur within the amplifier, discontinuities can be modelled with much lower order

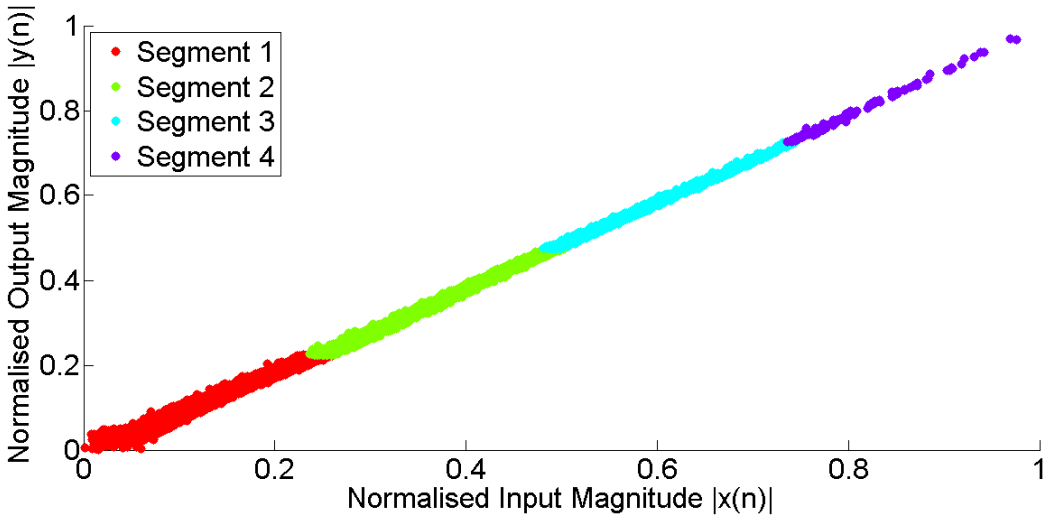


Figure 5.8: Piecewise segmentation using input magnitude

functions. This in turn reduces the potential for instability which can occur when fitting discontinuous functions. The piecewise polynomial in question is a piecewise version of the AMAM AMPM model introduced in Section 2.5.1.3. The individual segment coefficients h_n are applied to the polynomial kernels of the input, where the piecewise function is represented as the function $G(|x(n)|)$ which returns an array of coefficients. The piecewise polynomial is presented in equation 5.25 where P is the order of the polynomial function.

$$y(n) = \sum_{i=0}^{P} G(|x(n)|)_i |x(n)|^i \tag{5.25}$$

The additional flexibility offered by the segmentation of the polynomial reduces the generality of training a single function to characterise the entire system. This increased the accuracy of each individual segmented region and therefore the characterisation of the entire amplifier, the performance difference is presented in Figures 5.9 and 5.10. An additional 1.5 dB NMSE is achieved through a segmented implementation. The static models offer excellent performance when comparing figures of merit such as MSE and NMSE, however the spectral performance indicated that there is residual error between the model and the measured signal. To improve the characterisation performance of the segmentation the individual polynomial functions are replaced with time series non-linear functions in Section 5.3.2.

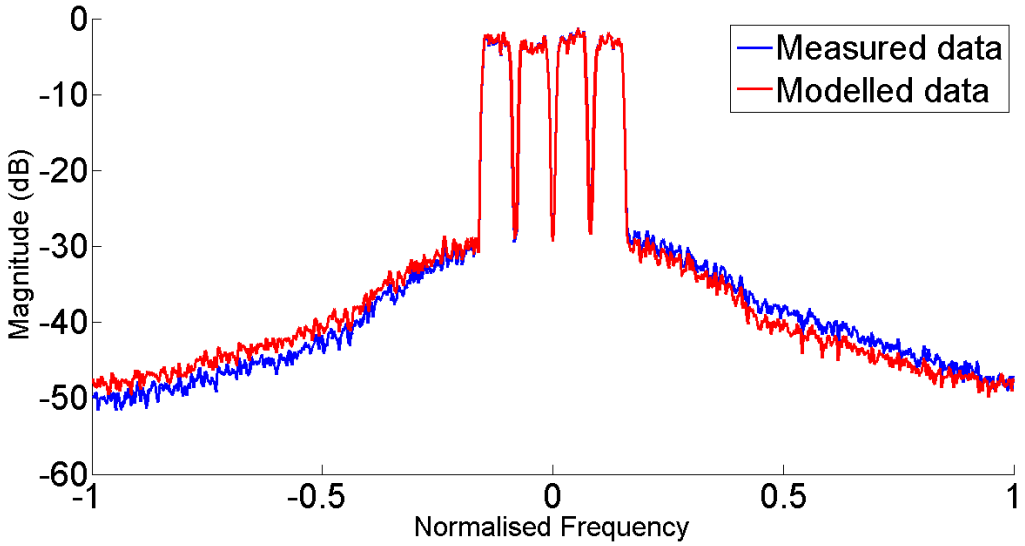


Figure 5.9: Modeling results for AMAM AMPM model - MSE of -43 dB, NMSE of -30 dB

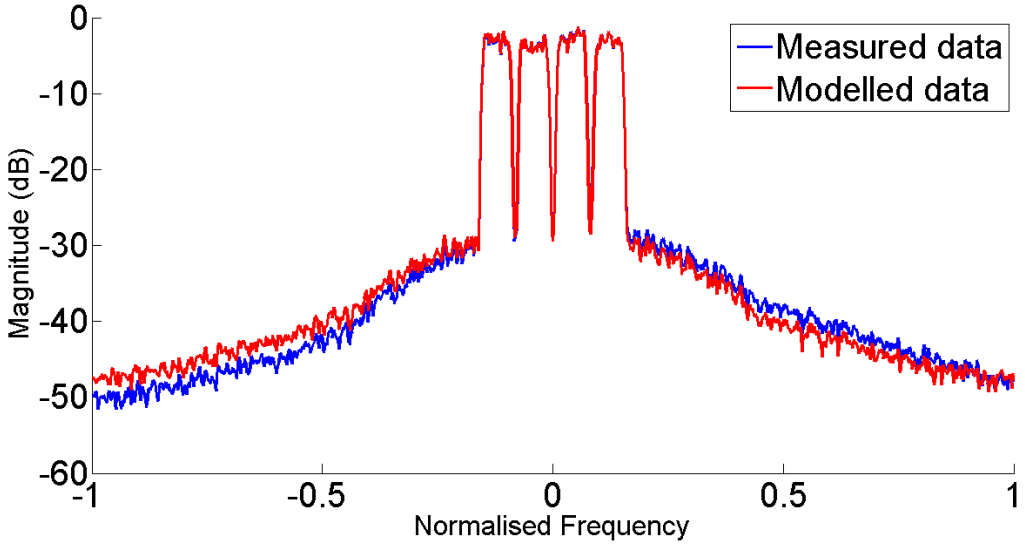


Figure 5.10: Modeling results for segmented AMAM AMPM model - MSE of -44 dB, NMSE of -31.5 dB

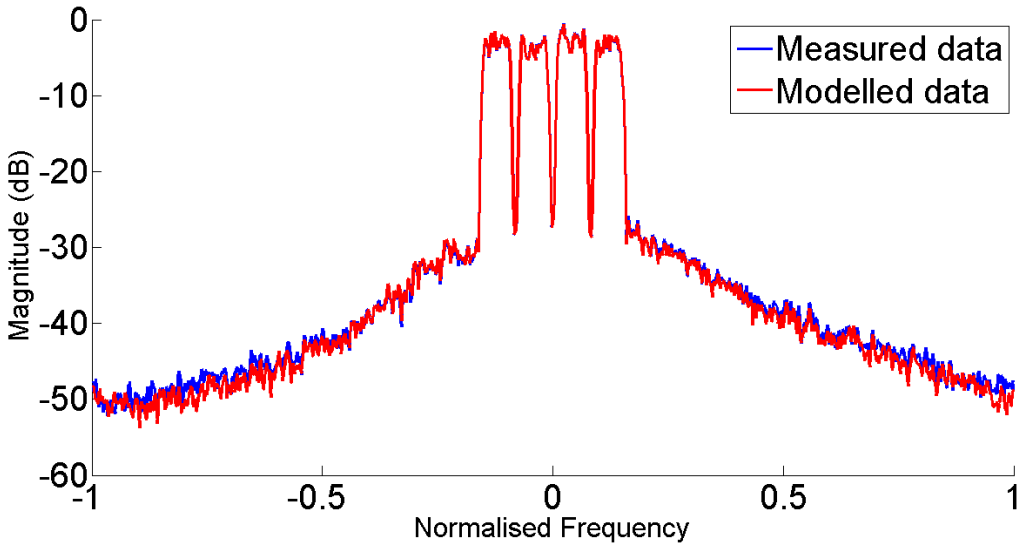


Figure 5.11: Modelling results for segmented Volterra model - MSE of -46 dB, NMSE of -34 dB

5.3.2 Piecewise Time series

A piecewise time series function similar to the piecewise polynomial in Section 5.3.1 uses a time series for each individual sub function in place of the polynomial. The added benefit in comparison to the polynomial time series is the addition of memory effects to the characterisation function. To train the model we first must calculate the kernels of the input to the time series $x(n)$, and group each kernel set $\prod_{p=0}^{P}\prod_{m=0}^{M-1} x(n-m)^p$. The kernel groups are then segmented using the piecewise classification in equation 5.24, this results in a matrix of time series kernels for each sample. An additional vector of outputs relative to the segmented samples is generated from the measured data $y(n)$. Using the segmented kernel and output grouping an approximation of each segment can be determined using the least squares approximation. Equation 5.26 demonstrates a piecewise Volterra series where the piecewise function returns a coefficient set $h_k(q_k)$. The model results for this powerful time series are demonstrated in Figure 5.11.

$$y(n) = \sum_{k=0}^{K}\sum_{qk=0}^{Q_k} G(|x(n)|)x(n-q1)\prod_{m=1}^{(k-1)/2} x(n-q_{2m})x^*(n-q_{2m+1}) \tag{5.26}$$

Care must be taken when extracting a segmented time series that enough samples are available in each segment to calculate the time series with sufficient accuracy. Additionally

segments should have sufficient points, especially in transition regions to provide continuity between segments. Typically to achieve good generality, model extraction requires a minimum number of samples between 10-20 times the number of coefficients. Given the high peak to average ratio of modulated communication signals, it may be difficult to achieve a large number of segments at larger output amplitudes.

5.3.3 Vector Switched Time Series

In [124] the author presents an advancement on previous segmentation techniques by using a clustering algorithm to dynamically generate a two dimensional segmentation process. The clustering process presented in [124] is performed on the magnitude of the input signals current value and a previous value determined by a set delay value. Feature space analysis and clustering enables segmentation based upon multiple characteristics of the input signal. In this case input signal magnitude and magnitude deviation. The individual clusters are analysed and individual non-linear time series functions are extracted for each. As with the piecewise approach, the individual non-linear sub functions can be estimated using fewer coefficients than a single larger time series function while maintaining and in some cases improving model accuracy.

5.3.3.1 Vector quantisation

Vector quantization is performed on the feature space generated from the magnitude of the input sample and the magnitude of a previous input sample $mag(x(n)), mag(x(n-m))$ where n is the current sample and m is an integer representing a delay factor. The K-means clustering algorithm is used to partition the data through vector quantization [124]. The method is shown to provide a significant performance improvement over traditional time series implementation alone when classifying systems with varying ranges of operation with individual non-linear regions. An example of the two dimensional feature space is demonstrated in Figure 5.12.

5.3.3.2 K-means

K-means is a popular method for data clustering and vector quantization [124]. It is computationally efficient and as a result very fast. The algorithm partitions the feature space into k non-overlapping clusters, the center of each cluster is a point called a centroid. Using

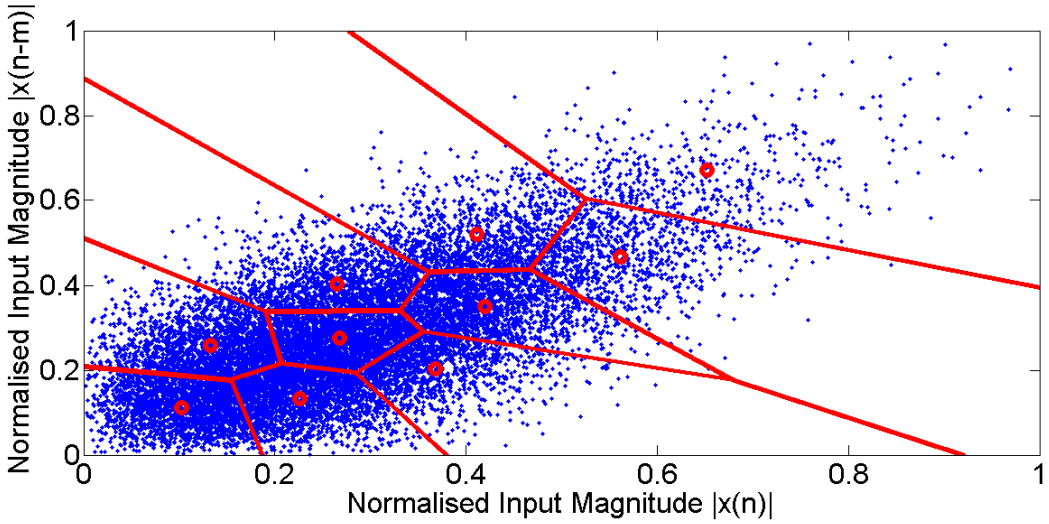


Figure 5.12: Example vector quantised feature space generated with K-means clustering

a measure of distance, typically Euclidean distance, a data point is assigned to its nearest centroid. This centroid then repositions itself reducing the sum of the distances between the points in its region. The location of the centroid and the point assigned to it are updated, and the results stored in a code book. This process continues until the centroids have settled and a threshold for minimum movement between iterations is reached. The final code book or look up table is then used in the model to select the appropriate time series.

$$H = f_k\left(x_n^{(M)}\right) \tag{5.27}$$

Where f_k is the decision function used to determined the sector from the vector quantisation function. In this case K-means is used as a method of vector quantisation. The region is chosen based upon the current points distance from each centroid using the Euclidean distance formula.

$$H = h_n = \{|x_n| : \|x_n - c_n\| < \|x_n - c_l\|, l = 1 \cdots N\} \tag{5.28}$$

5.3.4 Self Organising Maps

Self organizing maps (SOM) present a more robust method for clustering compared with K-means [125]. Derived from a special case of neural network they can be implemented using an array of adders and multipliers as well as a traditional cluster LUT method. The structure

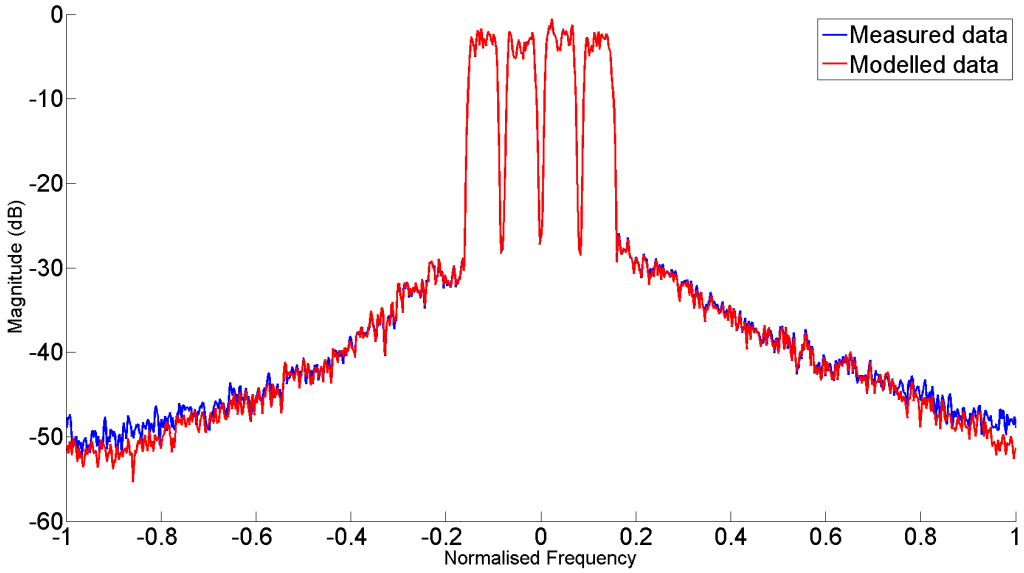


Figure 5.13: Modelling results for VSV Volterra model - MSE of -48 dB, NMSE of -36 dB

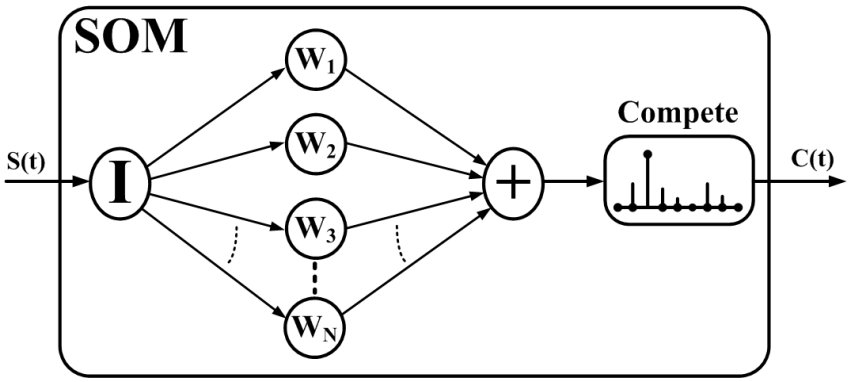


Figure 5.14: Overview of Self Organizing Map

of a SOM is presented in Figure 5.14, it is similar to a single neuron within a neural network. In comparison to a typical neuron in a neural network the main difference is the change in the output activation function from a linear/non-linear transfer function to a compete transfer function. As the name suggests the value of the input is compared to the possible outputs. The output that has the strongest correlation with it is chosen as the winner. This output is then set to one while the remaining outputs are set to zero. The SOM also does not use a bias weight in conjunction with the weights on the input signal. The results from clustering the input signal from a modulated signal is illustrated in Figure 5.15 in which the same parameters of the input signal as used in [124] to generate a vector space.

Training of the SOM is carried out using a Kohonen algorithm over several iterations. The

[h]

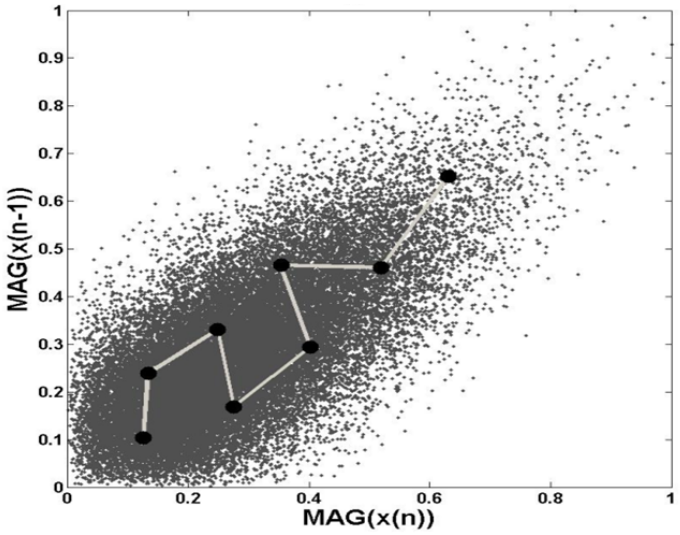


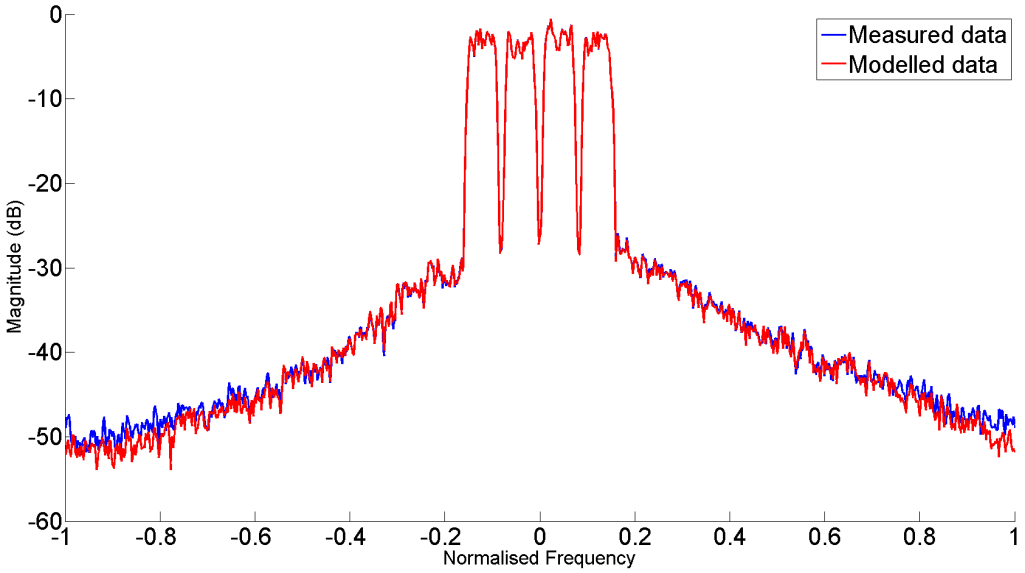
Figure 5.15: Self Organizing Map weight locations(Black), input data(Grey)

Kohonen algorithm is an unsupervised learning process [126]. The aim of the algorithm is to classify the input signal to the best of its ability using a limited number of neurons. A drawback to SOM is an increase in computational complexity in comparison to K-means. Equations 5.29 5.30 derived in [127] present the complexity per iteration of both K-means and SOM.

$$SOM = 2O((N^2 n_O)) + (NN_O Log(n_O))) \tag{5.29}$$

$$K - Means = O(n_O) \tag{5.30}$$

Where N is the number of inputs and n_O is the number of clusters. For a comparison of methods used in this paper there are eight cluster regions n_O and in the case of the SOM there are two inputs. The increase in the computational complexity for an SOM with eight output clusters is twelve times that for K-means. A dramatic increase, however the robustness of the SOM requires fewer iterations to reach as good or better model accuracy. In this example SOM ran for a total of 25 iterations, 25% fewer computational operations than the K-means algorithm required. An example of the SOM clustering is demonstrated in Figure 5.15 and the modeling results presented in Figure 5.16.



[h]

Figure 5.16: Modelling results for VSV Volterra model utilising SOM clustering - MSE of -48.7 dB, NMSE of -36.5 dB

5.4 Modelling analysis

In this chapter an array of modelling techniques, which have not previously been explored for outphasing power amplifiers are examined. The modelling algorithms have been dimensioned and in some cases customised to provide maximum characterisation performance for the digital outphasing power amplifier. The aggregated results are presented in Table 5.1. Included in the table are the results from Chapter 3, directly comparing existing outphasing modelling strategies to the methods presented in this chapter.

Table 5.1 includes an additional figure of merit, the adjacent channel error power ratio ACEPR [84] in addition to the already established MSE and NMSE. This is used to determine the accuracy of the model with regard to the spectral characteristics of the amplifier. The equation is presented in 5.31 where $E(f)$ is the Fourier transform of the error signal $d_k(n)-y_k(n)$ and $D(f)$ is the Fourier transform of the measured signal $d_k(n)$.

$$ACEPR = \frac{\int\limits_{adj} |\, E(f)\,|^2\, df}{\int\limits_{ch} |\, D(f)\,|^2\, df} \tag{5.31}$$

$$MSE = \frac{1}{n}\sum_{n}^{t=1} |\, \hat{y}(t) - y(t)\,|^2 \tag{5.32}$$

$$NMSE = \frac{1}{n}\sum_{n}^{t=1}\frac{|\hat{y}(t) - y(t)|^2}{|\hat{y}(t)|^2} \tag{5.33}$$

To accurately compare the models without bias all operations required to implement the models must be considered. In particular a distinction between real and complex coefficients must be made. In hardware a complex multiplication requires four real value multiplications and two additions as evident in equation 5.34. This must be taken into account when comparing complex models such as the Volterra series and the real value models such as AM/AM AM/PM and RVTDNN structures.

$$\begin{aligned} xy &= (a + ib)(c + id) \\ &= ac + ibc + iad - bd \\ &= (ac - bd) + i(ad + bc) \end{aligned} \tag{5.34}$$

Additional operations are required in an AM/AM AM/PM implementation, a conversion from Cartesian to polar form is required in order to apply the polynomial coefficients. In the case of the RVTDNN each neuron requires an activation function, if a non-linear function is required a LUT or a non-linear polynomial used to map the outputs of the non-linear neuron layer, this is typically applied to neurons in the hidden layer/layers. In Table 5.1 all real value coefficients are identified with $*$, any additional computations are stated in the operations column. The remainder of this section will discuss and compare the tabulated results on the following points:

- Optimisation of the algorithm dimensions for maximum characterisation performance.
- Performance of dual path outphasing models.
- Performance of single path outphasing models.
- Finding a practical linearisation solution from the models presented.

The optimal model dimensions: non-linear order; number of memory terms; and number of segments were discovered by sweeping these variables. The order of the models was swept from 3rd order to 9th order, using only odd values. The memory taps were swept from 2-6. The number of segments was swept from 5-20. In each case the optimum was identified by

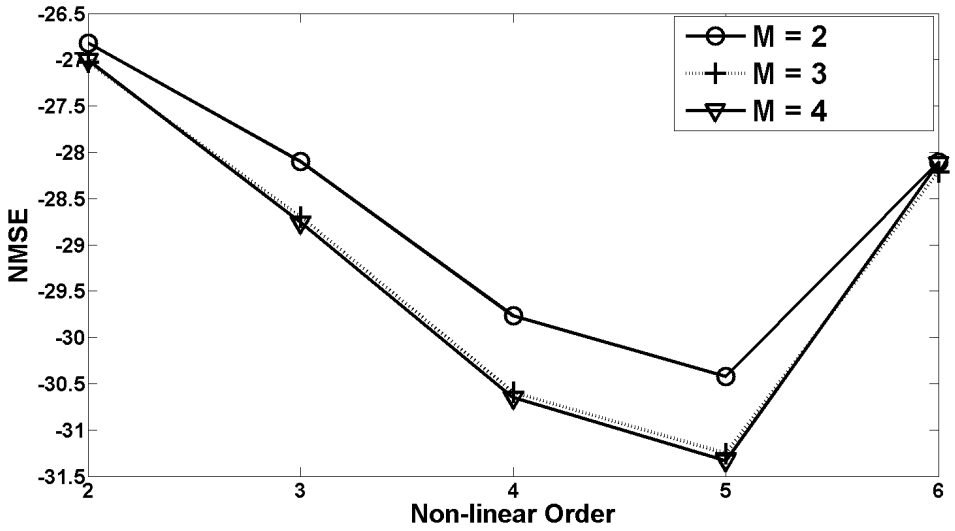


Figure 5.17: Two path Volterra performance with different dimensions, each line represents a different number of memory taps 2-4, each data point represents a different non-linear order 2-6.

a knee point, in which no additional performance or performance degradation was observed with a larger number of parameters. An example of this is presented in Figure 5.17 as the performance evaluation of the two path Volterra series, the best performance is achieved with 5th order non-linearity, the model with 3 memory taps is approximately equal to the model with 4 memory taps therefore the former is chosen as it is more computationally efficient.

Of the two path models the neural network implementation provides the best performance at -35 dB NMSE. The two path Volterra series performs in line with the amplitude distortion model proposed in [117]. However due to the rapid expansion in dimensionality associated with Volterra series when non-linear order or number of memory taps are increased the amplitude distortion is more efficient. Work outlined in Appendix A proposes an additional computational step which aims to reduce the number of coefficients required for dual path Volterra, while maintaining characterisation accuracy. All neural network computations are performed using real value coefficients, therefore even the largest neural network requires half as many system resources when compared with a complex time series of similar dimensions. The computational complexity required when extracting the ANN models is much greater due to the configuration of the multiple layer perceptron neural network. Back propagation algorithms are required, providing iterative training of the neurons in the network. The

computational expense of extracting the model is offset by the reduced computation of running the model.

Of the single path models outlined in Section 5.3, the best overall performance is achieved with the vector switch Volterra approach at -36.2 dB NMSE, a large improvement over the originally evaluated Volterra series at -26 dB. The more compact vector switch Volterra will also require fewer computations per forward operation as a single segment can provide the desired output for a single sample. The Volterra series is out performed by the less powerful AMAM AMPM algorithm. The main reason for this is the duality in amplifier characterisation between high and low output power. The Volterra series tries to characterise the memory effect at low power, however this effects the high power output introducing error into the system. This highlights an important point that should be taken into account, the training algorithm should be tailored for both the algorithm and the system that is being characterised. Something that is outside the scope of this current work, however should be examined further in future work.

Of the two approaches: multiple input time series; or modified single input time series, an algorithm capable of modelling the variation of memory effects at different power is required. This is highlighted by the improvements made in single and dual path modelling when compared with existing AMAM/AMPM and direct outphasing amplifier models. Of the proposed memory capable models the single input segmented approach requires the least additional complexity to train and implement as a linearisation solution. As it is implemented before the signal component separator and calibration stages, it cannot impact directly on the signal properties of the outphasing signal. Of which the signal amplitude is a concern, any information encoded upon the input amplitude will be removed before the outphasing stages by the digital limiters. The choice of linearisation algorithm will be discussed further in the following chapter.

Table 5.1: Power amplifier behavioural model performance compared

Model	Order	Memory depth	Segments	Number of coefficients	Operations	MSE	NMSE	ACEPR
Direct Model	NA	NA	NA	16	NA	-41 dB	-28 dB	-40.5 dB
Amplitude distortion Model	6	[1Mlin, 4Mnon-lin]	NA	50	NA	-43 dB	-31.5 dB	-43.9 dB
Volterra	7	3	NA	70	NA	-39 dB	-26 dB	-36.8 dB
Dual Path Volterra	5	3	NA	256	NA	-44 dB	-31 dB	-41.3 dB
TD Neural Network	5i-10h	3	NA	177*	10*Sig	-38 dB	-26 dB	-36.8 db
2 path TD Neural Network	5i-15h	3	NA	207*	15*Sig	-45 dB	-33 dB	-45.5 db
Direct model TD Neural Network	5i-25h	3	NA	417*	25*Sig	-47 dB	-35 dB	-47.1 db
AMAM AMPM	7	NA	NA	14*	2*CORDIC	-43 dB	-30 dB	-43 db
Piecewise AMAM AMPM	5	NA	4	4*10	2*CORDIC + Piecewise LUT	-44 dB	-31 dB	-44 db
Piecewise Volterra	5	3	7	7*119	Piecewise LUT	-46 dB	-34 dB	-46.8 dB
Vector Switch Volterra	5	3	10	10*119	VSV LUT	-48 dB	-35.9 dB	-49 dB
Vector Switch Volterra SOM	5	3	10	10*119	SOM ANN	-49 dB	-36.2 dB	-49.2 dB

5.5 Conclusion

In this chapter a selection of behavioural models were optimised for characterisation of digital outphasing power amplifiers. These novel results are compared against the current state of the art outphasing power amplifier modelling techniques with a select few offering increased accuracy. The algorithms demonstrated in this chapter provide improvements over existing modelling algorithms proposed for outphasing systems with an 8.5 dB and 4.7 dB improvement over the direct outphasing and the amplitude distortion models respectively.

The comparison of single input and multiple input behavioural models demonstrates that both approaches are valid for wideband operation of an outphasing system. In both cases the importance of a memory capable model was highlighted for accurate characterisation of the amplifier at all output powers. The single input models could not directly model the non-linearity that is experienced by path mismatch without the inclusion of segmentation. Segmentation enabled the application of different time series functions depending on the output amplitude, enabling a more accurate model of outphasing effects.

The results from the evaluation of the outphasing power amplifier have shaped the choices made in the subsequent linearisation work outlined in the following chapter. The simplicity of implementation and model performance make the vector switch Volterra approach the obvious choice for digital pre-distortion implementation.

CHAPTER 6

Pre-Distortion of outphasing power amplifiers

Digital pre-distortion is a widely adopted method for power amplifier linearisation in current communications systems, enabling efficient operation in several amplifier topologies, most notably commercial Class AB and Doherty amplifiers. The outphasing power amplifier were originally proposed to negate the non-linear effects associated with amplitude modulation. However the topology has some inherent design properties which hinder linear amplification of wide band signal standards. Previous publications have demonstrated that linear amplification of a 5 MHz signal is possible [29]. However challenges still remain for wider bandwidth signals. The target of this work is to achieve linear amplification for a 20 MHz signal, specifically a quad carrier WCDMA signal.

To establish the issues that are associated with wideband operation the non-linear effects of a 5 MHz and 20 MHz signal are compared, highlighting the issues sounding wideband operation. The behaviour of the amplifier and the outphasing system is analysed over the bandwidth of operation of the outphasing signals, identifying one of the main contributions to the output non-linearity, outphasing angle across frequency. Analysing the outphasing function to the input signal it is apparent that the input signal phase can provide a good approximation to the outphasing signals, therefore an additional attribute of the input signal, namely the rate of change of signal phase is used in a pre-distortion algorithm to increase linearisation

performance.

6.1 Test bench upgrade - Signal capture

The test-bench used in the following experiments has been outlined in Section 4.1. To ensure that the capture bandwidth of the FSQ was not limiting linearisation performance it was decided to upgrade the signal capture hardware in the feedback path. The goal is to have equal data rates in the signal conversion hardware to enable direct training of memory capable DPD. Finally the improved accuracy of the analogue to digital signal conversion, through an improvement from 12 to 16 bits of resolution provides increased sensitivity for non-linearity about the zero crossing point.

The Texas Instruments ADS5402, is capable of dual channel, 800 Msps, 16 bit conversion. To achieve maximum linearisation performance the input and output signals must correlate. This is ensured by directly supplying the conversion clock for the DAC and ADC from the same source. Reducing the possibility of fractional delay and removing any uncertainty or frequency drift associated with on-board phase lock loop (PLL) circuits. The chosen TSW1266 development board which contained the ADS5402 ADC with a compatible interface to the Texas Instruments FPGA evaluation platform is presented in Figure 6.1.

Figure 6.1: Texas Instruments signal capture board.

6.2 Analysis of Linearity in Relation to Instantaneous Bandwidth

This section investigates the linearisation potential of the digital outphasing amplifier with respect to increasing signal bandwidth. For the narrowband system analysis, a single carrier WCDMA signal will be used to excite the amplifier, and for wide bandwidth analysis a four carrier WCDMA signal will excite the amplifier. The input to the amplifier is calibrated and equalised using the methods outlined in Section 4.1.4. A lookup table is generated to determine the outphasing angle offset and angle range to achieve maximum signal dynamic range. A static linearisation technique is applied in order to correct any variations in outphasing combiner amplitude and phase with dynamic operation. A segmented AM/AM AM/PM pre-distortion technique is used to linearise both modulated signals. The technique was first implemented by Robin Wession, an RF systems engineer at NXP Eindhoven [29]. All system characterisation is carried out at the maximum amplifier output power of 19 watts. All signals are captured by the ADC signal capture set-up outlined above, the ACPR measurements and signal statistics are analysed using a Rhode and Schwartz FSQ signal analyser with appropriate software for WCDMA analysis.

The single carrier WCDMA signal has a bandwidth of 5 MHz and a peak to average power ratio of 7.6 dB. The pre and post linearisation performance is presented in Figure 6.2. The adjacent channel ACPR performance is improved by 26 dB when compared with the non-linear amplifier output. The result demonstrates that the amplifier is correctly statically calibrated and system as a whole has sufficient dynamic range to achieve linear amplification for amplitude

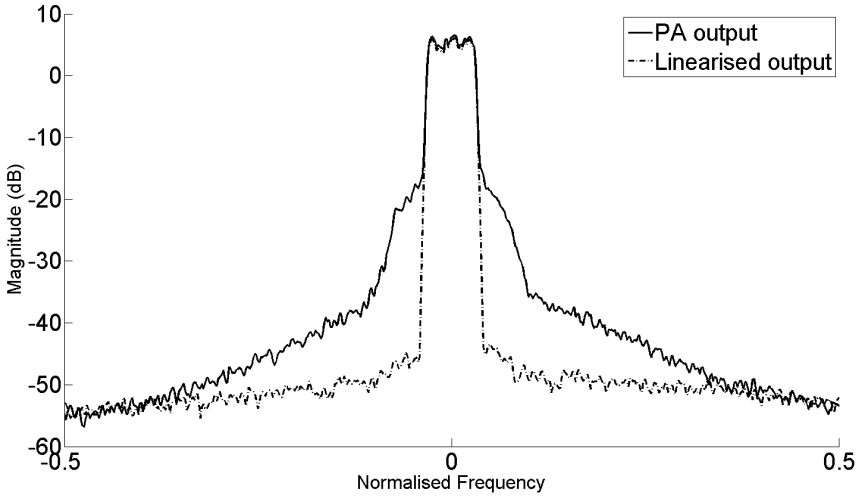


Figure 6.2: Single carrier WCDMA linearisation performance. Pre linearisation ACPR -29dB at +/- 5 MHz, -44 dB at +/- 10 MHz. Post linearisation ACPR -52dB at +/- 5 MHz, -55 dB at +/- 10 MHz.

modulated signal transmission.

The four carrier WCDMA signal has a bandwidth of 20 MHz and a peak to average power ratio of 9.6 dB. An increase in peak to average ratio is typical when signal bandwidth and the number of signal carriers is also increased. The pre and post linearisation performance is presented in Figure 6.3, the adjacent channel ACPR performance improved by 11 dB, a dramatic reduction when compared with the single carrier linearisation performance. As both signals have similar signal properties, the increase in ACPR is attributed directly to the increase in instantaneous operating bandwidth. The frequency characteristics of the amplifier are analysed in the following sections.

6.2.1 Outphasing Function Across Frequency

Bandwidth expansion is a well known side effect of outphasing signal encoding and has been introduced in Section 3.1.1. Bandwidth expansion is the consequence of phase only modulation and, as presented in [99], pure outphasing modulation will experience bandwidth expansion of between 10-12 times original signal bandwidth. Consequently the operational bandwidth when comparing the four carrier WCDMA to a single carrier WCDMA signal is much more demanding than first it appears. Taking bandwidth expansion to be 10-12 times original signal bandwidth a single carrier requires 50 - 60 MHz of operational bandwidth, in comparison the

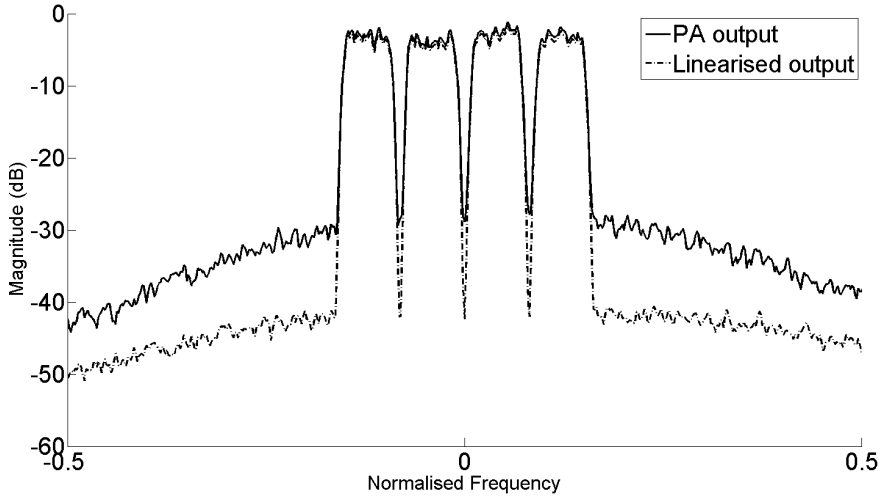


Figure 6.3: Quad carrier WCDMA linearisation performance. Pre linearisation ACPR -25dB at +/- 5 MHz, -28 dB at +/- 10 MHz. Post linearisation ACPR -38dB at +/- 5 MHz, -40 dB at +/- 10 MHz.

four carrier WCDMA signal requires 200 - 240 MHz of operational bandwidth.

The outphasing signal is made up of two properties of the communications signal, signal phase and a translated function of signal magnitude to outphasing angle. A single branch of the outphasing signal is analysed in Figure 6.4. The frequency spectrum of three signals are plotted: a full outphasing signal; an outphasing signals generated from signal phase only; and an outphasing signal comprised of signal amplitude only. Form this analysis it was determined that signal phase is the main factor of determining the bandwidth of the outphasing signal.

The instantaneous frequency of a signal can be estimated by the delta between the current sample and the previous sample. From the information illustrated in both Figure 6.4 and 6.5 it has been determined that the signal phase and more directly the delta of the signal phase between the current and previous sample will determine the majority of the instantaneous frequency of the outphasing signal. Of these delta's the largest occur at lower output powers, which has been identified in Chapter 3 as the region of operation of the outphasing topology with the largest residual memory effects. This will be further studied in a later section, with the aim of using this information to further develop a suitable linearisation algorithm.

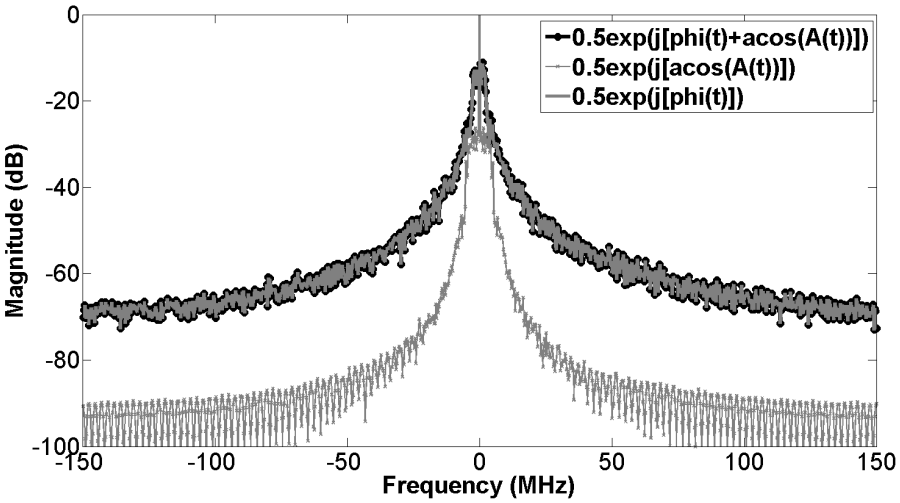


Figure 6.4: Fourier analysis of outphasing bandwidth expansion. The full outphasing signal $\frac{1}{2}e^{j(phi(t)+acos(A(t)))}$ is represented by a black line with a circular marker. A modified outphasing signal using only signal amplitude $\frac{1}{2}e^{jacos(A(t))}$ is represented by a grey line with cross markers. A modified outphasing signal using only signal amplitude $\frac{1}{2}e^{(jphi(t))}$ is represented by a grey line.

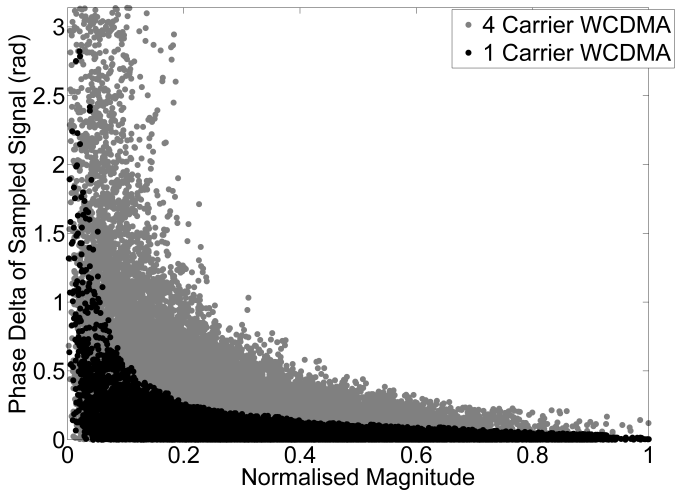


Figure 6.5: Rate of change of signal phase with respect to normalised signal magnitude. The signal carrier WCDMA signal is represented by the black markers and the four carrier WCDMA is represented by the grey Markers.

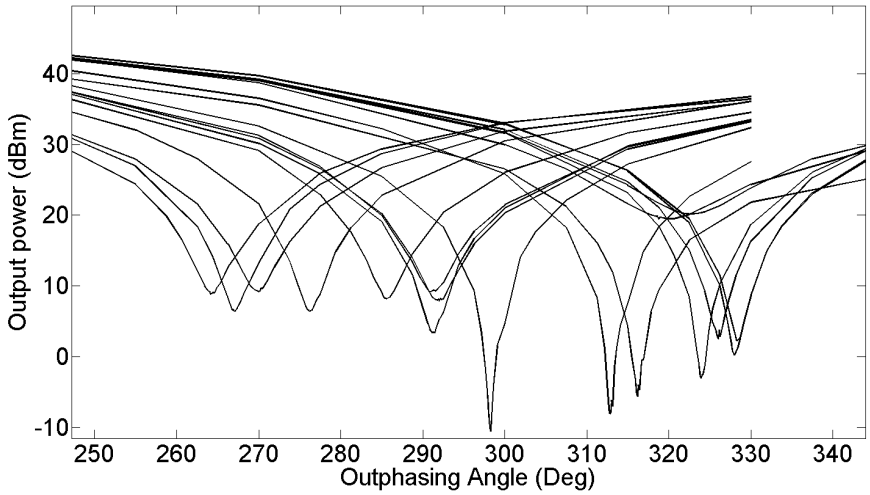


Figure 6.6: Digital outphasing amplifier characterisation sweep. Amplifier output power with respect to outphasing angle swept +/- 180 MHz around amplifier centre frequency 2.14 GHz.

6.2.1.1 Frequency Characterisation

To further understand the reasons behind the outphasing amplifier linearisation performance with respect to operating frequency, additional characterisation of the power amplifier is performed. An outphasing angle sweep across output frequencies is carried out. The amplifier is swept +/- 180 MHz from a centre frequency of 2.14 GHz. The sweep range was determined by the maximum available bandwidth of the signal generation system. The results of the sweep are presented in Figure 6.6. The focus of this work is to improve characterisation and linearisation of the outphasing amplifier operating in the lower output power regions, therefore this analysis focuses on the outphasing angles that provide the minimum output power across the operating frequency. The sweep is carried out using a single tone of 1 MHz and sweeping the outphasing angle. The result is a full characterisation of the amplifiers output power capability.

The results in Figure 6.6 demonstrate a large deviation in minimum outphasing angle across the chosen bandwidth. In addition the maximum achievable dynamic range also varies with operating frequency. Taking the minimum outphasing angle for each measured frequency step a trend in the outphasing angle across frequency can be found and is demonstrated in Figure 6.7. The analysis presents some interesting results. Using the predicted bandwidth of the outphasing signal for a single carrier WCDMA signal (50-60 MHz), a deviation of of between 10 - 12

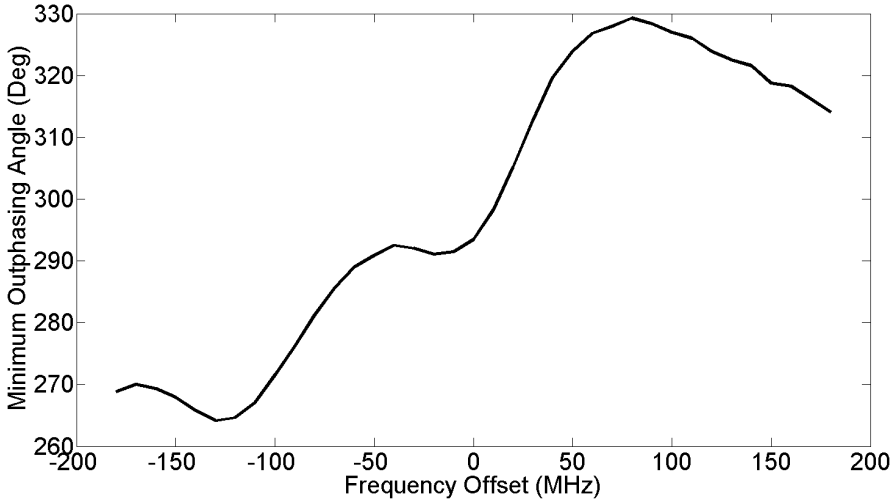


Figure 6.7: Digital outphasing amplifier minimum amplitude outphasing angle shift with respect to frequency.

degrees in the outphasing angle can be expected across the operating frequency of the amplifier. The four carrier WCDMA signal will on the other hand experience as much as 60 degrees of phase angle deviation, of which a much high percentage of the signal power experiences phase shifts of over 10 degrees. As a result the wider bandwidth signal will experience significantly more non-linear components. These findings agree with the linearisation performance using a static pre-distortion algorithm presented in Figures 6.2 and 6.3.

6.3 Digital Pre-distortion

Digital pre-distortion is the linearisation of a non-linear system by applying a correction function, the inverse of the non-linear system, implemented in digital logic that precedes the input of the non-linear system. An overview of digital pre-distortion is presented in Section 2.7.4. The process is closely linked with the worked carried out in Chapter 5, the performance of the pre-distortion algorithm is highly dependent on the capability of the discrete time mathematical function used. From the modelling analysis the most accurate pre-existing algorithm is the amplitude distortion direct model and of the proposed models the dual path neural network and the vector switch Volterra both offer similar characterisation performance. Firstly we will examine each of these to determine if they are suitable for digital pre-distortion of digital outphasing power amplifiers. Our target is to achieve the maximum ACPR for a

signal of 20 MHz bandwidth. The chosen signal standard is quad carrier WCDMA as such the specified limits are -45 dB ACPR for the adjacent channel and -50 dB ACPR for the first alternative channel.

The first major concern is the input signal to the amplifier post pre-distortion processing. The input signals must correct the non-linearity by only modifying the phase information of the input signal. The input to the amplifier must remain constant envelope or only fluctuate within a small margin. There are two main reasons for this, the digital architecture has a set of input buffers which strip the input signal of amplitude information, therefore if the correction algorithm relies on information encoded in signal amplitude it will fail to reach the output amplification stage. Secondly any variation in the input signal amplitude will result in a loss of efficiency from the architecture, as the outphasing amplifier requires switch-mode or deep saturation of the output stage in order to achieve the theoretical efficiency first proposed in [60].

$$Sn(t) = Sn(t) * A_m e^{-j[f_m(Sn(t)),ph_m]} \tag{6.1}$$

Ideally the correction function should be a memory capable algorithm that is only applied to the outphasing phase angle of the outphasing signals in each path. An example of such a function is outlined in equation 6.1. The correction function would have to be to the power of an exponential, as a result the extraction of the coefficients A_m and vector ph_m would require a non-convex optimisation algorithm. While this is possible as previously presented in [117], the increase in the number of coefficients associated with a non-linear memory capable function would dramatically impact the number of possible solutions, increasing the computational complexity when deriving a solution. Currently this is an impractical approach.

The modelling algorithms that were presented in Chapter 5 can accurately characterise the outphasing amplifier, however only a select few are suitable for consideration as pre-distortion algorithms. Of the dual path models presented only the direct outphasing algorithm maintains a constant envelope outphasing signal. The amplitude distortion, the two path Volterra series and the artificial neural network models all alter both the amplitude and phase of the signal and therefore are not suitable algorithms for the proposed digital outphasing module. However these algorithms should be revisited for the linear back-off outphasing amplifier, as amplitude information can be passed to the output combiner through the amplification stages.

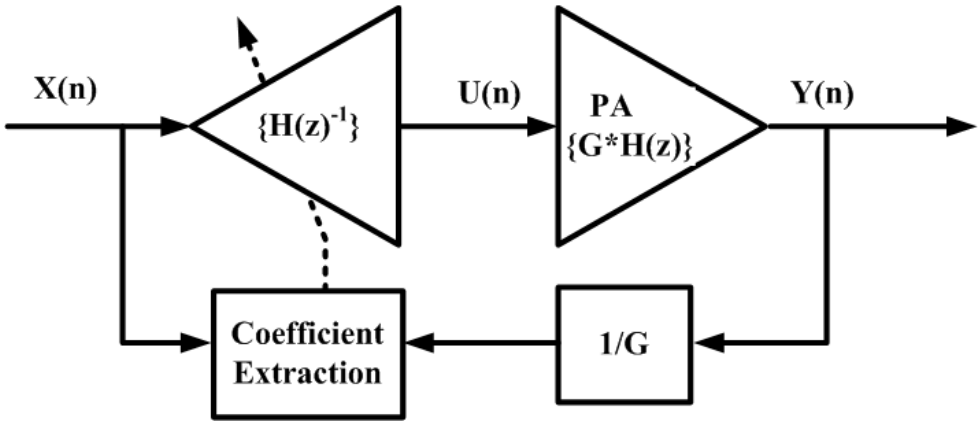


Figure 6.8: Direct learning architecture

Of the remaining algorithms the Volterra series and vector switched Volterra are capable of correcting memory non-linear functions. They do not effect the amplitude of the outphasing signals as they are implemented before the signal component separator. Single input algorithms require the calibration of the small signal system and the characterisation of the amplifier outphasing lookup table to fully extract the maximum dynamic range from the outphasing amplifier. Both the Volterra series and vector switched Volterra will be evaluated and compared as correction functions.

6.3.1 DPD structure

In practice there are two main extraction techniques [128], direct and indirect learning architectures are outlined in Figures 6.8 and 6.9. In both cases the aim is to extract the fixed point inverse function of the non-linear system, in this case a power amplifier. While both techniques aim to achieve the same result they have strengths and weaknesses which are as follows.

Direct learning trains the pre-distortion function on-line, observing the amplifiers output the weights are updated in order to minimise the error between the input signal $X(n)$ and the output amplified signal $Y(n)$. This method is robust to measurement noise and is immune to stability issues which can occur. However as the weights are updated in real time a system with a large amount of available resource is required to be implemented as a batch estimation process is required, resulting in high computational complexity. This is a limiting factor for many implementations.

Indirect learning uses a post inverse model to calculate the weights off-line. The extraction

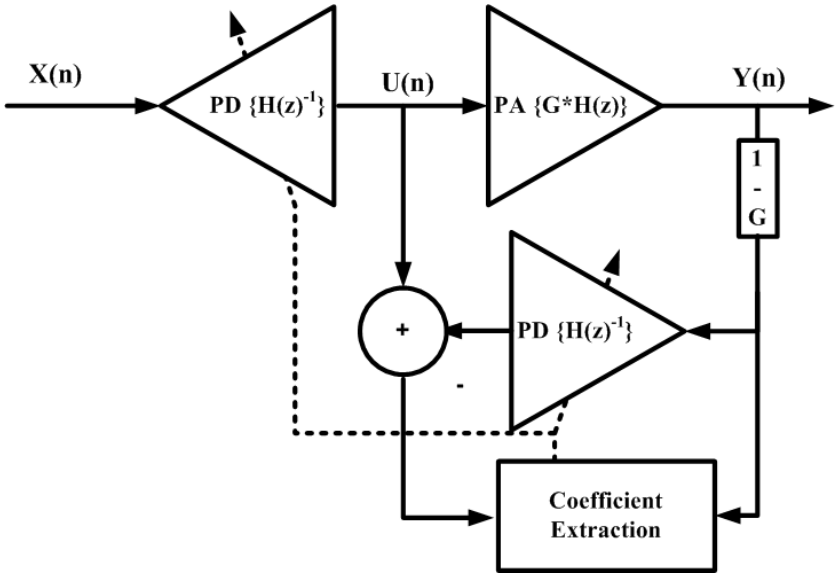


Figure 6.9: Indirect learning architecture

process can then be implemented using iterative algorithms, greatly reducing the system resources required and computation complexity compared with a batch approach. However this benefit comes at the cost of possible stability issues and a susceptibility to measurement noise. This problem has been mitigated to some extent by using more appropriate training algorithms for example a stochastic conjugate method presented in [129], or thorough modification of the signal information with single bit ridge regression to improve the condition factor [130]. Currently indirect training algorithms are the most popular due to resource constraints in base station applications.

6.3.2 DPD extraction algorithm

The digital pre-distorter is arranged as outlined in Figure 6.9. Given the construction of the test bench the indirect learning algorithm is more suitable as the calculation of the coefficients can be performed off-line. As outlined the indirect approach can be sensitive to measurement noise and changes in the amplifiers state of operation. To mitigate this the least squares approximation is chosen. Presented in 2.6.1 the least squares training algorithm has increased robustness to measurement noise. The proposed models will be constructed of differently dimensioned Volterra series functions. The Volterra series is outlined in detail in 2.5.2.4 and presented in equation 6.2. It consists of a linear vector of coefficients h_k, and a rectangular non-linear matrix of input values $\mathbf{X}$ outlined in 6.3. Where y is the output, x is the input, h

represents the Volterra coefficients, k is the order of non-linearity and q is the memory depth.

$$y(n) = \sum_{k=0}^{K} \sum_{qk=0}^{Q_k} h_k(q_k) x(n - q1) \prod_{m=1}^{(k-1)/2} x(n - q_{2m}) x^*(n - q_{2m+1}) \tag{6.2}$$

$$\mathbf{X} = x(n - q1) \prod_{m=1}^{(k-1)/2} x(n - q_{2m}) x^*(n - q_{2m+1}) \tag{6.3}$$

Equation 6.2 can be re-written as:

$$\mathbf{y} = \mathbf{X}h \tag{6.4}$$

The least squares approximation is therefore:

$$h \approx (\mathbf{X}^H \mathbf{X})^{-1} \mathbf{X}^H \mathbf{y} \tag{6.5}$$

where $\mathbf{X}^H$ is the complex transpose of the matrix $\mathbf{X}$. The steps for extracting the coefficients for the chosen pre-distortion algorithms are outlined below, in the case of the standard Volterra series no segmentation is carried out.

1. Capture the input data $U(n)$ and the output data $Y(n)$ for the power amplifier.
2. Form the matrix of non-linear terms for the chosen Volterra series $\mathbf{U}$.
3. Perform segmentation analysis where required.
4. Parse the rows of the extract matrix $\mathbf{X}$ and the captured data Y(n) into appropriate segment matrix's.
5. Extract the coefficients $\mathbf{w}$ for each segment.
6. Apply DPD function to the input signal $X(n)$
7. Evaluate the output of the PA if spectral requirements are met end process, else return to step 1.

6.3.3 Volterra Series

A comprehensive overview of amplifier characterisation techniques has been carried out in Section 2.5. Incorporating each possible combination of *P-th* order non-linear terms and *M*

memory taps in a summation of multidimensional convolutions [75]. Therefore it can be determined that special cases of the Volterra series such as Weiner, Hammerstein, Memory polynomial and Generalised memory polynomial are encapsulated within the full Volterra kernel.

The full complex form of the Volterra series is not efficient, however it serves as an excellent platform from which to compare the algorithms presented in the previous chapter as well as the novel implementations designed specifically for outphasing power amplifiers. The modelling performance of the Volterra series has been presented in Section 4.2.1. The model is capable of characterising the non-linear effects in band and in the adjacent channels, however the algorithm has some difficulty fully characterising wide-band, high order non-linear components.

The model dimensions discovered during characterisation analysis are also the optimal solution for linearisation, the polynomial order is chosen to the 7th and three memory taps are used. This was confirmed by investigating as series of model configurations, the non-linear order and memory taps were swept using the combinations [3, 5, 7, 9] and [1, 2, 3, 4] respectively. An off-line indirect learning process is used to extract the coefficients. Using the least squares algorithm ensured that the measurement noise did not greatly impact the training process. The linearisation process is an iterative one, and to achieve a steady state performance level a total of three iterations are required. The linearisation performance improved with each iteration -38 dB, -42 dB, -44 dB ACPR respectively. The spectral output of the amplifier with the third iteration of DPD is presented in Figure 6.10.

6.3.4 Vector Switched time series

In the characterisation analysis carried out in chapter 4 the single path, vector switch Volterra resulted in not only the most accurate but also one of the most efficient implementations. As a result it has been chosen for further study as a linearisation technique for outphasing amplifiers. As demonstrated in Chapter 5 there is performance to be gained by optimising both the time series and the vector quantisation algorithm, in the results section we consider both the k-means self organising maps as a segmentation method. The analysis performed in Chapter 3 and Section 6.2.1 emphasizes the occurrence of memory effects with respect to output power. By applying a segmented approach the different forms of memory across the output power

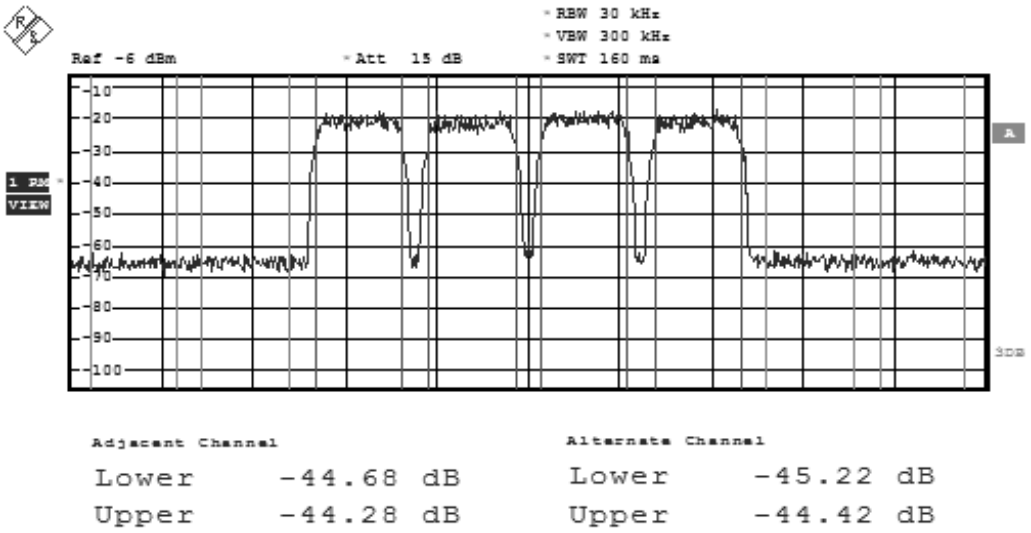


Figure 6.10: Digital pre-distortion measurement results for the Volterra algorithm.

range can be more accurately classified.

The polynomial order is chosen to be five and three memory taps are used. This was confirmed by investigating as series of model configurations, the non-linear order and memory taps were swept using the combinations [3, 5, 7, 9] and [1, 2, 3, 4] respectively. Similarly the number of segments was also swept however as with the modelling the optimum number was found to be 10. These settings were kept constant for both the K-means and SOM clustering methods and the performance of each is presented in Figure 6.11 and 6.12.

The pre-distortion algorithm is extracted as outlined in section 6.3.2 and the resulting coefficients are stored in a LUT corresponding to the segmentation code book in the case of k-means of the output of the SOM. The linearisation performance improved with each iteration -40 dB, -44 dB, -45 dB ACPR and -40 dB, -45 dB, -46 dB ACPR for the k-means and the SOM respectively. Further iterations did not yield an increase in linearisation performance. The performance from the linearisation process corresponds with the results form the modelling section, taking the ACPR values to be the minimum recorded from the FSQ a difference of less than 1 dB exists between upper adjacent and alternative channel power levels.

6.3.5 Three Dimensional Vector Switched Volterra

From previous investigations it was determined that the outphasing angle will vary with frequency, particularly for a Chireix combiner with load compensation. This directly impacts

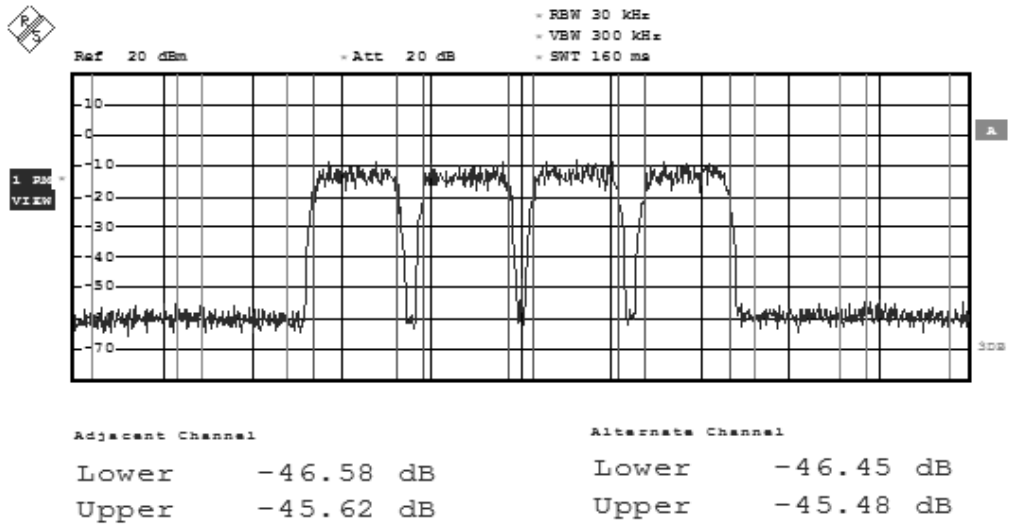


Figure 6.11: Digital pre-distortion measurement results for the K-means vector switch Volterra algorithm.

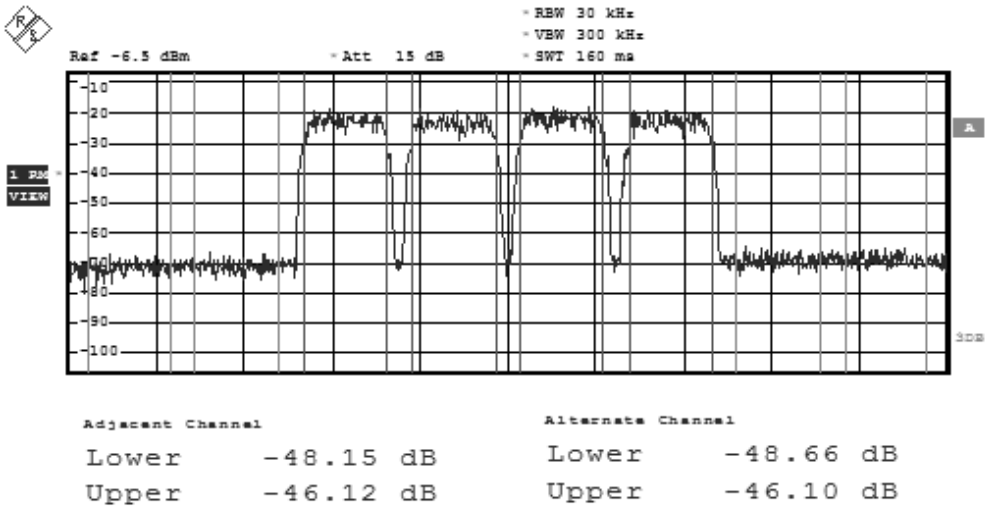


Figure 6.12: Digital pre-distortion measurement results for the self organising maps vector switch Volterra algorithm.

the output amplitude and phase of the amplified signal. As described in the introduction the majority of the non-linearity for the amplifier resides at lower output powers. This characteristic increases as the bandwidth of the modulated signal increases, as discussed in Section 6.2.1.

For single path implementation, the segmented time series provided the most robust solution. This is achieved by increasing the number of time series which can characterise the system, providing custom solutions for local non-linear function, which are independent of other localised regions of operation. To further increase the algorithms capability at lower output powers it was decided to introduce an additional clustering parameter, resulting in a three dimensional feature space from which the segments could be determined. For optimum performance the parameter must be a characteristic of the input signal, with relevance to the frequency of operation of the outphasing amplifier.

In [131] the author presents a series of methods for determining the instantaneous frequency of a modulated signal. In many cases this is difficult and computationally intensive to achieve, however in the case of constant envelope, phase only modulated signals the simplified formula of equation 6.6 can provide a accurate estimation of the signal frequency. From the analysis carried out in Section 6.2.1, and more particularly the information in Figure 6.4 it was determined that the signal's phase is the main component in determining the outphasing signal frequency and amplitude.

$$f_i = \frac{1}{2\pi}\frac{d\phi(t)}{dt} \tag{6.6}$$

Therefore for simplicity it is assumed that the phase of the input signal $\phi_{input}(t)$ is a good approximation the phase of the outphasing signal $\phi_S(t)$. With this assumption, it is therefore possible to assume that the instantaneous frequency of both outphasing paths S_1 and S_2 are approximately equal. In addition examining the findings presented in Figure 6.5 the rate of change of signal phase essentially only experiences large deviations at lower signal powers. As a result the rate of change of signals phase is an ideal parameter to include in the vector quantisation process in order to increase the number of segments at lower power. In addition this parameter of the input signal enabling further segmentation based upon the instantaneous frequency of the outphasing signal, a metric which cannot be obtained through evaluation of

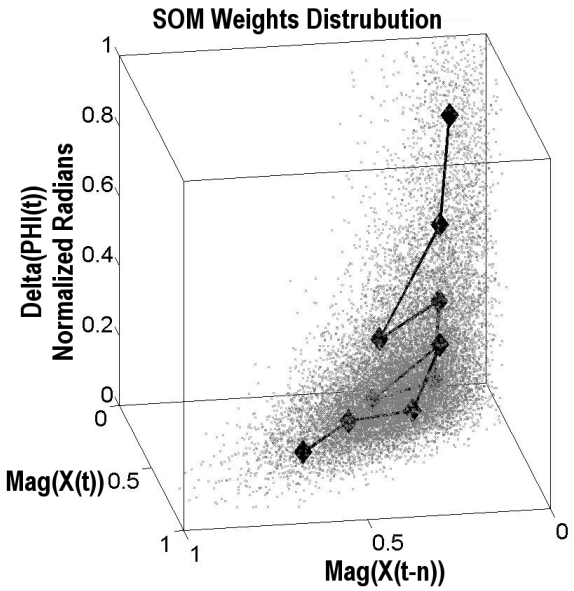


Figure 6.13: Three dimensional self organising maps. The grey points represent the distribution of data points with respect to the X, Y and Z attributes. The black diamond markers represent the locations of the center of the clusters, in the case of the SOM the locations of the individual neurons.

the input signal amplitude alone.

Equations 6.7 and 6.8 show the method of calculating a delta phase value where $\phi(t)$ is the phase of the current input signal $S(t)$, $\phi(t-n)$ is the phase of time delayed sample and $A(t)$ is the amplitude modulation component of the input signal. The unwrap function is used to remove discontinuities associated with phase as it rotates about the unit circle.

$$S(t) = A(t)e^{(-j2\pi\phi(t))} \tag{6.7}$$

$$\delta\phi(t) = unwrap(\phi(t) - \phi(t-n)) \tag{6.8}$$

Investigation into multi-dimensional clustering algorithms outlined some possible issues using K-means in practice. As the number of dimensions increases the code book, or LUT, for K-means will increase exponentially, possibly impacting the practicality of the hardware implementation. For this reason and the performance advantages outlined in Section 5.3.4 self organising maps are chosen as the vector quantisation method. Figure 6.13 illustrates the three dimensional mapping process proposed for outphasing amplifiers. The black diamond markers

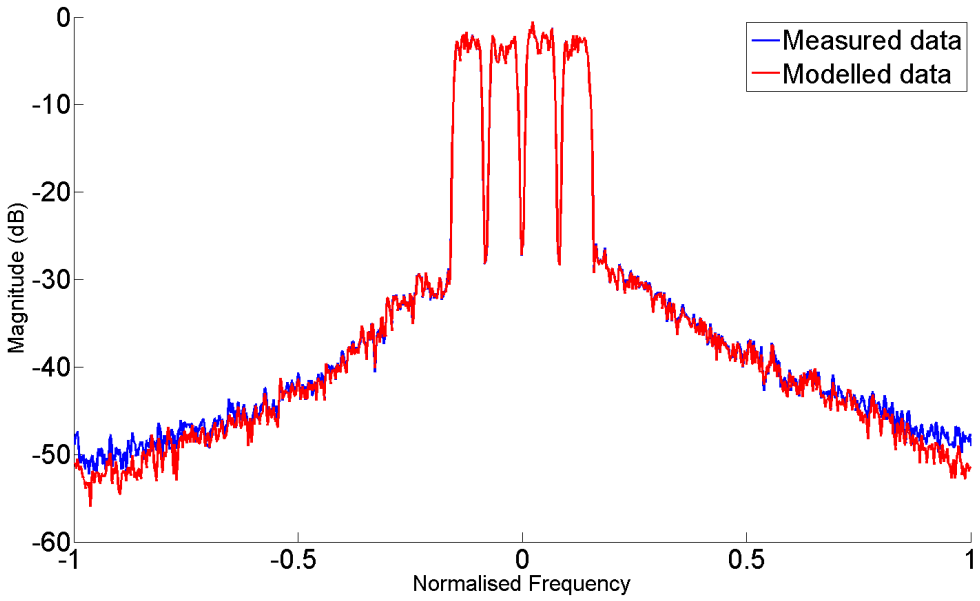


Figure 6.14: Modelling results for VSV Volterra model utilising three dimensional SOM clustering - MSE of -49.6 dB, NMSE of -37.5 dB

represent the centres of the individual clusters. In the original method these are solely on the lower plane of axis X and Z. However with the additional information clusters are formed in all three axis, providing increased diversity.

As with the models detailed in Chapter 5, the three dimensional vector switch time series is evaluated by its ability to characterise the amplifiers behaviour. The results of this are presented in Figure 6.14. The updated model is capable of reducing the normalised mean square error by an additional 1 dB while maintaining the wide band amplifier characteristics.

For linearisation the delay factor in the vector quantization function is a two tap delay. The individual Volterra series kernels have a 5th order non-linearity component with three memory terms. These optimum parameters were found by sweeping the values across the following ranges, non-linear order [3, 5, 7, 9], memory depth [2-5], delay taps for generating vector space [1-4] and number of segments in the vector space [6-15]. In the training process, vector quantization training is performed initially. The results are used to segment the training data and each time series is trained individually. The selected method of training the time series is a least squares algorithm. For stability of the training algorithm, QR decomposition is performed on the Volterra kernel matrix. The pre-distortion function was trained using five iterations,

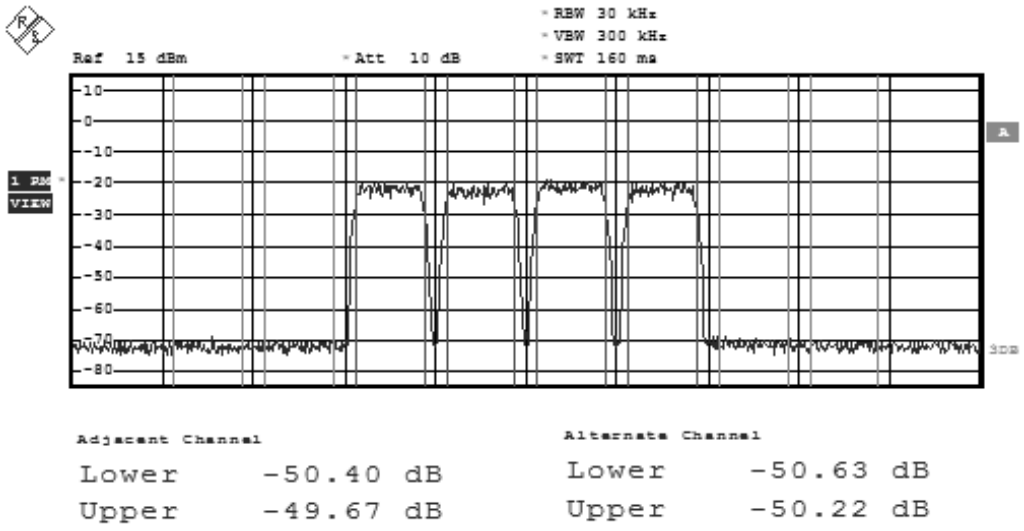


Figure 6.15: Digital pre-distortion measurement results for the three dimension vector switch Volterra algorithm.

additional iterations did not improve the linearisation effort. The resulting performance is presented in Figure 6.15.

6.4 Linearisation Analysis

In this chapter four memory capable linearisation algorithms are evaluated for the digital outphasing power amplifier. The multi-segment time series algorithms demonstrated improved characterisation accuracy for modelling of the outphasing power amplifier in Chapter 5, subsequently achieving comparable linearisation performance, experimentally validating their suitability for outphasing power amplifiers. While the multi-segment approach, vector switch Volterra, provided further improvements of between 2-3 dB when compared with standard Volterra, further analysis of the outphasing amplifiers characteristics indicated that additional performance could be achieved.

From analysis of the outphasing power amplifier at lower output power levels, under both static and dynamic operation, it was confirmed that memory effects are more pronounced when compared with higher output power levels. In order to improve the linearisation algorithms, it was determined that additional segmentation at lower output powers would be required. Specifically targeting the characteristics of the outphasing power amplifier, the rate of change of phase is combined with the existing signal amplitude feature space, generating a novel

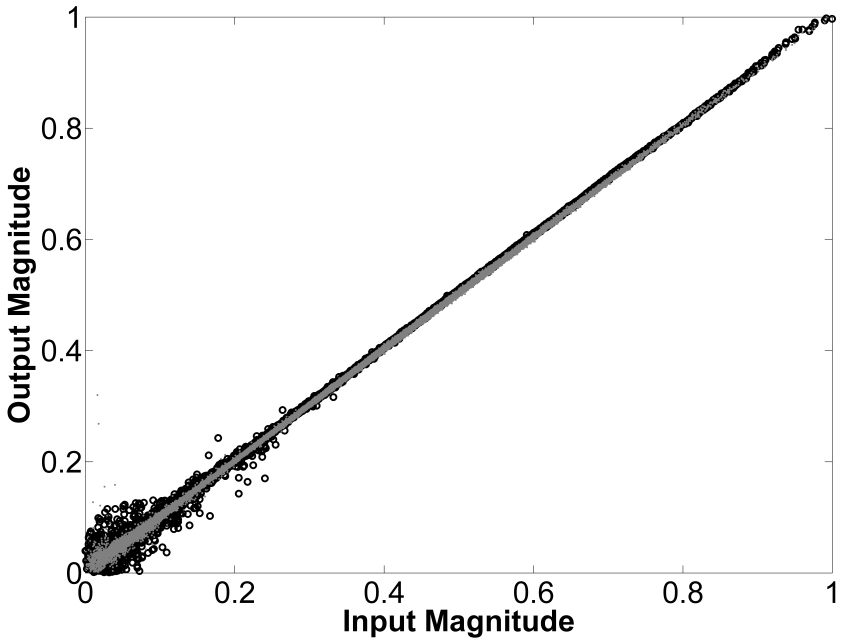


Figure 6.16: Comparison of memory at lower output power for VSV and 3D VSV. Standard VSV is presented in black and the 3D VSV is presented in grey

three dimensional vector quantisation map [2]. The modified vector space enabled additional segmentation to be applied to the lower output power region, as demonstrated in Section 6.2.1, more accurately describing the instantaneous frequency of the outphasing signal. Examining the AMAM plot of the linearisation with standard vector switch Volterra and the proposed modified algorithm improves linearity at lower output powers while maintaining linearity at higher output powers, this is highlighted in Figure 6.16.

This improvement achieved a further 2-2.5 dB linearisation performance. The optimum performance is demonstrated in Figure 6.17 with a linearisation performance of 49.5 dBc ACPR. The analysis from Figures 6.16 and 6.17 demonstrates an improvement over existing techniques, however the existence of residual outlines at low output power must still be further examined to achieve improved overall linearisation performance.

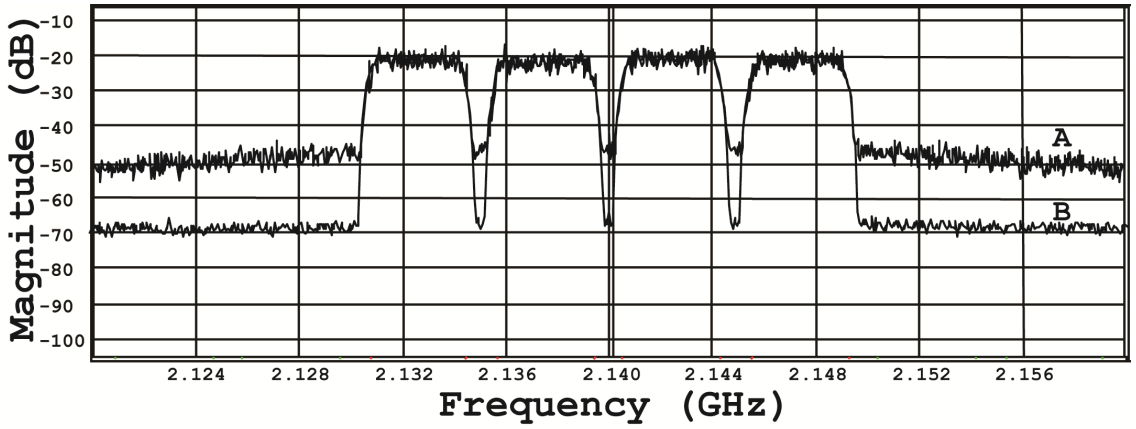


Figure 6.17: Illustration of un-linearised spectral plot (A), ACPR 26dBc, superimposed upon linearised spectral plot (B), ACPR 49.5 dBc. Linearisation performance greater than 23 dB with flat wideband performance.

6.5 Conclusions

In this chapter the linear operational bandwidth of the outphasing power amplifier is explored and three digital pre-distortion techniques are experimentally validated. Evaluation of results and measurement from the power amplifier confirmed that wideband operation required a memory capable algorithm. From the analysis carried out in Chapter 5 single input - output algorithms were determined to be the only memory capable methods viable for outphasing amplifier linearisation. Additionally the computational effort required to train single path linearisation algorithms is much simpler when compared with dual path.

The analysis of the operation of the outphasing amplifier across the frequency band which the outphasing signal occupies demonstrated the significant variation of the input-output function of the amplifier at lower output powers. A new method of segmentation was devised in order to enable improved characterisation of the outphasing amplifier. Using additional parameters in the input signal a novel three dimensional feature space, which more accurately represented the frequency response of the outphasing power amplifier was developed.

A single input-output linearisation algorithm can successfully correct a calibrated two path outphasing system, confirming the deviations observed at lower output powers are deterministic and therefore correctable. Utilizing a vector switch Volterra linearisation method with SOM, the linearisation performance of the system for wide-band multi-carrier signals was improved by as much as 6.5 dB over standard linearisation methods and 2.5 dB over existing segmented

linearisation methods. As a result the performance of the linearised outphasing power amplifier improves upon existing published outphasing amplifier linearisation performance. The linearisation of a 20 MHz modulated signal is a first for outphasing amplifier topologies.

CHAPTER 7

Bandwidth Expansion

Efficient operation of the digital outphasing power amplifier is enabled through switch mode amplification of constant envelope signals. The signal component separator encodes band-limited, amplitude and phase modulated signals onto coupled phase only outphasing signals to be amplified. The separation operation is fundamental to the amplifier operation, however the outphasing signals have very different spectral characteristics to the original input. The outphasing signals have varying degrees of spectral power at all frequencies within the signal sample rate as the phase transitions between π radians in both positive or negative frequencies. Statistically the majority of the outphasing signals power resides within 3-4 times the original signal bandwidth, however some information at higher frequency components is relevant to the recombination process. The authors in [99] analyse bandwidth expansion and estimate that a sample rate of between 10 and 12 times the original signal bandwidth is required in order to accurately re-construct the required signals in the analogue domain. The outphasing signal bandwidth is a requirement of all components in the system including the amplification stages. As the bandwidth of the communications signal to be amplified is increased, for example multi-carrier third and fourth generation signal standards, the design of the RF components becomes more challenging.

In this chapter a novel method of reducing bandwidth expansion is proposed [4]. Signal

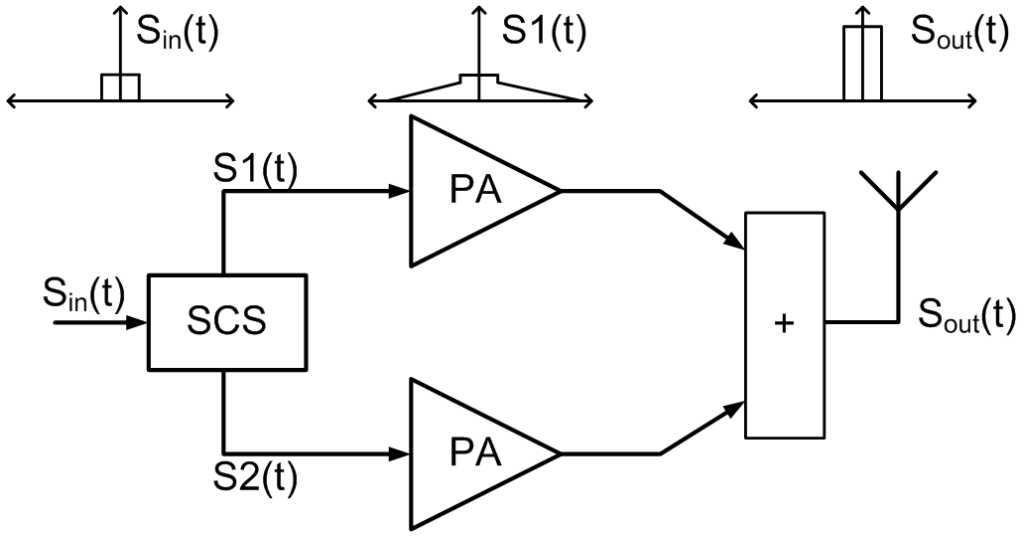


Figure 7.1: Top level view of the outphasing power amplifier depicting signal bandwidth through out the amplifier line-up.

processing on the input modulated signal is applied before the SCS, reducing the bandwidth of the outphasing signal. The proposed method is developed to maintain the constant envelope characteristic of the outphasing signal. Validation is carried out using both simulated and experimental test-benches, demonstrating the benefits and drawbacks associated with the proposed solution.

7.1 Bandwidth Expansion

The outphasing power amplifier is introduced at length in Chapter 3. A summary of the relationship between the input modulated signal and the outphasing signals are outlined in equations 7.1 and 7.2. The outphasing signals $S1(t)$ and $S2(t)$ are a function of the input signal phase $\theta(t)$ and the outphasing angle $\rho(t)$. In [131] the author presents a series of methods for determining the instantaneous frequency of a modulated signal. In many cases this is difficult and computationally intensive to achieve, however in the case of constant envelope modulated signals, a simple formulation presented in equation 7.3 can provide an accurate estimation of the signals instantaneous frequency.

$$S(t) = A(t)e^{-j\theta(t)} \tag{7.1}$$

$$S_n(t) = \frac{1}{2}e^{-j(\theta(t)\pm\rho(t))} \qquad where \quad \rho(t) = acos(A(t)) \tag{7.2}$$

$$f_i = \frac{1}{2\pi}\frac{d\phi(t)}{dt} \tag{7.3}$$

Figure 7.2 presents the Fourier transform of the outphasing signal S_n, the constant amplitude signal modulated with only signal phase component $\theta(t)$ and the constant amplitude signal modulated only with the input signal amplitude component $\rho(t)$. It is clearly visible that the signal phase $\theta(t)$ is responsible for the majority of the bandwidth expansion tracking the outphasing signal almost completely. The signal encoded with signal amplitude is responsible for some bandwidth expansion, of which the majority is located within twice the signal bandwidth of the original signals with the largest number of occurrences at a frequency close to the signals center frequency, for a base band signal this is the DC value.

$$\Delta\phi(t) = \Delta(\theta(t) \pm \rho(t)) \approx \Delta\theta(t) \tag{7.4}$$

$$\Delta\phi(t) = unwrap(\phi(t) - \phi(t-n)) \tag{7.5}$$

From the spectral analysis it is possible to make the assumption that the frequency response of the outphasing signal can be approximated by the exponent signal phase $\theta(t)$, this approximation is outlined in equation 7.4. The derivative of the signal phase when sampled discretely is presented in equation 7.5. In the following section the formulation and verification of the theory that by modifying the phase transitions of the modulated signal $S(t)$ the bandwidth expansion of the outphasing signals $S1(t)$ and $S2(t)$ can be controlled.

Further analysis of signal phase in relation to signal amplitude reveals that the magnitude of the rate of change of phase is inversely related to the signal amplitude for a modulated signal. Figure 7.3 illustrates that the higher rates of change occur as the signal is close to the zero crossing point. Considering the unit circle, a two dimensional representation of a modulated signal, if the complex signal envelope transitions between two data points and passes through the center of the unit circle it will cause a phase shift of $\mp\pi$ radians to occur, the largest possible phase delta and according to equation 7.3 the largest output frequency to occur, equal to the

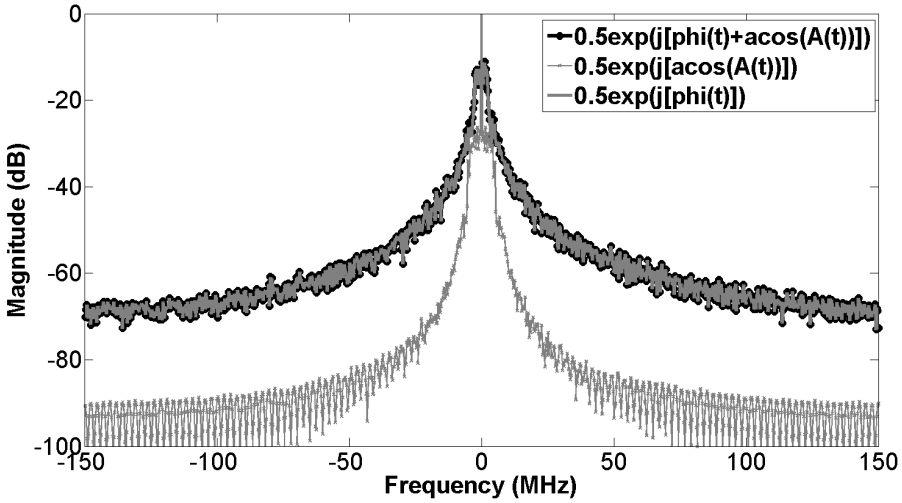


Figure 7.2: Fourier analysis of outphasing bandwidth expansion. The full outphasing signal $\frac{1}{2}e^{j(phi(t)+acos(A(t)))}$ is represented by a black line with a circular marker. A modified outphasing signal using only signal amplitude $\frac{1}{2}e^{jacos(A(t))}$ is represented by a grey line with cross markers. A modified outphasing signal using only signal amplitude $\frac{1}{2}e^{(jphi(t))}$ is represented by a grey line.

sample rate of the signal. By controlling transitions such as these it is possible to reduce the bandwidth expansion of the outphasing signals. This relationship will be further examined in Section 7.2.

7.1.1 Bandwidth limitation in outphasing systems

Our analysis attributes the source of bandwidth expansion to high frequency phase components about the zero crossing point. This section will explore the effects of a band limited outphasing system on a modulated QAM signal. A quadrature amplitude modulated (QAM) signal [132] consists of two digital signals which are orthogonal representing discrete data points on a constellation diagram. A higher number of data points in the constellation increases the spectral efficiency at the expense of overall robustness. A 5 MHz QAM signal with a sample rate of 100 MHz using a 64 point constellation diagram is generated for system evaluation. An ideal outphasing system model using the arc-cosine amplitude conversion function is used for the outphasing signals. Modified amplitude and phase are analysed in the frequency domain and presented in Figure 7.3.

To analyse the effects of band limiting of the outphasing signals an ideal filtering function is applied. The filtering function chosen for this analysis is a fast Fourier transform brick wall

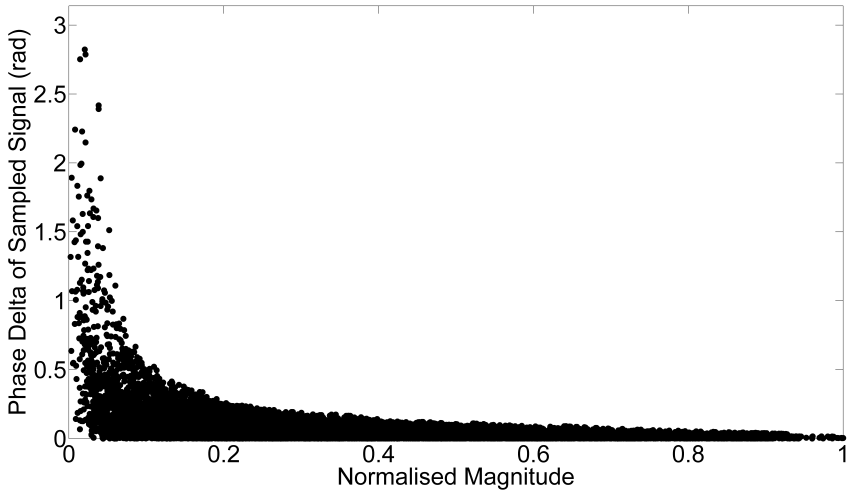


Figure 7.3: Delta of the signal phase with respect to signal amplitude.

function. A fast Fourier transform (FFT) [72] function in conjunction with a custom filter mask is used to suppress frequency component outside of the desired band of interest. The process is outlined in equations 7.6, 7.7 and 7.8 where the custom mask is function H_k.

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi K \frac{n}{N}} \quad K = 0, \cdots, N-1 \tag{7.6}$$

$$X_k^{'} = X_k * H_k \tag{7.7}$$

$$x_n^{'} = \frac{1}{N} \sum_{k=0}^{N-1} X_k^{'} e^{-j2\pi K \frac{n}{N}} \quad K = 0, \cdots, N-1 \tag{7.8}$$

There are two main outphasing system configurations: saturated PA outphasing; or full digital outphasing PA. This refers to the operation of the amplification stages that amplify the outphasing signals before recombination. The fundamental operation for a constant amplitude outphasing signal both systems operate exactly the same. Band limiting or filtering a constant envelope signal will introduce some amplitude modulation into the signal, resulting in slightly different operation from the outphasing topologies in each case.

Our analysis of band limited outphasing systems will focus on the following amplifier configurations:

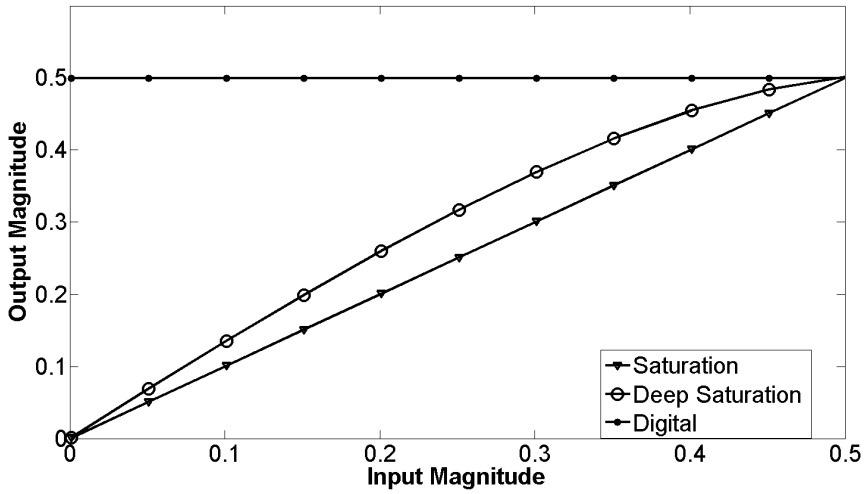


Figure 7.4: The input output relationship of different classes of outphasing power amplifier used in the bandwidth limitation analysis.

1. Saturated outphasing amplifier using linear amplifiers.

2. Deeply saturated outphasing amplifier using linear amplifiers.

3. Digital outphasing amplifier using switch mode amplifiers.

The systems are simulated in Matlab assuming an ideal outphasing system. The digital outphasing system is simulated using a hard limiting function, the deep saturated outphasing amplifier is simulated with a non-linear polynomial function. The response of each is presented in Figure 7.4. Analysis is carried out as the channel bandwidth of the outphasing system is reduced from 100 MHz to 10 MHz. Analysis is focused on the impact of the filtering to the signals EVM, output ACPR and the modification to the outphasing signals, particularly the inclusion of amplitude components to the outphasing signal.

Figure 7.5 and 7.6 visualise the impact limiting outphasing bandwidth has on the signal linearity. In previous publications a value of between 10-12 times over-sample ratio was stated as a requirement for linear outphasing amplification, this is confirmed in this analysis as the impact on linearity starts to increase as the bandwidth is reduced below 12 times oversample ratio (60 MHz). There is variation between the different amplification methods. Bandwidth reduction impacts the deeply saturated and digital outphasing architectures the most. An amplifier that just enters the saturation region maintain acceptable EVM and ACPR values. This however comes at a cost, in Figure 7.7 the resultant PAPR of the filtered outphasing

signals is presented, the filtering process introduces amplitude modulation into the outphasing signals, which will greatly impact system efficiency. The amplitude modulation is quantified using peak to average power ratio (PAPR), an amplifiers efficiency is determined in many cases by the average operating amplitude relative to peak output power. If the example of a GaN Class B amplifier, presented in section 3.5.2.1, is used to compare the effects of amplitude modulation, a signal with 2-3 dB PAPR will cause a drop of $15 - 25\%$ drain efficiency. The outphasing power amplifier's efficiency is dependent on achieving maximum efficiency from the amplification stages. The reduction in efficiency from bandwidth limitation would nullify much of the gains from the architecture.

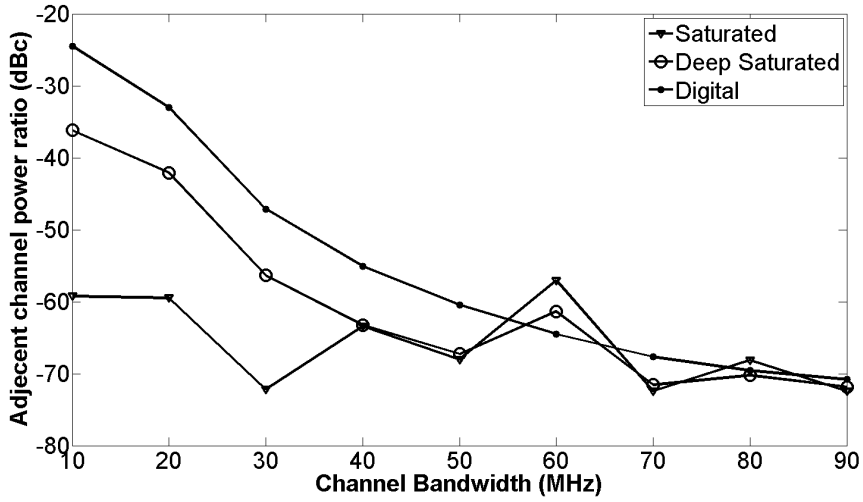


Figure 7.5: The effect of bandwidth limitation on linearity, represented here by the ACPR of recombined signal

7.1.2 Existing bandwidth limitation solutions

In [15] the authors present a method of bandwidth limitation of the outphasing signals by processing the SCS decomposed outphasing signals. The decomposed signals are then recombined and filtered. The technique in [15] is outlined in Figures 7.8 and 7.9. The proposed method in this chapter concentrates on modifying the input signal in the time domain, applying an output filtering process only where required. Ultimately both techniques aim to achieve the same result, a band-limited outphasing signal, increased robustness to system bandwidth limitations with minimal impact to signal linearity.

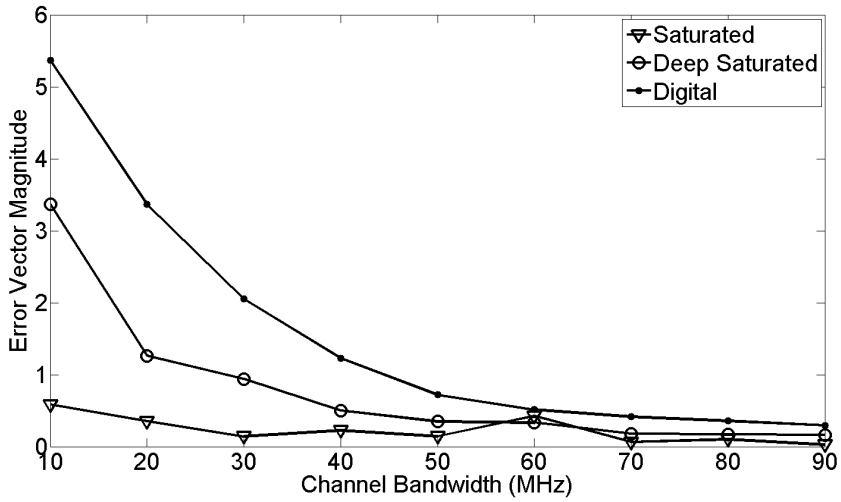


Figure 7.6: The effect of bandwidth limitation on EVM of recombined signal

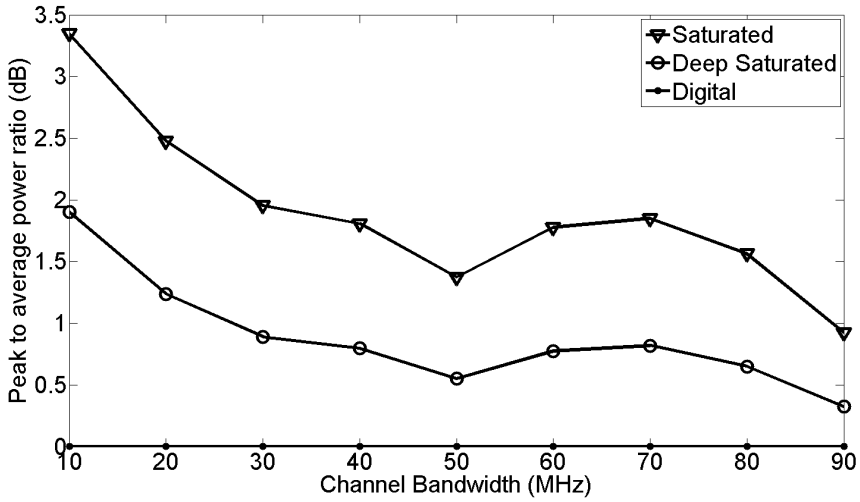


Figure 7.7: The effect of bandwidth limitation on PAPR of outphasing signal

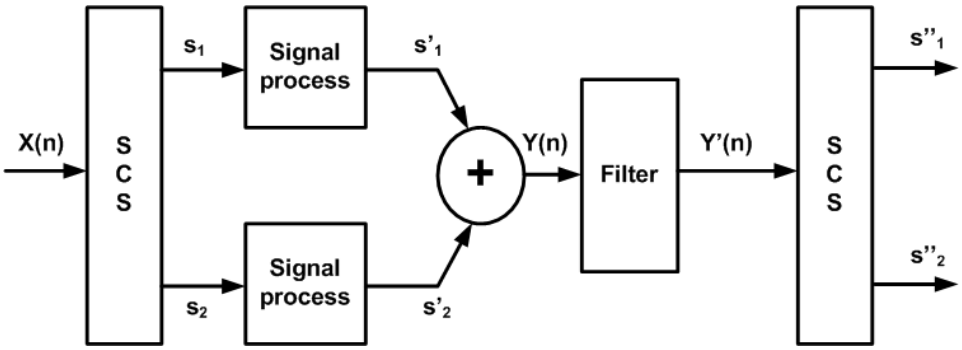


Figure 7.8: Bandwidth limitation process in [15].

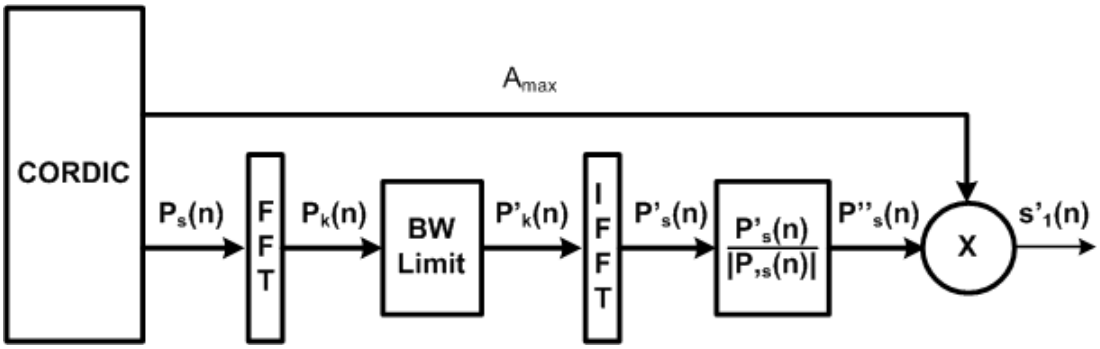


Figure 7.9: Bandwidth limitation outphasing signal process in [15].

7.2 Bandwidth expansion reduction

From the analysis that has been carried out so far it has been determined that the cause of the bandwidth expansion is the rate of change of signal phase. Large phase changes occur at lower output powers, in particular as the signal transitions through the centre of the unit circle. Using the knowledge gained from Section 7.1 an algorithm is proposed in this work to limit bandwidth expansion, altering the composition of the modulated input signal $S(t)$ only.

The signals phase must still make the phase change or the signals information would be altered. However making the transition over a small number of samples results in a large frequency component, the solution is to modify the trajectory over a number of samples, gradually making the transition from the initial phase value to the destination phase value. In this analysis the length of the window will be N number of samples. The starting point and the destination point will be an equal distance from the zero crossing point. The start point will be called *ni* and the destination point will the *nd*. The value of the window length N will determine the frequency reduction that can be achieved, higher the value of N the greater the bandwidth reduction. The value of N is also directly related to the error which is introduced into the signal, the longer the value of N the more data points that will be effected, increasing the impact on EVM.

A balance between signal accuracy and the achievable bandwidth reduction must be found. The windowing function will also determine the signal error and effectiveness of the bandwidth reduction achieved. The window must gradually transition between existing signal phase and the modified signal phase in order to prevent discontinuity in the signal. The window must also achieve full conversion at the zero crossing point therefore the modified signal phase must be at its maximum at this point. Several windowing structures which fit the criteria are investigated. In this work, the Tukey window, the Kaiser window, the Chebyshev window and the Gaussian window.

Ideally the modified signals would occupy the original signal bandwidth and have a flat out of band response. However, when aggressive bandwidth reduction is required some filtering of the processed signal is needed in order to remove unwanted out of band signal components. The characteristics of the filter must be controlled to avoid full re-generation of the high frequency phase components. For these reasons a balance must be found between the spectral

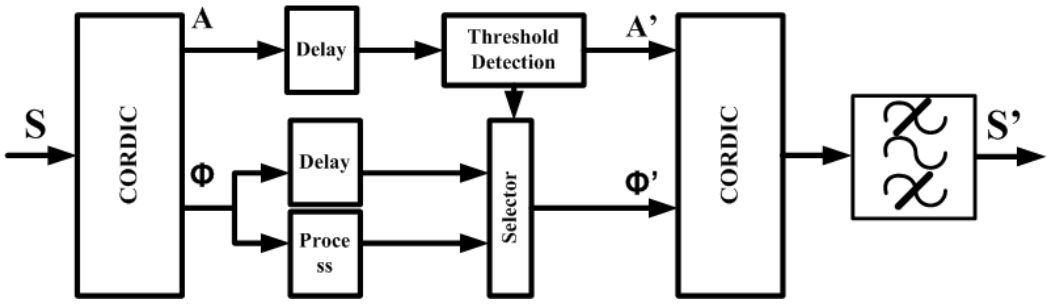


Figure 7.10: Overview of bandwidth expansion reduction process.

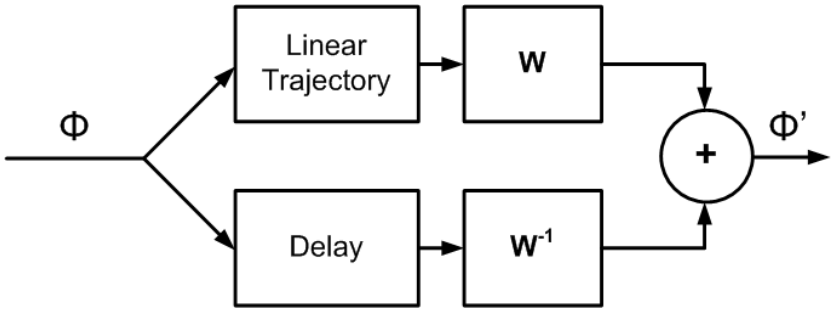


Figure 7.11: Bandwidth reduction process. W and W^{-1} are windowing functions of length L. The linear trajectory plots a linear slope between the starting and ending data points to generate a low frequency phase response.

characteristics of the signal and the bandwidth reduction performance.

The steps of the algorithm are outlined below:

1. Identify zero crossing points - the most likely position of a high frequency phase component.

2. Modify the phase trajectory using a window function of length N. The length will determine the new frequency component of signal phase.

3. The resulting signal is then filtered to remove any out of band components generated from the new phase trajectory.

7.3 Evaluation and optimisation

Implementation and evaluation of the proposed bandwidth expansion reduction algorithm is carried out in MATLAB. As with any signal modification the impact to signal linearity and spectral properties must be evaluated. The measure for bandwidth expansion reduction is

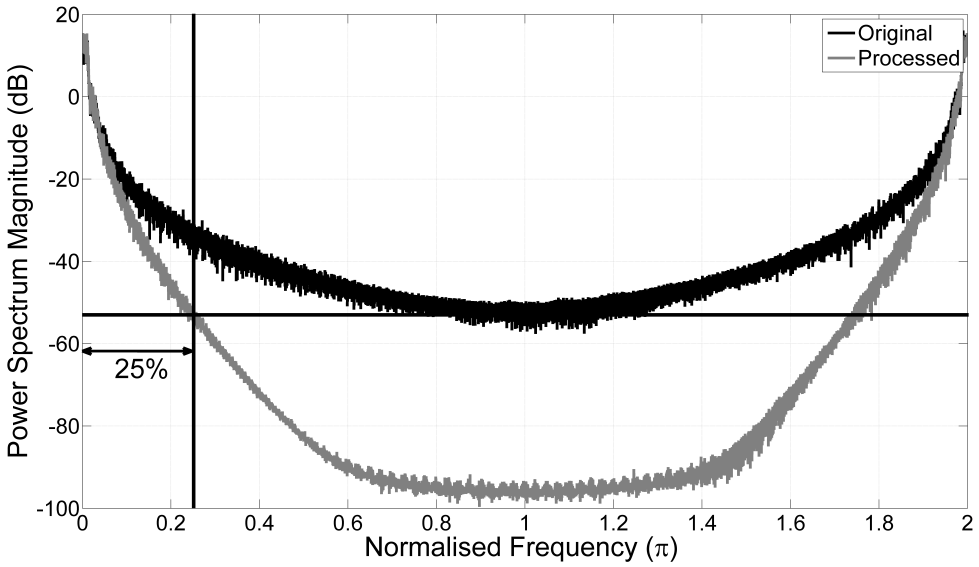


Figure 7.12: Bandwidth expansion reduction measurement.

determined as the percentage reduction of outphasing signal magnitude from the minimum signal magnitude for the original outphasing signal. An example of this is demonstrated in Figure 7.12. The black signal is the original signal and the grey signal is the processed signal. For similar output performance of the outphasing PA the bandwidth expansion of the outphasing signals can be reduced by a factor of four. In our analysis we assume that the original signal bandwidth expansion to be half the sample rate of the modulated signal. The new outphasing signal bandwidth are calculated with reference to the power level of the outphasing signals at that point.

Quadrature amplitude modulated signals are used to analyse the performance of the bandwidth reduction process and its impact on an amplitude modulated signal. The QAM signal is chosen for two very practical reasons, during the evaluation of the bandwidth reduction processing in simulation it is possible to quickly and computationally efficiently evaluate the error introduced into the signals data symbols.

$$EVM_{RMS} = \left[\frac{\frac{1}{n} \sum_{n=1}^{N} | S_{ideal}(n) - S_{meas}(n) |^2}{\frac{1}{n} \sum_{n=1}^{N} | S_{ideal}(n) |^2} \right]^{\frac{1}{2}} \tag{7.9}$$

The identification of the rapid change of phase is currently processed by a threshold

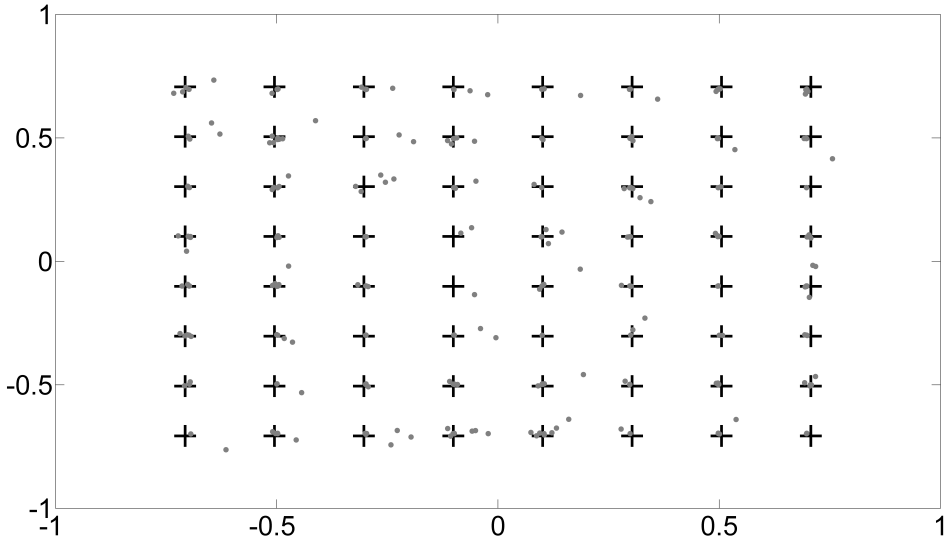


Figure 7.13: Modified constellation diagram of BWR signal, an illustration of the effect of bandwidth reduction on a 64 QAM constellation diagram.

detection method. If the amplitude of the modulated signal $S(t)$ crosses a lower boundary threshold M the algorithm will be applied to $N/2$ previous and $N/2$ preceding signal samples. The threshold M is variable and directly impacts the amount of the signal that is processed. This method does not guarantee that all high frequency phase components are processed however from Figure 7.3 we can be confident that a large majority are processed.

The impact of the process on the signal information is carried out using a figure of merit called error vector magnitude (EVM). EVM is a common figure of merit for assessing the quality of digitally modulated telecommunication signals [133]. EVM expresses the difference between the expected complex voltage value of a demodulated symbol and the value of the actual received symbol. The expected complex signal value is the ideal constellation of the modulated signal. The EVM is calculated from the down converted signal values which correspond to the symbol locations. An example of the ideal constellation and the post processed signal is presented in Figure 7.13. The EVM calculation is outlined in equation 7.9 where S_{ideal} are the ideal constellation points and S_{meas} is the processed signal.

7.3.1 Simulated annealing

The algorithm now has various operators which can be tuned in order to achieve a balance between bandwidth reduction and the impact on signal data. A modification to the threshold value will impact the required length of the windowing function. As the parameters and design goals are interlinked it was decided to perform an optimization function in order to determine the values of the algorithm parameters which provide the best compromise between bandwidth reduction and signal accuracy. The optimization algorithm chosen is simulated annealing, using a user defined cost function the algorithm searches the feature space of possible parameters. The goal is to minimize the cost function within the given boundaries.

$$Pr(i) = q_i(c) = \frac{1}{Q(c)} \cdot e^{-\frac{C(i)}{c}} \tag{7.10}$$

Simulated annealing optimisation is based on the comparison between problem solving of large combinational optimisation problems and the simulation of annealing solids [134]. Annealing is the process of heating a component to a maximum pre-defined temperature, followed by slow cooling period. In this way all partials arrange themselves in the low energy ground state of their region provided that enough heat has been applied and a sufficiently slow cooling period is observed. This process is translated into an algorithm which can be applied to an optimisation problem. In the algorithm the heating is the formation of a feature space with pre-defined probability distribution. The algorithm makes a decision on its movement to a neighbouring state based upon the probability function and the temperature decay constant. the probability is determined by the Boltzmann distribution and outlined in equation 7.10 where the cost function is C the control parameter c is the temperature control and Q is the normalization constant dependant of the control parameter. The algorithm follows the following steps:

1. Initialize parameters to starting state s_0
2. Perturb the state from i to $i + 1$
3. If the cost function is lowered then accept the new state *or* if the cost function is is greater than a random number between $0 \rightarrow 1$ then accept.
4. If the new state is accepted update the state s from i to $i + 1$.

5. If the stop criteria is achieved or a ”frozen” state is achieved output the current value of s else return to step 2.

Simulated annealing is particularly suited to the problem of searching a large feature space for an approximation to a global optimum. This heuristic technique may not be guaranteed to find the optimum solution in every case however given the quantized values of the window length and the small variation required in the threshold level for zero crossing detection the algorithm finds an optimum far quicker than manually searching. The process is repeated until the computational threshold is reached. The initial cost function as outlined in equation 7.11, is a function of the bandwidth expansion reduction process and the signals EVM where A and B are scaling factors to weight the importance of each figure of merit. For the following iterations A is set to 10 and B is varied [1-4], a tuning factor between bandwidth reduction and the impact to EVM. Table 7.1 presents the initial optimisation using the methods outlined above. The optimisation and therefore the cost function is working as expected, increasing the tuning parameter B controls the bandwidth reduction performance at the expense of signal EVM. This initial optimisation function is designed for algorithm development, outlined in the following sections.

$$G = BW * A + \frac{EVM_{rms}}{B} \tag{7.11}$$

Table 7.1: Initial results from optimization.

B	EVM(RMS)	BW Reduction
4	3	0.25
3	2.2	0.28
2	1.35	0.33
1	1.19	0.36

7.3.2 Windowing functions

The selected samples will have a new phase profile applied to the signal and will transition based upon the magnitude of a windowing function. The windowing function must have unity magnitude at its centre. This criterion ensures the process completely removes the large phase shift at the zero crossing point. The algorithm therefore will evaluate 4 windowing functions, the Gaussian window, the Kaiser window, the Tukey window and the Chebyshev window

outlined in equations 7.12 - 7.15, the composition of which is presented in Figure 7.14. The performance of the windowing functions are outlined in Table 7.2. The Chebyshev and the Kaiser result in the largest EVM but the best bandwidth reduction performance. The Tukey and the Gaussian windows have comparable bandwidth reduction and EVM however the Tukey is chosen for the following simulations as the impact on EVM is not as severe.

$$W(n) = e^{-\frac{1}{2}\left(\alpha \frac{n}{\frac{(n-1)}{2}}\right)^2} \tag{7.12}$$

$$W(n) = \begin{cases} \frac{I_0\left(\pi\alpha\sqrt{1-\left(\frac{2n}{n-1}-1\right)}\right)^2}{I_0(\pi\alpha)} & 0 \leq n \leq N-1 \\ 0 & else \end{cases} \tag{7.13}$$

$$W(n) = \begin{cases} \frac{1}{2}\left\{1 + cos\left(\frac{2\pi}{R}\left[n - fracR2\right]\right)\right\} & 0 \leq n \leq \frac{R}{2} \\ 1 & \frac{R}{2} \leq n \leq \left(1 - \frac{R}{2}\right) \\ \frac{1}{2}\left\{1 + cos\left(\frac{2\pi}{R}\left[n - 1 + fracR2\right]\right)\right\} & \left(1 - \frac{R}{2}\right) \leq n \leq 1 \end{cases} \tag{7.14}$$

$$W(n) = \begin{cases} cos(ncos^{-1}x) & x \leq 1 \\ cosh(ncosh^{-1}x) & > 1 \end{cases} \tag{7.15}$$

Table 7.2: Analysis of windowing functions.

Window	EVM RMS	BW Reduction
Gaussian	0.89	0.36
kaiser	1.2	0.33
Tukey	0.65	0.38
Chebwin	1.8	0.33

7.3.3 Signal oversample ratio

Processes used to reduce the bandwidth expansion is to alter the phase of the signal over a number of samples, therefore an oversample is required. The greater the oversample the smoother the modification and the smaller the widow size relative to the data symbols. The impact of the oversampling is evaluated through signal EVM and effective bandwidth reduction. The results are presented in Table 7.3, and it is clear that the processing has less impact on EVM as the over sample ratio (OSR) is increased, in addition the bandwidth

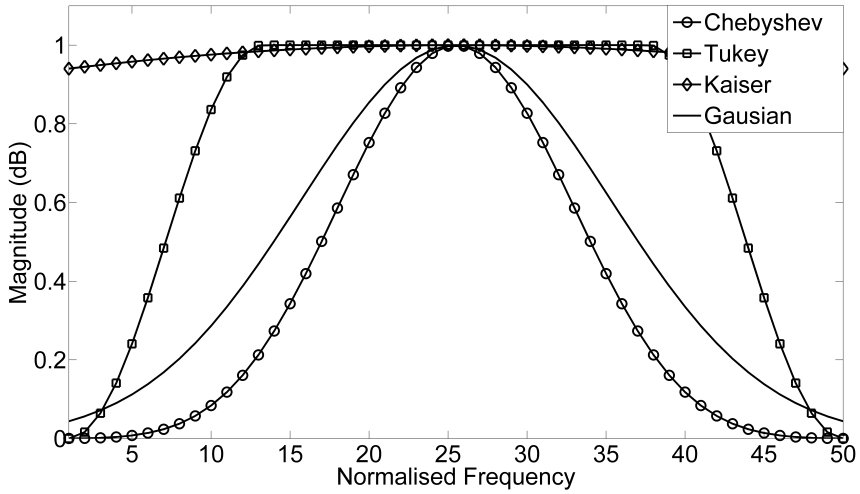


Figure 7.14: Magnitude response of the windowing function over a 50 sample length.

reduction achieved is also reduced however the relationship between error reduction and signal bandwidth is not linear.

Table 7.3: Analysis of the impact of over sample ratio.

OSR	EVM RMS	BW Reduction	Effective BW Reduction
25	0.88	0.36	0.36
20	1.85	0.36	0.288
15	2.0	0.46	0.264
10	2.5	0.6	0.24

7.3.4 Spectral characteristics

The spectral characteristics of the signal are evaluated using the adjacent channel power ratio (ACPR). ACPR is a figure of merit generally used in determining if a signal has the required dynamic range to pass the spectral mask requirements of a transmission standard. In this case it will be used to determine the increase in out of band signal power which is added to the processed signal. It can therefore be used in determining if a final filtering stage is required. If one is required the ACPR can determine the filter specification. The signals ACPR is determined using the equation outlined in equation 7.16 where the in band signal power is P_{ch} and the adjacent channel power is P_{adj}. The adjacent channel power is generally the signal power in a channel of bandwidth similar to the transmitted signal specification and is located a

single channel spacing both above and below the desired channel or channels in the frequency domain. Therefore there are two values for the ACPR, in our calculations the maximum value is used as the comparative figure of merit. The goal for the optimization algorithm was modified to include the system ACPR presented in equation 7.17. $ACPR_m$ is the maximum ACPR from either the upper or lower channel measurements and $ACPR_{lim}$ is the ACPR limit which is acceptable after processing the signal. The optimization algorithm will modify the parameters until the ACPR limit is achieved or exceeded at the expense of bandwidth reduction.

$$ACPR = 10log_{10}\left(\frac{P_{adj}}{P_{ch}}\right) \tag{7.16}$$

$$G = BW * A + \frac{EVM_{rms}}{B} + ACPR_m + ACPR_{lim} \tag{7.17}$$

In order to achieve the required ACPR levels for the modulation standard and achieve reasonable bandwidth reduction a final filtering stage will be required. The aim of the algorithm is to find the minimum attenuation which will provide the required ACPR. To determine this value an ideal filtering algorithm is used in the optimization process as filter design and implementation is computationally expensive and impacts the optimization speed. The filtering process preceding the signal modification reconstructs some zero crossing components of the original signal, however the final number of these are greatly reduced. FFT filtering allows for a highly flexible filter mask to be implemented. There is a balance between the regeneration of the zero crossing points and the spectral emissions that must be achieved. Implementing the filter using the FFT process means dynamic changes to the filter specifications can be implemented.

Table 7.4: Comparison of ACPR limit implementation, tuning value B is set to 4.

ACPR Limit	EVM	BWR	ACPR -10	ACPR -5	ACPR +5	ACPR +10
-50	2	0.307	-55	-50	-50	-55
-52	2.2	0.307	-54	-52	-52	-55

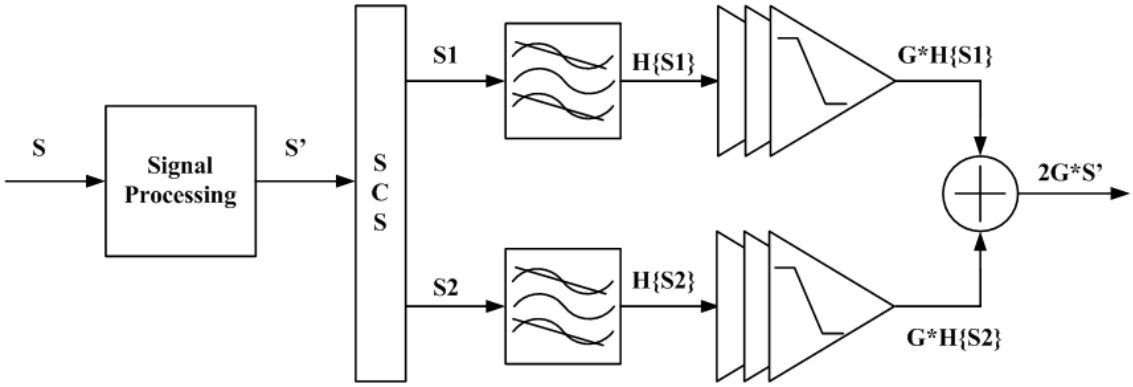


Figure 7.15: Simulation set-up with band pass filters to evaluate the effect of a band pass system on the outphasing signals.

7.4 Simulating a band-limited outphasing system

Simulation were carried out to investigate the impact of band limitations in an outphasing system. This will provide a base line upon which the performance of the bandwidth limited outphasing process can be compared against. The simulation is carried out using the set-up outlined in Figure 7.16. The signal processing is carried out upon the input modulated signal S, the resultant signal S is decomposed by the signals component separator (SCS). The signal is then further processed by a Butterworth band pass filter to simulate a bandwidth limitation system, the signal output is $H[S\,x]$. The outphasing amplifier operates with saturated or switched mode power amplifiers to achieve maximum efficiency. The signal is therefore limited after filtering to simulate the effect of saturated operation, stripping the amplitude information from the outphasing signal before recombination. The optimization algorithm arrived at the values given in Table 7.5, B is the EVM scalar in the cost function and ACPR is the desired ACPR limit of the post processed signal. The resulting EVM for a bandwidth reduction of 70% is 4.1%. The QAM signal is a 5 MHz bandwidth signal with a 20 times over sample. The process used a Tukey window of length L. The threshold of M is the magnitude upon which the process will be performed once the limit is reached. The post processing filtering requires an out of band attenuation Att in order to achieve the desired ACPR limit.

Table 7.5: Design values for the bandwidth reduction algorithm used in system simulations.

B	ACPR	EVM	BWR	L	M	Att
4	-48	4.1%	0.7	36	0.095	-17.2

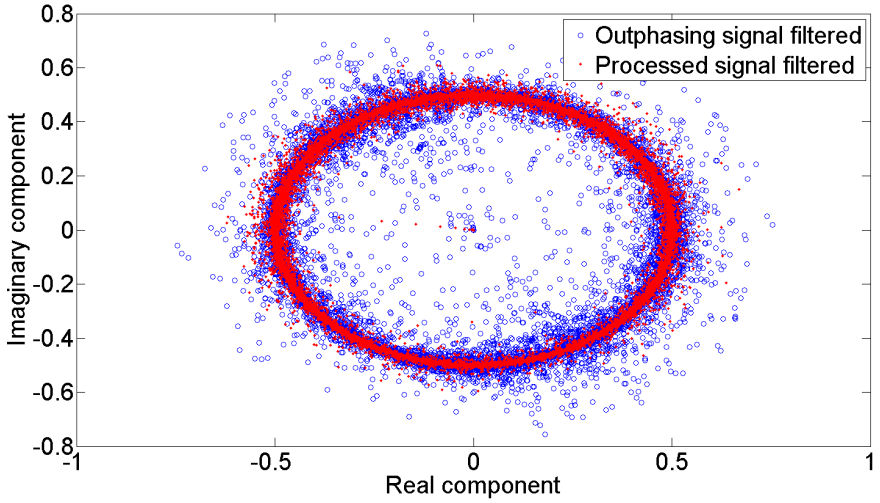


Figure 7.16: Example of constant envelope after band pass filtering.

Bandwidth reduction is desirable as it reduces the system requirements of the outphasing system as a whole and increases the operational bandwidth of the amplifier. Therefore our analysis will centre on the accurate recombination of an outphasing signal which has been subjected to band pass filtering. Figure 7.16 demonstrates the effects on the amplitude of the signals, the blue unprocessed outphasing signal has much greater spread than the red processed signal. Ideally both signals should have a constant magnitude of half A_{max} where the S is normalised then the maximum amplitude is unity. The outphasing amplification was originally developed as a method for removing the non-linear effects that are associated with amplitude modulation and deeply saturated for switch-mode amplifiers. The amplifiers topology requires constant envelope input signals to achieve efficient operation. The amplitude variation from filtering outlined in Figure 7.16 will reduce the efficiency of the structure. The processed signals experience far less amplitude variation and therefore should provide a more stable input signal and efficient drive signal to the final stage amplifier.

In Figure 7.17 the spectrum of the recombined signal $2G * S$ and the regular outphasing signal are plotted. Both signals experience some out of band non-linear effects when compared to the ideal recombined signal. However the out of band ACPR level of the processed signal presented in red is relatively flat up to the filter response and falls away after that point. In contrast the unprocessed signal experiences the same adjacent channel effects as the processed signals however further out of band significant non-linear effects are constructed,

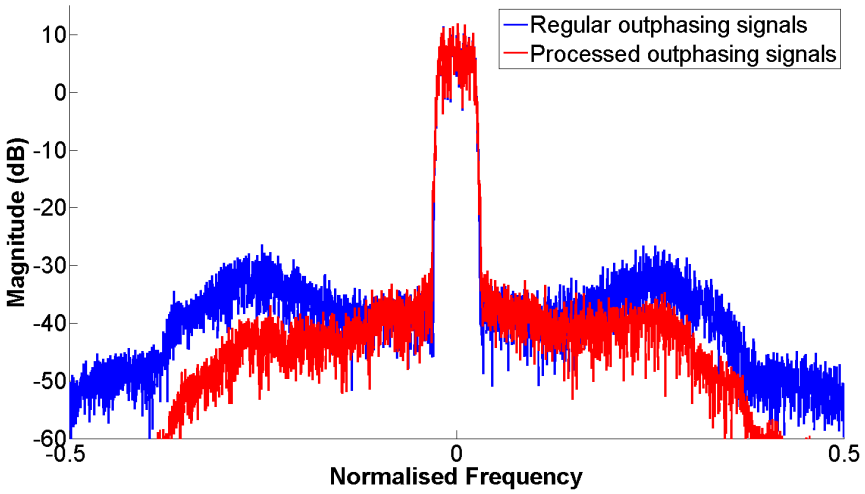


Figure 7.17: Spectral characteristics post constant envelope signal filtering. Original outphasing signal peak ACPR value -37 dB, processed bandwidth reduction signal peak ACPR value -46 dB.

These unwanted effects range from 5 to 10 dB above the adjacent channel power level.

7.5 Test bench

Further verification is carried out with a modified version of the outphasing test bench introduced in Chapter 4. In place of the digital outphasing power amplifier an ideal power combiner is used in conjunction with RF power limiters to ensure that any non-linear occurrence is a function of the bandwidth limitation. The test bench is outlined in Figure 7.18, the filters are placed before the recombined signal and the power couplers allowing the outphasing signal to be examined before recombination.

As outlined in Section 4.1.4.3 the system is wide band and has a flat frequency response capable of ideal outphasing operation for multi-carrier signals. The bandwidth limitation was introduced with the use of band pass filters. Coupled strip-line band pass filters [135] were designed in ADS to provide the required bass band about an operating frequency of 2 GHz. A passive strip-line structure ensured that the filters would achieve a performance similar to the simulated design. In addition the manufacturing process should introduce fewer variations when compared to lumped element design.

The bandpass filters are designed using a Rodgers 4350 B substrate, the high quality and low dialectic constant allows a more uniform response from the designed filter. The filter was designed using ideal equations, however the dimensions required for optimal performance were not compatible with the manufacturing capabilities at hand. For maximum power transfer the first transformer section required an air gap of less than 0.1 mm. With the available milling tool and cutting bits the minimum air gap achievable is 0.15 mm. Therefore these constraints are applied to the filter design and further optimisation was carried out in order to achieve a feasible filter design. The result there was an increase in insertion loss from 0.5 dB to 2.2 dB, however with tuning the passband and filter characteristics were similar to the original design. The resulting filter response is presented in Figure 7.19. The measured response of both filters is outlined in Figure 7.20.

There is a variation between design and actual circuit with a centre frequency shift of 2 GHz to 1.96 GHz however the filter bandwidth is the same approximately 100 MHz. There are two possible factors which can cause such a shift to occur. Variation in the dielectric constant between the simulated and actual substrate material will affect the centre frequency. Also the position and solder joint of the SMA connectors, the only possible variation in assembly

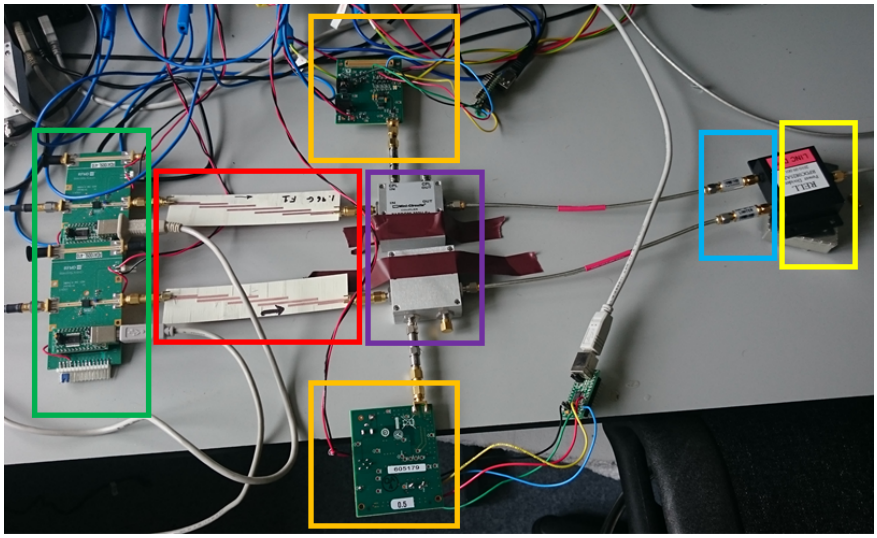


Figure 7.18: Banswidth limitation test bench. The main components of the test bench are highlighted with the variable gain amplifiers are highlighted in **Green**, Coupled transmission line filters are outlined in **Red**, power couplers are outlined in **Purple**, power meters are outlined in **Orange**, the RF limiters are outlined in **Blue** and the power combiner is outlined in **Yellow**.

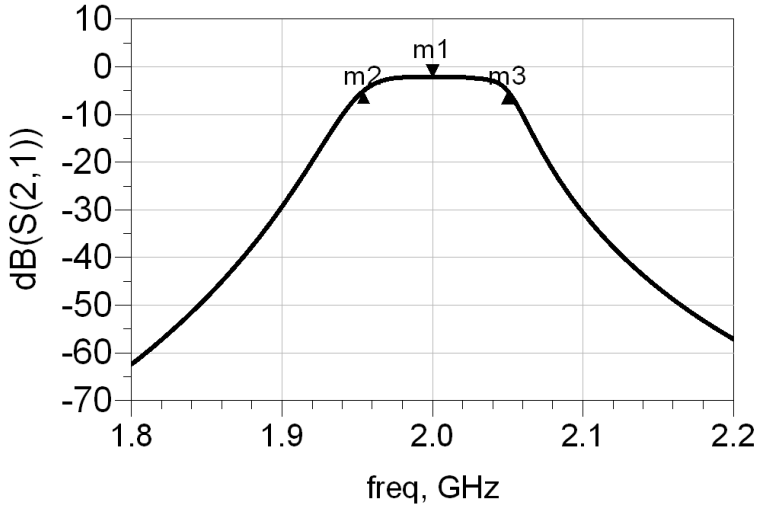


Figure 7.19: Coupled transmission line bandpass filters pass band. Design centred at 2 GHz and had approximately 100 MHz bandwidth at the 3 dB points highlighted by m2 and m3.

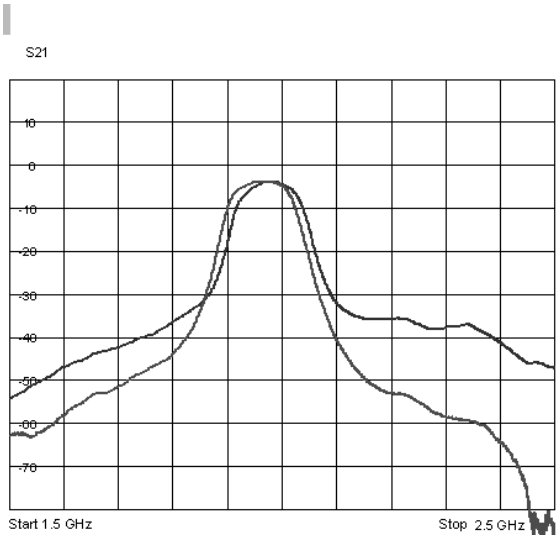


Figure 7.20: Coupled transmission line bandpass filters. Placed in outphasing test bench to emulate bandwidth limitation.

can also alter the loading on the resonators, resulting in a frequency shift. The substrate is a precision material from Rodgers designed for such applications therefore an offset between the data sheet and the actual material is less likely. The SMA connector placement is carried out by hand, therefore this is the most probable cause of variation. This is also the most probable cause of variation between the filters. The frequency shift will not affect the test bench, all of the remaining components are wideband therefore the new test-bench frequency is set to 1.96 GHz.

The RF limiter is used as an analogue of a high gain digital amplification stage removing amplitude information introduced by the band pass filters. The response of the RF limiter is presented in Figure 7.21. The sweep is carried out over 0 - 20 dBm on a vector network analyser. The graph is plotted as the gain of the circuit across the input power range. The device starts limiting the output power at approximately 6 dBm and the response is almost flat as the output power increases. To ensure that the amplitude information of the outphasing signal is removed in almost all cases the input power to the limiter is set to 15 dBm on each path. Each signal will therefore experience attenuation in the region of 8 dBm, providing a consent output power of approximately 7 dBm.

With the filtering and limiting components introduced into the test bench, calibration is carried out at the centre frequency of 1.96 GHz. Any imbalance introduced by the physical

Figure 7.21: RF power limiters used to limit the maximum amplitude to of an RF signal. the output is linear up to 10dB, after which point the output is clamped to that value.

difference between the filters and limiters in each path will be calibrated out, enabling maximum dynamic range at the centre frequency. The remaining offsets are the frequency effects of the filtering stage which we wish to observe.

7.6 Experimental Results

The main difference between the simulation set up and the experimental hardware is that the system bandwidth is now fixed by the band pass filter design. The signal bandwidth is the only variable that can be tuned in order to observe the effects of bandwidth limitation. The FSQ will be used as the signal receiver in this case, with a maximum bandwidth of 122.88 MHz some limitations will apply to the test signal. Therefore in order to achieve the effects associated with bandwidth limitation and still have the ability to fully observe the outphasing signal in both time domain and frequency domain a signal bandwidth of 12 MHz is chosen, using the rule of thumb this will result in an outphasing bandwidth of 120 - 144 MHz.

The bandwidth expansion reduction is carried out on the outphasing signal, the target is to achieve maximum reduction for a given EVM. The signals that are chosen for this evaluation are the original signal, a 50% bandwidth reduction with 2% EVM and a 55% bandwidth reduction with an EVM of 4%. The spectral characteristics of the signals are outlined in Figure 7.22.

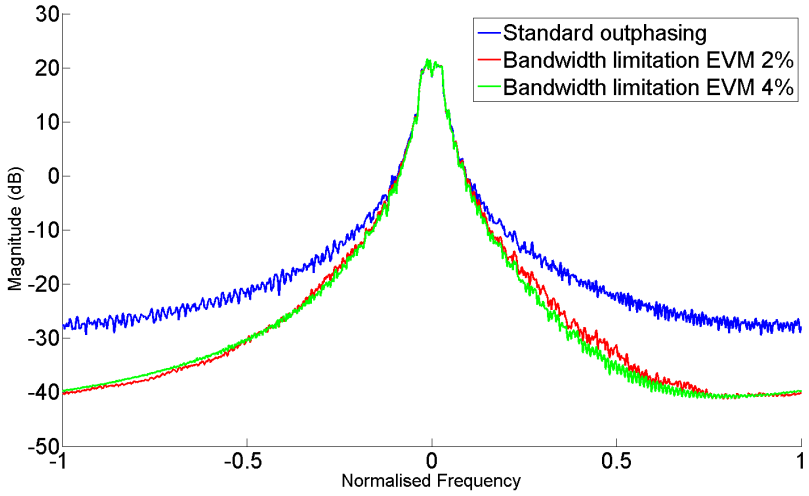


Figure 7.22: Spectral characteristics of the outphasing signals post bandwidth reduction processing.

The impact of the filtering on the outphasing signal in the time domain is illustrated in Figure 7.23. The introduction of amplitude modulation is clear in the original outphasing signal in red. The bandwidth reduced signal has some amplitude information however the signal is now constant envelope with some ripple.

In order to ensure that the noise observed is solely attributed to the filtering process an AM/AM AM/PM function is used to correct any static non-linear intermodulation effect which can be attributed to the outphasing recombination. The results are presented in Figure 7.24, a clear improvement can be observed both in the adjacent and alternative frequency bands. An improvement of 4-6 dB can be observed in the adjacent channel ACPR levels. Further out of band the increased noise floor associated with the filter transition band is also viable. While less pronounced than the simulated signal, it is still present and an issue. The out of band noise has been reduced by as much as 10 dB for both signals with 2% and 4% EVM.

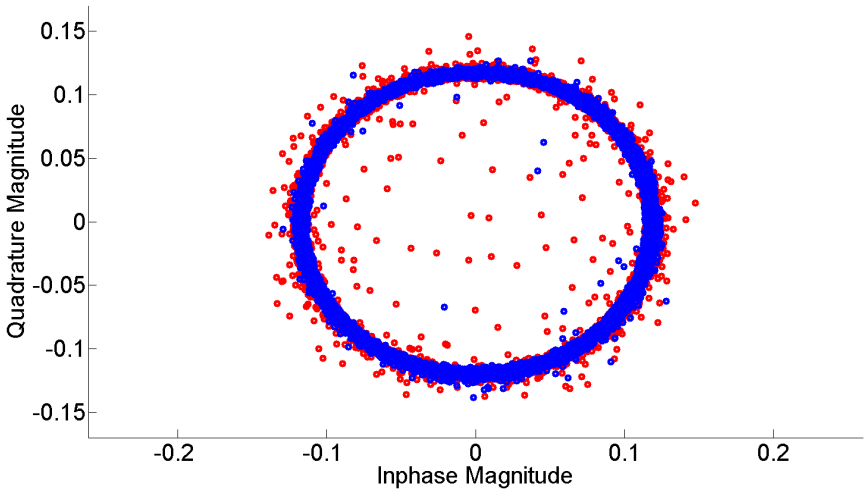


Figure 7.23: Comparison of outphasing signal post filtering. The red is the original outphasing signals and the blue is the modified outphasing signal.

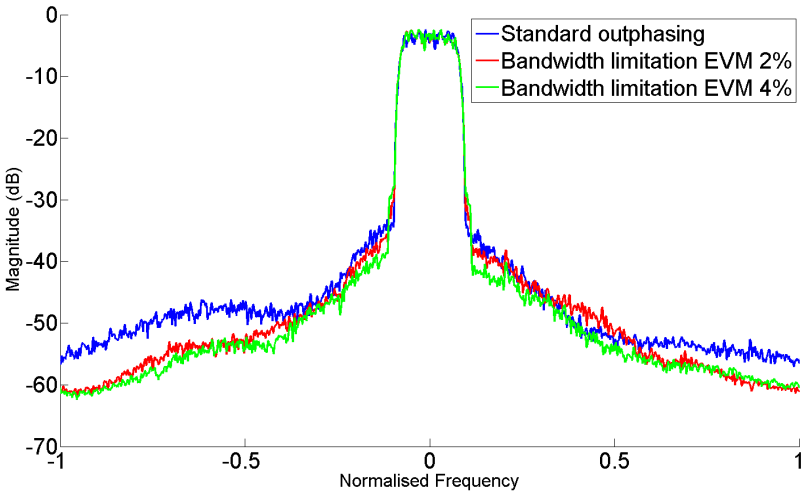


Figure 7.24: Spectral characteristics post constant envelope signal filtering. Original outphasing signal peak ACPR value -38dB, processed bandwidth reduction signal peak ACPR value -44dB. Out of band spectral noise floor is improved by as much as 10dB.

7.7 Conclusion

In this chapter a novel method of reducing bandwidth expansion is proposed. Signal processing on the input modulated signal is carried out, resulting in a bandwidth reduction in the outphasing signal [4]. The proposed method is developed to maintain the constant envelope characteristic of the outphasing signal. The algorithm includes parameters which determine the achievable bandwidth reduction. Through optimisation a balance between bandwidth expansion reduction, EVM and the spectral characteristics of the output signal can be achieved. A detailed account of each of the parameters is provided and how each affects the optimisation process.

Both the simulation and measurement results correlate, the process can negate some of the adjacent channel ACPR noise and a large quantity of the out of band noise introduced by the filtering process. The cost of this improvement is an increase in signal EVM. However in the experimental set up, introducing as little as 2% additional EVM, resulted in as much as a 10 dB reduction. An added benefit the signal maintains the constant envelope input to the amplifier.

Further work will be carried out to investigate the limitations of this process for modern communications signals. The goal is to reduce the out of band spectral power of the outphasing signal, in turn reducing the cost of signal generation and RF components in both of the outphasing signal paths. Further refinement to both the process and the optimisation will be investigated to determine the optimum performance with minimal impact.

CHAPTER 8

Zero Crossing Distortion

In the case of outphasing, envelope elimination and restoration (EER), and Class-S power amplifiers the amplitude modulation of a communications impacts on the amplifiers linearity. In the case of outphasing and EER, the topologies have difficulty in achieving accurate low power outputs, resulting in wideband harmonic distortion [136] [137]. In the case of class S power amplifiers, it has been noted that the digital pulse encoding of the modulated signal can experience issues at low output powers [138]. Failing to achieve a minimum output power to sufficiently describe the modulated signal will result in low power discontinuities in the time domain signal. This is commonly refereed to as zero crossing error. It occurs at a much lower spectral power when compared with intermodulation products which result from continuous non-linear operation. It cannot be removed by traditional linearisation methods. The result is a fixed noise floor for the amplifier. In this paper the source and impact of limited dynamic range will be analysed. Furthermore a solution is proposed; by modifying the characteristics of the modulated signal before amplification it is possible to avoid the non-linear region, reducing the impact of the discontinuous non-linearity about the zero crossing point. This work will concentrate on the outphasing power amplifier utilizing a non-isolating Cheriex combiner for efficient operation at back off output powers.

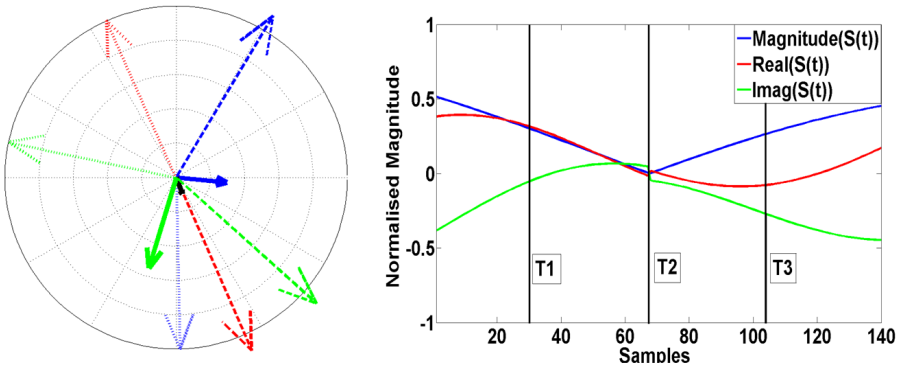


Figure 8.1: The impact of dynamic range mismatch on the time domain signal is presented. The lef hand plot is a vector plot if the outphasing signals S1(t) dotted arrow, S2(t) dashed arrow and the recombined signal S(t) solid arrow, with additional gain on S2(t). The arrows correspond to three point in time, blue = T1, red = T2 and green = T3. The time domain signal is presented on the right hand side with the point T1 - T3 outlined. The point T2 highlights the discontinuity in the I and Q as the signal should transition through zero, but the path mismatch from S2(t) prevents this.

8.1 Dynamic Range

Dynamic range is a figure of merit more commonly used in analysing the performance of signal converters such as digital to analogue converters (DACs) and analogue to digital converters (ADCs). In this context dynamic range is a function of the peak output power achievable by a system and minimum step in power which can be taken, the spectral components of which are referred to as the noise floor. Power amplifiers are assumed to be analogue circuits and as such in theory have infinite resolution; therefore the step size is infinitely small. However the amplifiers that are outlined in the introduction have a finite minimum output power level. As such the dynamic range of the amplifier is the ratio of the maximum achievable output power to the minimum achievable output power. The minimum achievable output power is now the maximum achievable noise floor for the amplifier. Dynamic range can also be compared to the peak to minimum power ratio (PMPR) of the communications signals, which is the ratio of maximum to minimum power of the signal. Our goal is to reduce this value by increasing the minimum power level of the communications signal with out impacting the signal information. Dynamic range and PMPR figures of merit can be compared in equations 8.2 and 8.3.

$$S(t) = A(t)e^{-j\phi(t)} \tag{8.1}$$

$$Dr = \frac{max(A(t))}{min(A(t))} \tag{8.2}$$

$$PMPR = \frac{|max(A(t))|^2}{|min(A(t))|^2} \tag{8.3}$$

Modern communication signals consist of modulated amplitude and phase components. The quadrature modulation provides increased throughput per unit bandwidth or bits per hertz when compared with amplitude or phase modulated signals alone. Equation 8.1 presents the function of a quadrature modulated signal. If we assume that the limited dynamic range of the signal only affects the amplitude modulation then the phase component of the signal will continue as expected. Limited dynamic range will affect the signal at the zero crossing point, where the signal's phase transitions at high frequency. This is more likely to occur as the signals passes through the centre of the unit circle, transition to constellation points 360 degrees from one another. Figure 8.1 provides an illustrated example of the impact of path mismatch at the zero crossing point. The illustration outlines the operation of the outphasing signal in the vector space and the recombined time domain side by side. The transition point T2 indicates the original zero crossing point, the black vector indicates the error in $S(t)$ resulting from the path imbalance. As the signal's phase is unopposed the transition at the zero crossing point will result in a high frequency noise when examining the Cartesian form of the signal. This undesirable non-linearity will result in a high number of intermodulation products being formed.

This work will concentrate on the impact of limited dynamic range within the outphasing power amplifier with the aim of reducing the period of time the modulated signals is in the low power non-linear region. The reasons for the dynamic range limitation within the outphasing power amplifier is mainly attributed to path mismatch which is a result of amplitude or phase imbalances introduced by the amplification stages or an asymmetric pass band of the system. In [136] and [139] the authors relate directly the impact of the path mismatches to system dynamic range and subsequently the power associated with the intermodulation products. Selecting one path as the reference the relative gain and phase mismatch can be attributed to the other without loss of generality. Equations 8.4 and 8.5 present the outphasing model which includes path mismatch in path two, δG is the gain delta between the paths and $\delta\rho$ is the phase delta between

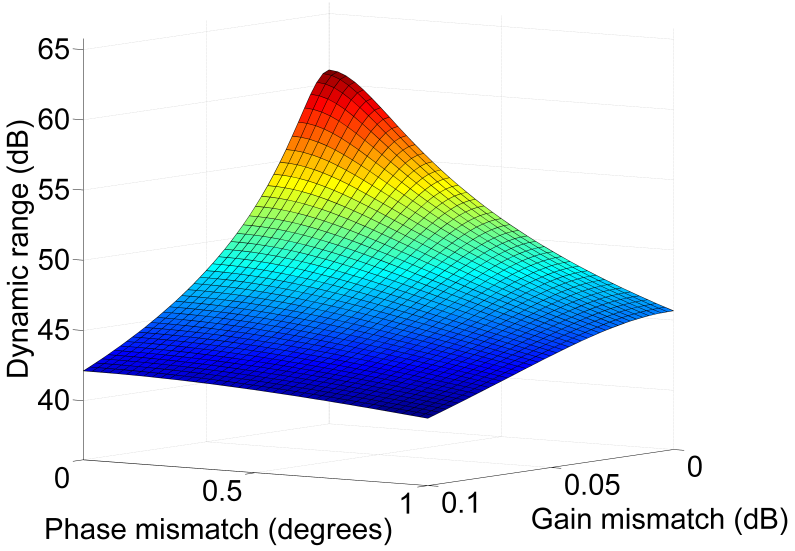


Figure 8.2: Dynamic range of outphasing amplifier as phase mismatch is swept from 0 to 1 degrees and gain mismatch is swept from 0 to 0.1 dB.

the paths.

$$S_1' = \frac{A_{max}}{2} e^{-j(\phi(t)+\rho(t))} \tag{8.4}$$

$$S_2' = \delta G e^{-j\delta\rho(t)} \frac{A_{max}}{2} e^{-j(\phi(t)+\rho(t))} \tag{8.5}$$

The dynamic range can be calculated by finding the noise floor of the system for the path mismatch parameters. Assuming that the system is normalised and the maximum output amplitude is 1 then the dynamic range is the log scale of the error from path mismatch in equation 8.6. The value δ is the error offset which is a result of the path mismatch.

$$Dr = 10log_{10} \mid \frac{\delta}{2 - delta} \mid^2 \tag{8.6}$$

$$\delta = 1 - e^{-j\delta\rho} - \delta G e^{-j\delta\rho} \tag{8.7}$$

In [136] the author provides a calculation for intermodulation (IM) distortion which can be

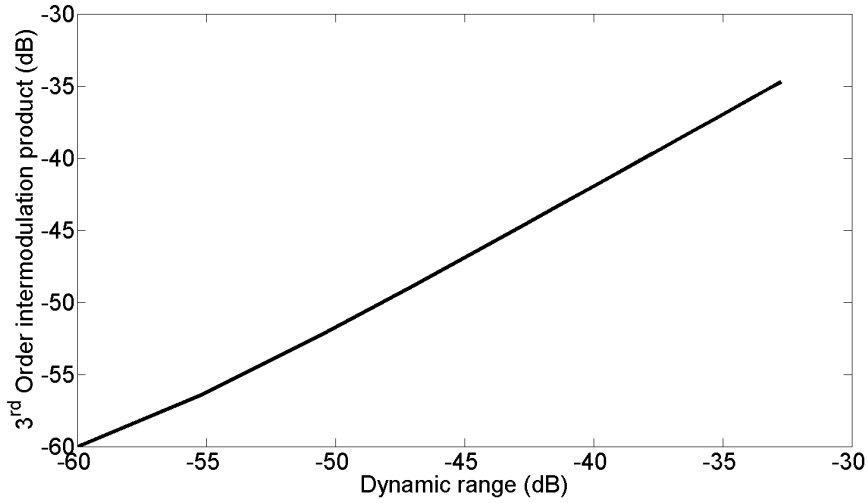


Figure 8.3: Relationship between dynamic range and the third order intermodulation product.

calculated from the linear scale of the dynamic range. The formula can be used to calculate any order of intermodulation which will result from a two tone test. Using the equations 8.6 and 8.8, the effect of path imbalance on the outphasing amplifier is displayed in Figure 8.2. The resulting 3rd order intermodulation product power is presented in Figure 8.3. The value assumes that no other non-linear effects are introduced by the amplifier.

$$IMn = 10log_{10}\left(2\frac{-1^n - 1(-1^{\frac{n+1}{2}} + 1)}{\pi(n^2 - 1)} \mid \frac{\delta}{2 - delta} \mid^2\right) \tag{8.8}$$

Figure 8.2 shows the impact of gain and phase imbalance and how they limit dynamic range based upon equation 8.6. Figure 8.3 presents an estimation of the impact of dynamic range on intermodulation distortion based upon the relationship described in equation 8.8 [136]. The intermodulation produce for a given order that results from low dynamic range can be directly calculated, this relationship is experimentally verified in [136]. In many systems advanced calibration techniques have been developed to reduce these effects. However system bandwidth and the fundamental design of the output combiner mean that the dynamic range will change with frequency. This requires dynamic calibration which must update with the changing environmental parameters of the amplifier. An alternative approach is examined in this paper - by modifying the input signal to avoid operation in these low power regions the presence of the intermodulation products due to limited dynamic range are negated.

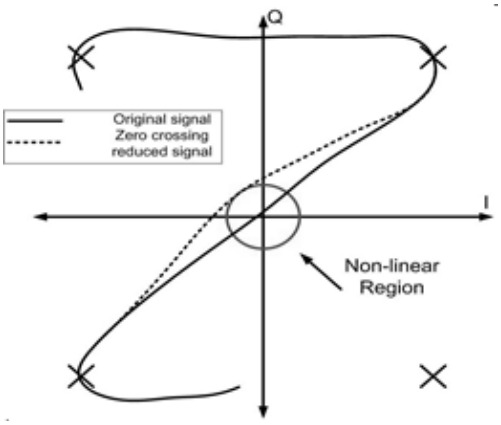


Figure 8.4: Illustration of how to avoiding zero crossing points. Avoiding zero crossing points can reduce the dynamic range requirement for acceptable ACPR levels.

8.1.1 Zero Crossing Reduction (ZCR)

As outlined in the previous section, a non-linearity occurs when the input signal enters a low power region i.e. going through the centre of the unit circle. In Figure 8.4 this region has been outlined with a red circle. As the signal enters this region the output of the non-linear system is more uncertain, the result can be large errors in both signal amplitude and phase. To circumvent this we aim to route the signal around this region [4], an illustration of this is outlined by the broken line in Figure 8.4. To achieve this, the input signal must be oversampled; the additional samples between symbols allow us to modify the signal trajectory gradually, maintaining the majority of the modified signal components within the original signal bandwidth. Increased signal sample rate is a common occurrence in many modern signal processing techniques, for example digital pre-distortion and crest factor reduction require the increased sample rates, commonly 5-7 times the original signal bandwidth. The typical signal expansion required for outphasing amplifiers is between 10-12 times as outlined in [99]. Our method can therefore take advantage of the increased signal sample rate to achieve ZCR.

The process for ZCR is outlined in the following steps:

1. Generate an appropriate band limited window function W. The window function is manipulated to provide the scaled window function $W * M$. M is the inverse of the minimum amplitude value.

2. Separate signal amplitude $A(t)$ and phase $\phi(t)$, using the CORDIC algorithm.

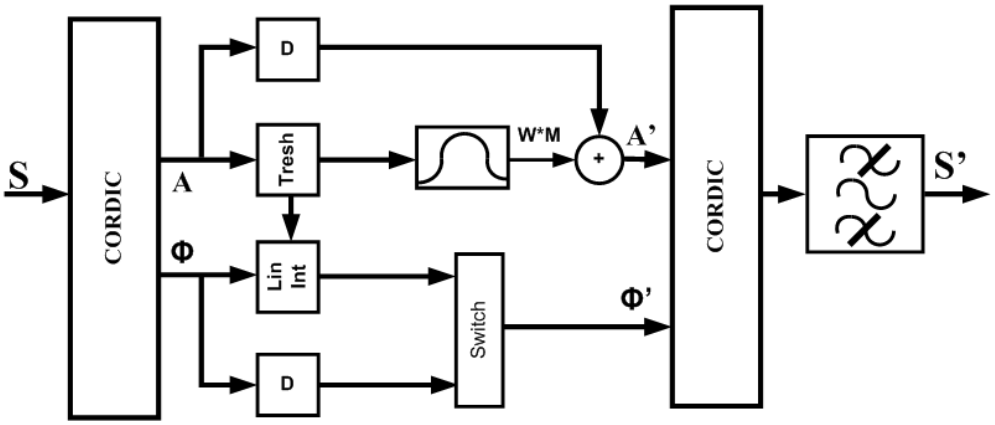


Figure 8.5: Block diagram of proposed zero crossing reduction process.

3. Identify the zero crossing points from the signal amplitude $A(t)$ using the non-linear threshold M.

4. Modify the signal amplitude $A(t)$, at zero crossing points by adding the scaled window function to increase the minimum amplitude $A(t)$.

5. Modify the signal phase $\phi(t)$. A new phase trajectory is selected to replace the original signal phase. The new phase is a linear interpolation between the initial and final phase values determined by the length of the window function.

6. The processed signal amplitude $A(t)$ and phase $'(t)$ are recombined using the CORDIC algorithm.

7. Filter the modified signal to reduce the out of band impact of the preceding steps.

If the signal amplitude falls below the minimum threshold value a triggering process is initiated. For optimum operation of the proposed algorithm, the centre of the window is ideally placed at the minimum signal amplitude, to achieve this the signal amplitude is delayed for half the length of the windowing process. When the amplitude of the signal begins to increase a trigger is sent to begin the process. If an increase in signal amplitude is not detected a trigger signal is sent and the process is begun at $N/2$ samples later.

The modification of the signal amplitude will change the characteristics of the signal in both the time and frequency domain. Using a windowed pulse reduces out of band spectral emissions generated by the zero crossing process, in turn reducing the requirements of the

final filtering stage. This is beneficial for reasons of computational complexity and due to the performance reduction of the ZCR process. Signal reconstruction can occur if the filter requires a narrow passband and high out of band attenuation, regenerating the original input signal before the ZCR processing. The Chebyshev windowing function is highly flexible as both the bandwidth and the out of band noise suppression. The window is scaled by the minimum detected magnitude, the resulting signal of length N is a pulse which is used to increase the minimum signal magnitude of the communications signal. It is desirable to have the window length as short as possible to prevent signal error, yet long enough so that the additional signal energy remains within the signal bandwidth.

To modify the phase gradually over the length of the window chosen for the amplitude modification a continuous rate of change is applied over the window length N. The continuous rate of change may not follow the initial or final slope of the phase signal and therefore a discontinuity may occur. Using the filtering outlined in step 6 we can remove this discontinuity, this step is however continually being investigated and it is our belief that a more robust windowing and cancellation process in future iterations, negating the requirement for the filtering step is possible.

A fast Fourier transform (FFT) [72] function, in conjunction with a custom filter mask, is used to suppress any out of band noise which is generated. The filtering process preceding the signal modification reconstructs some zero crossing components of the original signal, however the number of which is greatly reduced. FFT filtering allows for a highly flexible filter mask to be implemented. There is a balance between the regeneration of the zero crossing points and the spectral emissions that must be achieved.

As outlined in the steps there are several variables that will impact the zero crossing reduction process. We must first identify the linear amplitude range that the non-linear system can achieve, the remaining non-linear range is the undesirable region that we aim to avoid. This is below the threshold magnitude of the process, M. The length of the window is a function of the sample rate and signal bandwidth. The filter type and out of band suppression are also tunable depending on the non-linear region of the system.

The ZCR process has an impact on the characteristics of the output signal, some of which are undesirable such as an increase in ACPR and EVM. The aim of the process is to limit the introduction of ACPR and EVM, the logic is that the ZCR process introduces significantly

less distortion and is controllable through careful consideration of the tunable parameters. A balance between the achievable minimum dynamic range with the ACPR and EVM enables an overall improvement in system linearity. Appropriate values for the tunable variables will be simulated and measured in the following section.

8.1.2 Simulation and system integration

A series of simulations were carried out in MATLAB to evaluate the effects of the zero crossing reduction processing on a modulated signal and the performance improvements that can be achieved of outphasing systems. Using the communications toolbox, a 64 QAM signal was generated. The characteristics of the signal are 3.84 Msps, band limited to 5 MHz using a root raised cosine transmission filter. As described in Section 8.1.1 the signal is interpolated and the zero crossing reduction method is carried out. It is important that this method will not interfere with standard signal processing techniques, mainly crest factor reduction (CFR) which like ZCR modifies the signal magnitude and was originally developed to reduce the impact of non-linear operation by similarly avoiding the non-linear region. In current communications systems, CFR provides a signal processing method to reduce the signals peak to average power ratio, increasing the operational efficiency of the power amplifier.

8.1.2.1 Crest factor reduction

Crest factor reduction (CFR) is a technique which is used to limit the peak to average ratio (PAPR) of a modulated signal. The benefits of this are that the average power of the signal can be increased. The average power of the signal is an important figure of merit when dealing with power amplifiers as it ultimately determines the energy efficiency with which the power amplifier operates at. There are many methods of implementing the CFR algorithm, the method which is used in most digital communications systems due to its performance and computational efficiency is the peak cancellation method outlined in [140]. The algorithm is outlined in the following steps:

1. The peak of the signal is detected once the threshold value is exceeded.

2. The cancellation function is derived from the original signal and a windowing function. The result is a band limited cancellation signal.

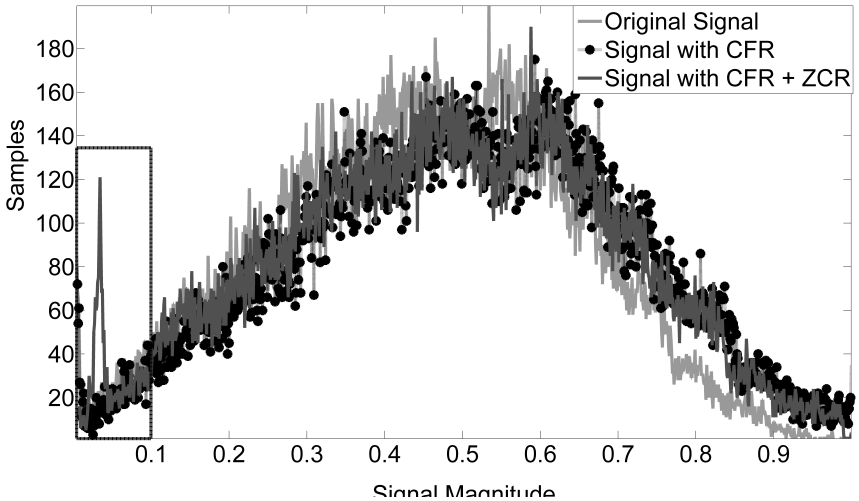


Figure 8.6: Signal properties after each stage of processing, the ZCR removes any DC components, resulting in a larger number of samples about 0.05. The black rectangle is the region where ZCR processing is carried out and is presented in Figure 8.7.

3. The cancellation signal is scaled relative to the threshold of the CFR.

4. The cancellation signal is added to a delayed version if the input signal.

These steps may need to be carried out several times in order to achieve the PAPR level that is required to achieve efficient operation. CFR is performed on the QAM signal; a comparison of the signal magnitude for each process is presented in Figures 8.6 and 8.7, where a histogram distribution of the signal magnitude is presented. While the changes are subtle for this signal it can be seen that the mean power of the signal is increased slightly. CFR is carried out before the ZCR process, in signals with high PAPR CFR can help the ZCR, as the signal is now compressed, there are fewer points below the ZCR threshold that need to be processed.

The aim of the ZCR algorithm is to reduce the number of times the signal goes through the centre of the unit circle. By doing this an artificial minimum is created, this can be seen in Figure 8.6 where the number of samples about the signal magnitude of 0.25 has greatly increased.

8.1.2.2 Digital pre-distortion

The proposed zero crossing reduction algorithm is designed to negate the non-linear effects which occur during the signal nulling process. Outside the non-linear region of the path

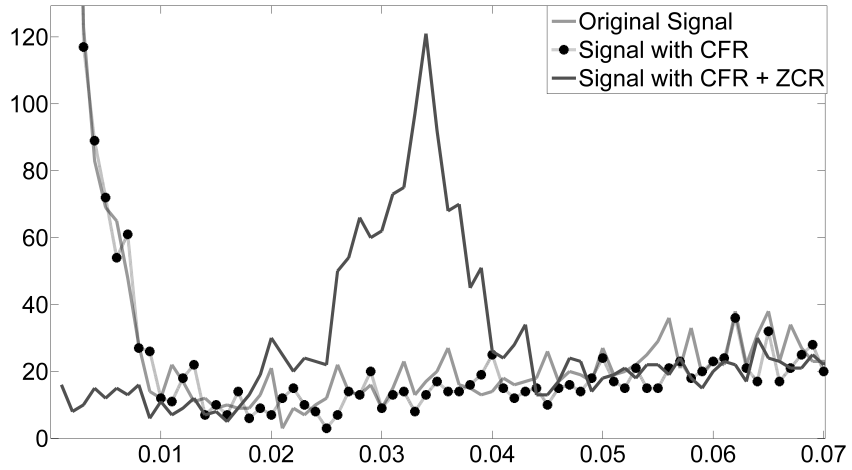


Figure 8.7: Signal properties after each stage of processing, magnified at lower powers. The ZCR removes any DC components, resulting in a larger number of samples about 0.05.

mismatch and combiner, effects still exist and as such require a correction. Digital pre-distortion is an established technique of power amplifier linearisation. Vector switch Volterra has successfully been used for wide band linearisation of outphasing power amplifiers [2]. In Chapter 6 non-linear models using piecewise segmentation have been shown as a robust way to achieve this. Applied to both polynomial [123] and time-series [92] non-linear functions for modelling the power amplifier perform well. Segmentation has many advantages, for one it enables accurate estimation of localized non-linear characteristics it can also increase stability when training due to the use of lower model orders. The chosen digital pre-distortion algorithm is vector switched Volterra with self organising maps clustering. Vector quantization is performed upon the feature space generated from the magnitude of the input sample and the magnitude of a previous input sample $mag(x(n)), mag(x(n-m))$ where n is the current sample and m is an integer representing a delay factor. The Volterra series, outlined in equation 8.9, as the non-linear time series for the individual clusters.

$$y(n) = \sum_{k} \sum_{l_1} \cdots \sum_{l_{2k+1}} h_{2k+1}(l_1, l_2, \cdots, l_{2k+1}) \prod_{i=1}^{k+1} z(n-l_i) \prod_{i=k+2}^{2k+1} z^*(n-l_i) \tag{8.9}$$

To evaluate the performance of the ZCR algorithm a simulation is carried out in MATLAB using a QAM signal. The following simulations are carried out using a 64 QAM signal. Using the formula outlined in equations 8.4 and 8.5 path mismatch can be introduced into a single

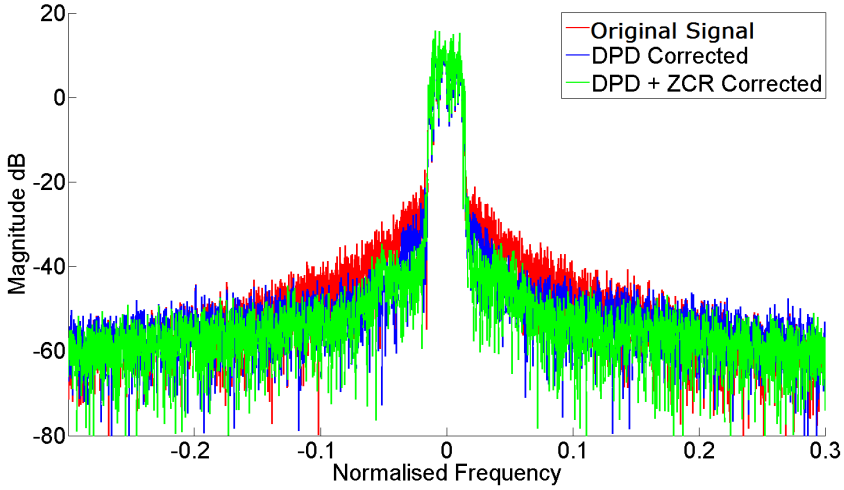


Figure 8.8: Effect of ZCR on simulated outphasing non-linearity.

path of the outphasing signals. The results of the simulation are presented in Figure 8.8. The simulated outphasing mismatch had 0.1 dB gain mismatch and 4 degree phase mismatch. Applying digital pre-distortion to the signal improved system performance marginally however large ACPR still exists. By performing ZCR with M set to 0.025 of the maximum signal amplitude and a window length of 60 samples the digital pre-distortion performance can be greatly improved. The output filtering stage of the ZCR process is currently set with 15 dB attenuation for out of band signals and the filter bandwidth is set to have a bandwidth of 5.5 MHz. The additional bandwidth provides room for some spectral growth but is insufficient for full reconstruction, this prevents the filter from fully reconstructing the original output signal. A consequence of the ZCR process is an increase in EVM, an increase of 1.2% EVM to the signal in this particular case. The trade-of for additional EVM is a reduction in ACPR levels. This is demonstrated in Table 8.1.

Table 8.1: Spectral impact of outphasing mismatch.

Signals	ACPR -10MHz	ACPR -5 MHz	ACPR 5 MHz	ACPR 10 MHz
Original	-47.5	-37.9	-37.9	-47.4
DPD	-54.8	-43.2	-43.1	-54.8
DPD + ZCR	-55.7	-50.0	-50.2	-56.3

8.1.3 Experimental Set-up

Evaluating the operation of an outphasing system in a circuit simulator can be computationally expensive for even static operation such as harmonic balance and s-parameter simulations. Modulated signal simulators such as envelope simulations can take an order of magnitude more computations. Due to the impracticality of envelope simulations it was decided to continue evaluation using an experimental set-up. The non-ideal characteristics which the zero crossing reduction algorithm is designed to negate are inherent in non-isolating power combiners. A test bench using non-isolating power combiners. This is a good approximation to an outphasing power amplifier due to gain, phase imbalances and path length mismatch.

8.1.3.1 Combiner design

The Chireix combiner is a non-isolating structure as depicted in Figure 8.9. Each path passes through a quarter wavelength micro strip before being connected to the output. There are many different topologies to achieve this arrangement. For simplicity we chose an arrangement similar to the structure presented in [141]. The structure is attractive from an assembly point of view as the only tuning element is the shunt capacitance. The design was carried out in Agilent's advanced design systems and fabricated an FR4 substraite. Given the center frequency of the other components of the test bench the center frequency of the design was chosen at 2.14 GHz. The operation of the combiner was verified experimentally before further measurements were carried out. The simulated combiner structure can be seen in Figure 8.9 and the board produced can be seen in Figure 8.10. The final design was tuned by moving the position of the capacitor for load compensation. The final design had an optimal center frequency of 2.13 GHz, very close to the desired simulated circuit. For our application the combiner is only used to demonstrate the non-linear characteristics of signal recombination.

8.1.3.2 Test bench

The small signal system is calibrated initially to remove IQ imbalance, LO feed through, amplitude imbalance between outphasing paths and amplitude and phase ripple over frequency. The test set-up is outlined in Chapter 4. The inclusion of a wide band signal capture, outlined in Section 6.1, will enable digital pre-distortion to be carried out using the full signal generation

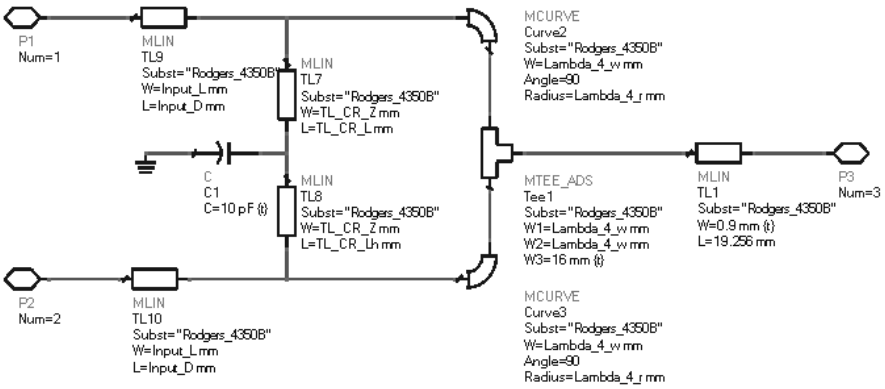


Figure 8.9: ADS schematic of Chireix combiner. The design is centered at 2.14 GHz and targeted for implementation of FR4 substrate.

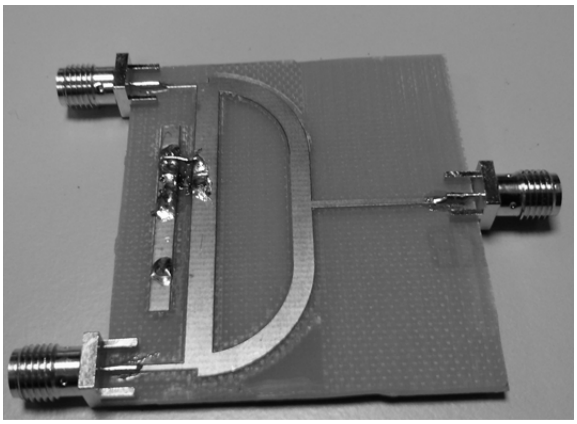


Figure 8.10: Implementation of Chireix power combiner. The centre frequency shifted from 2.14 GHz to 2.13 GHz when analysed after fabrication.

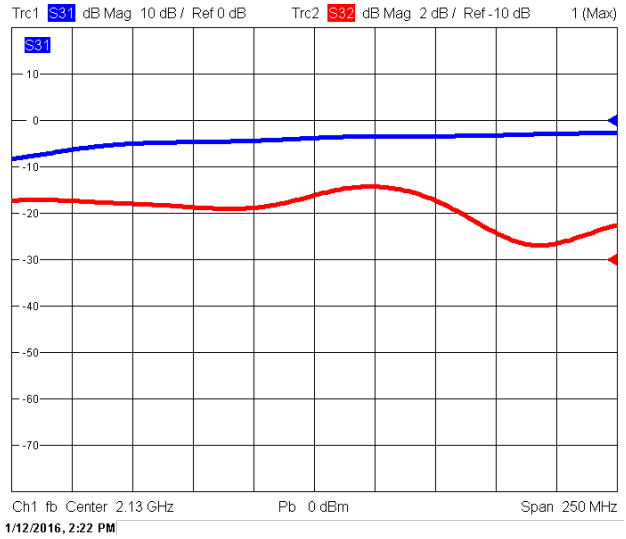


Figure 8.11: Amplitude imbalance of outphasing combiner paths across frequency, S31 is the amplitude imbalance in path 1 and S32 is the amplitude imbalance in path 2.

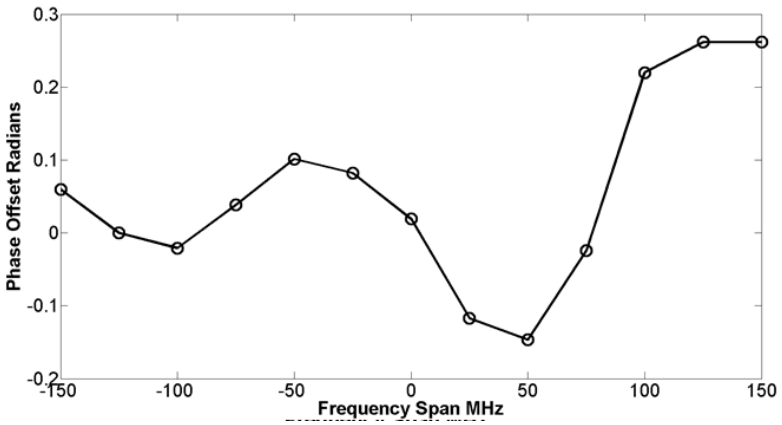


Figure 8.12: Outphasing angle deviation of system channels across frequency.

bandwidth. The system has been validated for linear outphasing operation using an isolating Wilkinson power combiner, this ensures that path mismatch effects which are outlined in the following section are attributed to the Chireix power combiner.

The system operation was compared to that of a integrated outphasing module. The aim of this work is to analyse any improvements to linear operation; therefore we examine the amplitude and outphasing angle imbalance across frequency and compare the variation in amplitude for a modulated signal. The variation in amplitude and outphasing angle across frequency can be seen in Figure 8.11 and 8.12. The amplitude of the input and output signals are presented in Figure 8.13. It can be seen that the system has limited dynamic range due

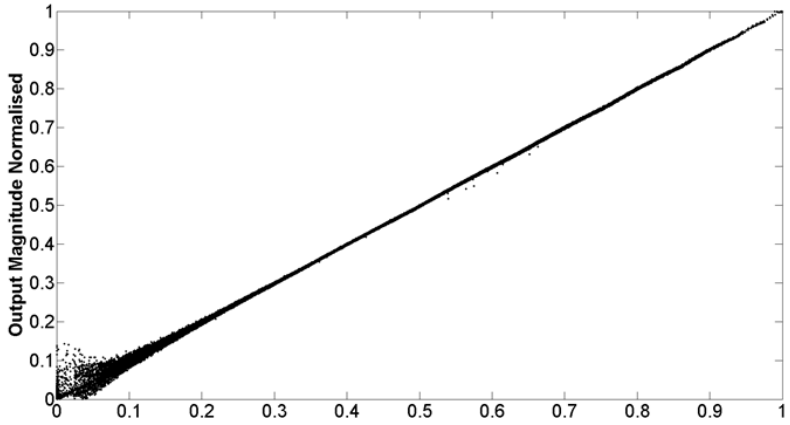


Figure 8.13: Input amplitude verses output amplitude of a QAM signal on the outphasing system. This plot demonstrates the linearity and memory functions of the system. It is evident that the largest deltas occur at lower output powers.

to path mismatch, which we wish to correct for. As the input modulated signal enters the region below 0.2 input magnitude additional memory is present in the signal. This behaviour is further increased as the signal reduces below 0.2 of the normalised input magnitude, additional memory effects can be seen. From these results it can be seen that our test bench is an accurate analogy for an outphasing power amplifier.

8.1.4 Measurements and Results

Using the same modulated QAM signal from the simulations, we evaluated the impact of the ZCR process on the test bench. First a lookup table is generated for the outphasing angle verses signal magnitude. This has two important roles: first the lookup table converts the non-linear outphasing angle to magnitude relationship to a linear mapping in order to modulate the signal; secondly by searching across outphasing angle we can determine the maximum signal null and therefore the dynamic range of the amplifier system. For static operation a dynamic range of greater than 60 dB can be achieved, however it is evident from Section 8.1.3 this is not the case for dynamic operation. In Figure 8.14 the time domain signals relating to the Chireix combiner can be seen with the signal illustrated in rectangular form, the white trace is the real component and the red trace is the imaginary component. Signal A is the QAM input signal. Signal B is the result after input to the calibrated outphasing test bench, the uncertainty about zero crossings can be clearly seen. The discontinuous nature of the non-linearity results in power at almost all frequencies within the sample range. Examining the time domain signal indicated that a

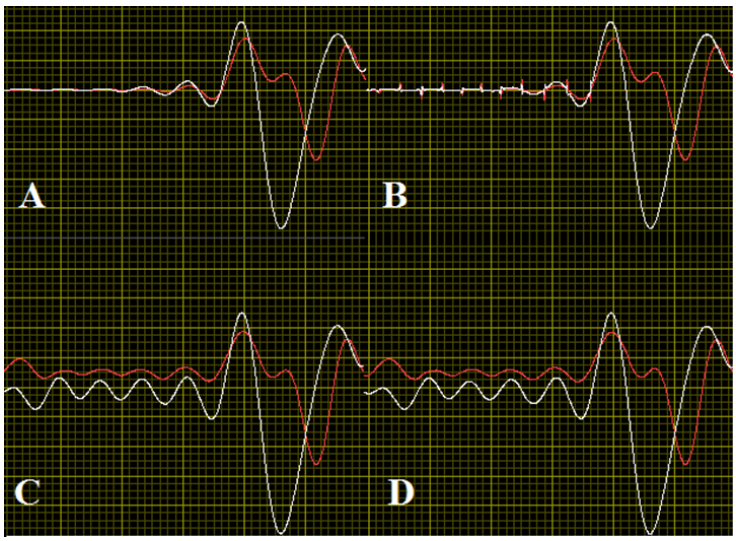


Figure 8.14: Time domain comparison of modulates signals captured from the output of the power combiner.

minimum magnitude of greater than 0.05 is required to avoid the discontinuities. Signal C is the ZCR signal to be input to the outphasing test bench, additional signal power has been added as outlined on the method in section 8.1.1. The combined output signal can be seen in signal D, it correlates very well to the modified input signal and the discontinuities that resulted in signal B have been avoided.

In Figure 8.14 and table 8.2 a direct comparisoncan be made between the outphasing of the QAM signal alone and the ZCR QAM signal. From this it is evident that while some improvement is gained in the adjacent transmission channels, approximately 3-4 dB, it is the out of band performance where the improvement is most evident, power levels in the third alternative channel number is 7-8 dB lower, and further out of band an improvement of up to 12-15 dB can be seen. In Figure 8.16 an advanced pre-distortion algorithm is applied to both signals and again the ZCR provides further improvement in both the adjacent and alternative channels. The improvement in the frequency spectrum is in line with what we expect from the simulations that were carried out. This confirms that the ZCR method can be implemented in systems that include CFR and DPD and still provide a substantial improvement in performance.

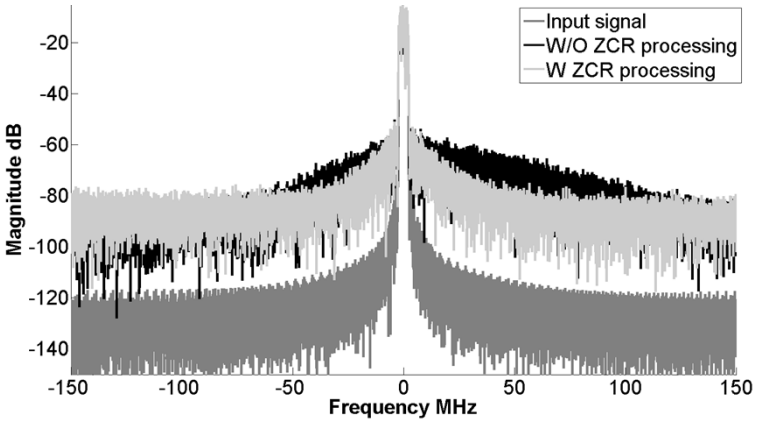


Figure 8.15: Frequency domain analysis of outphasing test bench with ZCR signal applied

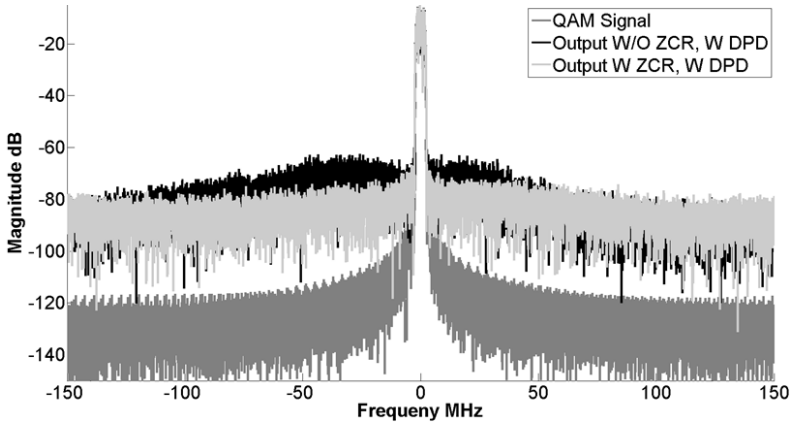


Figure 8.16: Frequency domain analysis of outphasing test bench with DPD and ZCR applied.

Table 8.2: Performance comparison of experimental evaluation.

	Average Signal Power dBm	ACPR Adj ch dB	ACPR Alt ch 1 dB	ACPR Alt ch 3 dB	EVM	EVM increase
QAM	-6.8	-42	-49	-51	3.3 %	0%
QAM + DPD	-5.8	-46	-51	-55	3.3 %	0%
QAM + CFR	-5.9	-44	-49	-54	3.5 %	0.2%
QAM + CFR + DPD dB	-5.8	-45	-51	-55	3.5 %	0.2%
QAM + CFR + CFR dB	-6	-46	-50	-58	6 %	2.7%
QAM + CFR + CFR + DPD	-5.8	-49	-53	-60	6 %	2.7%

8.2 Conclusions

A requirement of all amplifier topologies is the capability of achieving sufficient dynamic range to fully describe the modulated signal as a continuous function. Failing to achieve this results in a dramatic impact on system linearity, and the generation of a wideband noise floor. The outphasing amplifier topology suffers from this issue, achieving a high dynamic range can be difficult to achieve at a signal operational frequency, achieving a high dynamic range across frequency is even more so. This chapter analyses the importance of system dynamic range and proposes a technique which can reduce the non-linear impact on the output signal for certain dynamic range limited systems.

Previous solutions aimed to achieve the highest possible dynamic range at a centre frequency of operation, these include static DPD and system calibration. The effects which result in limited dynamic range quickly reappear when analysed away from the centre frequency. From the analysis carried out in this chapter it is evident that these effects limit the possibility of wideband signal transmission. The proposed zero crossing reduction method reduced the dynamic range of the modulated signal, enabling linear transmission in systems with limited or localised dynamic range.

The zero crossing reduction method alters the trajectory of the signal as it tries to pass through the centre of the unit circle, avoiding the problem region and reducing the complex non-linearity that occurs in this area. This is achieved by adding a low power pulse to the original signal and altering the signal phase, gradually circumnavigating a predefined region. Altering the signals properties introduces some error into the signal information.

The zero crossing reduction algorithm in conjunction with digital pre distortion provided +4 dB adjacent channel ACPR and +5 dB alternative channel ACPR over digital pre-distortion alone for an non-isolating outphasing combiner. Additionally it enabled a frequency flat wideband response, free from what is typically referred to as outphasing noise, on a test bench which exhibited strong out of band branch mismatch.

The increased EVM of the processed signals was within acceptable limits however with further development and optimisation of the algorithm, the authors will target this figure of merit as the key area of improvement. Ideally further development will reduce the EVM introduced by the process to levels that are in-line with current CFR algorithms, these are deemed as acceptable by current base station manufactures. Further optimisation of the windowing process and signal phase alteration will be targeted to remove the current requirement for output filtering.

Further exploration is required to determine if the outphasing system design could be optimised with the integration of ZCR. Alleviating the requirement for wideband dynamic range will increase design freedom of other design parameters, for example overall system bandwidth.

CHAPTER 9

Discussion, Future Work and Conclusions

The motivation for this work is to increase the efficiency of base station transmitters, counteracting the increasing power consumption in cellular networks due to the increasing number of nodes to meet current bandwidth requirements. The power amplifier is the single largest element of power consumption in the transceiver architecture. Switch-mode outphasing power amplifiers have demonstrated the potential for increased efficiency. This work focuses on linear amplification of wide bandwidth communication signals for this topology.

Chapter 3 highlights the operation of the topology in further depth and outlined the requirements from an amplifier design and system implementation point of view. The system components, signal generation and RF channels, as well as the amplifier must comply with the requirements for outphasing amplification. These include matching gain and phase characteristics in each amplification path, synchronised transmission of the outphasing signals and a matching frequency response. The latter being extremely important for wideband operation.

Simulations provide an excellent basis for analysis of the ideal amplifier, however not all real world effects can be studied in simulation. This is partly due to some simplification of the system, assumptions about physical components and computational limitations. The latter in particular can cause issues when analysis of modulated signals was carried out with circuit

simulations.

A test-bench which is presented in Chapter 4, enabled characterisation of the amplifier for static and modulated signals, single tones, multi-tones and various communications standards. Substantial work was carried out to verify the operation of the test-bench as an outphasing signal generation system. Doing so provided empirical knowledge of the amplifiers operation to be gained with out bias. This work thus achieved a better understanding of the non-linear mechanisms of a outphasing system for a modulated signal, the following areas were targeted as having the most potential for enabling linear operation:

- Increased non-linear memory at low power operation.
- Sensitivity of the outphasing signal to bandwidth limitation.
- Impact of limited dynamic range on modulated signal.

These properties are not mutually exclusive, both the sensitivity of the outphasing signals and the variability of dynamic range across frequency directly impact the spreading that is observed at low output powers.

To counteract the non-linearity of path mismatch across frequency, which is particularly visible at lower output powers, digital pre-distortion was investigated. Digital pre-distortion uses an inverse model of the non-linear system to counteract non-linear output. This work is therefore carried out in two separate parts. First analysis is carried out on a variety of single and dual path algorithms optimised for the characteristics of the outphasing topology. This analysis enabled the discovery of the most capable algorithms for characterising the non-linearity of the outphasing power amplifier. Behavioural modelling can serve a dual purpose, in comparison to circuit simulators a more computation efficient amplifier model can be used for system evaluation and the inverse of the model can be used for linearisation applications.

Chapter 5 presents the model development for digital outphasing power amplifiers using measured data from an outphasing PA module to verify the model accuracy. As a result two algorithms: segmented single path time series; and dual path time delayed neural networks were found to achieve better performance than existing published behavioural modelling techniques.

Chapter 6 presents the inversion of appropriate models for the purpose of linearisation.

Here the digital outphasing amplifier was linearised to achieve spectral mask performance for a 20 MHz multiple carrier WCDMA signal, improving on existing published outphasing linearisation material.

Investigating the effects of bandwidth limitation on an outphasing system is carried out in Chapter 7. A novel algorithm to limit the bandwidth expansion of the outphasing signal and therefore negating the effects of bandwidth limitation is presented. The algorithm concentrated on signal phase as the source of the majority of bandwidth expansion on an outphasing system. As such the bandwidth of the outphasing signal can be directly controlled by processing the input modulated signal. The proposed technique is optimised in order to minimise signal error.

Dynamic range is a function of the peak output power achievable by a system and minimum step in power which can be taken. Some power amplifier structures have difficulty achieving a linear output at lower power operation, compromising the amplifier ability to describe the desired modulation signal. A novel technique is presented in Chapter 8 which modified the modulated signal, reducing the dynamic range requirement for linear operation. The zero crossing reduction method alters the trajectory of the signal as it tries to pass through the centre of the unit circle, avoiding the problem region and reducing the complex non-linearity that occurs in this area. The algorithms enabled a frequency flat wideband response, free from what is typically referred to as outphasing noise. The algorithm was validated on a test-bench which exhibited strong out of band non-linearity by design.

9.1 Contributions

The primary contributions of this thesis are:

- An understanding of the non-linear effects within the outphasing power amplifier, relating them to signal processing. The impact of thermal variations within the devices of the outphasing topology is explored in simulation. Chapter 3.
- Developed novel modelling techniques with increased accuracy in both the time domain and spectrally in comparison to existing techniques. Chapter 5.
- Memory capable digital pre-distortion algorithms suitable for the digital outphasing power amplifier capable of wide-band linearisation. Chapter 6.

- Developed and verified a bandwidth limiting technique for the outphasing signals, acting on the modulated signal before SCS process maintains the constant envelope signal required for efficient operation. Chapter 7.

- Developed and verified a signal processing technique for the modulated signals to limit the dynamic range required for linear amplification. Chapter 8.

While the main theme of this work is to enable linear operation of outphasing power amplifiers the techniques outlined in Chapters 7 and 8 are applicable to outphasing, envelope elimination and restoration and class-S power amplifiers.

9.2 Future work

As with the work carried out in this thesis, there are direct extensions to each of the linearisation methods outlined above.

- Bandwidth expansion reduction algorithm addresses a concern of system designers over the bandwidth requirement of all components in the outphasing system, particularly as the bandwidth of modulated signals increase. While the initial results from testing the algorithm are promising further evaluation, particularly with a practical outphasing system would help further refine the method. A target for further development is the cancellation process, with a view to reducing the algorithms impact on signal ACPR. This would subsequently remove the need for the final filtering stage, reducing the overall computational cost of the algorithm.

- Zero crossing reduction algorithm has been developed to address limited dynamic range that the outphasing amplifier experiences, particularly as the outphasing signal deviated from the centre frequency of the system. This method warrants further analysis, in combination with outphasing amplifier design, the potential for a more flexible outphasing system implementation could be achieved.

- The RVTDNN characterisation of the outphasing power amplifier has been proven as a highly accurate behavioural model. Future work will concentrate on investigating training methods for the RVTDNN as a two path - linearisation method. To achieve

this some modification to the structure may be required in order to ensure a constant envelope input to the outphasing amplifier once the linearisation has been applied.

Further investigation of the non-linear mechanisms in alternative outphasing architectures and how the linearisation techniques proposed in this thesis can be applied. Work is currently under way on analysis of the linear back-off outphasing power amplifier in conjunction with NXP. The topology shares the majority of the non-linear characteristics of the switch-mode outphasing system, however additional non-linear components are introduced as the amplification stages transition from a deeply saturated outphasing mode, to a linear mode of operation.

9.3 Conclusion

The work carried out in this thesis furthers the understanding of the non-linear effects which impact switch-mode outphasing power amplifiers. Three distinct yet complementary methods of improving linearisation are examined. Novel techniques identified and validated in the course of this work have improved the linearity of the switch-mode outphasing topology and helped to advance the outphasing amplification system towards a commercially viable solution. This was demonstrated by a milestone in linearisation for an outphasing topology, a 20 MHz quad carrier WCDMA signal achieving 3G 3GPP spectral mask requirements. The proposed signal processing techniques in the latter part of this thesis provides the potential to extend the performance of our achievements in future work.

APPENDIX A

Time Series Coefficient Reduction

Coefficient reduction tools for data analysis are very important for prediction accuracy and model interpretation. With a large number of weights the system can provide a very accurate model however is susceptible to over fitting. The aim of parameter reduction is to reduce possibility of over fitting while maintaining suitable model accuracy. When applied to behavioural modelling it has the added benefit of reducing computational complexity of the implemented model. Parameter reduction is not a new concept in amplifier behavioural modelling and has been achieved in the past through the use of more compact and flexible models such as the memory polynomial discussed in Section 2.5.2.5 or the selective pruning of coefficients from a full Volterra kernel as demonstrated in [142].

Many of the models presented in this chapter are based upon the Volterra kernel as it provides a comprehensive set of non-linear coefficients which can comprehensibly describe non-linear systems. The complexity of this algorithm increases exponentially with an increase in non-linear order and dramatically with an increase in the number of memory terms. This is extremely apparent in the two path Volterra model where the number of terms is more than two times that of a conventional Volterra series of the same order and memory length. To ensure maximum efficiency for the model a unique subset of coefficients for each non-linear system must be extracted. The analysis is preformed on a Class AB 10W NXP power amplifier

which is driven into non-linear operation. This work presents a method to determine the most important delay taps for time series models [143] as well as coefficient reduction methods applied to power amplifier behavioural modelling [3].

A.1 Time series

Volterra series behavioural modelling is a powerful time series estimator for non-linear systems. The model uses every possible combination of terms up to a given order and for a given memory depth. It has been extensively used in both biological and financial modelling in both its continuous time and discrete form. Modelling RF power amplifier we use the discrete time, base-band complex from the the series [73]. To date it has been successfully used to model power amplification systems. The Volterra series is outlined in equations A.1. Where y is the output, x is the input, h represents the Volterra coefficients, k is the order of non-linearity and l is the memory depth.

$$y_k(n) = \sum_{n_1=-M+1}^{M-1} \sum_{n_2=-M+1}^{M-1} \cdots \sum_{n_k=-M+1}^{M-1} g_{n_1,\ldots,n_{k-1}}(n) * \left[x(n) \prod_{l=1}^{k-1} x(n-n_l) \right] \tag{A.1}$$

Subsets of the Volterra such as the memory polynomial, generalised memory polynomial and cross memory polynomial are designed to reduce the number of coefficients in a time series yet maintain accuracy for the general operation of a non-linear system, in the case of the generalised memory polynomial and cross memory polynomial the are both designed with power amplifier in mind. The algorithms outlined are optimised to some extent, they cannot be determined as the most accurate solution or the minimum implementation. The following Sections outline methods of determining the optimum time series for a specific system, in terms of both the reduced number of coefficients or the system accuracy.

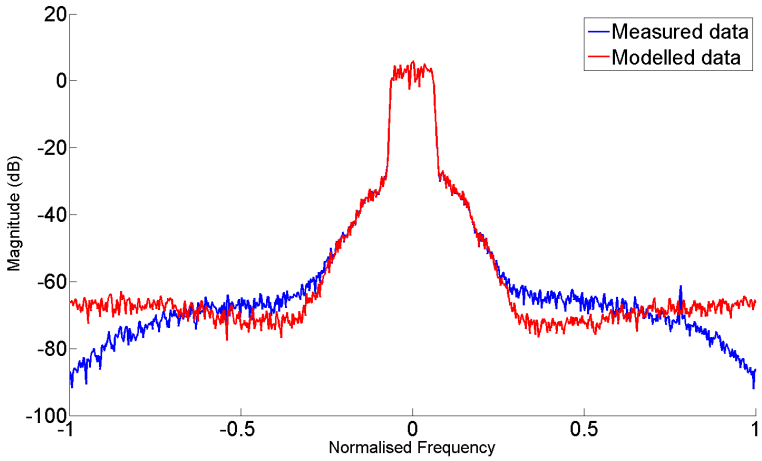


Figure A.1: Volterra series behavioural model - NMSE -44.6 dB - 329 coefficents.

A.2 Lipshitz Algorithm

In many cases the modelling data is analysed in order to obtain an optimum training data set, to reduce the computational complexity of the training process. This is generally carried out with statistical methods such as principle component analysis. The authors in [144] the Lipshitz algorithm as a method for determining the memory length required in amplifier behavioural model applications. This is further explored in [8] as a method for model parameter reduction through the exclusion of unneeded memory terms. This method presents a very useful method for efficient model extraction of systems with long term memory effects. As the sample rate and operational bandwidth of RF systems increases, memory terms may become increasingly sparse, this method provides an ideal method for model extraction with out the need for sample rate conversion.

$$q_{ij} = \frac{\mid y(i) - y(j) \mid}{\mid x(i) - x(j)}, (i \neq j) \tag{A.2}$$

$$q^n = \left(\prod_{k=1}^{p} \sqrt{n} q^{(n)}(k) \right)^{1/p} \tag{A.3}$$

The Lipshitz algorithm is applied to the power amplifier data set in the following manor:

1. N input - output data pairs are acquired for the system and the maximum number of delays for the system is decided.

2. Set a threshold value relative to the total number of all Lipschitz numbers.

3. Calculate the Lipschitz numbers for sample points up to a set maximum delay.

    - Compute Lipschitz quotients for input - output pairs using equation A.2.
    - Determine the p largest quotients.
    - Calculate the corresponding Lipschitz numbers using equation A.3.

4. Calculate the first difference between the Lipschitz numbers.

5. Determine what first differences are greater than the threshold value.

To determine the maximum memory length required for an amplifier structure steps 1-3 are implemented. The Lipschitz quotient is computed using the distance between two input samples $\mid x(i) - x(j) \mid$ and the distance between two output samples $\mid y(i) - y(j) \mid$. From this the Lipschitz number is computed using equation A.3 where $q^{(n)}(k)$ is the kth largest Lipschitz quotient among all $q_{ij}^{(n)}(i \neq j; i, j = 1, 2, \ldots, N)$. The parameter p is a positive integer whose value is typically a smaller fraction of the number of input samples N. The addition of steps 4-5 in [8] involves subtracting the Lipschitz number magnitudes from on another to gauge the relative influence of a delay tap relative to the previous one. This method extends the algorithm to determine the most important delay samples from which a reduced kernel set can be extracted. The Volterra series is presented in equation A.1 where M is a finite memory length and k is the order of non-linearity. Using a vector of selected memory terms j of length J the reduced Lipschitz Volterra function is presented in equation A.4.

$$y_k(n) = \sum_{n_1=j(1)}^{J} \sum_{n_2=j(2)}^{J} \cdots \sum_{n_k=j(k)}^{J} g_{n_1,\ldots,n_{k-1}}(n) * \left[x(n) \prod_{l=1}^{k-1} x(n - n_l) \right] \tag{A.4}$$

Figures A.2 and A.3 demonstrate the Lipshitz algorithm applied to the Class AB power amplifier data. From the analysis of the delay taps it is evident that the model requires four taps, $x(n, ..., n-3)$, to get the best modelling solution. The analysis also indicates that if reduction is to occur that the least important tap is $x(n-2)$, removing this should have the least impact on the modelling performance, which is presented in Figure A.3. The modelling performance is equivalent to the full Volterra series however the number of coefficients has reduced from 329 to 119.

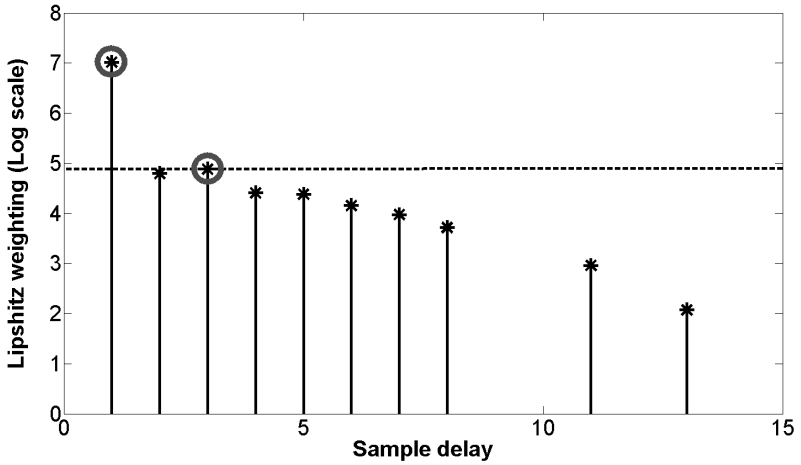


Figure A.2: An example of the Lipshitz analysis on the input and output signals from the Class AB amplifier. The analysis was carried out over 15 tap delays, the reduction identified that along with the 1st tap delay the 3rd tap delay held the next greatest importance.

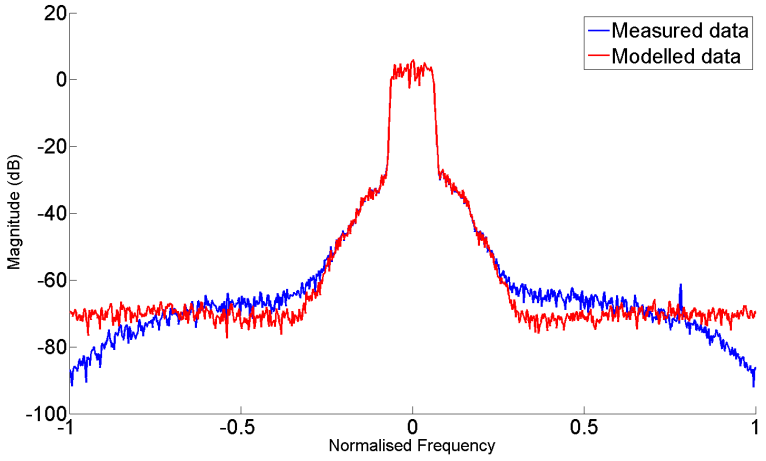


Figure A.3: Lipshitz time series reduction of a Volterra series - NMSE -44.8 dB - 119 of 329 coefficents.

A.3 Genetic Algorithm

In [145] the author uses a genetic algorithm to generate a reduced coefficient set for the Volterra series. The full Volterra kernel is extracted, using the genetic algorithm a predefined number of kernel elements are chosen which best describe the non-linear system. To evaluate the subset of kernel elements for each operation of the genetic algorithm the least squares method is applied, ant he resulting model is evaluated using the mean squared error estimation. The method demonstrates a dramatic reduction in the number of coefficients, in addition the development of a forces mutation operation within the GA greatly reduced the number of iterations required to achieve conversion. This method provides an optimum model for a resource constrained system.

Genetic algorithms are based upon evolutionary theory, by assigning a given solution is an individual a group of individual can form a population. Within a individual solution there are a number of coefficients called chromosome's. The algorithm will search through the population to find the individual solutions which provide the an answer closest to the desired goal. By selecting a group of best solutions and crossing sharing their individual chromosome's in multiple arrangements a new population can be formed. This new population is referred to as the preceding generation. In addition to this every population has a subset of individuals which are not formed from the previous generation, but have random chromosome's. This is referred to as mutation, this occurs within the population in order to diversify the chromosomes, preventing the algorithm from settling in a local minimum when a global minimum exists.

A discrete or binary genetic algorithm finds the optimum subset of kernels, the length of which is predefined C. A fitness function complies a kernel subset of the input signal and extracts the corresponding set of weights. The results are evaluated using the target data set and the Figure of merit, in this case the NMSE is passed back to the GA. The Figure of merit is minimised by the genetic algorithm, the chromosome with the lowest NMSE is the winning kernel subset x_i which consists of the kernel values $[x_{c(1)}, x_{c(2)}, \ldots, x_{c(C)}]$. The resulting function is a linear vector equation represented in equation A.5.

$$y_v = \sum_{i=0}^{M-1} w_i x_i \tag{A.5}$$

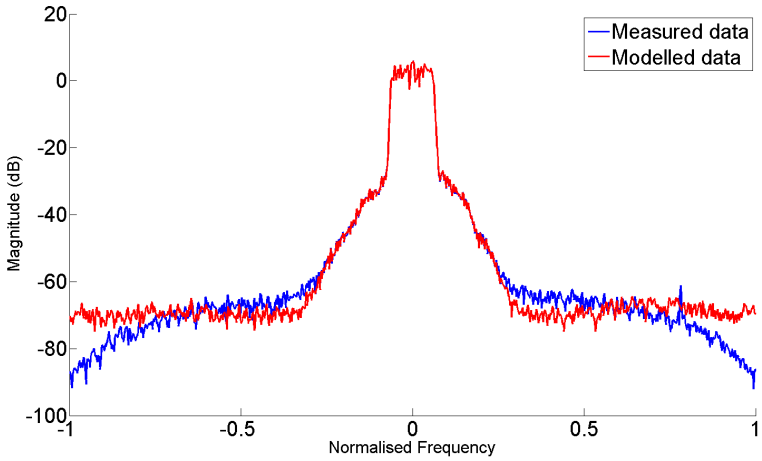


Figure A.4: GA time series reduction of a Volterra series - NMSE -42.1 dB - 90 of 329 coefficents.

A.4 Least-absolute shrinkage and selection operator

The Least-absolute shrinkage and selection operator (Lasso) algorithm is method for linear estimation of models first presented in [146]. Using a combination of regression and shrinkage selection it demonstrates greater performance than regression algorithms alone. It is typically demonstrated for linear systems however in [147] the author demonstrates the capability of the algorithm for non-linear systems in which the kernel coefficients calculation is linear, namely the Volterra series.The Lasso definition for a time series is outlined as follows, $xt = (x_t, 1, ..., x_{tp})^T$ where x_t are the computed kernels of the input signal and yt are a vector of training data. The following assumptions, common to regression methods are made: the observations y_t are independent and we assume that xtp is normalised so that the mean of x_{tp} is zero and the mean of x_{2tp} is one. The Lasso estimate is defined by

$$\sum_p \mid \beta_p \mid \leq k \tag{A.6}$$

$$(\alpha, \beta) = argmin \left[\sum_{t=1}^{N} (y_t - \alpha - \sum_p \beta_p x_{tp})^2 \right] \tag{A.7}$$

Where $k \leq 0$ is a tuning parameter, given that the mean of y_t is also zero we can omit without loss of generality. By tuning the value of k the reduction function can be controlled to find a balance between model accuracy and number of remaining weights. In this paper

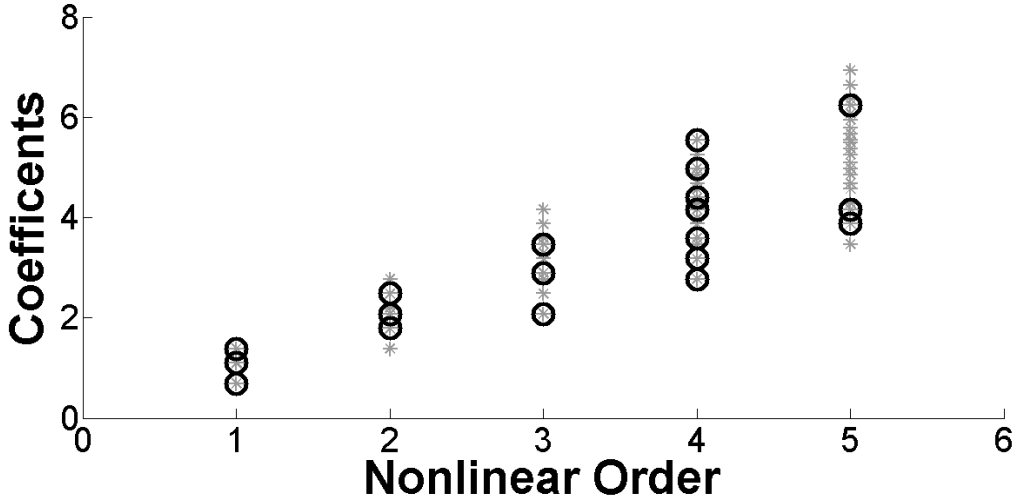


Figure A.5: Example kernel Reduction utilizing Lasso function. Grey is the full Volterra series, Black are the chosen parameters for reduced model.

the optimization of the tuning parameter is performed as outlined in [146] a vector of possible values for k is analysed using the generalized cross validation technique [148]. The array is constructed of N values equally spaced from k_0 to 0 where k_0 corresponds to the least squares solution with zero shrinkage, $k_0 = \sum | \, {}^{0}_{p} \, |$ where β_p^0 is the least squares solution.

The method provides a automated and flexible algorithm for determining the most efficient number of coefficients required to accurately model a given system. In [4] the method is applied to the Volterra model for a power amplifier system. The result is a subset of kernels for similar to that in Section A.3. Due to the fact that a power amplifier is a largely deterministic system and the input and output data is highly correlated, the Lasso method can be very effective in reducing the number of weights in the time series. Figure A.5 shows a visual representation of the Lasso selection on a 5th order Volterra series.

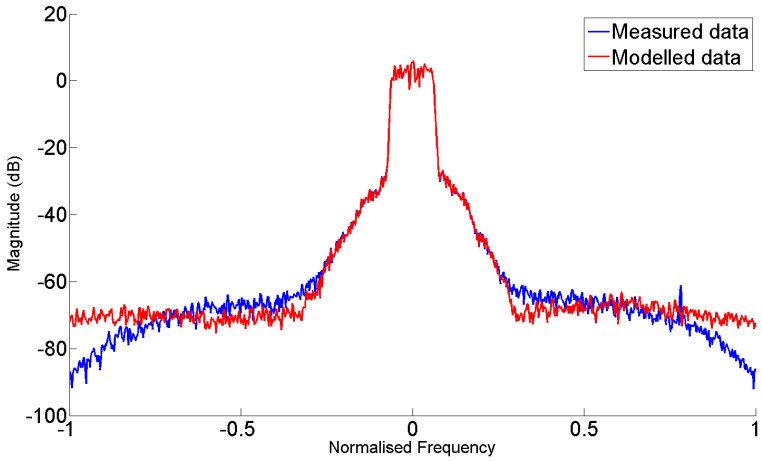


Figure A.6: Lasso time series reduction of a Volterra series - NMSE -45.2 dB - 86 of 329 coefficents.

A.5 Analysis of chosen methods

In this chapter three different approaches of coefficient reduction are for time series non-linear models are presented. The Lipshitz algorithm can efficiently determine the required memory taps by analysing the input and output signals alone. In comparison to the genetic algorithms reduction or the Lasso reduction the kernel for the non-linear time series is not required. On the down side reduction can only occur for the number of memory taps, selection of individual coefficients is not possible.

Both the genetic algorithm and the Lasso algorithm have the ability to select individual coefficients, therefore they have the ability to achieve the optimum minimisation of the time series. The Lasso algorithms provides increased performance and reduced computation time as demonstrated from the analysis carried out on the Class AB power amplifier in Figures A.6, A.4.

A.6 Time series reduction for outphasing power amplifier models

The outphasing power amplifier described in Chapter 3, is a multi input signal output system. Many of the existing outphasing power amplifier models are also MISO structures as they closely resemble the topology of the outphasing power amplifier. In Section 5.2.1 the two path Volterra model is presented. Computationally the two path Volterra is on average between 2.5-3

times greater than a single Volterra series. As stated in [120] the number of inputs is not limited a two path system, however the number of computations in the model increases dramatically as the number of inputs are increased, care must be taken to balance between computation complexity and model performance.

To increase the computational efficiency during model implementation the Lasso algorithm was applied to two path Volterra as well as the Volterra and vector switched Volterra time series during training. As a result a reduction of 90%, 68% and 48% was seen for the models respectively. The weights that survive the regression process then form a new reduced model structure while retaining the model accuracy and in some cases increasing the generality. From Table 1 it can be seen that the reduced models maintain accuracy within 1 dB NMSE of the original model. The results are summarised in the table below.

Analysis was carried out in Matlab 2013, the processing was carried out a Windows 7 computer utilizing an Core i7 - 2600 processor and 8 gigabytes of memory. In each case the processing of the individual model special requirements are carried before the final sets of weights are extracted, this includes piecewise segmentation and vector switched segmentation of the data and Lasso reduction. Both the training and test data sets contain 16,000 data samples, for our analysis all of the training samples are used in both vector switched and Lasso analysis, for larger data sets a subsets of the training data can be used in these processing steps without an impact on the process accuracy, in some cases this can provide a dramatic reduction in computation time.

Evaluation includes mean squared error in equation A.9 and normalised mean squared error in equation A.10 and the adjacent channel error power ratio ACEPR A.10 as figures of merit.

$$ACEPR = \frac{\int\limits_{adj} | E(f) |^2 \, df}{\int\limits_{ch} | D(f) |^2 \, df} \tag{A.8}$$

$$MSE = \frac{1}{n} \sum_{n}^{t=1} | \hat{y}(t) - y(t) |^2 \tag{A.9}$$

$$NMSE = \frac{1}{n} \sum_{n}^{t=1} \frac{| \hat{y}(t) - y(t) |^2}{| \hat{y}(t) |^2} \tag{A.10}$$

Model	Model segments	Model order	Memory Taps	Training Time (seconds)	Test MSE	Test NMSE	Weights (total)	ACEPR
Volterra	NA	7	3	13.3	-39dB	-26.7dB	70	-36.8dB
Volterra - Lasso	NA	7	3	47.7	-39dB	-26.2dB	38	-37.0dB
VSV SOM	10	5	3	11.57	-49dB	-36.2dB	1190	-49.2dB
VSV SOM - Lasso	10	5	3	87	-45dB	-33.2dB	616	-46.0dB
Two Path Volterra	NA	5	3	23.9	-44dB	-31.1dB	256	-43.1dB
Two Path Volterra - Lasso	NA	5	3	133.6	-43dB	-30.68dB	23	-43.1dB

A.7 Conclusion

In this Section three methods for time series coefficient reduction are presented and compared using measured data from an Class AB power amplifier. By applying the full Volterra series as a behavioural model for the non-linear system, an accurate characterisation is possible at the expense of computational efficiency. In most cases the Volterra series is know to be sparse, meaning that a subset of coefficients are performing the characterisation, the others are set to almost zero, not contributing and in some cases hindering the accuracy of the model.

Two distinctly different approached are presented for coefficient reduction, the first optimises the number of delay taps required to characterise the system, an important parameter as demonstrated in Section A.2. The reduction in delay taps is not directly proportional to the number of coefficients, reducing the number of delay taps by 25% reduced the model size by 63%. The second approach optimises the entire coefficient set by analysing the impact on accuracy of disabling certain coefficients. A genetic algorithm and the Lasso algorithm both optimise the dataset in this way, of the two the Lasso algorithm provides better performance in terms of number of coefficients in the final model and the characterisation accuracy.

The Lasso and genetic algorithms both reduce the data set in a more desirable manor when compared with the Lipshitz algorithm, however this is achieved at the cost of computational complexity. For single input models such as the SISO Volterra the Lipshitz provides the best compromise between computational efficiency and reduction as the analysis is only performed on the input and output signal vectors, orders of magnitude smaller than the extracted kernel matrix required for the genetic algorithm and Lasso methods. However for the MISO Volterra designed for the outphasing power amplifier, the non-linear order and model structures is responsible for the large number of coefficients. Therefore the Lasso algorithms is more suitable, this is apparent in the outphasing power amplifier model as a reduction of 90% was possible for the two path outphasing model.

APPENDIX B

Switch model power amplifier modulators

Class-S power amplifiers are a combination of a switch mode power amplifier, driven by a digital modulator. The switch mode power amplifiers class D/E/F have been successfully implemented for RF frequencies [149] [150]. A challenge still remains in efficiently and linearly driving the switch mode power amplifier. An overview of the class-S power amplifier is presented in Figure B.1, and demonstrates the requirement for a digital modulator to convert the amplitude modulated communications signal into a constant amplitude, digital signal. The power amplifier output is passed through a reconstruction filter to convert digital signal back to a analogue amplitude modulated signal. The reconstruction filter specifications will be defined by the available bandwidth of the modulator, defining the reconfigurability of the amplifier. This chapter will analysis the existing digital modulators for class-S operation. A FPGA has the possibility to offer a cheap and reconfigurable option for digital modulators, presented is a topology of linear transmission of quadrature modulated signals [7]. The performance of the currently available FPGA's for digital signal generation is also analysed [6].

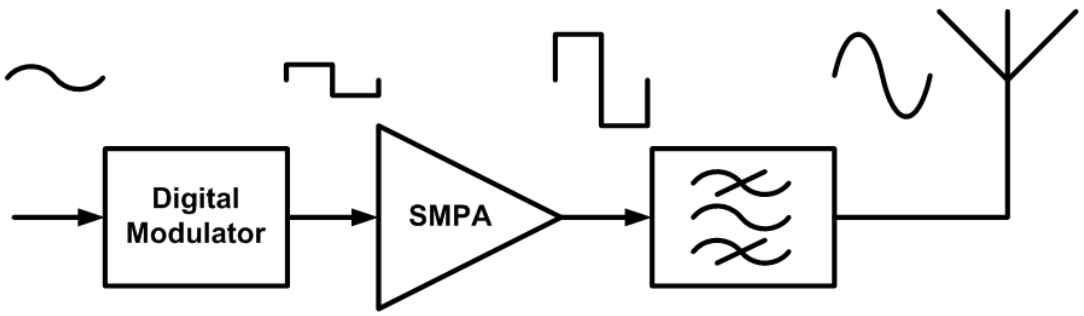


Figure B.1: SMPA transmitter chain

B.1 Digital Modulator

The purpose of the modulator is to encode the desired high resolution, low speed, amplitude modulated signal in to a low resolution (typically a single bit), high speed, digital modulated signal. The information is modulated in many ways, the sigma delta modulator encodes the data on pulse density, the pulse width modulator encodes the data on pulse width or percentage duty cycle and the pulse position modulator positions a fixed pulse at varying distances to encode the amplitude modulation. Both the pulse density modulator and the pulse width modulator offer the ability to achieve maximum signal dynamic range and therefore are more commonly used for communications signal modulation. The following section will give a brief overview of the sigma delta modulator and pulse width modulator topology.

B.1.1 Pulse Width Modulators

Pulse width modulator in Figure B.3 encodes information in a 2 level signal using the width of each pulse to represent the input signal as seen in Figure B.2. To achieve a usable noise floor the resolution of the pulse widths needs to be very fine, requiring high speed analogue implementations to meet the required resolution. Pulse width modulators operate by comparing the analogue input to a reference signal, the reference signal varies with time, when the input analogue signal is lower than the reference signal the output will be low, when the input signal is higher than the reference signal the output will be high. The reference signal varies with time in such a way that the output pulse will only be in a high or low state for a percentage of the time depending on the input signal. There are various reference signals used such as a triangular wave and a ramp signal , these signals provide a linear comparison between input amplitude and output pulse percentage allowing signal linearity to be maintained. PWM performance

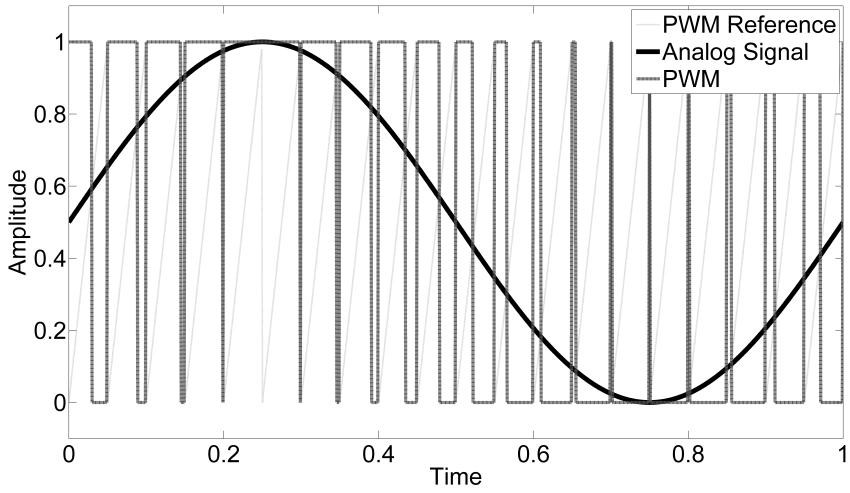


Figure B.2: Pulse Width Modulation

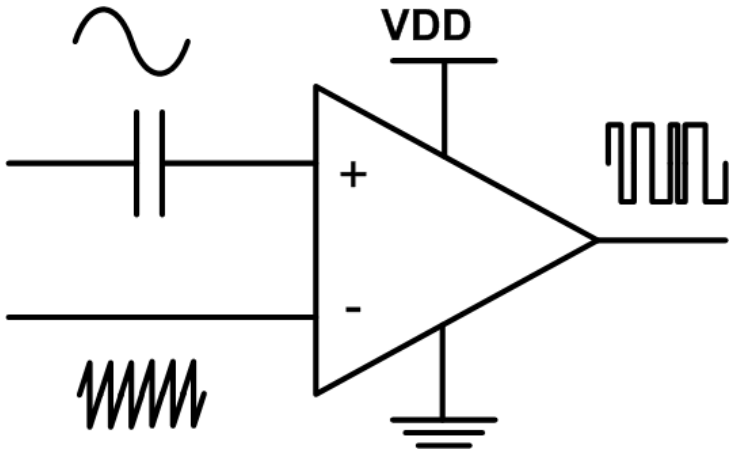


Figure B.3: Pulse Width Modulator

depends on the quality of design, in [151] a PWM with 80 MHz bandwidth and -52 dB ACPR was designed for Class-S operation. The low noise floor associated with PWM modulators and allows for wide band operation.

B.1.2 Pulse Density Modulators

Pulse density modulation uses a series of binary bits of equal width to represent a analogue signal in the digital domain. The arrangement of the pulses or the **density** is used to represent the input signal. The modulation scheme can be used in both digital and analogue systems allowing for flexible implementation. A Sigma Delta modulator is required to encode a analogue input signal into a digital PDM output.

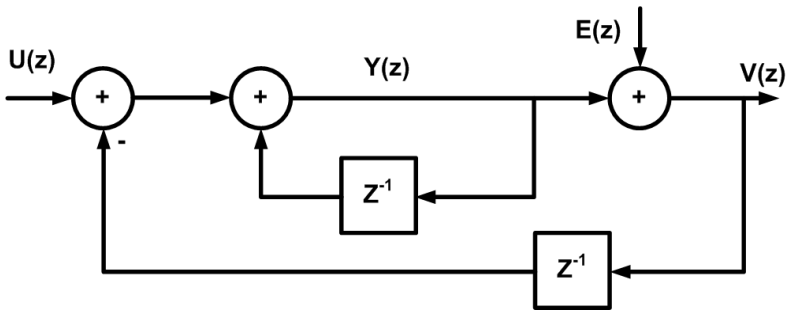


Figure B.4: First order SDM

$$Y(z) = U(z) - V(z) + Y(z-1) \tag{B.1}$$

$$V(z) = Y(z) + E(z) \tag{B.2}$$

A Sigma Delta Modulator (SDM) operates by converting the output to a digitised version of the input, however quantisation of the signal increases the noise floor of the output. Figure B.4 illustrates the outline of a first order modulator, the integrator operates as a first order low pass loop filter, the quantise is represented by the error source E. The operation of the modulator is outlined in equations B.1 and B.2 The SDM is designed to reduce the in band noise, allowing course levels of quantisation to achieve dynamic range similar to finer levels of quantisation in a standard system. At any instance of time the error of the output relative to the input may be high, however the SDM operates by agitating the error over time using the error to influence future output's. This is achieved by a feedback path from output to input. The error is calculated using the difference between current input and previous output, the loop filter is then updated using this value. The filter shapes the quantisation noise of the output rejecting it from the desired frequency band and spreading it across the remaining spectrum, the shape of this response is called the noise transfer function (NTF) and can be described by equation B.3 similarly the signal pass band of the modulator is described by equation B.4. The quantisation noise generated from the output is at a constant power level, therefore by increasing the available spectrum the power level of the quantisation noise can be reduced across the entire frequency band. The frequency of operation will however be limited

by implementation and circuit constraints.

$$NTF = \frac{1}{1 + H(z)} \tag{B.3}$$

$$STF = \frac{H(z)}{1 + H(z)} \tag{B.4}$$

Sigma delta modulation performance is defined by three parameters, frequency of operation, modulator order, and the number of quantisation levels of the output [152]. In direct analogue to digital conversion the noise floor of the signal is defined by the number of levels of quantisation, a sigma delta modulator changes this, using an internal loop filter to push the unwanted quantisation noise out of band, increasing the dynamic range of the signal. In a SDM the number of poles in the system define the order of the modulator and the arrangement of the poles define the type of modulator that is being implemented, either low pass, band pass or high pass. Pole placement in sigma delta modulators can be used to shape the out of band quantisation noise also know as the noise transfer function of the modulator. Increased number of poles in the system will allow greater flexibility in the system when designing the modulator however they can effect the frequency of operation if the designer is not careful [153]. The order of the modulator system effects the depth of the NTF notch as well as the rate of increase of the NTF about the notch as illustrated in Figure B.5, each pole in the notch adds another 20 dB per decade slope to the NTF.

As stated above the SDM aims to reduce the error between the input and its output, operating frequency of the modulator has a strong influence on the modulators ability to reduce error. The modulator aggregates the error over successive iterations, increasing the number of iteration reduced the overall error attributed to the input. In terms of the frequency spectrum this leads to increased depth in the noise transfer function as well as increased bandwidth within the notch. The ratio of operating frequency to the converted signal is refereed to as the oversampling ratio (OSR), This value can be used as a performance metric for the modulator structure. For radio frequency systems the bandwidth of the signal can be between 5-80 MHz for multiple carrier signals. To achieve sufficient performance form a sigma delta modulator a high OSR is required leading to GHz operating frequencies [154]. This requires designs to be developed on Application Specific Integrated Circuits (ASIC's) which are both time

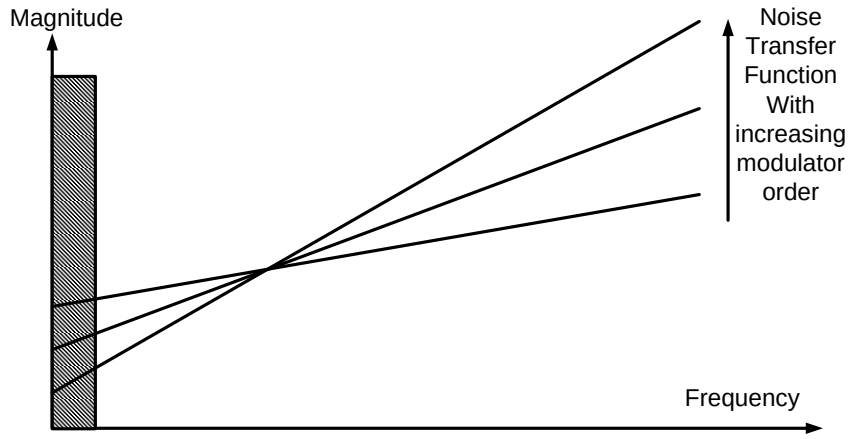


Figure B.5: Effect of modulator order

consuming and expensive to develop. This leads to alternative modulator designs to aimed to be implement on reconfigurable hardware such as Field Programmable Gate Arrays (FPGA's) or Digital Signal Processor's (DSP's) such as a Parallel modulator configuration [155] and a low frequency modulator structure that uses the effect of spectral copping and up conversion to place a signal at a higher carrier frequency while also negating the effects of Sinc shaping in the frequency spectrum [156].

The number of levels of quantisation on the output can be varied depending on the application of the SDM, as the output quantisation is responsible for generating noise in the SDM increasing the number of levels can reduce the overall noise output of the modulator. However in the context of digital power amplifiers it is generally more desirable for 1 bit quantisation, generating a 2 level switching signal for the power amplifier. There are exceptions to this such as [157] where a multiple level PDM is converted to a type of PWM using a look up table on the output. This has the advantage of reduced noise however the PWM conversation increase the output speed of the bit stream, for high speed SDM designs this may tax the digital I/O capability.

B.1.2.1 ASIC Sigma Delta Modulators

In order to modulate SMPA's at RF carrier frequencies SDM's must output the digital bit stream at gigahertz frequencies. Implementing such a circuit is only possible using dedicated integrated circuit's or possibly FPGA's. ASIC implementation while being a costly process can produce the fastest implementations of the SDM circuits and circuits operating up to 6 GHz have been developed [158]. The following is a comparison table of state of the art designs in Table B.1. The table presents the performance of the modulator structures, the designs that are of interest for SMPA operation are bandpass structures that are designed to operate with communications signals, of the designs presented [154] and [159] show the best results with dynamic range performance of approximately 53 dB each. and wide bands of operation. The designs are capable of such performance due to their operating frequency greater than 4 GHz, this allows them to maintain the SNR value over large bandwidths greater than 50 MHz, this makes them extremely useful in wide-band communications and reconfigurable radio systems.

B.1.2.2 FPGA Sigma Delta Modulators

Due to the cost and time required to implement an ASIC design there have been some efforts to implement an discrete version of the modulator structure on an programmable platform such as a DSP or FPGA. Implementation on programmable logic not only reduces cost, increases time between design iterations but also allows the option and flexibility of dynamic reconfiguration to operate as part of a software defined radio for multiple standard transmission. The system outlined in [62] uses a commercial FPGA development board to generate a binary pulse density signal capable of driving a Class-D amplifier. The limitation of performance of FPGA designs is the maximum operating frequency of the modulator. FPGA's are groups of generic logic blocks, and are configured by selecting routing paths and enabling functions. This provides a flexible platform for design implementation at the cost of maximum performance. Standard SDM designs are limited to hundreds of mega hertz operating frequency compared to the gigahertz operating frequency of ASIC designs. The designs outlined in Table B.2 outline a performance comparison between modulator structures and their operation is described in the following paragraphs.

In [62] a sample and hold process followed by a frequency up conversation known as

Implementation	ADC	ADC	SMPA	SMPA	SMPA	SMPA
Company	Texas Instruments	NXP	-	-	-	-
Reference	[158]	[160]	[161]	[154]	[159]	[162]
Sample Frequency	6GHz	4GHz	7.5GHz	4Gsps	1.4 - 6 GHz	2.5GHz
Bandwidth	60MHz	125MHz	20MHz	50MHz	100MHz	10MHz
SNR	61.5dB	65.5dB	45.5dB	53.6dB	50dB	46.6dB
Technology	45nm CMOS	45nm CMOS	SiGe Bipolar	90nm CMOS	90nm CMOS	0.25um SiGe BiCMOS
Resolution	1 bit	4 bit	1 bit	1 bit	1 bit	1 bit
Modulator Type	Low Pass	Low Pass	Bandpass 1.5-2.45GHz	Bandpass 1GHz	Bandpass 0.7-3GHz	Bandpass 2.1 - 2.2 GHz
Dynamic Range	73dB	70dB	45.5dB	53.6dB	53dB	46.6dB
Test signal	Sin Wave	Sin Wave	2 Tone Sin Wave	WCDMA 5MHz	WCDMA 5MHz	WCDMA 5MHz

Table B.1: ASIC modulator comparison of state of the art

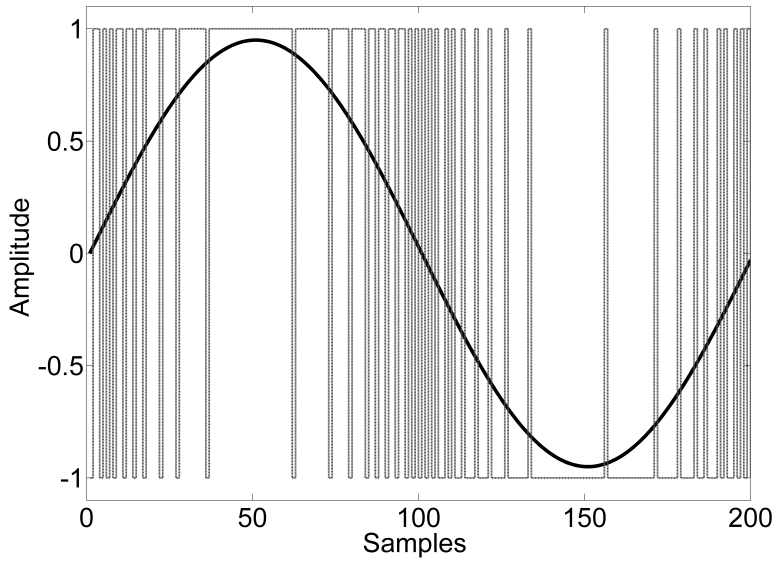


Figure B.6: Pulse Density Modulation

Manchester encoding are preformed to up convert a low frequency SDM output to a carrier frequency at a usable carrier frequency, While this method can reduce the output efficiency by amplifying unwanted copies of the transmit signal. In [163] The author presents a method of Manchester encoding using external logic that can suppress the copied transmit signal using the properties of the Sinc response of a sample and hold function. A Sinc response in the frequency domain is generated by the transmission of a digital signal in the time domain, by correctly arranging the sample frequency and the modulator output the nulls in the Sinc function can be placed at the unwanted copies of the transmit signal.

In [155] the modulator structure is modified to operate in parallel allowing the output to be a multiple of the logic operating frequency. The paper discusses the modulator structures that are best suited to parallel implementation as well as the effects of Sinc shaping on output signal power. In [164] a method of reducing the impact due to noise is outline the author uses a novel structure that uses two modulator each of the I and Q paths these are then unconverted using four sing waves 45^O out of phase. This technique reduces peak noise by as much as 6 dB at he expense of increased output bit stream frequency. While the modified structure are showing promising improvements in performance the operating frequency is still the major factor that impacts modulator performance.

Reference	Dooley '08 [62]	Podsiadlik '12	Thiel '11 [165]	Thiel '12 [164]	Dooley '11[26]	Helaoui '08[163]
Operating Frequency	106.25MHz	400MHz	277MHz	400MHz	98MHz	250MHz
Carrier Frequency	1.0625GHz	100MHz	2.5GHz	400MHz	930MHz	150MHz/1.96GHz
Bandwidth	5MHz	-	-	-	9MHz	5MHz
SNR	40dB	40dB	30dB	-	45dB	41dB
Resolution	1 bit	1 bit	1 bit	2 bit	1 bit	1 bit
Modulator	LP ME	LP QM	LP QM + ME	LP + Modified QM	10th order BP + ME	3rd order LP + ME
Signal	4 tone sinusoidal	625KHz 4 QAM	OFDM	OFDM	-	CDMA 250 KHz
Tech	Virtex II Pro	Virtex II Pro	-	-	Virtex II Pro	-

Table B.2: FPGA modulator comparison of state of the art

B.1.3 Modulator Comparison

Of the results presented in the previous chapter both the pulse width modulators and the pulse density modulators are capable of generating digitally modulated communications signals. There are pro's and con's for each implementation, of the two it is clear that the pulse width modulator is capable of the best SNR and dynamic range [151], however this comes at the cost of costly ASIC design and therefore lack of flexibility. The pulse density modulator can be designed in both analogue ASIC design or programmable digital logic. The programmable digital logic cannot compete with dedicated ASIC design for either pulse width or density modulators, however the flexibility and cost of implication is much more desirable. Advancements in digital logic and particularly programmable logic will inevitably increase operating frequency, as it stands the current implementations will limit the maximum achievable sample rate. Design of Custom ASIC analogue or digital circuitry is not within the scope of the work which follows therefore further analysis is carried out on FPGA based sigma delta modulators for communications signals. Additional operational parameters aside from operational speed can be investigated that can improve signal noise ration (SNR) or linearity.

The following section will evaluate the digital output of current FPGA designs and the capability of generating a digital pulse with sufficient clarity to describe the modulator on the digital circuitry. Additionally a proposed modulator structure for quadrature communications signals with the ability to efficiency cancel IQ imbalance generate through IF operation.

B.2 FPGA SerDes Capability as Switch mode PA Modulator

Implementation of a discrete time (DT) SDM in an ASIC or FPGA logic has an advantage of reduced component count compared with discrete implementations as the feedback DAC is inherent in digital implementation. The output of the modulator is then translated from digital to analogue domain through the use of a SerDes. In this paper we will concentrate on two level SDM's using a SerDes. It is available on many currently available FPGA's, the two level output combined with the SDM can generate a drive signal for a class D amplifier capable of transmitting a carrier signal at one quarter of the output switching frequency. This platform pushes the digital boundary of the transmitter closer to the antenna. The DT SDM when fully implemented in digital logic for example on an FPGA will not suffer from clock jitter

associated with output quantizer, DAC and loop filter. Therefore the output from the modulator from within the FPGA structure will be almost ideal, aside from quantization error associated with fixed point calculation. The output from the SerDes is an analogue representation of a digital signal and as such will only approximate the digital signal. The analogue output will have a finite rising and falling slope, as well as jitter about the transition points of the signal. These are two important points when generating a pulsed driven signal for a digital PA. In the Xilinx Virtex 6 FPGA family there are three classes of transceiver, each designed for specific frequency ranges of operation and cost. In this paper we will analyze two of these namely: GTX and GTH, which can operate at 6 Gb/s and 11 Gb/s respectively. The transceivers are designed for digital wired communication standards and as such their figure of performance is bit error rate (BER), they must comply with the specified bit error rate of each standard. For SMPA operation a delay between transition of on/off state can introduce dead time in the amplifier output, this is undesirable as it can lead to a distorted output, and also reduce the efficiency of the amplifier. It is important that the FPGA output has a sufficiently fast rise and fall period to avoid this occurring. In the discrete time to continuous time transformation that is carried out in the FPGA SerDes, the rise time of the signal will affect the sinc shaping that is applied to the spectrum of the output as can be seen in Figure B.7. The result as stated in [166] is the reduction of power in higher frequency signal component's as they approach the sample frequency.

$$\eta_p(CT) = \eta_p(DT) * [(sinc(F_c T_s) * sinc(F_c T_e)]^2 \tag{B.5}$$

Where η_p is the relative signal power, F_c is the frequency at which the power transformation is being performed, T_s is the period of the square waves and Te is the rise time of the square wave. Using our test case for a band pass SDM operating at 3 Gbps and a carrier frequency of approximately 750 MHz, a GTX with a typical rise time of 120 ps will attenuate the carrier by approximately 1.02 dB and a GTH with a typical rise time of 50 ps will attenuate the carrier by 0.91 dB. These losses are minor in comparison to matching and coupling losses, however from Figure B.7 it is apparent that these losses will have a greater impact as frequency increases.

The increased jitter in the output will increase the noise in the output of the signal across the band. However due to the existing high noise level present from the output of a sigma delta

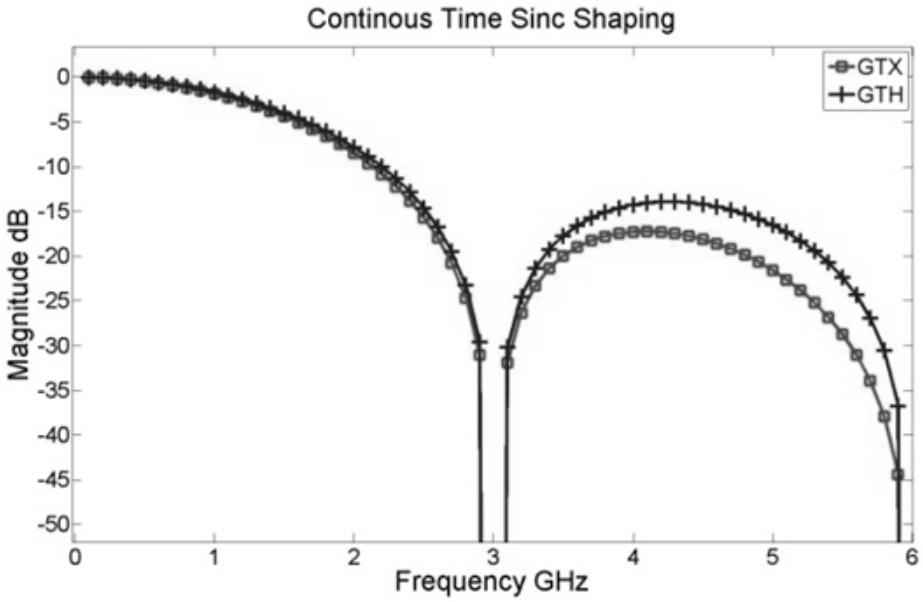


Figure B.7: Effects of Sinc Shaping

modulator the only area this additional noise will effect is the depth of the notch of the in band signal. The following equation derives a figure for the pulse width jitter of the output from a pulsed signal modulator.

$$SNR = 10 * log_{10} \frac{(T_s)^2}{(2 * \delta_{jrms})^2} \tag{B.6}$$

Where T_s is the clock cycle of the output signal and δ_{jrms} is the RMS jitter applied to the signal. A SDM has a varying output pulse width period however the formula only uses a fixed pulse width period. It will provide an approximate figure for the jitter noise. The jitter in any SerDes device can be classified as random jitter introduced by the clock and its supporting circuitry and deterministic jitter introduced by the transceiver circuitry its self. Therefore the quality of the input clock and PLL directly effects the jitter performance of the device. For the measurements a ML605 development board with GTX and ML628 development board with a GTH were used, with a figure of total jitter of 50 ps and 22 ps respectively [167]. Using equation B.6 we can simulate a theoretical noise floor for the transceivers. From Figure B.8 it can be seen that for a carrier frequency of 750 Mhz the theoretical SNR is 47 dB and 38.5 dB for the GTH and GTX transceivers respectively. It is apparent from the graph that the impact of jitter on the output signal quality is quite large, however the GTH transceiver has the ability to meet the required spectral mask noise floor for both LTE and UMTS signals at frequencies

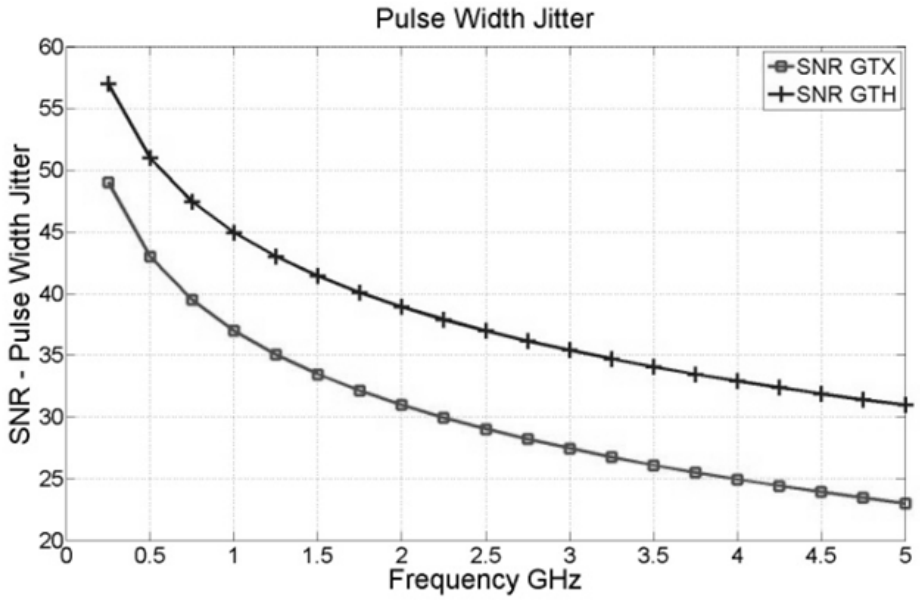


Figure B.8: SNR - Pulse Width Jitter

below 1 GHz. The main difference between the transceiver structures which impacts on jitter performance is the tunable phase lock loop (PLL). The lower frequency GTX transceiver can tolerate more jitter due to its lower operating frequency and still achieve the required bit error rate (BER) for the standards targeted by the GTX. Therefore two separate PLL architectures are implemented, the GTX uses a ring oscillator structures. This is a frequency flexible design that consists of cascaded inverters that operate at a resonant frequency dependent on the input reference signal. This structure is compact, requiring only capacitive and logic components which can be easily achieved in CMOS circuitry.

The GTH on the other hand uses an LC tank PLL [168], that offers reduced output jitter at the cost of frequency flexibility. The LC tank PLL structure can offer up to an order of magnitude reduction in RMS jitter compared with a ring oscillator design. However the inclusion of a inductor in the design increases the die area of the PLL making it expensive.

B.2.1 Measurements

Measurements were carried out using Xilinx ML628 in Figure B.10 and ML605 in Figure B.9 development boards. The SDM bit stream was generated in Matlab using quadrature modulator structure [7] and a memory stream provided the multi gigabit transceivers with the digital signal. The input to the modulator is a single carrier WCDMA signal at baseband. The

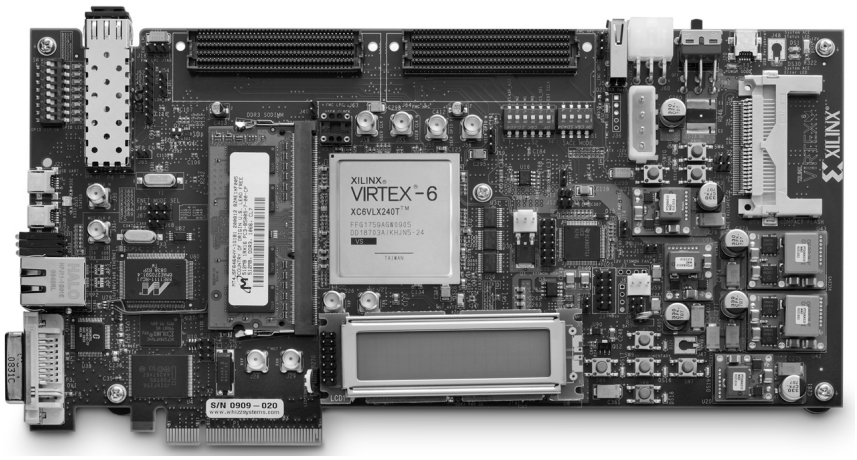


Figure B.9: Xilinx ML605 General FPGA development platform.

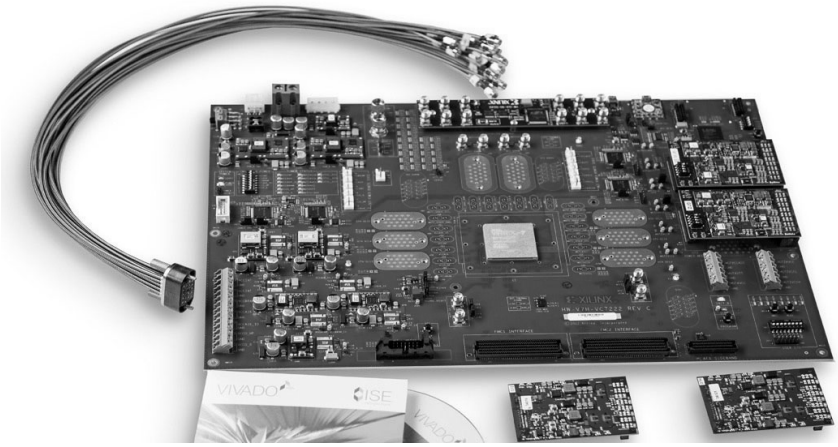


Figure B.10: Xilinx ML628 High speed communications characterisation platform.

amplitude of the output waveform was kept constant across transceiver outputs at 200 mV. For the purposes of the measurements a single ended output from the transceivers was measured, its complementary port from the transceiver was terminated with a 50 ohm load. The output from the ML605 was a 30 cm SMA cable, the ML628 uses a bull's-eye test port with 30 cm cables. A differential 150 MHz reference clock was supplied to the transceivers directly and the internal PLL multiplied this to the required operating frequency to obtain a 3 Gb/s bit stream.

Figure B.11 shows the spectral performance of the GTX output, using an adjacent channel power ratio (ACPR) measurement on the frequency analyser a value of -37 dBc was calculated for the noise floor from the transceiver at the 750 MHz carrier frequency. Figure B.12 shows an eye diagram for the GTX output at 3 Gb/s, amplitude of the eye is approximately 220 mV. The eye is clearly visible and the RMS jitter was calculated at 10 ps. Using equation B.5 a theoretical value for the noise floor was calculated as 39 dBc. Simulation and measurement

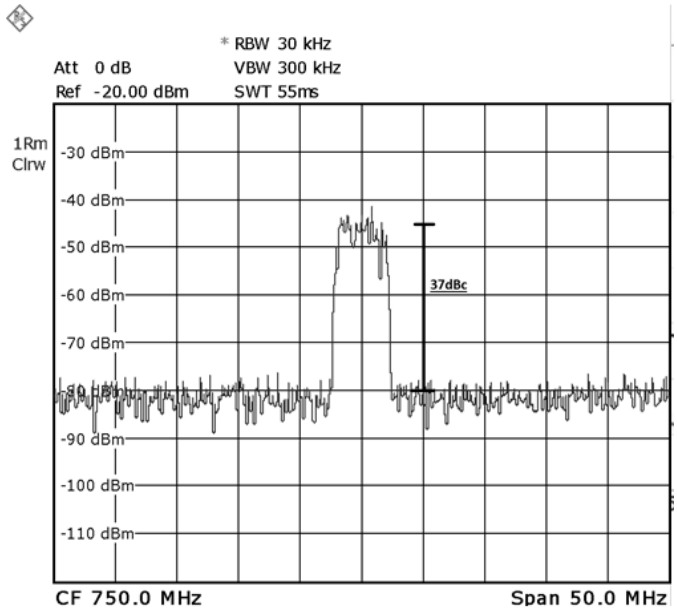


Figure B.11: WCDMA 5 MHz Signal at 750 MHz GTX Transceiver

are in good agreement. Figure B.13 shows the spectral performance of a GTH transceiver transmitting the same bit stream. The reduced jitter from the transceiver lowers the noise floor. The ACPR measurement was increased to 50 dBc, which is enough to meet ACPR requirements for a 5MHz WCDMA single carrier or 5 MHz LTE signal. The RMS jitter measurement in Figure B.14 gives 4 ps of jitter. The ACPR and the noise floor of 47 dBc calculated with equation B.5 also closely agree. The reduced rise and fall time from the GTH transceiver will also provide a better switching signal to the PA.

B.2.2 Analysis

This analysis presents the effect of jitter from commercial FPGA boards on PDM signals and demonstrates that it is possible to meet the spectral mask requirements of modulation schemes such as UMTS and LTE. The signal exits the FPGA at RF frequency, moving the digital boundary right up to the amplifier input. Hardware limitations prevented measurements above 750 MHz carrier, from the theory we should expect a 3 dB rise in jitter noise from 750 MHz to 1 GHz, future work will test this. The results show that FPGA's can provide a frequency flexible modulator for RF PA's which can meet spectral mask performance requirements up to 1 GHz.

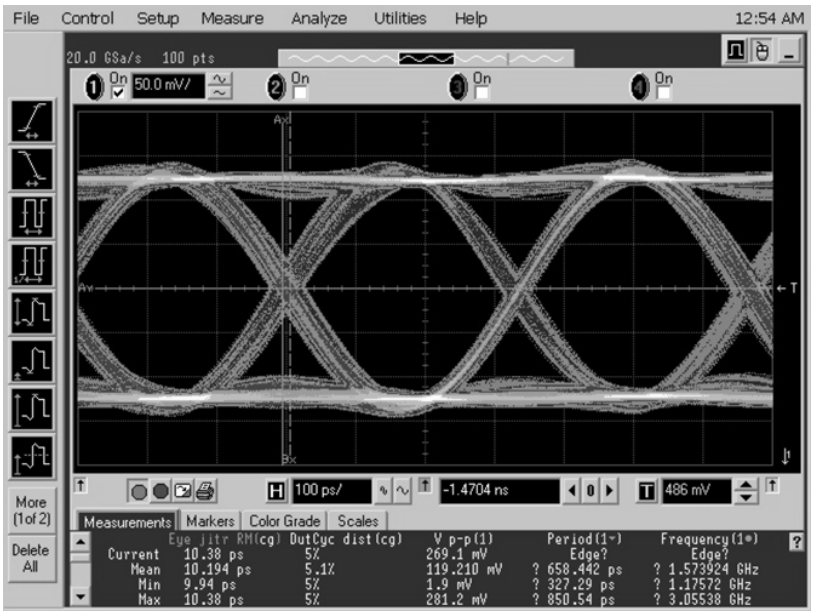


Figure B.12: GTX RMS Jitter PDM Signal

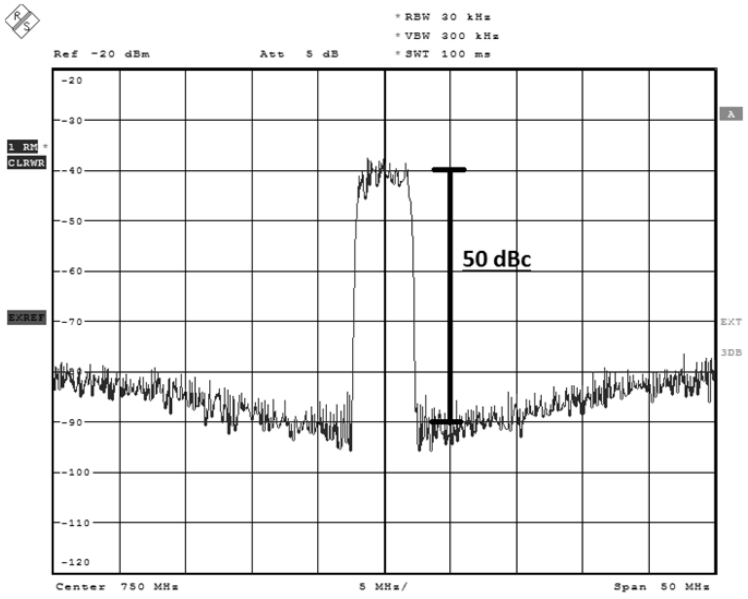


Figure B.13: WCDMA 5 MHz Signal at 750MHz GTH Transceiver

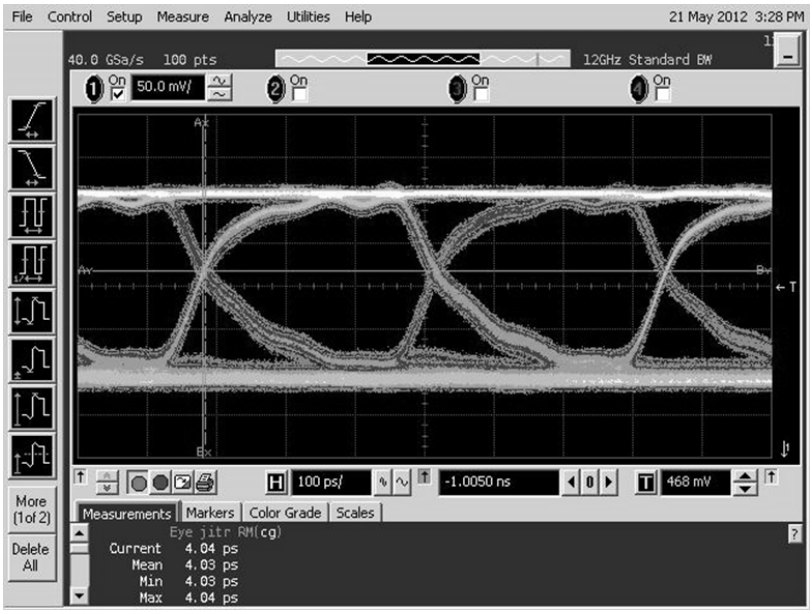


Figure B.14: GTH RMS Jitter PDM Signal

B.3 Quadrature modulator pulse density modulator

When a signal is digitally mixed from Low-IF up to a carrier frequency an image of the signal is created. The position of the signal will depend on the position of the carrier signal and the Low-IF of the signal before up conversion. The image of the signal is undesirable as it has to be filtered before the signal can be transmitted. Quadrature mixing is a method which cancels the unwanted image caused by up converting a signal from Low-IF.

Quadrature mixing combines the two components of a complex signal, I and Q, which are at Low IF and modulate an RF carrier. By doing this a wanted signal and image signal will be created about the RF carrier. The Q component of the signal has both the desired signal and the image in phase in the real frequency domain. The I component has the desired signal and image out of phase by 180^O in the imaginary axis frequency domain as demonstrated in Figure B.17. During the up conversion a 90^O phase shift is applied to the I component relative to the Q component, this is achieved by multiplying I component by a sin wave and the Q component by a cosine wave. This brings I and Q components of the desired signals into phase and they add to amplify the signal. The imaginary components are now 180^O out of phase which means that they cancel. The cancellation can be seen in Figure B.16. The quadrature mixing is implemented after the sigma delta stage which is carried out on each of the channels (I and Q). It is important to keep the phase and amplitude of the signal constant as slight changes will affect the image cancellation.

The switch mode PA requires a binary bit stream at an RF carrier frequency. It is possible to generate high frequency bit streams using commercially available FPGA development boards however when the complex modulation signal is digitally up converted an unwanted image is generated close to the wanted RF signal. In order to remove the unwanted image we cancel the imaginary part by phase compensated digital mixing. An overview of the system can be seen in Figure B.15. This shows the coarse method for implementing quadrature mixing after the SDM. The signal is up converted using Manchester encoding or signal chopping, this transports the desired signal from baseband to half the operating frequency of the SDM (FDSM). The combination of I and Q components and phase shift is performed by the time interleaving process. This method preserves the bits stream in the 1, -1 from that is required to drive the switch mode PA, however due to the time interleaving the signal is now at twice the sample

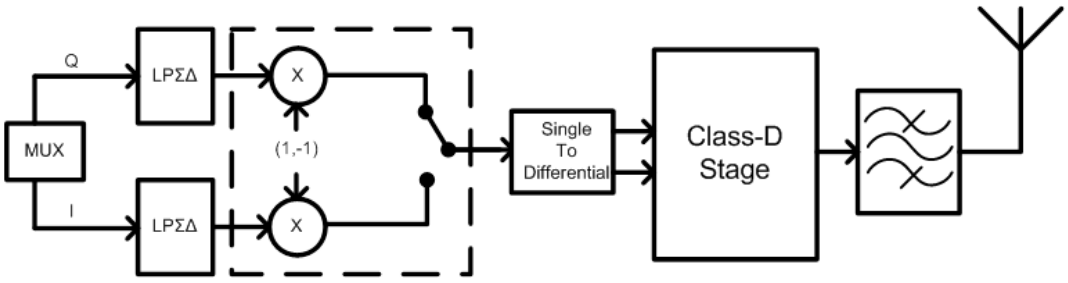


Figure B.15: System overview

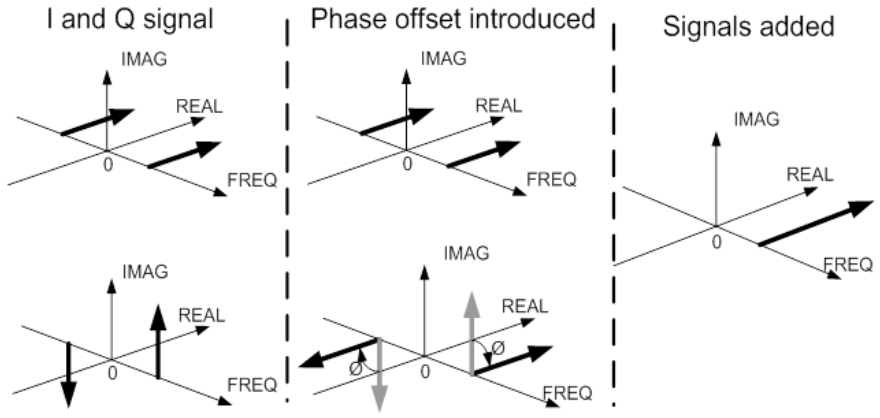


Figure B.16: Ideal quadrature mixing

frequency of the original input signal, this up converts the signal from baseband to one quarter the systems sample frequency (Fs = 2*FDSM).

The phase that is introduced to a signal converted from baseband to Fs/4 is 90^O due to the fact that the time interleaving introduces a unit sample delay in a signal. However the phase introduced by interleaving changes as the signal moves away from base band. The phase depends on the frequency difference between a signal up converted from a Low-IF with the sample frequency of system after time interleaving. If the phase introduced by time interleaving is different than 90^O the quadrature mixing will be affected resulting in an image at twice the Low-IF from the wanted signal. Equation B.7 calculates the phase offset incurred from quadrature mixing a Low-IF signal.

$$\phi = \frac{2\pi}{\frac{Fs}{BW}} \tag{B.7}$$

An example of the resulting image from the phase imbalance can be seen in Figure B.18. The image can have enough power to appear above the NTF and reduce the overall bandwidth

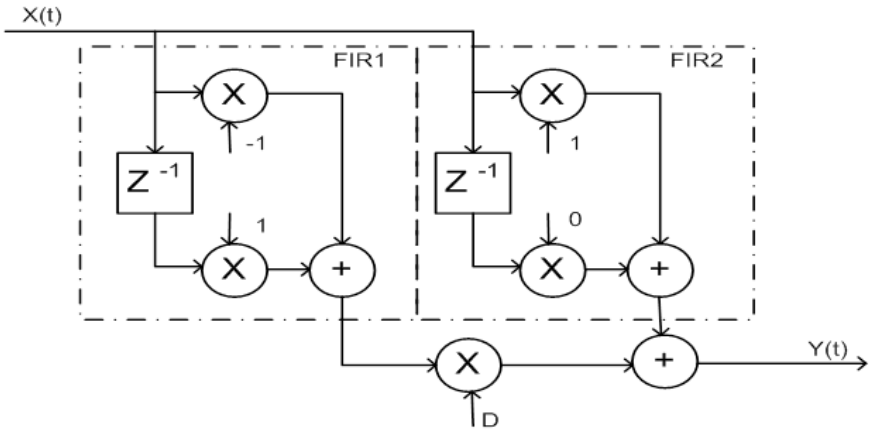


Figure B.17: Lagrange Filter using Farrow structure.

within the notch of the NTF. To improve the image cancellation to a point where the image no longer appears above the NTF of the sigma delta a phase offset $90^O - \phi$ must be introduced to one of the signal paths before the SDM.

If the phase offset between two signal paths is smaller than 90^O and cannot be corrected using an integer sample delay a fractional delay must be used. As explained in the design methodology for fractional delay filters outlined in [169], the Lagrange filter can be designed to act as an all pass fractional delay filter. Figure B.17 outlines a Farrow structure which can be used to implement the relative fractional delay required in this application [170]. This structure uses FIR filters in parallel, the outputs are weighted, D corresponds to the delay that the filter will implement. The coefficients of the filter are (-1, 1) for FIR 1 and (1,0) for FIR 2.

$$Y(t) = X(t) + D * X(t-1) - X(t) \tag{B.8}$$

Equation B.8 describes the function of the filter, the delay is a factor of the difference between the current and previous value of X(t). This provides a varying change in phase with the rate of change of the signal. This characteristic means that the filter will work for a range of frequencies without needing to be reconfigured. Figure B.18 shows the effect a fractional delay has on the phase of the signal before entering the SDM, the additional phase added to the system now allows the image cancellation to be preformed fully. The removal of the image allows for full utilization of the bandwidth within the notch of the sigma delta.

The implementation of the fractional delay filter in a digital system will introduce a two

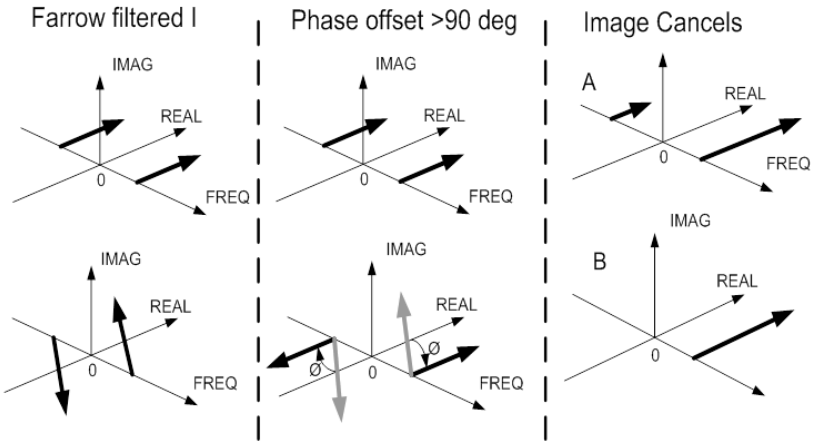


Figure B.18: The effects of a fractional delay (A) result before fractional delay filter is added (B) result after fractional delay filter is added.

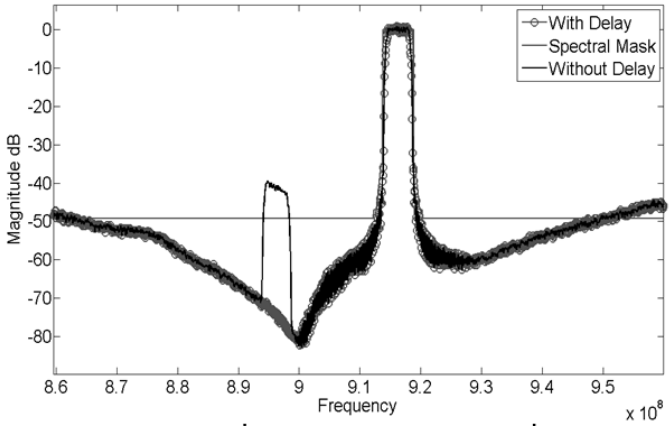


Figure B.19: Quadrature mixing, effect of fractional delay.

sample delay as well as the fractional delay. To align the signal to allow quadrature mixing to be performed it is necessary to also place a two sample delay in the non filtered signal path.

Figure B.19 shows the effect the fractional delay has on the output of the system. The image is at -40 dBc, this is above the spectral mask floor for 3GPP and as such would be required to be removed, however after a relative fractional delay is added between the I and Q signal paths the image is below the NTF of the SDM.

B.3.1 Measurements

The compensation of quadrature phase mismatch has been evaluated in simulation in the previous section. The final validation is carried out using a FPGA implementation of the quadrature sigma delta modulator structure and delay compensation. The chosen SDM

topology is a first order, low pass, parallel sigma delta modulator. The low pass structure is required for the quadrature implementation, the parallel implementation of the first order modulator enabled efficient implementation of a SDM structure, with an output multiple times that of the maximum achievable clock frequency of the digital logic. This is a method which has been extensively analysed in previous publications [155]. The low pass pulse density modulator achieved an 800 MHz operating frequency with four parallel modulators and multiplexed outputs. The topology of the SDM limited the number of parallel computations that could be preformed simultaneously, as the critical path is a function of the output feedback and therefore a function of all parallel elements. The physical and electrical characteristics of the FPGA define a fundamental limit. In the quadrature configuration the operating frequency of the SDM was 1.6 GHz with a notch in the noise floor at 400 MHz.

The fractional delay filter was required to operate at the same operating frequency of the low pass SDM and therefore required a parallel implementation as well. The topology of the fractional delay filter is distinctly different when compared with the SDM, not requiring a feedback for calculation the parallel implementation is far simpler and does not have a practical limit on the number of parallel computations.

Using a Virtex 6 ML605 development board in Figure B.9, the digital modulated signal could be generated and output through a Multi Gigabit Transceiver (MGT). The available MGT is a GTX Xilinx design which has been extensively analysed in Section B.2 as a limiting factor for high dynamic range SDM implementations. In this case the first order implementation for low RF frequencies does not have enough of a notch in the noise floor to be limited by the hardware implementation. The notch is sufficient to illustrate the proposed mismatch cancellation method. Figures B.20 and B.21 demonstrated the measured performance of the implementation. The IQ mismatch has been compensated for by the fractional delay filter and the image reduced by at least 5 dB, in line with the SDM noise floor.

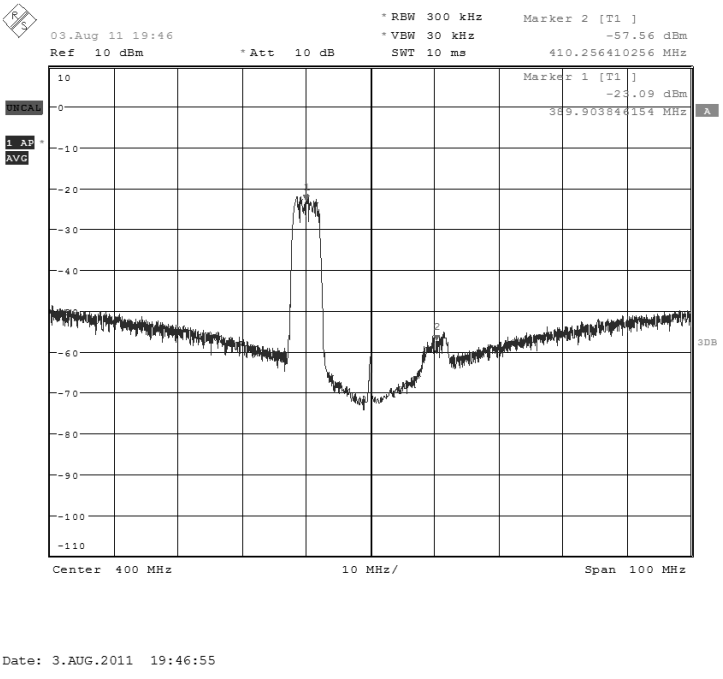


Figure B.20: Spectral analysis of the implementation system with out the compensation filter. The 5 MHz WCDMA signal is placed at an 10 MHz low side intermediate frequency before modulation. The corresponding image is clearly viable above the noise floor of the SDM.

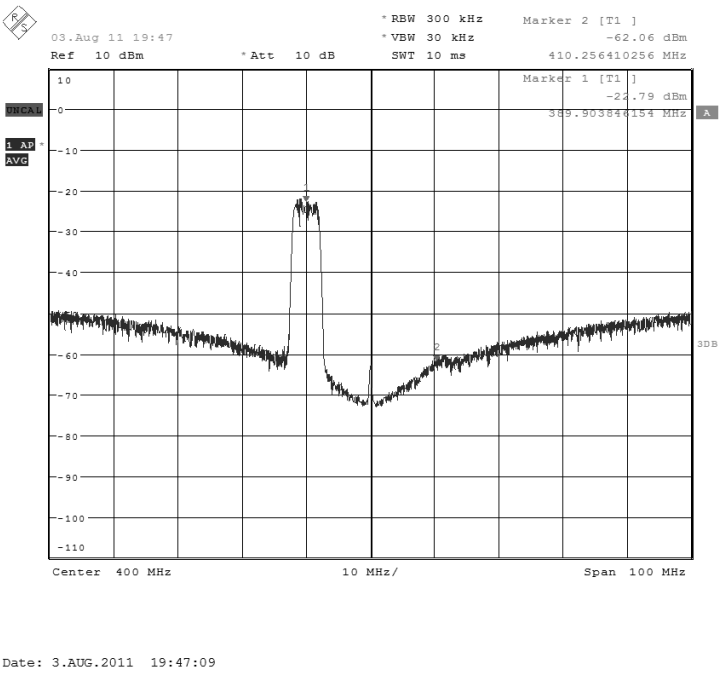


Figure B.21: Spectral analysis of the implementation system with the compensation filter. The 5 MHz WCDMA signal is placed at an 10 MHz low side IF frequency before modulation. The corresponding image has been reduced in line with the SDM noise floor.

B.4 Analysis of Class-S power amplifier

In the work outlined above the current state of the art for digital modulators is outlined. The pulse density modulator and pulse width modulator have been demonstrated as plausible options for digital Class-S power amplifier. However for each of the proposed designs, some compromise must be made, the performance of a pulse width implementation is offset by cost and limited flexibility. The pulse density modulator has potential for reduced cost and highly flexible in an FPGA proposed solution however performance is scarified in many implementations.

While advancements outlined in this work and other research areas have demonstrated potential advancements and targets for improvement some out standing issues prevent commercial implementations of the Class-S amplifier. Some of the issues will be improved as the technology becomes available, there still exists areas which require further research. These include flexibility for pulse width implementations and the increased operational bandwidth and coding efficiency for pulse density implementations to name a few. As such these road blocks prevent a commercial, efficient and economical implementation of the Class-S amplifier from being achieved.

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