

Wideband MEMS Switched Delay Lines with High Phase Linearity

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¹ **Abstract**—This paper presents a study on different microwave structures used to integrate MEMS devices in printed circuit boards, and their effect on the linear phase response for switched delay lines applications. Three different prototypes were designed to realize the RF tracks required to integrate 0.5 mm pitch MEMS devices together with the meander delay lines. The structures includes: microstrip lines, conventional coplanar waveguides (CPW) and finite grounded coplanar waveguides (FGCPW). The three prototypes were designed to deliver a group delay of 600 ps. Simulations were carried out using CST Microwave Studio. The FGCPW proved to have the highest phase linearity with only ± 4 ps ($\pm 0.67\%$) delay deviations up to 2.7 GHz. The paper also presents the design of two wideband MEMS switched time delay line circuits; one used to provide a fine tuning for the group delay with a step of only 10 ps and another for coarse tuning with 50 ps delay step. Finite grounded coplanar waveguides were selected to obtain a high linearity of phase response. The simulation of the two circuits resulted in a constant delay with relatively small deviations, as well as low insertion and return losses of 0.75 dB and 20 dB, respectively for frequencies up to 5 GHz.

Index Terms—group delay, MEMS Switches, linear phase, wideband, coplanar waveguide.

I. INTRODUCTION

OVER the next decade, a new generation of wireless communication systems (e.g. 5G systems) is expected to be deployed, inevitably pushing signal bandwidths into a multiple of 100 MHz, increasing carrier frequencies and requiring much precise control of signal phase matching as well as time delays. High performance time delay circuits with high phase linearity are essential for many other applications to keep the distortion of wideband signals to minimum. Examples include: adaptive antennas and tracking radar systems (where phase characteristics are controlled for successful beam forming [1]), power amplifiers feed forward linearisation and leakage cancellation in RF transceivers [2].

Passive delay circuits are commonly designed using meander microstrip transmission lines. Variable time delays can be obtained by switching the input signal across variable routes of different path lengths [3]. For many wideband applications, RF micro electromechanical systems (MEMS) switches have been employed as an alternative technology for PIN diodes and FET transistor switches, since they offer a substantially higher performance [4]. RF MEMS are characterized by very low insertion loss over a wide frequency band (<1 dB),

low power consumption as well as fast switching response. Important issues such as packaging, long term reliability and low production cost of the MEMS devices are currently being addressed. Many modern MEMS devices come in packages with only 0.5 mm pitch between the RF signal ports (e.g. ADG1904 MEMS) which adds some challenges to the process of integrating these devices into printed circuit boards [5]. Golden-wires and thermosonic ball soldering were suggested earlier to integrate MEMS [6]. Others use micro gold traces in semi-insulating GaAs resulting in high performance at the expense of adding complexity to the fabrication process [7]. Others use RF transmission lines on Silicon substrates resulting in high insertion losses [3].

The objective of this paper is to design a MEMS switched delay lines circuit that operates over a wide band of frequency (700 MHz up to 2.7 GHz, such that it covers new LTE frequency bands). The design of the MEMS RF interface together with the transmission delay lines should be characterized by very high phase linearity ($<\pm 1\%$ time delay variations over a 10% fractional bandwidth centered at the highest frequency of operation which is 2.7 GHz), as well as low insertion and return losses (< 1 dB and < 20 dB, respectively). Other important parameters such as small size and low fabrication cost need to be delivered.

Section II presents the design of both the RF interface used to integrate the MEMS devices as well as the meander delay lines using different microwave structures. The switching device used in this paper is ADG1904, it is a wideband single pole four throw switch. It was designed and fabricated using Analog Devices, Inc. micro electromechanical system switch technology. In order to allow for fair performance comparison between the structures, 600 ps delay lines were designed and simulated using conventional coplanar waveguides (CPW), finite grounded coplanar waveguides (FGCPW) and microstrip lines (MSL). Finally, Section III focuses on two MEMS switched delay lines circuits which were constructed using FGCPW, it also presents the simulations results of the two circuits.

II. DESIGN PROCEDURES OF MEMS RF INTERFACE AND MEANDER DELAY LINES

Fig. 1 shows the land pattern of the MEMS switch whose RF pins are only 0.5 mm away. The switch consists of five RF signal inputs/outputs matched to 50Ω impedance system, where each RF pin is surrounded by two RF ground pins. Thus, the design of the RF interface requires very narrow CPW

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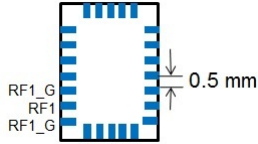


Figure 1. The land pattern for SP4T MEMS Switch (ADG1904).

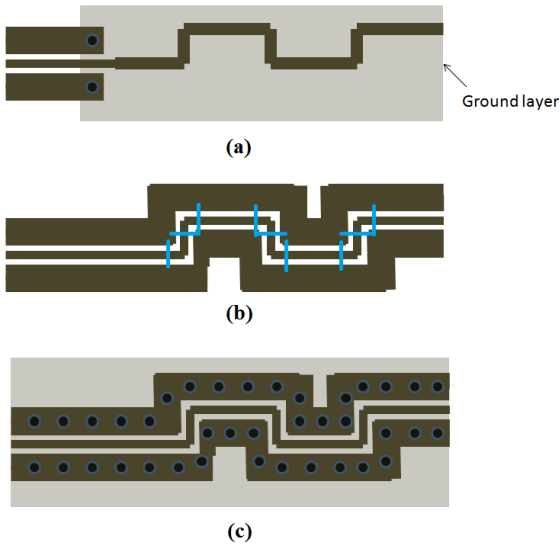


Figure 2. The structure for the RF tracks together with the meander delay lines (a) CPW to MSL transition (b) CPW with airbridges (c) FGCPW with vias.

lines whose signal line width is only 0.3 mm, and a signal to ground gap of only 0.2 mm. There are several different CPW structures creating different ways of realizing the RF interface/tracks for the MEMS switches as well as the meander delay lines. In this paper, three different prototypes were designed, simulated using CST Microwave Studio and compared.

In the first prototype, microstrip lines (MSL) were used to serve the function of delay lines. In fact, MSL are usually used to design meander delay lines, since they are more robust to the excitation of undesired parasitic modes resulted from line bending. In addition to the the small size they offer when compared to other microwave structures. As mentioned earlier, the RF interface of the MEMS devices used in this paper requires two RF ground connections surrounding the RF signal. Accordingly, conventional CPW were selected to design the RF interface of MEMS devices, and the line dimensions were matched to a 50Ω impedance using a very high permittivity substrate (Rogers 6010, $\epsilon_r=10.2$, $t=1.9$ mm). In this case, a transition is required to connect MSL meander lines to the CPW RF tracks. As introduced earlier by Chen et. al. [8], MSL to CPW transitions can be designed by extending the lower ground of the MSL line underneath the CPW line, then inserting two vias to connect the upper ground of the CPW lines with the lower ground of the MSL line. Fig. 2a shows the structure of the first prototype. CPW to MSL

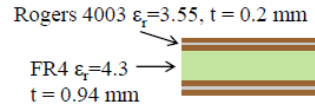


Figure 3. The three layer substrate used for the FGCPW line.

transition proved to deliver a good wideband performance with low insertion and return losses. However, the effect of MSL to CPW transition on phase linearity was never mentioned. For the consideration of this paper, poor phase linearity can hugely degrade the signal cancellation performance causing large deviations in the group delay.

The second prototype used conventional CPW lines to design the RF interface of the MEMS device together with the meander delay lines as shown in Fig. 2b. Wire airbridges were introduced across the bends of the CPW line in order to suppress any undesired propagating modes which can have a significant effect on the characteristics of the line (e.g. increasing the insertion loss). These higher modes are usually excited in CPW line bends because the fields propagating in both the inner and outer slot of the line encounter different path lengths creating a potential difference between the two upper ground planes [9]. Wire airbridges should be designed such that the parasitic capacitance added to the structure is minimum. Copper wires were selected for airbridges with only 0.1 mm radius placed 2 mm above the signal line.

In the third prototype, FGCPW lines were chosen to design both the RF tracks and the meander lines. Like most CPW structures, GCPW lines also suffer from undesired higher modes, which are not only excited due to line bending but mainly because of having two ground layers on both sides of the substrate. In fact, the GCPW mode in these structures is always accompanied by either parallel plates mode or microstrip line mode, which are again due to unequal potential between the upper and lower ground planes [10]. This problem can be solved by inserting vias along the whole line on both left and right upper ground planes. The separation between the vias should not exceed one tenth of the propagating wavelength at the highest operating frequency. Also, thin layer substrates are recommended in order to reduce the parasitic inductance of the vias. In addition, using multilayer substrates can further suppress the parallel plate modes. Fig. 2c shows the structure of the 50Ω GCPW lines designed using a three layer substrate. The upper and lower layers are identical for PCB manufacturing symmetry, each is formed of Rogers 4003 whose dielectric constant (ϵ_r) is 3.66 with thickness of 0.2 mm, while for the inner layer, FR4 substrate was selected with 0.94 mm thick in order to make the board rigid enough for mounting the devices. All the inner copper layers are grounded. The GCPW vias are separated by 1 mm, and the radius of each via is 0.2 mm.

A 600 ps group delay was designed and simulated using the three proposed prototypes shown in Fig. 2 using CST Microwave Studio. Fig. 4 shows the simulated group delay of the three different prototypes. The FGCPW lines showed

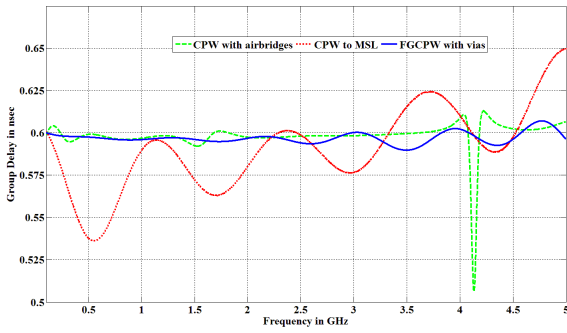


Figure 4. A comparison between the simulated group delays for the three different prototypes.

Table I
A COMPARISON BETWEEN THE SIMULATION RESULTS OF THE THREE PROPOSED PROTOTYPES

Device interface	CPW	CPW	FGCPW
Meander lines	MSL	CPW+ airbridges	FGCPW+ vias
Substrate	Single subs.	Single subs.	Multilayer subs.
Insertion loss	<0.8 dB	<1 dB	<0.28 dB
Return loss	Better than 20 dB		
$\tau_{deviation}$	± 63 ps (10%)	± 7 ps (1.16%)	± 4 ps (0.67%)

a minimum delay deviations ($\tau_{deviation}$) with only ± 4 ps ($\pm 1\%$) up to 2.7 GHz. While for the conventional CPW lines (the first prototype), a large deviations in the group delay appeared with ± 63 ps ($\pm 10.5\%$) over the same bandwidth. Table.I shows a comparison between the three prototypes including a summary for the simulation results up to 2.7 GHz.

III. SWITCHED DELAY LINES CIRCUITS SIMULATION AND EXPERIMENTAL VALIDATION

Based on the comparison conducted above between the three different prototypes, FGCPW was selected to design two switched group delay circuits; one is used to provide a fine tuning for the group delay with a step of 10 ps (Δ), and another for coarse tuning with a delay step of 50 ps (δ). The first circuit was designed based on our previous work [11],

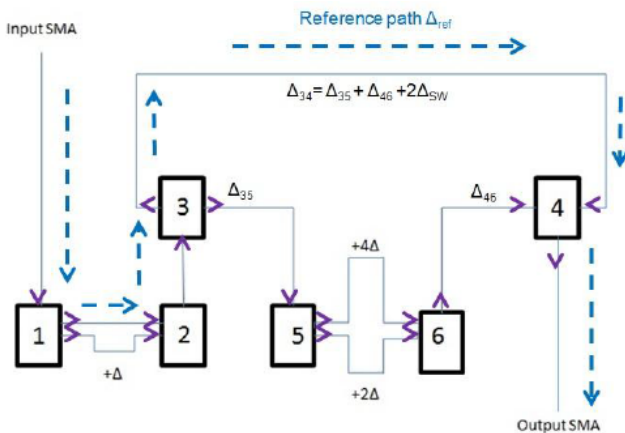


Figure 5. The block diagram for MEMS switched delay lines with fine tuning ($\Delta=10$ ps) [11].

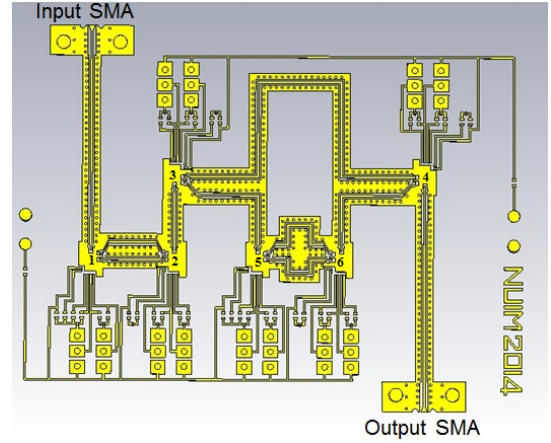


Figure 6. The layout of MEMS switched delay lines with fine tuning ($\Delta=10$ ps). The circuit size is 90 x 65 mm².

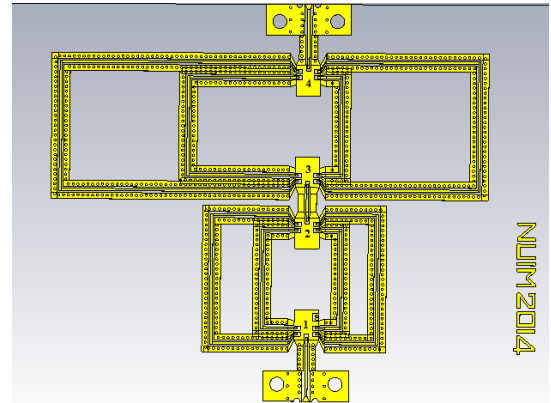


Figure 7. The layout of MEMS switched delay lines with coarse tuning ($\delta=50$ ps). The circuit size is 90 x 85 mm².

with the block diagram shown in Fig. 5, where six MEMS switches were used and a total maximum delay of 50 ps was delivered. The second circuit was designed to provide a maximum delay of 600 ps using four MEMS switches. Fig. 6 and Fig. 7 show the layout for the fine tuning and coarse tuning switched delay circuits, respectively. Simulations were carried out for both circuits up to 5 GHz which is higher than the frequency of interest (2.7 GHz), in order to investigate their performance at higher frequency bands, since these types of circuits can be employed in many other applications. The pads underneath each of the MEMS devices were included in the simulation so as to address any interfacing issues. The simulation approach used in this paper was validated on the basis of some preliminary experimental results which were presented earlier in [11]. Fig. 8 shows the simulated group delays for the first circuit with a fine tuning delay step, while Fig. 9 shows the simulated insertion loss. Both indicates a maximum delay deviations of only ± 1 ps ($\pm 0.1\%$) and less than 0.28 dB insertion loss over the whole frequency band.

Similarly, Fig. 10 and Fig. 11 show the simulated group delay and insertion loss for the second circuit with a coarse tuning delay step, respectively. Both figures show time delay deviations below ± 3 ps ($\pm 0.5\%$) and less than 0.45 dB

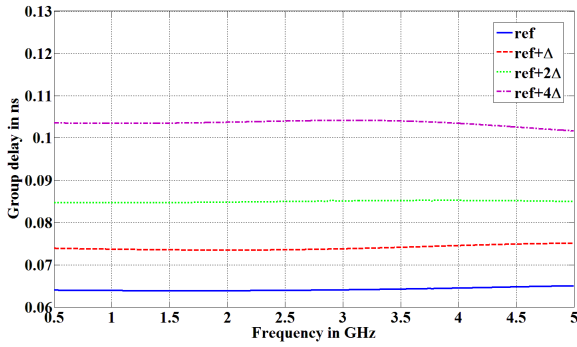


Figure 8. Simulated group delay for MEMS switched delay circuit with $\Delta=10$ ps delay step.

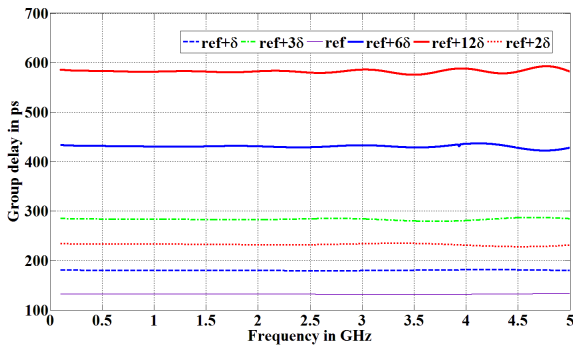


Figure 9. Simulated group delay for MEMS switched delay circuit with $\delta=50$ ps delay step.

insertion loss over the same frequency band.

IV. CONCLUSION

In this paper, a study was presented on different microwave structures that can be used in the design of wideband MEMS switched delay line applications. Three different prototypes for both the MEMS RF interface and meander delay lines were designed using MSL, CPW and FGCPW lines. The three prototypes were used to design a 600 ps delay line. FGCPW proved to have the highest phase linearity with only ± 4 ps delay deviations up to 2.7 GHz compared to

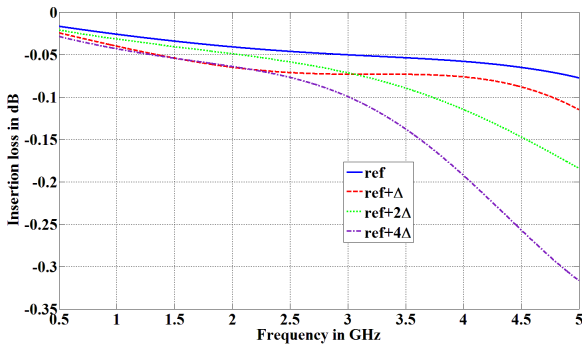


Figure 10. Simulated insertion loss for the meander delay line of MEMS switched delay circuit with $\Delta=10$ ps delay step.

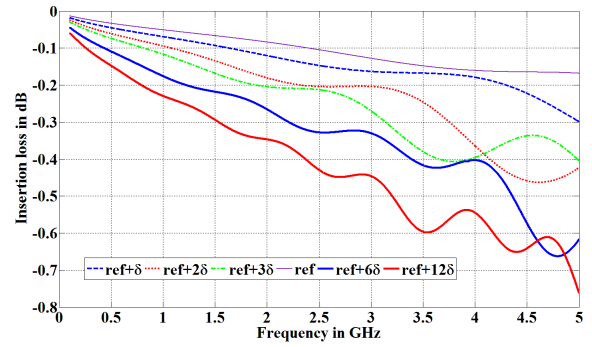


Figure 11. Simulated insertion loss for the meander lines of MEMS switched delay circuit with $\delta=50$ ps delay step.

conventional CPW and MSL lines. In addition, two wideband MEMS switched time delay lines circuits were designed to switch the group delay up to 650 ps; one circuit was used to provide a fine tuning with a delay step of only 10 ps (Δ), and another for coarse tuning with a delay step of 50 ps (δ). Simulations showed low insertion and return losses (< 0.75 dB and < 20 dB, respectively) up to 5 GHz, as well as very high phase linearity with less than ± 3 ps ($\pm 0.5\%$) delay deviations over the whole frequency band.

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