Fast Frequency Calibration of VCO's in Phase-Locked Loops

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Abstract — **This paper presents a novel technique to achieve fast calibration of the voltage-controlled oscillator (VCO) into the optimum subband of operation. The proposed technique is pre-dominantly digital thus exhibiting low power/area requirements, in addition to greatly reduced calibration times, suitable for application in lower technology nodes. To verify the proposed technique the VCO and corresponding calibration circuitry is modelled as part of a charge-pump phase locked loop (CP-PLL) in UMC's 90nm process. VCO operation is split into 16 different subbands (i.e. 4-bit calibration) with each subband exhibiting a gain (K_{VCO}) of $\approx$ 50MHz/V to achieve an overall tuning range of $\approx$ 10%. Through application of the proposed technique, calibration into the optimum subband of VCO operation is shown to occur in minimal time.**

Keywords — **Voltage-controlled oscillator (VCO), calibration, subband, phase-locked loop (PLL)**

I Introduction

Phase-locked loops (PLLs) are important building blocks in modern communication systems. At the heart of a PLL is the voltage-controlled oscillator (VCO), which oscillates at the desired frequency, controlled by a control voltage. In order to account for process, voltage and temperature (PVT) variation in the VCO operation, and to support multistandard operation, the VCO is required to have a sufficiently large frequency range. This large frequency range coupled with the reduced supply voltages that accompany modern nanoscale technologies, implies the use of a VCO with a high gain (K_{VCO} — frequency change per volt). Large K_{VCO} values degrade noise performance as any noise on the VCO control line (V_{ctrl}) will lead to greater frequency excursions on the output and larger magnitude spurious frequencies (spurs) on the output signal. Such spurs are highly undesirable as they create interference which can be particularily problematic for PLLs operating as frequency synthesizers [1].

This issue can be addressed by dividing the tuning range into discrete smaller bands (subbands) such that a wide frequency range can be realised with a small K_{VCO} within each band [2]. As shown in Fig. 1, the original tuning curve is subdivided into 2^n discrete subands, each exhibiting a small K_{VCO}, with each subband selectable via an n-bit digital word. The n-bit word switches in a particular capacitor for the LC tank (in this case, though it could also select a "slugger" capacitor for a ring oscillator-type VCO) to put the VCO into a desired frequency band.

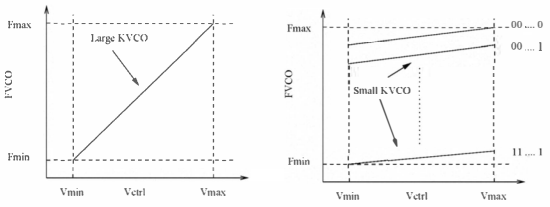

Fig. 1: Subbanding of single VCO tuning curve

In order to select the optimum subband for the desired frequency, calibration circuitry is required. This represents a power, area and most impor-

tantly time overhead to the system as it adds to the PLL locking time. For systems requiring frequent switching, such as frequency hopping systems commonly used in today's wireless systems, these calibration times must be minimised.

In this paper we present a novel technique suitable for low feature size technology nodes that achieves fast calibration of VCO operation into the optimal subband. The paper is organised as follows: Section II reviews current published work relating to VCO subband calibration, section III describes the novel fast VCO calibration technique in detail, with the model used to demonstrate the technique being presented in section IV. Simulation results are then presented in section V with a final conclusion presented in section VI.

II Related Work

Current approaches to subband calibration focus on finding the optimum VCO subband by either:

1. Measuring the VCO frequency (f_{VCO}) for a desired control voltage
2. Measuring the VCO control voltage (V_{ctrl}) when the PLL is in lock

In [3], approach 1 is taken and f_{VCO} is measured, by counting cycles and comparing to counts of the reference clock, f_{ref}, with V_{ctrl} clamped to $Vdd/2$, to determine if f_{VCO} is within a specified frequency window determined by end application requirements. The advantage of this approach is that it is predominantly digital and thus more suited to lower technology nodes, with its main disadvantage being long calibration times due to the large number of counts required in the comparison process. In [4], approach 2 is used and V_{ctrl} is monitored for a given input reference frequency (f_{ref}) to see if it lies within a specified voltage window determined by the available tuning range. The disadvantage of this approach is that it requires two identical PLL loops, thus making it less suited to lower technology nodes where device mismatch increases [5],[6]. In addition, the PLL loop must settle each time an adjustment is made to the subband control word before V_{ctrl} can be measured leading to long calibration times. An improvement to this approach is presented in [7] where only one loop is employed thus removing errors arising from mismatches between loops and reducing area. Nevertheless, the PLL loop still needs time to settle before each measurement of V_{ctrl}, leading to similar prolonged calibration times. In addition, both [4] and [7] employ comparators for V_{ctrl} monitoring leading to concerns regarding offset voltages for lower technology nodes. An alternative approach is presented in [8] where f_{VCO} is monitored by directly converting signal periods into voltages, thereby eliminating the need of waiting for loop settling times or long counts in the comparison process. The advantage of this is fast calibration ($< 4\ \mu s$) with the disadvantage being the complex circuitry needed to achieve it. The resulting calibration circuitry is area and power consuming, places heavy demands on matching and employs comparators, making it less suited to low power applications fabricated in lower technology nodes.

III Proposed Fast VCO Frequency Calibration Technique

The proposed novel fast VCO frequency calibration technique aims at achieving fast calibration times through a modified version of the approach reported in [3]. This predominantly digital approach thus achieves fast VCO frequency calibration, with low power/area requirements, suitable for lower technology nodes. In [3], frequencies were compared in a digital counter, whereby a large number of counts was required to guarantee the required f_{VCO} was calibrated to within a specified degree of accuracy. This resulted in calibration times defined by:

$$T_{cal} = \frac{2^n \cdot 100}{f_{ref} \cdot \%_{cal}} \tag{1}$$

where calibration time, calibration resolution, input reference frequency and required percentage accuracy are represented by T_{cal}, n, f_{ref} and $\%_{cal}$ respectively.

The proposed technique achieves an effective upsampling of the input reference frequecy by a factor of M. This means the system counts M times faster to a specified accuracy thereby reducing T_{cal} by the same amount, as shown in (2):

$$T_{cal} = \frac{2^n \cdot 100}{M \cdot f_{ref} \cdot \%_{cal}} \tag{2}$$

The block diagram for the proposed system is shown in Fig. 2.

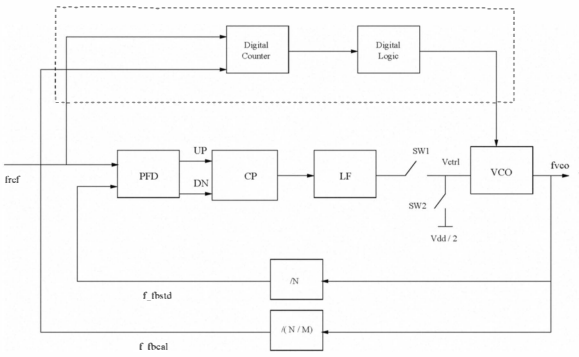

Fig. 2: Block diagram of the proposed calibration system

Shown in Fig. 2 is a standard Charge Pump PLL (CP-PLL) loop consisting of a phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and integer N feedback divider (/N). Additional to this is the VCO calibration loop which consists of an integer N/M feedback divider (/(N/M)), digital counter and digital logic. This "dual loop system" gives rise to two feedback frequencies — the standard feedback frequency (f_{fbstd}) required for normal operation of the PLL, and the calibration feedback frequency (f_{fbcal}) required for calibrating the VCO to operate within the optimal subband. As shown below, f_{fbcal} is effectively an upsampled version of f_{ref} by a factor of M:

$$f_{fbstd} = \frac{f_{VCO}}{N} = f_{ref} \tag{3}$$

$$f_{fbcal} = \frac{f_{VCO}}{N\,/\,M} = M \cdot \frac{f_{VCO}}{N} = M \cdot f_{ref} \tag{4}$$

Upon start up, or whenever a frequency hop occurs, SW1 opens to disable the PLL loop and SW2 closes to clamp V_{ctrl} to $V_{dd}/2$. The feedback signal f_{fbcal} and the reference clock f_{ref} are then counted to determine whether the feedback signal is at the correct rate. Due to the effective upsampling of the calibration feedback loop, and the required accuracy, overflow values for each counter are defined as:

$$ov_{cal} = \frac{100}{\%_{cal}} \qquad ov_{ref} = \frac{100}{M \cdot \%_{cal}} \tag{5}$$

where overflow counter values for f_{fbcal} and f_{ref} are represented by ov_{cal} and ov_{ref} respectively. When the reference counter reaches ov_{ref}, the feedback counter is stopped and its value compared with ov_{cal} to determine whether the VCO is operating within the optimal subband. If f_{fbcal} is less than ov_{cal}, an incrementally faster setting is chosen, if too high, a slower setting is selected. Once the correct subband has been found, calibration is complete and SW2 opens to disable the calibration loop and SW1 closes enabling the PLL loop for normal operation. As comparisons only occur when a counter reaches ov_{ref}, T_{cal} is determined by it. Therefore the M term introduced into the denominator of ov_{ref} by the effective upsampling process results in a direct reduction of T_{cal} by a factor of M.

For example, taking the same parameters as presented in [8], one has $n = 3$, $\%_{cal} = 1\%$ and f_{ref} = 40 MHz. Setting $M = 10$ results, from (4), in an effective upsampling by a factor of 10 which, from (2), results in a final T_{cal} of 2 μs. This leads to the requirement of a counter operating at 400 MHz, achievable for on-chip logic fabricated at the smaller technology nodes.

IV Circuit Description

To verify the proposed technique, a PLL with fast VCO frequency calibration is being designed for implementation on UMC's 1P9M 90nm process. The full design is a CP-PLL with a calibrated charge pump and LC-tank VCO; with f_{ref} and f_{VCO} set to 40 MHz and 4.8 GHz respectively. A standard PFD is used, consisting of a pair of D-type flip flops (D-FF) with outputs connected to the reset inputs of both D-FF's through an AND gate and delay cell. These gate delays introduce a delay time (Δt_{pd}) of 1ns. A differential CP is employed due to its superior performance over its single-ended counterparts [9]. The modelled differential CP is taken from [10] with I_{cp} set to 100μA. A 2nd-order LF is modelled to minimise noise on V_{ctrl}, with pole and zero positions set to $\approx$ 2.7 and 0.4 times the loop bandwidth (ω_n) to achieve a phase margin of 49° [11]. The loop bandwidth, ω_n, is set to 20 kHz to minimise the overall noise of the PLL. Increasing the number of subbands indefinitely increases complexity and does not result in a corresponding improvement in phase noise performance [12] — in practice, the subbanding capacitors become impractically small and comparable with circuit parasitic capacitances. For this work, 4-bit calibration is employed, with the 16 switchable capacitors placed in a switched capacitor array (SCA), as shown below in Fig. 3. With the 16 subbands, a K_{VCO} of $\approx$ 50 MHz/V is used to achieve a VCO tuning range of 10% (to allow for some subband overlap).

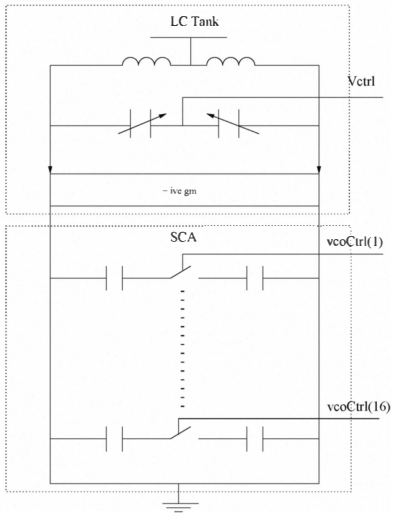

Fig. 3: VCO block diagram with 4-bit SCA

The integer feedback constants are set to N = 120 and M = 10 for the desired f_{ref} and upsampling ratio. The digital control logic for implementing the algorithm has been implemented in Verilog and synthesised to a 90nm cell library, yielding a gatecount of $<$ 1000.

V Simulation Results

The full PLL has been simulated in ADMS, a mixed-mode simulator, with the digital sections described in Verilog and the analog sections in a mixture of VHDL-AMS and SPICE-level components. On start-up or after loss of lock, the VCO is set to its correct subband using the algorithm outlined above. The steps are:

1. Connect V_{ctrl} to mid-scale voltage
2. Set control word to mid value
3. Set feedback divider to give f_{fbcal}
4. Count reference and feedback cycles
5. Increment or decrement control word and repeat counts until desired frequency reached
6. Set feedback divider to give the normal f_{fb}

A plot of simulated results is shown in Fig. 4. Shown in the Figure are (from top to bottom):

- VCO control word
- Reference counter – refCnt
- Feedback counter – vcoCnt
- Mux control signal VCO input voltage and feedback divider setting
- Feedback signal
- Reference input

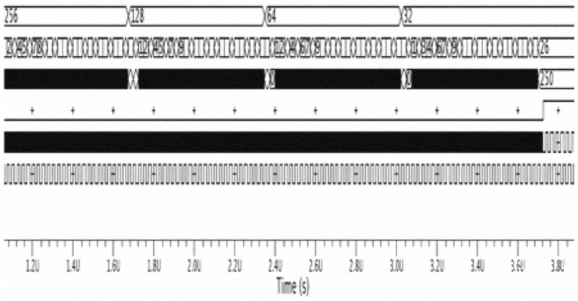

Fig. 4: Simulation of VCO Subbanding Scheme

In this case, we have an input reference clock of 40MHz, a nominal VCO frequency of 4.8GHz, 4-bit tuning of the VCO and an M of 10, meaning that ov_{cal} is 10 × the value of ov_{ref} and the f_{fbcal} frequency is 400MHz. To obtain 0.4% frequency accuracy, we count up to 25 on the f_{ref} counter and check for 250 on the f_{fbcal} counter.

In the plot, it can be seen that the VCO control word changes from 256 to 32, corresponding to VCO control bits 8 down to 5 being selected in turn, switching in different VCO configurations — in this case, higher bits control faster configurations, vcoCtrl[0] selecting the highest oscillation frequency and vcoCtrl[15] the slowest.

When refCnt reaches 25, the value on vcoCnt is checked; this should be 250. In the simulation, the values on vcoCnt are 253, 252, 251 and 250 for the vcoCtrl control words used. When a count of 250 is reached, the algorithm finishes and the mux setting for the VCO input is switched to reconnect the normal PLL loop. At the same time, the feedback divider is changed back to 120 and the feedback signal is seen to change back to close to 40MHz, to be exactly set by the PLL loop.

For this case, the time taken is 2.5 μs, for 0.4% accuracy and four count iterations. The maximum number of iterations is eight, starting at the midpoint VCO control setting. For 1% frequency accuracy, we would count to 10 (ov_{ref}) and have a target of 100 for f_{fbcal} and the time taken would be 40% of the present simulation, i.e. 1 μs.

To compare with the approaches in section II; approach 1, as used by [3] counts frequency directly without any effective upsampling, meaning that each conversion will take 100 counts of f_{ref} for 1% accuracy, whereas our scheme would take 10 cycles of f_{ref}. Approach 2, as used by [4] depends on the loop bandwidth, which will be somewhat slower, taking an estimated ([8]) 30 f_{ref} cycles. The time-to-voltage conversion proposed by [8] offers similar speed to the upsampled counting (8 cycles of f_{ref}) at the expense of extra analog circuitry.

VI Conclusion

In this paper a novel technique for fast VCO subband calibration is presented. The proposed technique is based on effective upsampling of the reference input such that the time taken to find optimal subband of operation is greatly reduced. Modelled with a 4.8GHz CMOS PLL in UMC's 90nm process, this novel approach has been shown to yield reduced calibration times over previouly reported architectures. Unlike previously reported analog-based solutions, this technique employs a predominantly digital approach which exhibits low power/area requirements and is more suited to lower technology nodes. This technique is therefore suitable for high performance systems requiring fast and frequent calibration, such a frequency hopping systems commonly used in todays wireless communications systems.

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