Pulse Width Modulation of Multilevel Delta-Sigma Output for Class S Power Amplifier

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Abstract — In this paper a platform that implements the digital processing and RF carrier generation for class S PA operation is presented. This implementation consists of a bandpass delta sigma modulator (DSM) with a multi-level quantizer followed by a pulse width modulator and frequency upconversion stage. The principle of operation is described and validation is provided through simulation and experimental measurements on a prototype of the modulator. It is shown that the output from the new modulator can achieve significant improvements in SNR performance compared to a two level DSM with little added computational overhead.

I. INTRODUCTION

Power amplifier (PA) efficiency is a major factor in the overall system efficiency of wireless systems. Switch mode power amplifiers, such as class E, F, and S, have the potential for 100% power efficiency. Unlike traditional power amplifiers, these architectures utilize the transistors as highly non-linear switches, driven by a modulated stream of pulses. The primary challenge is that these devices must switch at some multiple of the signal frequency. For modern wireless communications in the GHz range, this makes the design of switches and modulators highly challenging. Recently there has been much progress in the development of suitable nonlinear switching devices that are capable of switching power at the required frequencies [1-3]. However progress in the realtime generation of the modulated pulse stream has lagged and viable systems that utilize standard technologies (such as FPGAs) do not yet exist. In this paper, a scheme for realtime generation of the digital pulse stream is presented. This scheme offers significant improvement over existing proposals in terms of noise performance and complexity.

II. EXISTING MODULATOR ARCHITECTURES

An early pioneer in the area of digital RF power amplifiers, Stapleton used a 1 bit bandpass delta sigma modulator (BPDSM) to produce a square wave PA driving signal [4] – Fig. 1(a). For ease of implementation, the bandpass delta-sigma modulator operated at four times the required signal frequency, and the input signal to the modulator was centered at the desired transmitter frequency. The disadvantage of this design is that the high operational frequency of the modulator is highly challenging to implement for modern communication frequencies, result in an expensive, high-power design. Another approach is to use a single bit DSM with a sampling frequency several times lower than the transmitter frequency, and to utilize a higher Nyquist image in the output - see Fig. 1(c). Any non-linear system will generate harmonic images of the desired output. A digital power amplifier is such a device and in this approach the bandpass filter at the output of the power amplifier selects an image at the desired frequency. This approach allows the generation of modulated pulse streams using relatively low-cost components however it has some significant disadvantages. By operating at low frequencies, the effective oversampling ratio of the modulator is decreased, yielding a narrower effective signal bandwidth or correspondingly a greater degree of in-band noise. Another impact is that the other images do not come without cost and there is a reduction in coding efficiency of the delta sigma modulator, reducing the available output power. Other similar schemes, such as Manchester encoded signals [5] or digital multiplication [6] can achieve similar results but suffer from the same disadvantages.

Digital multiplication of the delta-sigma modulator with a binary signal at twice the desired carrier frequency is an interesting case of the previous technique [7]. Binary multiplication is a single bit operation and easy to implement. Spectrally such a multiplication will convert a lowpass transfer function into a highpass transfer function without loss – Fig 1(b). This scheme has been used widely in analog-to-digital converters to minimize dc offsets. In digital power amplifiers, it is possible to place the intermediate frequency for the signal near zero and obtain an image close to half the switching frequency. This mechanism allows the reduction of the switching frequency by roughly half, though typically a ratio of 2.3-2.4 is used to provide a separation from the image

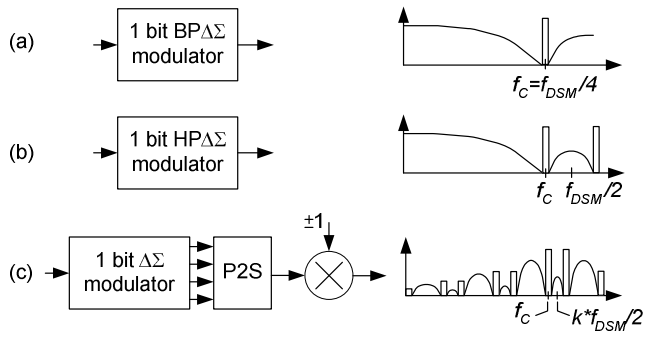

Figure 1. Past modulators architectures for class S PA. (a) Direct band pass DSM. (b) Direct high pass DSM . (c) Up-converted one bit DSM.

above fs/2. The performance of this approach is limited by the speed of the delta-sigma modulator and the corresponding oversampling ratio. As the output of the modulator must be 2-level, this limits the overall noise performance available using this approach.

In this paper we present an approach which expands upon the lowpass-highpass transformation but also provides an improvement in the SNR of the modulator while utilizing the same signal processing power. The remainder of the paper will initially describe the architecture and expected performance. The next section will present some simulated and experimental results as validation of the concept.

III. ARCHITECTURE

The proposed modulator architecture, depicted in Fig. 2, consists of two blocks: an n level delta sigma modulator and a look-up table (LUT) whose contents are binary pulse width modulated sequences, of length m, corresponding to the value of the quantizer levels. The LUT converts the multilevel delta-sigma output into a stream of binary outputs such that the mean of the PWM sequence corresponds to the value of the delta-sigma output. The LUT output is delivered as a parallel output which can be serialized into a high speed bitstream. The final stage is to use binary multiplication to convert the lowpass transfer function to the equivalent highpass structure, placing the signal band at the required RF frequency. proposed modulator architecture consists of two blocks: an n level delta sigma modulator and a memory block whose contents are n (n>2) digital pulse width sequences of the quantizer levels.

This approach has several benefits: first the LUT table implicitly implements frequency scaling. For each delta-sigma modulator output, m binary outputs are generated that can be serialized into a pulse stream of frequency mf_{DSM}. The second benefit is that this approach enables us to utilize a high order delta-sigma modulator and thus avail of the more aggressive noise-shaping that is possible. This will help reduce the inband noise and improve overall performance.

The length of the LUT sequence is determined by two factors: the degree of frequency scaling desired; and the number of levels in the delta-sigma modulator output. To encode n levels in a PWM sequence will require a sequence length of n-1 bits (Fig. 2). The output rate of the modulator is likely technology constrained thus the length of the sequence will be determined by the degree of frequency scaling required. As the output resolution of the delta-sigma modulator is unconstrained, an optimal choice would be to set the resolution of the modulator to match that of the PWM sequence length.

In order to evaluate the combined LUT-DSM system, a comparison against fourth-order, 11 level bandpass DSM is carried out, where the LUT sequences are of length 20. The delta-sigma modulator output sample rate is 80 MHz and the passband is centred on 8 MHz with a bandwidth of 2 MHz. As he LUT-DSM output is transformed to a highpass structure, the lowest frequency image of the LUT-DSM is the pertinent signal band to compare with the 11-level BPDSM. As can be seen from Figure 4, the passband signal-to-noise ratio of the two systems are similar, though the LUT-DSM scheme experiences increased noise (~8 dB) for high input signal amplitudes. This suggests that improved signal-to noise ratios will be possible in the final system when compared to an equivalent bandpass delta-sigma modulator only solution with two output levels.

One of the advantages of using a higher order delta-sigma modulator is the increased flexibility to change the location of the passband. In the overall communication system, the passband centre frequency is effectively an intermediate frequency (f_{IF}) and the signal band around will later be frequency translated to the needed carrier frequency (f_C). Using the fourth-order BPDSM it is possible to place the intermediate frequency anywhere from DC to just below the delta-sigma modulator output frequency (f_{DSM}).

As shown in Fig. 1(c) the resulting signal after up conversion will contain image centered at $f_{lower} = ½f_C - f_{IF}$ (our carrier frequency), and another at $f_{upper} = ½f_C + f_{IF}$, along with all the out of band quantization noise. For this reason a bandpass filter (BPF) is included in the power amplifier platform of Fig. 5 to filter out the unwanted image at $½f_C + f_{IF}$ and quantization noise. This filtering effort is proportional to

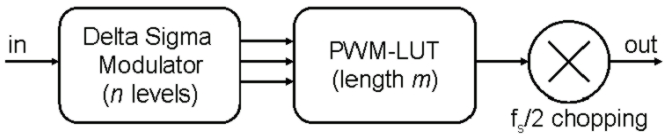

Figure 2. Block diagram of LUT-DSM

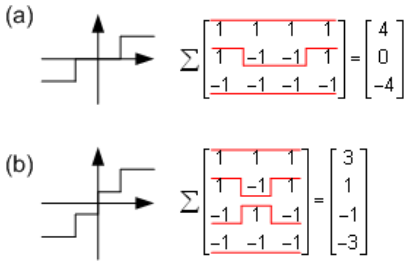

Figure 3. Conversion from multilevel to 2-level PWM signal. (a) odd number of quantizer levels. (b) even number of quantizer levels.

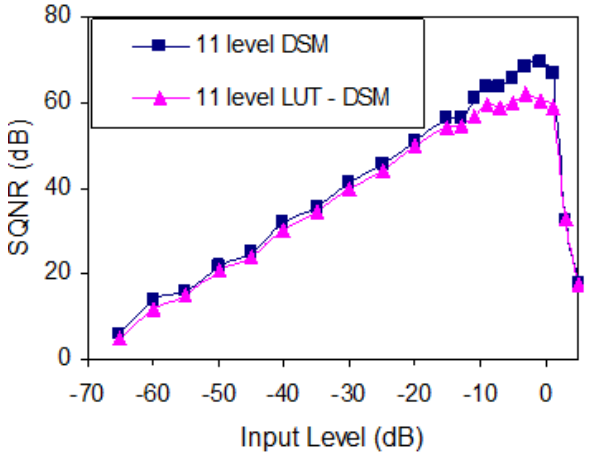

Figure 4. The SQNR of proposed 11 Level LUT-DSM and 11 Level DSM

the separation between the wanted signal at f_{lower} and the image at f_{upper}, denoted here as $f_{SI} = 2\eta_{IF} f_{DSM}$.

Although the performance of the LUT-DSM can be close in terms of SNR to the n-level DSM, the SNR performance of LUT-DSM degrades as the center frequency f_{IF} moves from 0 towards ½ f_{DSM}, as a result of introducing noise by a digital pulse width modulation. This effect on SNR performance as a function of center frequency f_{IF} was investigated using a Matlab simulation of a multi-tone input signal with a 4MHz bandwidth, a 10 level DSM followed by a 9 bit LUT in Matlab simulations. Fig. 6 shows the degradation as the bandpass frequency (f_{IF}) increases. This is likely due to the conflict between PWM encoding which is fundamentally a low-pass encoding with the bandpass delta-sigma modulator as the passband moves further away from dc. One of the key arguments for using the additional complexity of a 2-step approach compared to a direct 2-level delta sigma modulator was that we could take advantage of the lower noise floor from a multi-level converter. Fig. 6 also shows the performance of the same 4th order modulator with only 2 output levels. As to be expected, the performance of the 2-level DSM system remains approximately constant irrespective of the bandpass location. However when the passband is low, the LUT-DSM system shows significant improvement (about 8-10 dB) over the 2-level output. Thus there is a tradeoff in this implementation between the improvement in noise performance that is obtained by having a low fIF and the easier filtering of the high frequency image that is implied by a larger f_{SI} (and thus a larger f_{IF}).

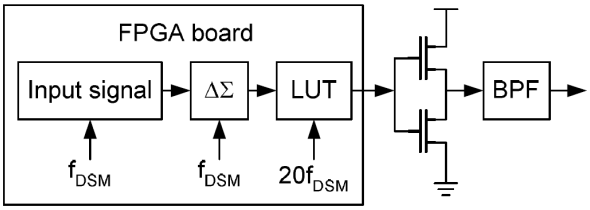

Figure 5. Reconfigurable switchmode power amplifier platform.

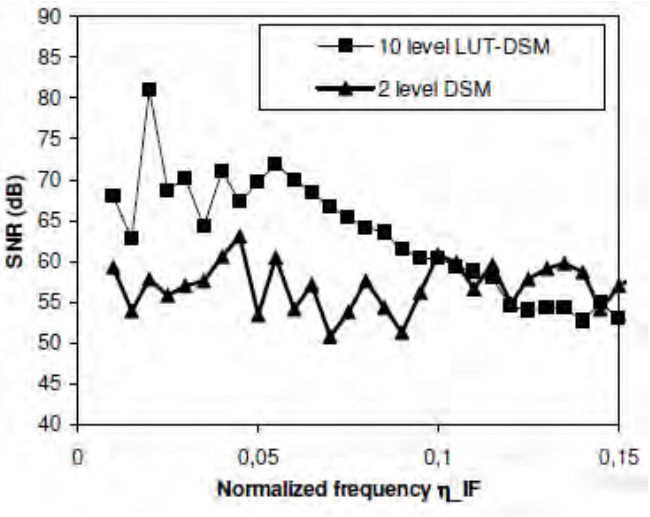

Figure 6. Comparison of SNR versus center frequency in the NTF for two level DSM and DSM-LUT modulator (three tone input signal).

IV. Reconfigurable Platform

The experimental platform has been implemented using the Xilinx Virtex II Pro development board [8]. It consists of three major blocks allowing the modulation and shifting of the signal to RF. The input signal is generated in four direct 14 bit digital synthesizers (DDS), and these are fed to the input of the DSM block. The DSM used in the testbench is a fourth order CRFB structure that, depending on the coefficients used can be configured to produce the signal of a center frequency in the range 0 to 2 f_{DSM} . A 75MHz output sample rate was selected as this matches accessible FPGA clock frequencies. The LUT has a sequence length of 20 and the output of the LUT is serialized by a fast shift register implemented in the onboard MultiGigabit Transceiver (MGT). This produces a bitstream at 1500 MHz. The output of the MGT drives the switching power amplifier followed by a band pass filter. The maximum achieved sampling frequency of the CRFB structure for this board is 75MHz, allowing the IF signal to be placed in a range of 0 to 18.75MHz, and the resulting carrier frequency f_C between 731.25MHz to 750MHz. The frequency range limitation however can be improved using an FPGA board with a faster clock frequency. It may also be possible to achieve a higher DSM sampling frequency using a more computationally efficient structure such as that described in [9]. For validation, the Virtex II Pro board provides adequate speed to prove the concept of this approach and can serve as a cheap test bench for other groups working in this field of research. An important point to note when viewing the experimental results displayed in Figs. 7 and 8 is that the measurements where taken at the output of Xilinx multi-gigabit transceiver. This allows one to generate high speed outputs however these outputs are optimized for high speed serial communications and are not square. The effect of this is that the noise floor of any results will be dominated by the contribution from the gigabit transceivers. However despite the large contributed noise, this platform allows for concept verification as the out-of-band delta-sigma noise transfer functions is clearly visible.

V. Example Design and Validation

Using the procedures outlined earlier, the available sampling frequency of 75 DSM f = MHz of the 11 level DSM along with a 20bit LUT is sufficient to generate an RF signal in the range from 731.25MHz to 750MHz. The multi-tone output signal and its image appear at 741.4 MHz and 758.7 MHz respectively, and are shown in Figs. 7 and 8. It is observed that the noise level in the vicinity of the signal is -50dB to -40dB for two level DSM against -60dB to -45dB in a LUT-DSM spectrum, which displays better inband noise performance. The side band noise level in a displayed range of 50MHz is -23dB to -20dB in a two level DSM's spectrum against -45dB to -40dB in a spectrum of a LUT-DSM. Thus the LUT-DSM system achieves 20dB lower noise level near the signal band,

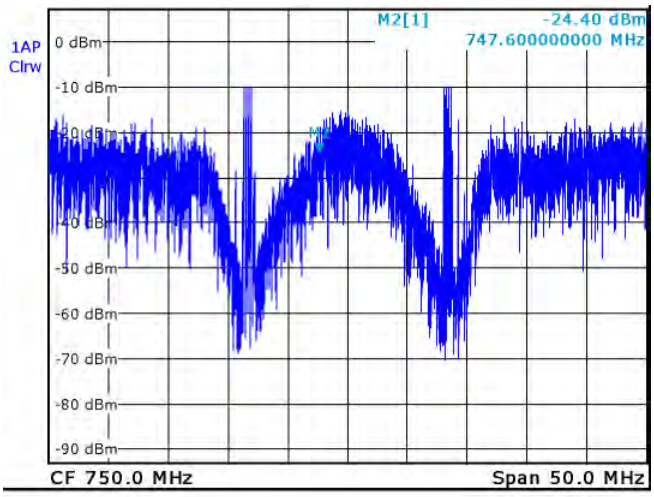

Figure 7. Measured high frequency spectrum of up-converted two level DSM

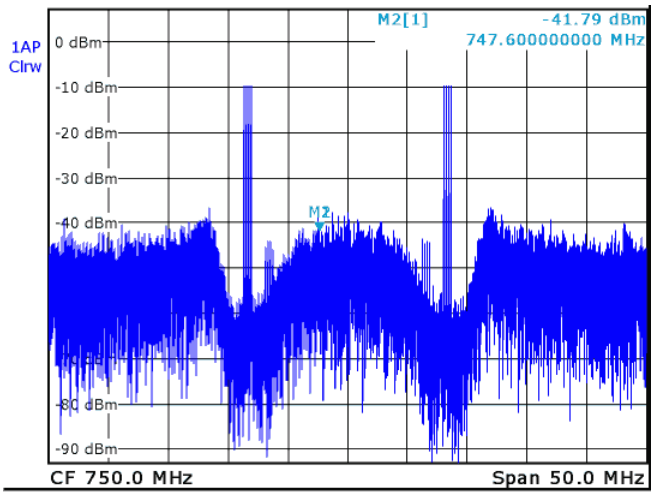

Figure 8. Measured high frequency spectrum of eleven level LUT-DSM

relaxing requirements for an output band pass filter in a class S PA structure depicted in Fig. 5.

Lowering the noise level in the DSM-LUT output signal spectrum revealed images of the signal that were not visible in the 2 level DSM modulator's spectrum because of the higher noise floor. Similar distortion has been observed in the literature [10] and is an effect of the dc component in the output signal. These artifacts may be removed from the spectrum by using a signal whose spectrum does not contain any dc component to drive the switch mode PA stage.

VI. Conclusion

In this paper a new modulator system for Class S PA has been proposed. The LUT-DSM structure offers better SNR performance than an equivalent two level DSM approach previously used. The new architecture has been validated through experimental measurements displaying approximately a 10 dB improvement in dynamic range and a 20 dB lowering of the out-of-band noise floor.

VII. Acgnowlement

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